Design How-To

Ensuring high-qualityvideo communications

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As the migration to high definition (HD) picks up speed, video system designers are faced with new challenges related to bandwidth requirements, image quality, transcoding and digital media codec flexibility. These are difficult issues even for relatively closed systems that operate in proximity to each other.

In order of magnitude, more processing power is required to encode and decode HD video than standard-definition (SD) video.Whereas a single DSP can handle a stream of SD video encode/decode, for example, up to five may be needed for HD720p at 30 frames per second (fps), and 12 to 13 DSPs may be required for HD1080p at 30 fps.

No one has a trickier set of problems to solve than designers whose systems interface with the Internet Protocol (IP) network--or private networks--to transmit video to distant endpoints. IP-based videoconferencing is one of the most obvious examples of this application. There are many subsets of video communications, ranging from IP video telephony to sophisticated applications in which enhanced wideband audio, presentation data and video boxes are integral parts of the complete real-time system solution.

In addition to handling the difficult migration from SD to HD video, video communications engineers must find ways to minimize end-to-end latency. Visual artifacts such as distorted video caused by network contention/congestion or inadequate video compression implementations can pose problems, but the most challenging user experience is ensuring a natural video communications flow among partici- pants. The task sets ag- gressive limits on system latency.

For a natural communications experience, system designers typically target a less-than-250-millisecond end-to-end d elay, which includes an undeterministic network, audio and video compression and decompression, and other system latencies. Video communications design engineers must also deal with endpoints that can vary widely and sometimes dynamically. Two examples would be:

• Multiple conference rooms with high-end endpoint systems that display large-screen, high-resolution video at 30 fps, as well as picture boxes, menus, on-screen displays (OSDs) and presentation data;

• PCs, video phones and portable phones scattered around the enterprise with smaller resolution displays.

Each may have its own preferred codec. System design thus should be flexible and scalable to virtually any scenario.

From a system-level perspective, designers have an urgent need to manage heavy processing yet still fill a large number of end-user products by simply adding or subtracting peripherals. An IP-based

video phone, for example, would require both a camera and an LCD, but a streaming IP-based set-top would require only the display. At the other end of the product spectrum, a sophisticated videoconferencing system might need to handle multiple HD video streams.

Ideally, system designers would prefer to handle these challenges with a silicon platform that is scalable to up to 16 data streams; software configurable, to accommodate new algorithms as well as upgrades to existing ones; and flexible enough to change product types without much additional design effort. In other words, they seek the familiar formula: performance, flexibility and scalability at attractive price points. Conventional architectures, however, all seem to fall short.

Thanks to the processing and power efficiencies that can be derived from being designed for specific systems, ASICs have historically been a viable choice for video. But the case for ASICs is not strong in HD video. It is dif- ficult to utilize a "boxed" compression engine to perform codec processing, because bit rate and delay requirements can only be fulfilled by being able to tune the codec to user-scenario conditions. Since user scenarios are constantly evolving and may change dynamically during a video session, conventional hardwired ASIC technology fails the flexibility test. The cost of ASIC development is another inhibitor; nonrecurring engineering costs could easily reach millions of dollars.

Integrating multiple conventional, programmable DSPs on a board can provide the flexibility needed for HD video. Performance goals can also be attained. But the silicon cost multiplies too quickly to provide the magic combination of a sophisticated, scalable solution that hits the right price point. Interchip communication among too many chips can also break the total system latency budget for some product types.

System-on-chip technology offers the most viable alternative. Careful chip partitioning and design can turbocharge performance. That goes a long way toward addressing the order-of-magnitude higher performance required for the leap from SD to HD. It also addresses total system latency by paring the latency contribution of encoding, decoding and, frequently, transcoding.

On the other hand, with the right architectural choices, system performance can be efficiently scaled by putting multiple SoCs and/or a cluster of programmable DSPs on a board.

SoC partitioning
With a little thought, many design engineers would be likely to arrive at an ideal partitioning solution for HD video communications. A simplified version would have six components:

• Basic algorithmic flexibility that can be supplied by a DSP core to handle both a portion of encode/decode operations and a share of transport functionality. A critical adjunct to the DSP core would be a set of carefully selected video processing peripherals also integrated on-chip.

• Since DSPs are not particularly efficient at control operations--and there are a lot of control operations in video communications--a microprocessor core is also highly desirable.

• For certain fixed-function algorithms common to video processing, video accelerators provide significantly more processing muscle than general-purpose programmable DSPs. But the dynamism of the user scenarios requires that the accelerators remain accessible and configurable--a hugely important qualification for the accelerator block's functionality.

• A direct-memory-access (DMA) engine for transmitting data among the accelerator, the DSP core and DDR memory without CPU intervention.

• A crossbar switch for highly efficient intrachip communication.

• High-speed DDR memory.

A simplified typical SoC architecture platform would provide full multiformat hardware acceleration for key video codec algorithmic functions.

DSP core and peripherals
To handle its share of the processing, the DSP core should run at about 600 MHz and be capable of executing 4,800 Mips. Signal processing metrics must be at the high end of the performance spectrum. Texas Instruments' TMS320C64x+ core, for example, can execute four 16-bit multiply-accumulates (MACs) per cycle, for

a total of 2,376 million MACs (MMACs) per second, or eight 8-bit MACs per cycle, for a total of 4,752 MMACS/s.

The DSP core in the SoC would be assigned to perform rate control, mode decision, and high-level motion estimation and slice-level processing. (Low-level motion estimation such as SAD control and subpixel interpolations would be performed by the accelerators.)

The codec processing assigned to the DSP is usually light enough to implement other algorithms such as camera panning detection, skip macroblocking detection and light detection. In order to perform this additional work, the DSP needs access to the accelerator buffer via the high-bandwidth crossbar switch fabric.

The signal processing performance of the core can be enhanced by integrating a video processing subsystem on the SoC. Having many audio/video features integrated in hardware saves programming time and reduces the need to dedicate software cycles to interfacing with and controlling external devices.

Some peripherals would handle specific video requirements at the front end and back end. Front-end functionality should include an image pipeline for camera image capturing and processing. Because of the unpredictability of user scenarios, the image pipeline should support both BT.656/BT.1120-compliant de- vices and CCD/CMOS sensors.

Back-end functionality should include an integrated on-screen display driver and integrated digital-to-analog converters to provide analog and/or digital RGB/YCbCr video output. Other desirable integrated features would include networking peripherals, A/V interfaces and an enhanced direct memory access controller with support for up to 64 simultaneous transfer channels.

Video accelerators
The challenge for the integrated video accelerators is to meet the computation requirements of HD encoding and, at the same time, preserve the programmability of the codec implementation.

To reduce latency and increase performance, the codec should be tunable for specific video communications applications. The SoC would use high-performance coprocessors for fixed functions in the codec. At the same time, the microprocessor retains full access to these accelerators so functions such as rate control, mode decision and motion estimation can be tuned for the specific application with full freedom.

In the SoC architecture discussed here, video accelerators are configurable to support multiple video formats such as ISO MPEG-2, ITU MPEG-4, ITU H.264 and Microsoft VC1/WMV9. Each accelerator should deliver a guaranteed processing time in terms of coprocessor cycles, to enable small-slice capturing and processing for minimum delay.

The SoC architecture minimizes system delay by enabling slice-based processing, reducing algorithm delay for rate control and minimizing processing-delay variation due to bit-rate variation.

When implemented with hardware blocks with performance as described earlier, this pipelined codec design can deliver minimum system delay as low as 10 macroblocks. Each accelerator has a guaranteed processing time of less than 1,000 coprocessor cycles, enabling small-slice capturing and processing. In a typical four-slice partition for a 720p30 video encoder, encoding delay (capturing, preprocessing and encoding) can be as low as 16 to 22 ms.


A typical scalable architecture using four SoCs together wih a programmable DSP, DDR memory and video DACs enables quick-turn of multi-video-stream based products.

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