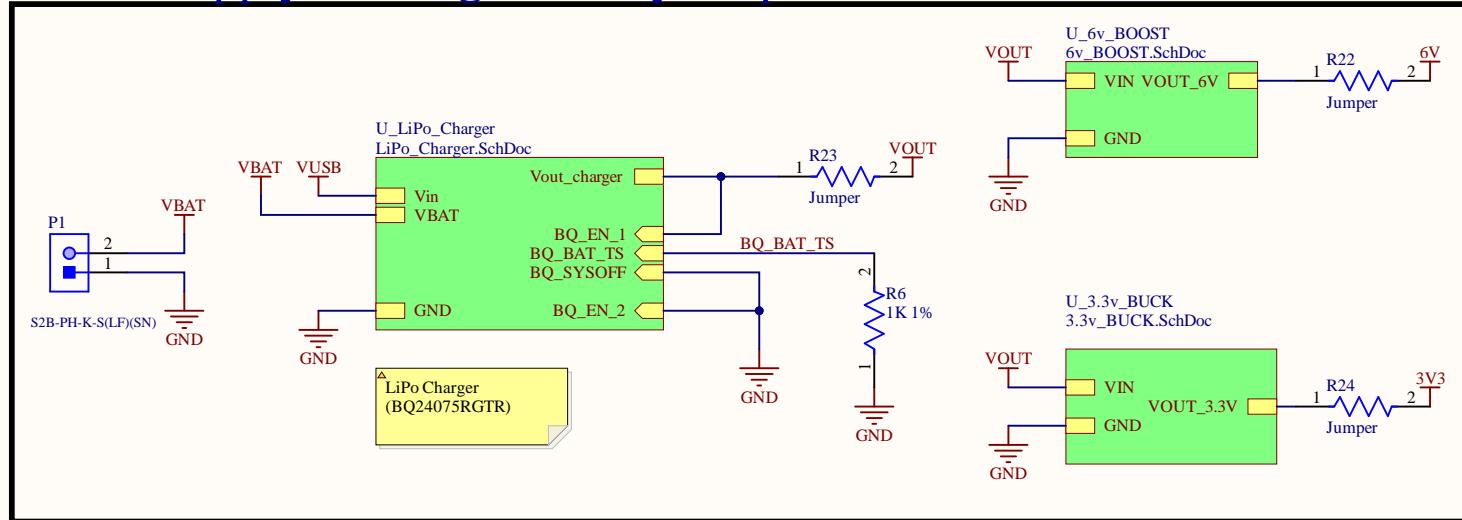
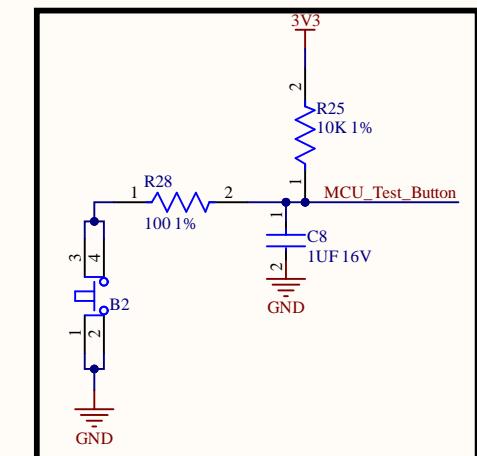


Power Supply - Change me to your power architecture



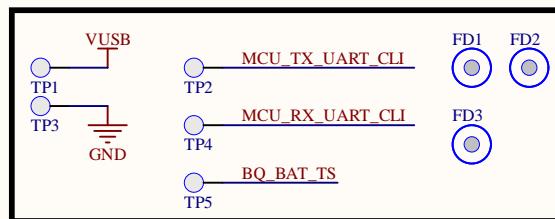
MCU Test Button



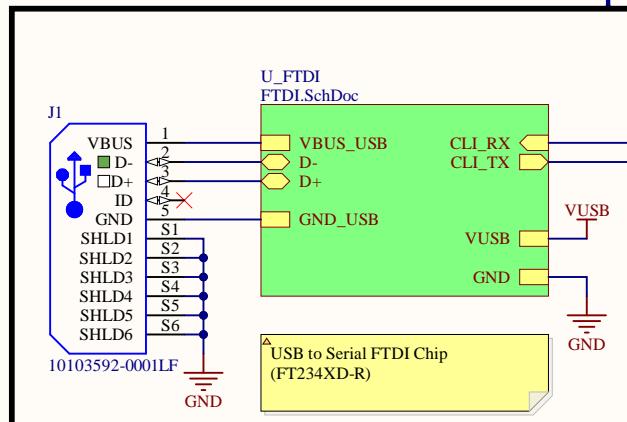
Notes

Section to add version notes or any other general information

Test Points + Fiducials

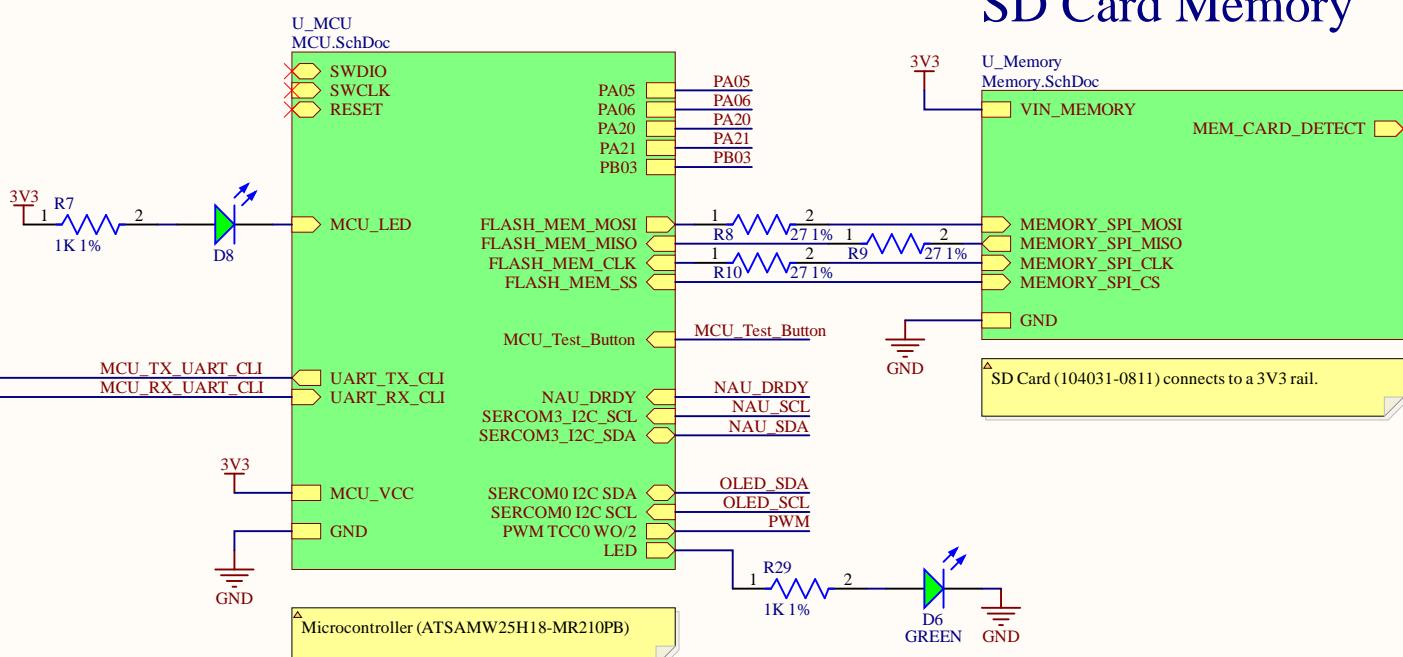


USB Connector + FTDI Chip

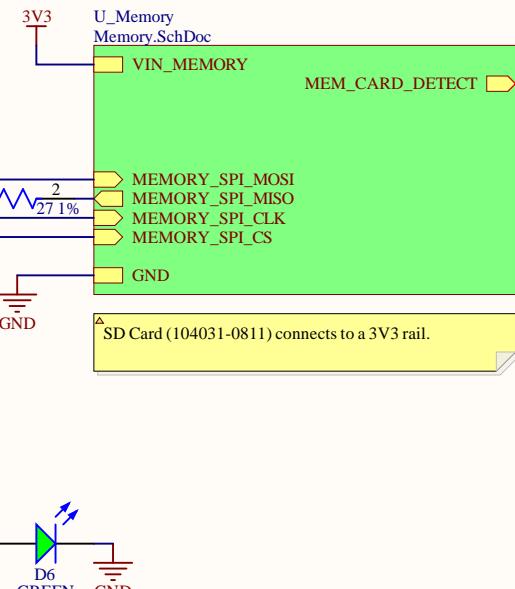


NOTE:
The FTDI Chip is an useful chip that allows us to convert USART messages into USB signals. It allows us to connect the MCU directly to the USB port of a computer and use the serial terminal (it is the same bridge used on the SAMW25 Xplained Board). The FTDI device also contains protection circuitry for the USB.

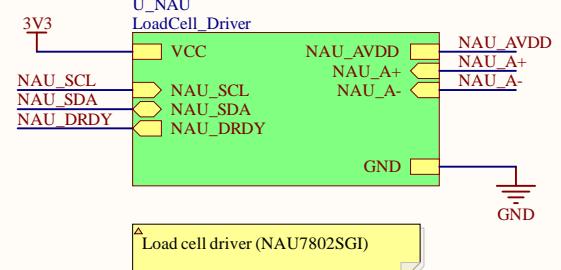
Microcontroller



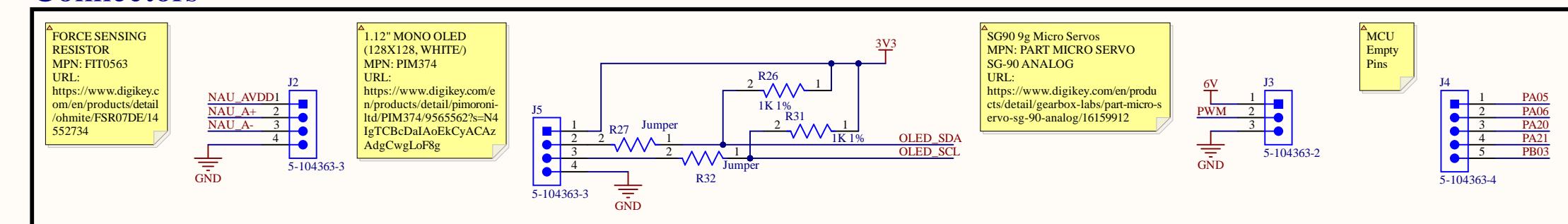
SD Card Memory

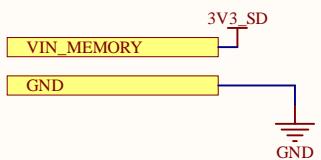
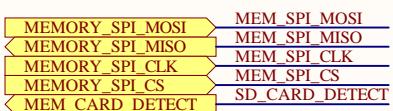


Load Cell Driver

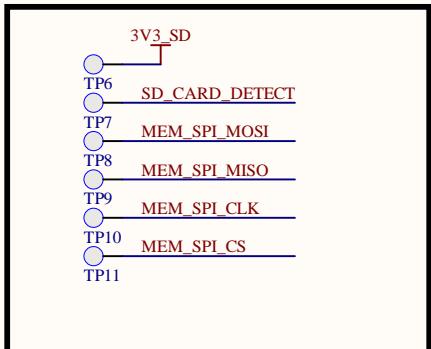


Connectors

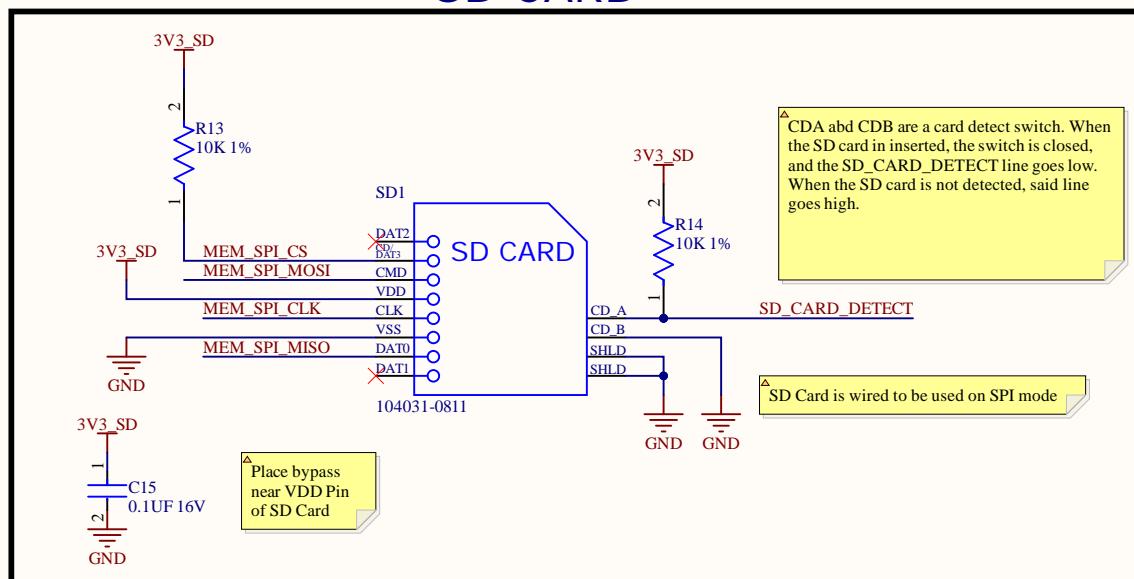




TESTPOINTS



SD CARD



Title: **Memory.SchDoc**

Desc:

Size: Letter Auth: Lihong;Chenwei Proj: Highway_Final_Version.PrtPcb

VCS: 3f612015761f81906738873ce96cddeecfc1831a [No modification]

Date: 3/2/2023 5:34:18 PM AD Ver. 23.1.1.15 Doc. * Sheet 2 of 8

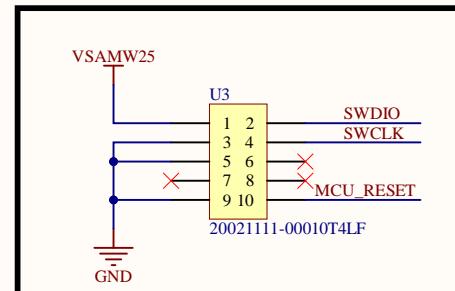
File: C:\Users\Public\Documents\Altium\Highway_Final_Version\Memory.SchDoc



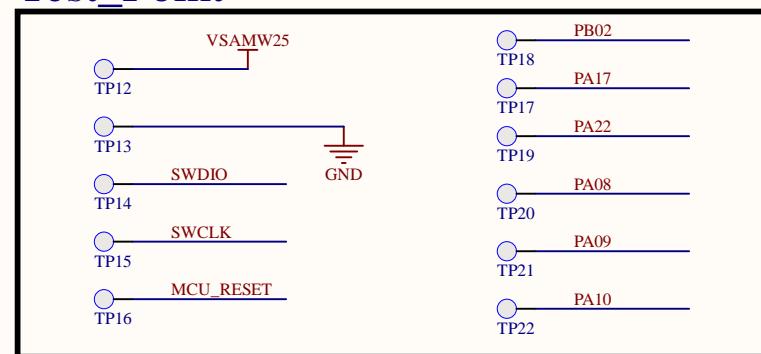
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Electrical and Systems Engineering

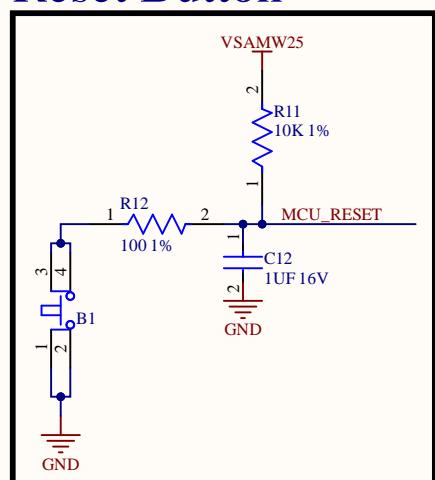
Debugger Port



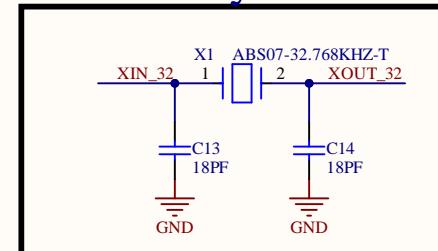
Test_Point



Reset Button



32.768 Crystal



Δ Calculation of crystal load capacitors:
 $C_{ext} = 2x (C_{crystal} - C_{para} - C_{pcb})$

 $C_{crystal} = 12.5\text{pF}$ (from crystal
 datasheet)
 $C_{para} = 3.15\text{pF}$ (from MCU datasheet)
 $C_{pcb} = 0.5\text{pF}$ (estimate)

 $C_{ext} = 2x(12.5\text{pF} - 3.15\text{pF} - 0.5\text{pF}) =$
 17.7pF

PA11	MCU_Test_Button
PA03	LED
PB02	NAU_DRDY
PA17	SERCOM3_I2C_SCL
PA22	SERCOM3_I2C_SDA
PA08	SERCOM0_I2C_SDA
PA09	SERCOM0_I2C_SCL
PA10	PWM TCC0 WO/2
SERCOM1_PAD2_SPI_MOSI	FLASH_MEM_MOSI
SERCOM1_PAD2_SPI_MISO	FLASH_MEM_MISO
SERCOM1_PAD3_SPI_SCK	FLASH_MEM_CLK
FLASH_MEM_SPI_SS	FLASH_MEM_SS
SERCOM4_UART_TX_CLI	UART_TX_CLI
SERCOM4_UART_RX_CLI	UART_RX_CLI
SWCLK	SWCLK
SWDIO	SWDIO
MCU_RESET	RESET
MCU_LED	MCU_LED

Title: MCII SchDoc

1

VCS: 261001576/169100/732873--0/-1--6-1921-[No. 175-156-415-1]

Date: 3/2/2023 5:34:19 PM | AD Ver. 23.1.1.15 | Doc. * | Sheet 3 of

Date: 3/27/2023 3:34:19 PM AD Ver: 23.1.1.13 Doc: Sheet 3 of File: C:\Users\Public\Documents\Altium\Highway_Final_Version\MCU.SchDoc

File: C:\Users\Public\Documents\Altium\Highway_Finder_Version\MCU.SCHDOC

3



A

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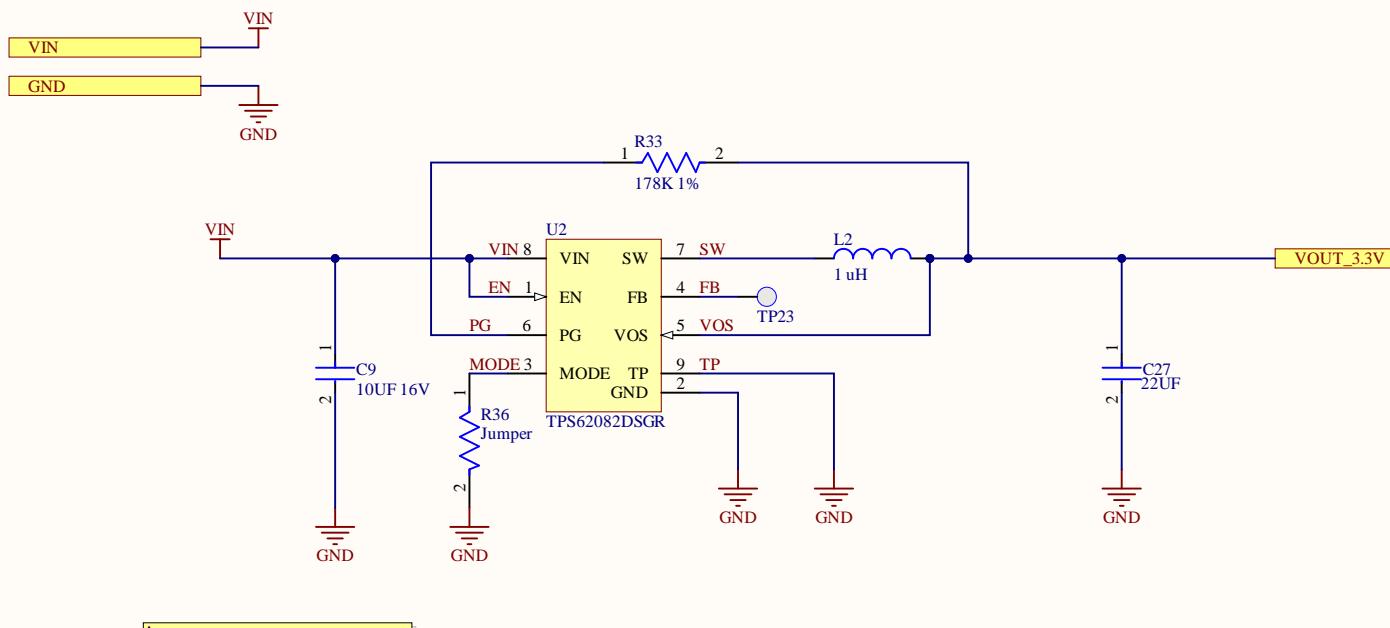
B

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C

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D



TPS62082DSGR
VIN: 4.2V to 6V
OUT: 3.3V up to 1.2A

Title: 3.3v_BUCK.SchDoc

Desc:

Size: Letter Auth: Lihong; Chenwei Proj: Highway_Final_Version.PjPcb

VCS: 3f612015761f81906738873ce96cddeecfc1831a [No modification]

Date: 3/2/2023 5:34:19 PM AD Ver. 23.1.1.15 Doc. * Sheet 4 of 8

File: C:\Users\Public\Documents\Altium\Highway_Final_Version\3.3v_BUCK.SchDoc

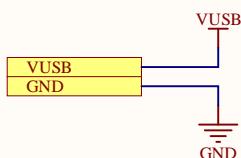


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A

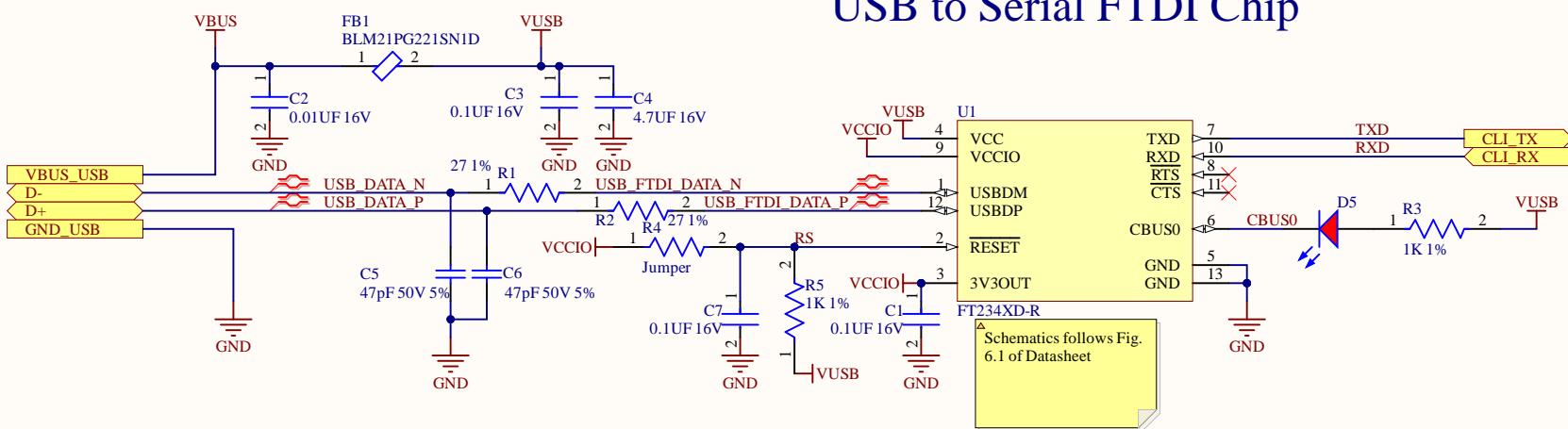
A



USB to Serial FTDI Chip

B

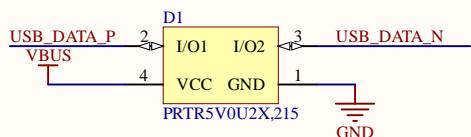
1



USB ESD Protection

C

6

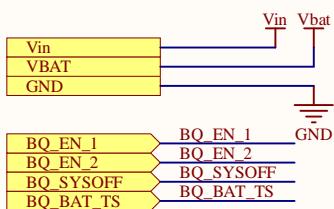


D

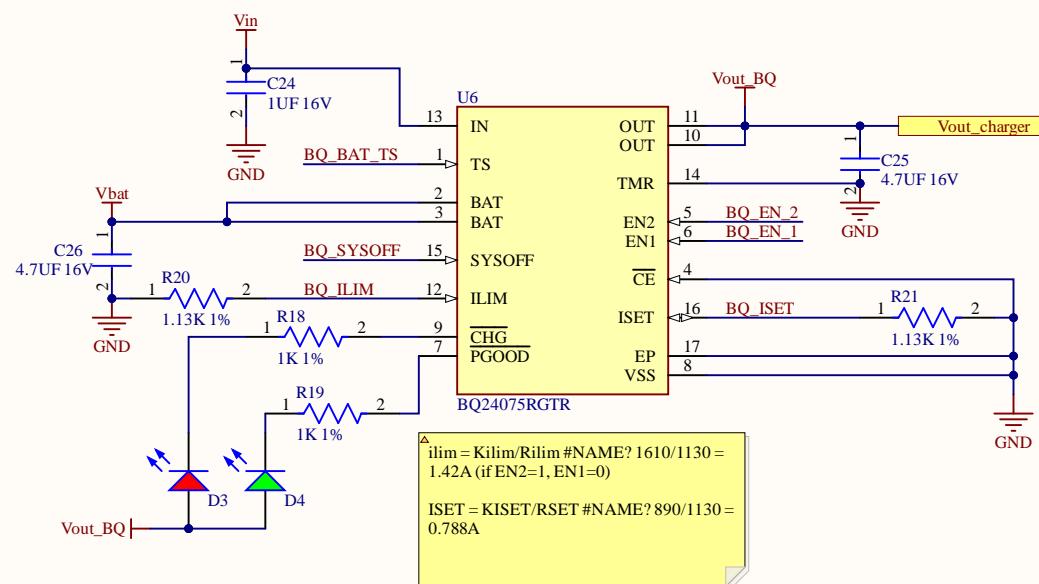
1

Title: FTDI.SchDoc	Desc:		Size: Letter Auth: Lihong;Chenwei Proj: Highway_Final_Version.PjPcb		 Penn Engineering UNIVERSITY OF PENNSYLVANIA	
VCS: 3f612015761f81906738873ce96cddeecfc1831a [No modification]						
Date: 3/2/2023 5:34:19 PM	Ø	AD Ver. 23.1.1.15	Doc. *	Sheet 5	of 8	Electrical and Systems Engineering
File: C:\Users\Public\Documents\Altium\Highway_Final_Version\FTDI.SchDoc						

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Title: *LiPo_Charger.SchDoc*

Desc:

Size: Letter Auth: Lihong; Chenwei Proj: Highway_Final_Version.PjPcb

VCS: 3f612015761f81906738873ce96cddeecfc1831a [No modification]

Date: 3/2/2023 5:34:19 PM AD Ver. 23.1.1.15 Doc. * Sheet 6 of 8

File: C:\Users\Public\Documents\Altium\Highway_Final_Version\LiPo_Charger.SchDoc



Penn
Engineering
UNIVERSITY OF PENNSYLVANIA

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Electrical and Systems Engineering

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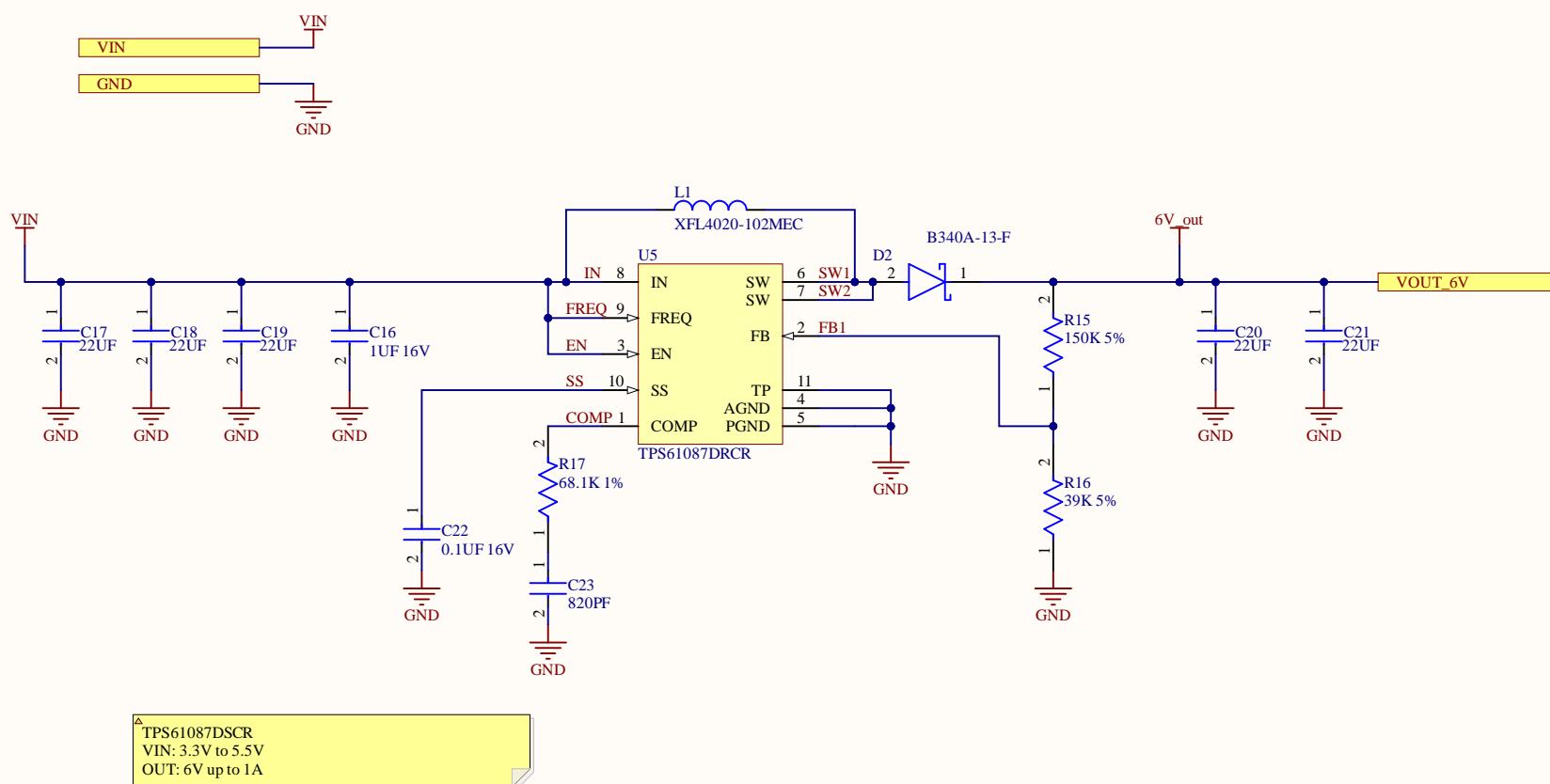
B

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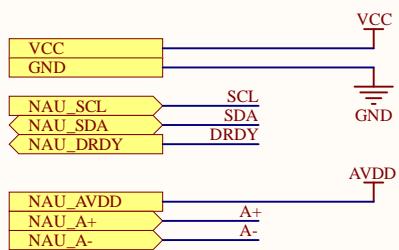
D



Title: 6v_BOOST.SchDoc							
Desc:							
Size: Letter	Auth: Lihong;Chenwei	Proj: Highway_Final_Version.PjPcb					
VCS: 3f612015161f81906738873ce96cd0ecfc1831a [No modification]							
Date: 3/2/2023	5:34:19 PM	AD Ver: 23.1.1.15	Doc. *	Sheet 7	of 8	www.seas.upenn.edu	
File: C:\Users\Public\Documents\Altium\Highway_Final_Version\6v_BOOST.SchDoc						Electrical and Systems Engineering	

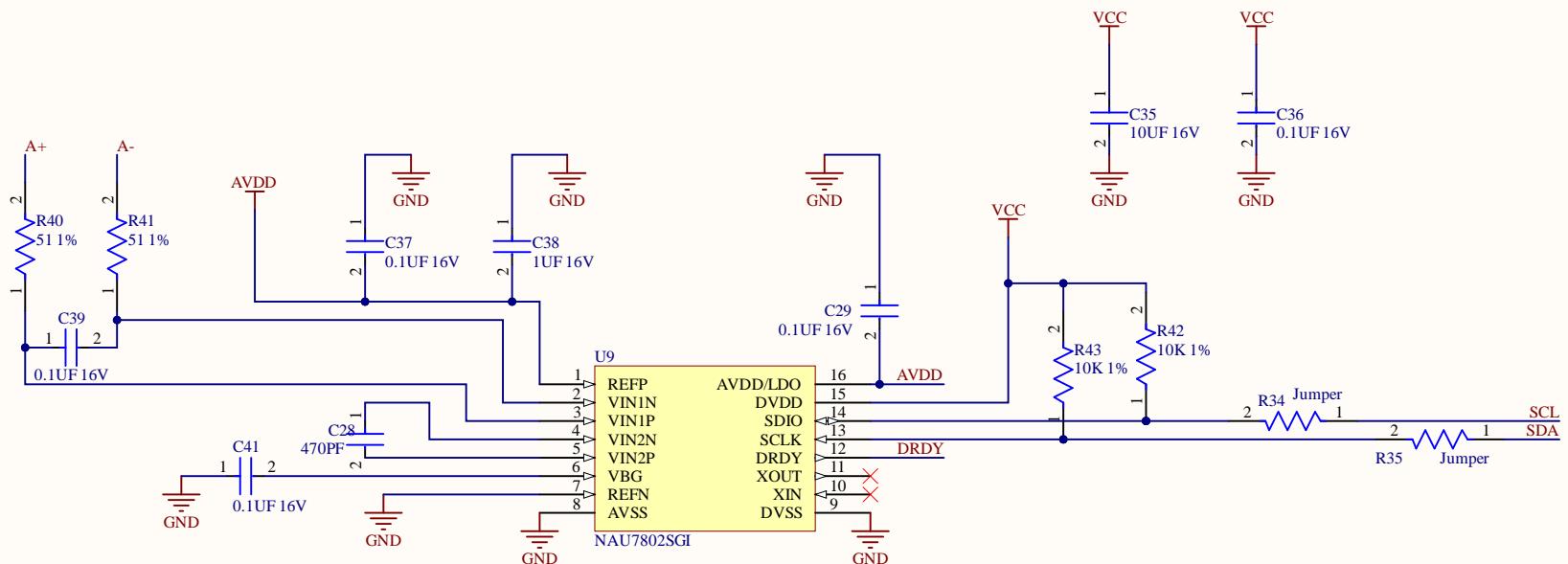
A

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B

B



1

Title: LoadCell_Driver.SchDoc			
Desc:			
Size: Letter	Auth: Lihong;Chenwei	Proj: Highway_Final_Version.PjPcb	
VCS: 3f612015f61f81906738873ce96cddeecfc1831a [No modification]			www.seas.upenn.edu
Date: 3/2/2023	5:34:19 PM	AD Ver. 23.1.1.15	Doc. * Sheet 8 of 8
File: C:\Users\Public\Documents\Altium\Highway_Final_Version\LoadCell_Driver.SchDoc			

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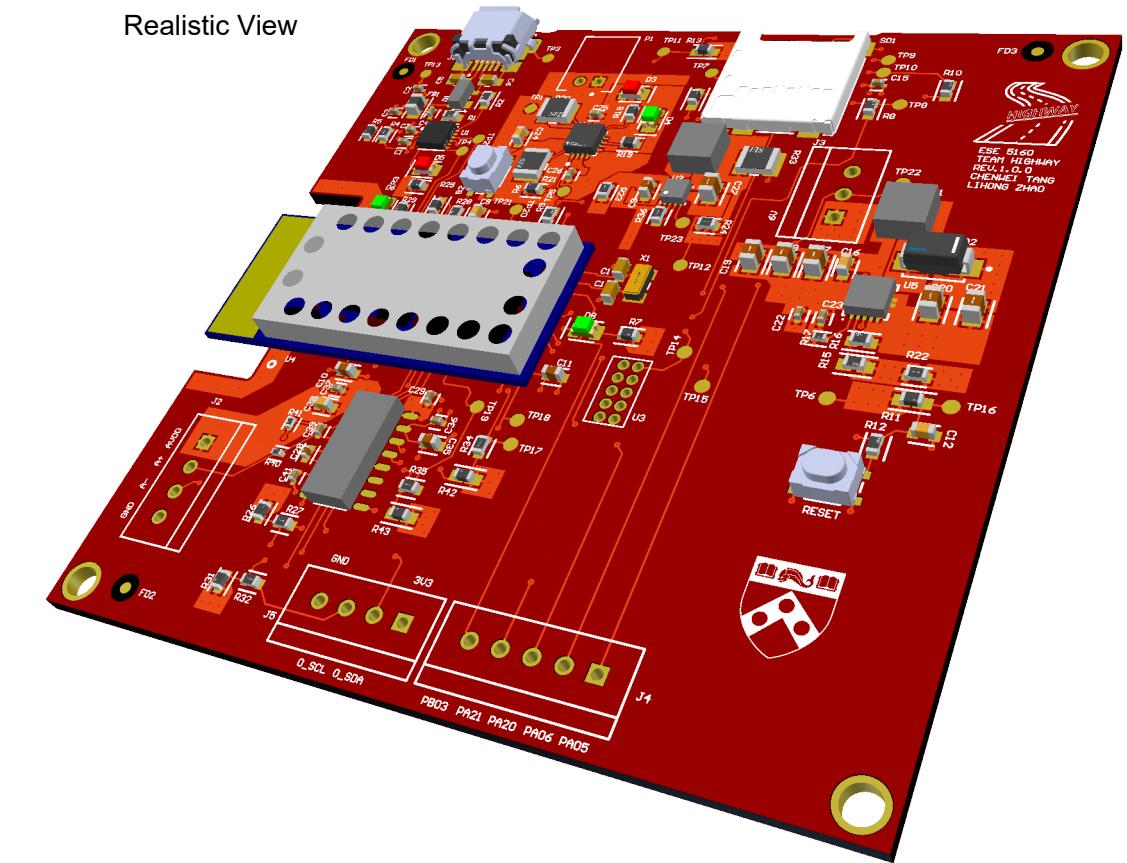
E

F

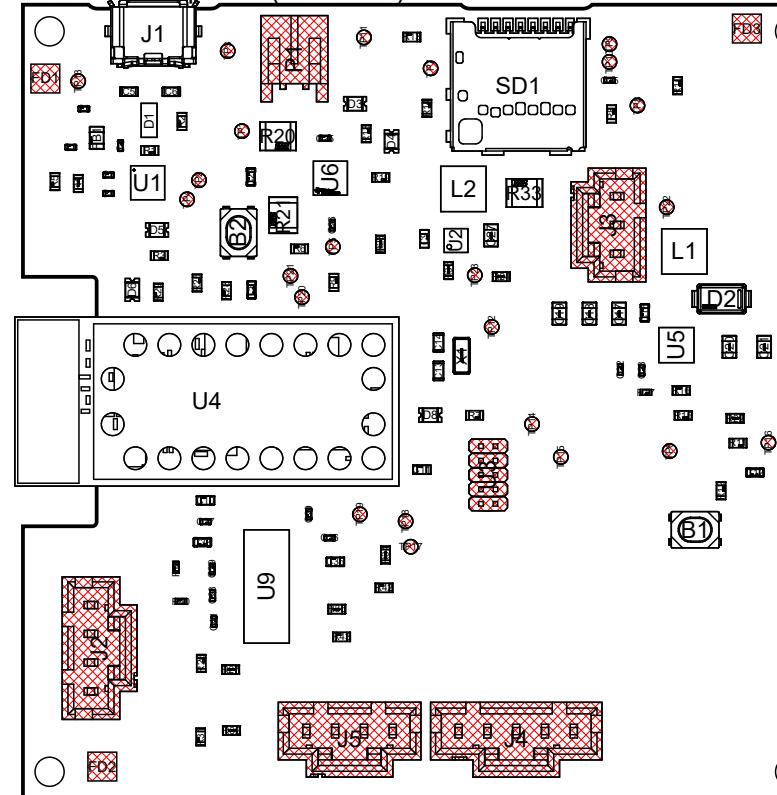
REV STATUS OF SHEETS		REV				
SHEET						
1						
2						
3						
4						

REVISIONS		DESCRIPTION	DATE	APPROVED

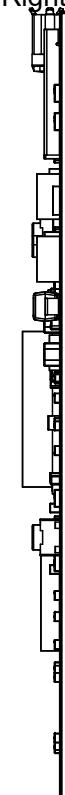
Realistic View



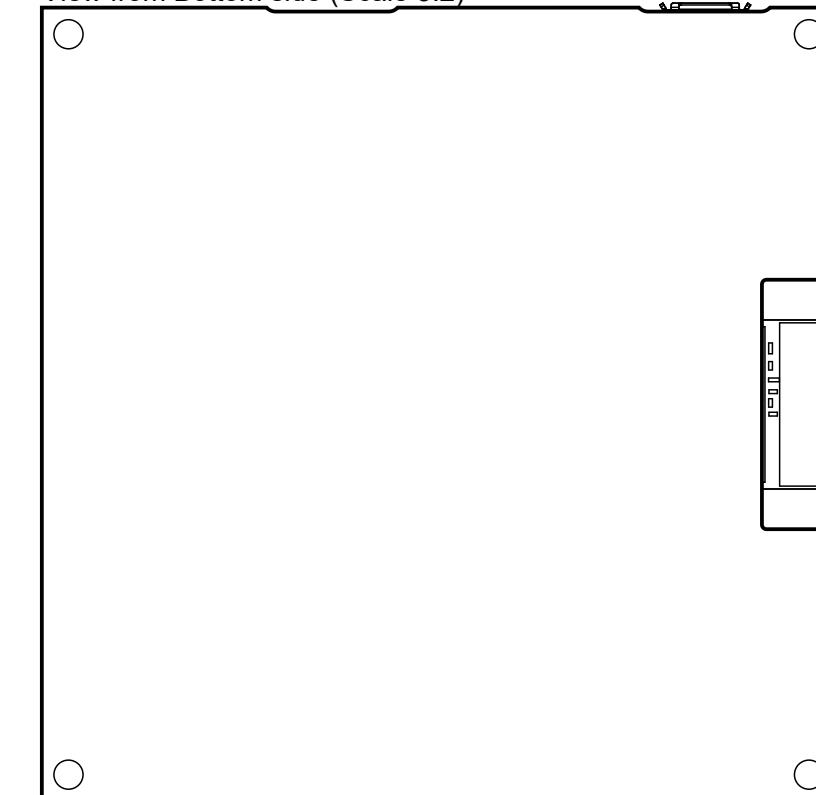
View from Top side (Scale 3:2)



View from Right side (Scale 3:2)



View from Bottom side (Scale 3:2)



PART NO: =PCB_PART_NUMBER

APPROVALS

DATE

ENGINEER:

CHENWEI TANG

02/28/2023

DESIGNER:

LIHONG ZHAO

LIHONG

CHECKER:

YIANG GONG

YIANG

Reference Documents

BOM DOC: ESE516_ExampleProject.

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: MAIN.SchDoc

NEXT ASSY

USED ON

PCB DOC: ESE516_PCB.PcbDoc

APPLICATION

Altium
TM

 ADDRESS 1
 ADDRESS 2
 ADDRESS 3
 ADDRESS 4

 DESIGN ITEM: .Item
 DESIGN ITEM REVISION: .ItemRevision

=PCB_TITLE_2

 SIZE: CAGE CODE: DWG NO:
B =CAGE_CO

REV:

SCALE: FILE NAME: StarterBoardAssembly.PcbDwf SHEET: 1 OF 3

A

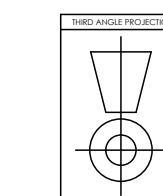
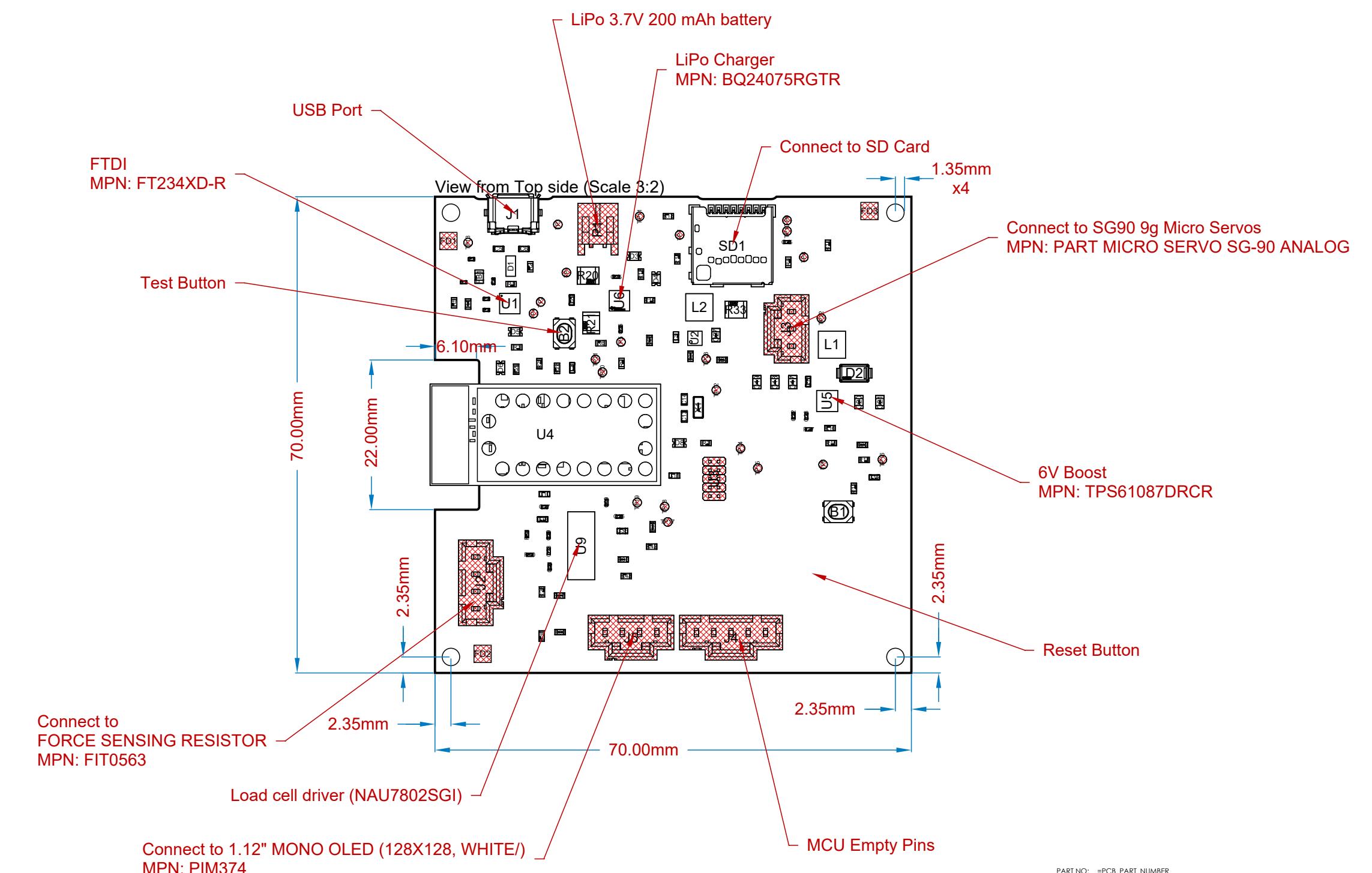
B

C

D

E

F



PART NO: =PCB_PART_NUMBER			
APPROVALS		DATE	
ENGINEER:	CHENWEI TANG	02/28/2023	
DESIGNER:	LIHONG ZHAO	LIHONG	
CHECKER:	YIANG GONG	YIANG	
Reference Documents			
BOM DOC: ESE516_ExampleProject.			
ASSY DOC: =DOC_NO_FAB_DWG			
SCH DOC: MAIN.SchDoc			
PCB DOC: ESE516_PCB.PcbDoc			
		ADDRESS 1 ADDRESS 2 ADDRESS 3 ADDRESS 4	
DESIGN ITEM: .Item		DESIGN ITEM REVISION: .ItemRevision	
TITLE: =PCB_TITLE_2			
SIZE:	CAGE CODE:	DWG NO:	REV:
B	=CAGE_CO		
SCALE:	FILE NAME:	StarterBoardAssembly.PCBDwf	SHEET: 2 OF 3

B

C

D

E

F

Manufacturing Notes

Four (4) Layers

Dimensions: 70mmx70mm

Thickness: 1.53mm

Material: PP-006; Core-009

All layers are unmirrored - should be able to "see straight through"

Scoring: Yes

Finished Thickness: 1.53mm

Surface Finish: ENEPIG

Gold Fingers: Yes

Outer Layer Finish Copper: 1oz

Inner Copper: 0.5oz

Number of Holes Per Board: 295

Minimum Hole size: 0.20mm

Minimum Trace (Outer layer): 6mil

Minimum Space (Outer layer): 6mil

Minimum Trace (Inner layer): None (no Trace)

Minimum Space (Inner layer): None (no Trace)

Solder Mask: Yes

Solder Mask Sides: Top and Bottom

Solder Mask Color: Red

Solder Mask Type: LPI

Solder Mask Finish: Standard (Semi-Gloss)

Silk Screen: Yes

Logo Allowed: Silk Screen

Silk Screen Sides: Top and bottom

Silk Screen Color: N/A

Internal Slots: No

Counter Sink: No

Counter Bore: No

Edge Plating: No

Route and Retain: N/A

Scoring: N/A

Controlled Impedance: No

Controlled Dielectric: No

Thru-Hole Via in Pad: No

Thickness Tolerance: +/-10%

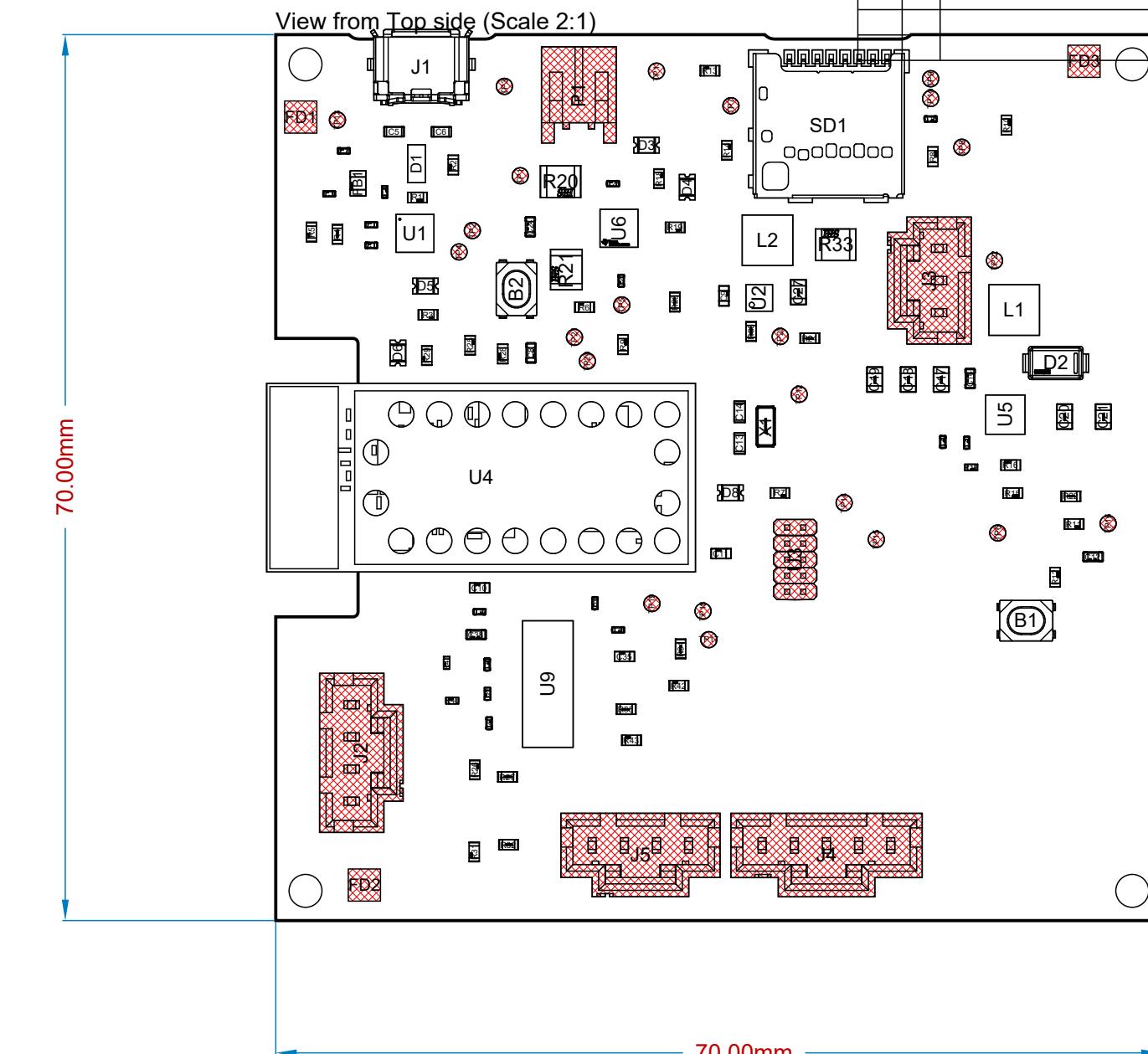
UL Marking Required: No

Rohs Marking: No

ITAR?: No

Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Surface Material	Top Overlay			Legend	GTO
	Copper	Top Solder	0.03mm	Solder Resist	Solder Mask	GTS
	Copper	Top Layer	0.04mm		Signal	GTL
	Prepreg		0.33mm	PP-006	Dielectric	
	CF-004	GroundPlane	0.02mm		Signal	G1
	Core		0.71mm	Core-009	Dielectric	
	CF-004	PowerPlane	0.02mm		Signal	G2
	Prepreg		0.33mm	PP-006	Dielectric	
	Copper	Bottom Layer	0.04mm		Signal	GBL
	Surface Material	Bottom Solder	0.03mm	Solder Resist	Solder Mask	GBS
		Bottom Overlay			Legend	GBO
	Total thickness: 1.53mm					



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	 DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision TITLE: =PCB_TITLE_1 =PCB_TITLE_2 SIZE: CAGE CODE: DWG NO: B =CAGE_CO REV: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 1 OF 12
ENGINEER: CHENWEI TANG	CHENWEI		
DESIGNER: LIHONG ZHAO	LIHONG		
CHECKER: YIANG GONG	YIANG		
Reference Documents			
BOM DOC: ESE516_ExampleProject.			
ASSY DOC: =DOC_NO_FAB_DWG			
SCH DOC:	MAIN.SchDoc		
PCB DOC:	ESE516_PCB.PcbDoc		
APPLICATION			

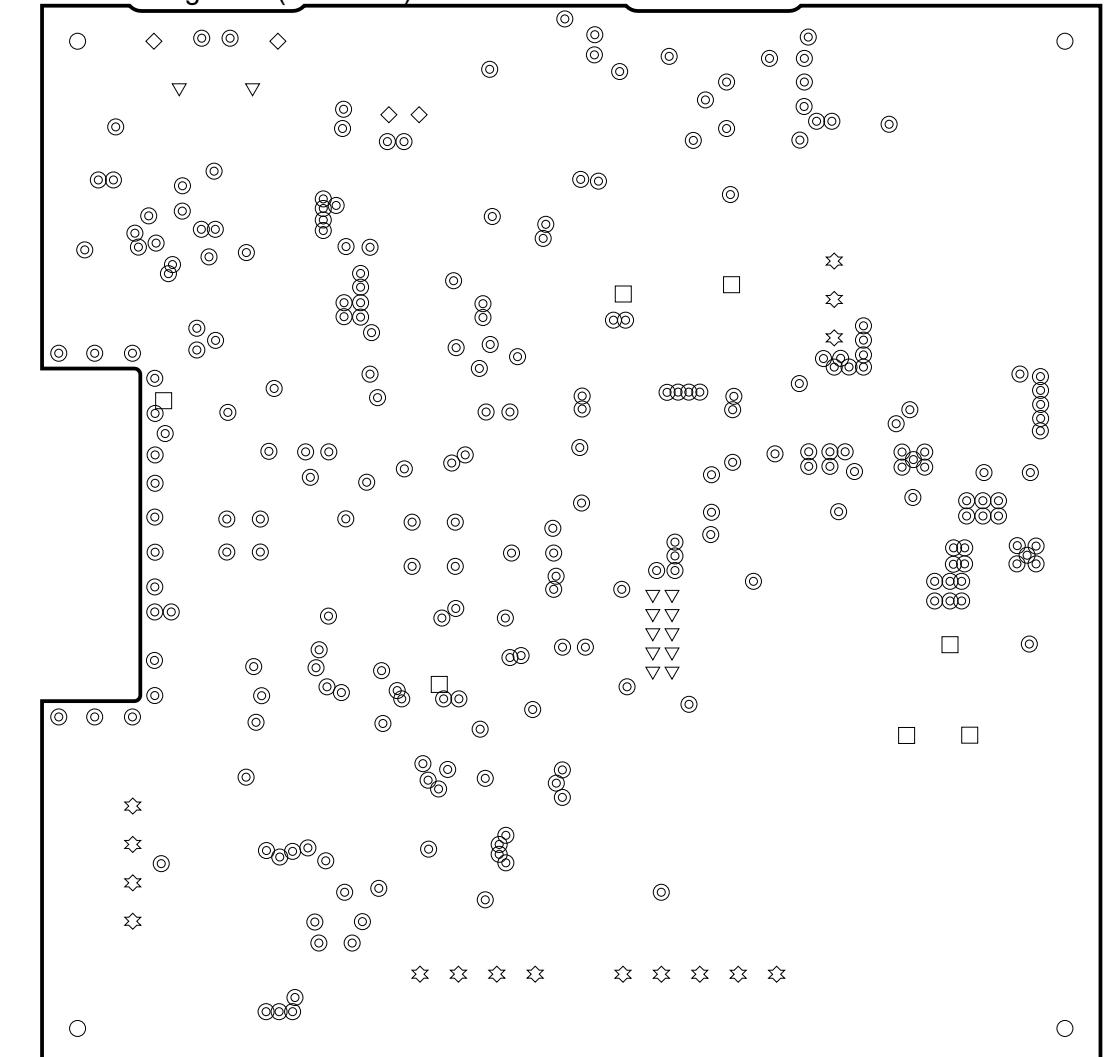
REV STATUS OF SHEETS		REV							
SHEET									

DWG NO.: =DOC_NO_ASSY_DWG	REV: .lfe	REVISIONS	DESCRIPTION	DATE	APPROVED

1 Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
□	7	0.20mm	Plated	
○	252	0.20mm	Plated	
▽	12	0.65mm	Plated	
◇	4	0.70mm	Plated	
✖	16	0.89mm	Plated	
○	4	2.70mm	Plated	
295 Total				

2 Drill Drawing View (Scale 2:1)



3 PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: CHENWEI TANG CHENWEI

DESIGNER: LIHONG ZHAO LIHONG

CHECKER: YIANG GONG YIANG

Reference Documents

BOM DOC: ESE516_ExampleProject.

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: MAIN.SchDoc

NEXT ASSY USED ON PCB DOC:

APPLICATION ESE516_PCB.PcbDoc

4 ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4

Altium™

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: =PCB_TITLE_1

=PCB_TITLE_2

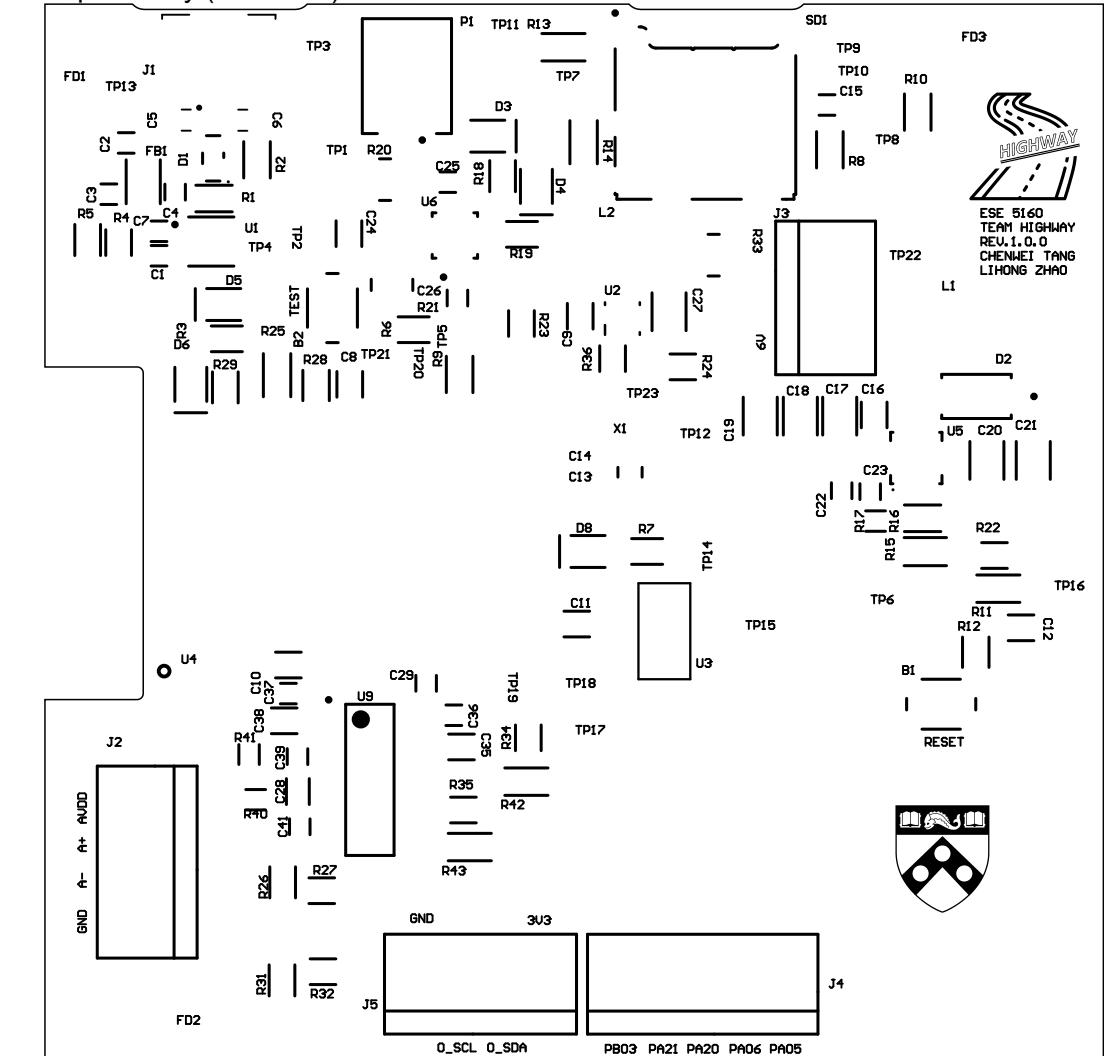
SIZE: CAGE CODE: DWG NO:

B =CAGE_CO

REV:



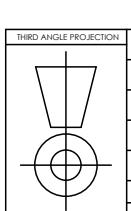
Top Overlay (Scale 2:



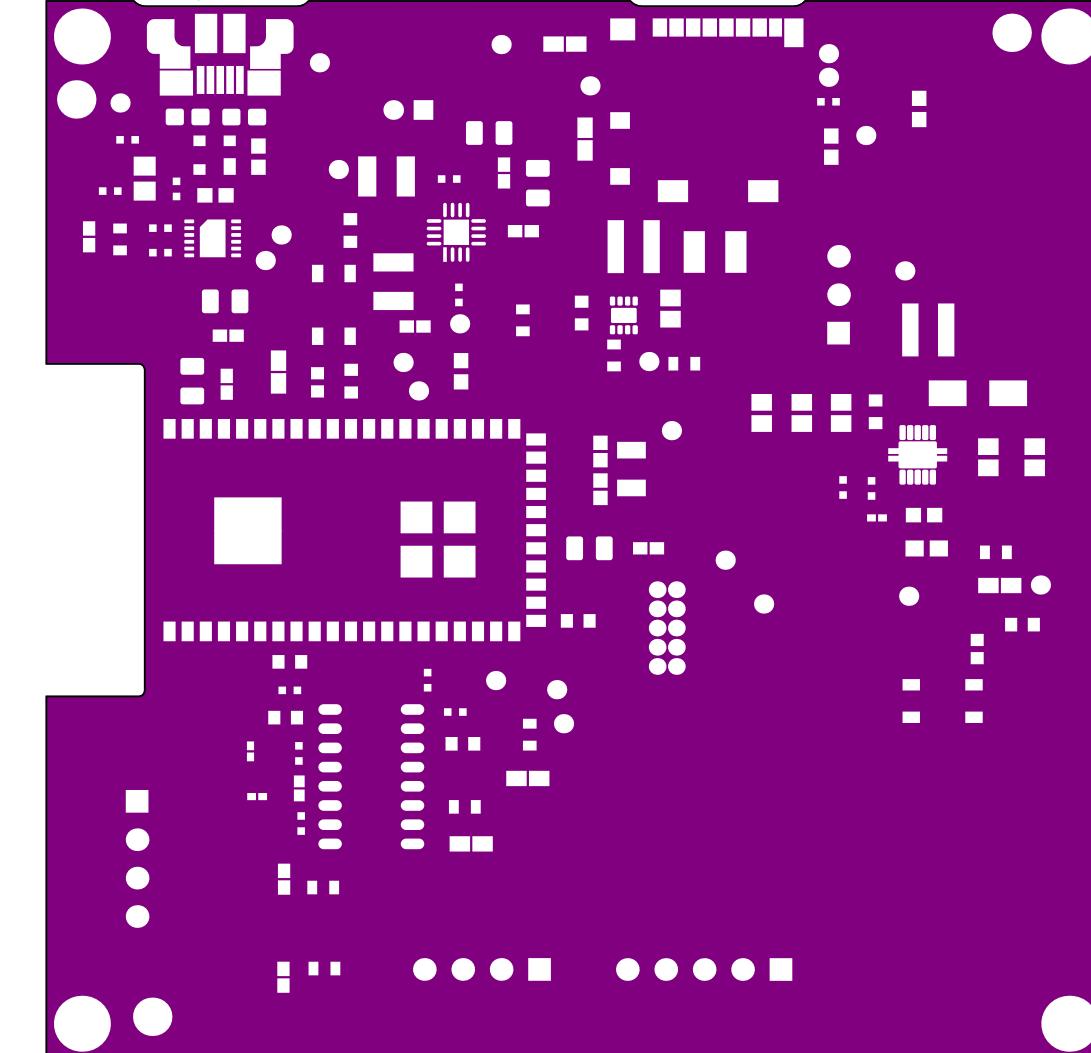
PART NO.: -PCB PART NUMBER

APPROVALS		DATE	
ENGINEER:	CHENWEI TANG	CHENWEI	
DESIGNER:	LIHONG ZHAO	LIHONG	
CHECKER:	YIANG GONG	YIANG	DESIGN
Reference Documents			TITLE:
BOM DOC:	ESE516_ExampleProject.		
ASSY DOC:	=DOC_NO_FAB_DWG		
SCH DOC:	MAIN.SchDoc		
PCB DOC:	ESE516_PCB.PcbDoc		

Altium ™		ADDRESS 1 ADDRESS 2 ADDRESS 3 ADDRESS 4
ITEM: .Item		DESIGN ITEM REVISION: .ItemRevision
=PCB_TITLE_1 =PCB_TITLE_2		
CAGE CODE: =CAGE_CO	DWG NO:	R
FILE NAME: StarterBoardFabrication.PCDBdwf	SHEET: 3	OF 1



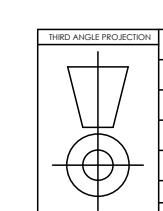
Top Solder (Scale 2:1)



It

PART NO: =PCB PART NUMBER

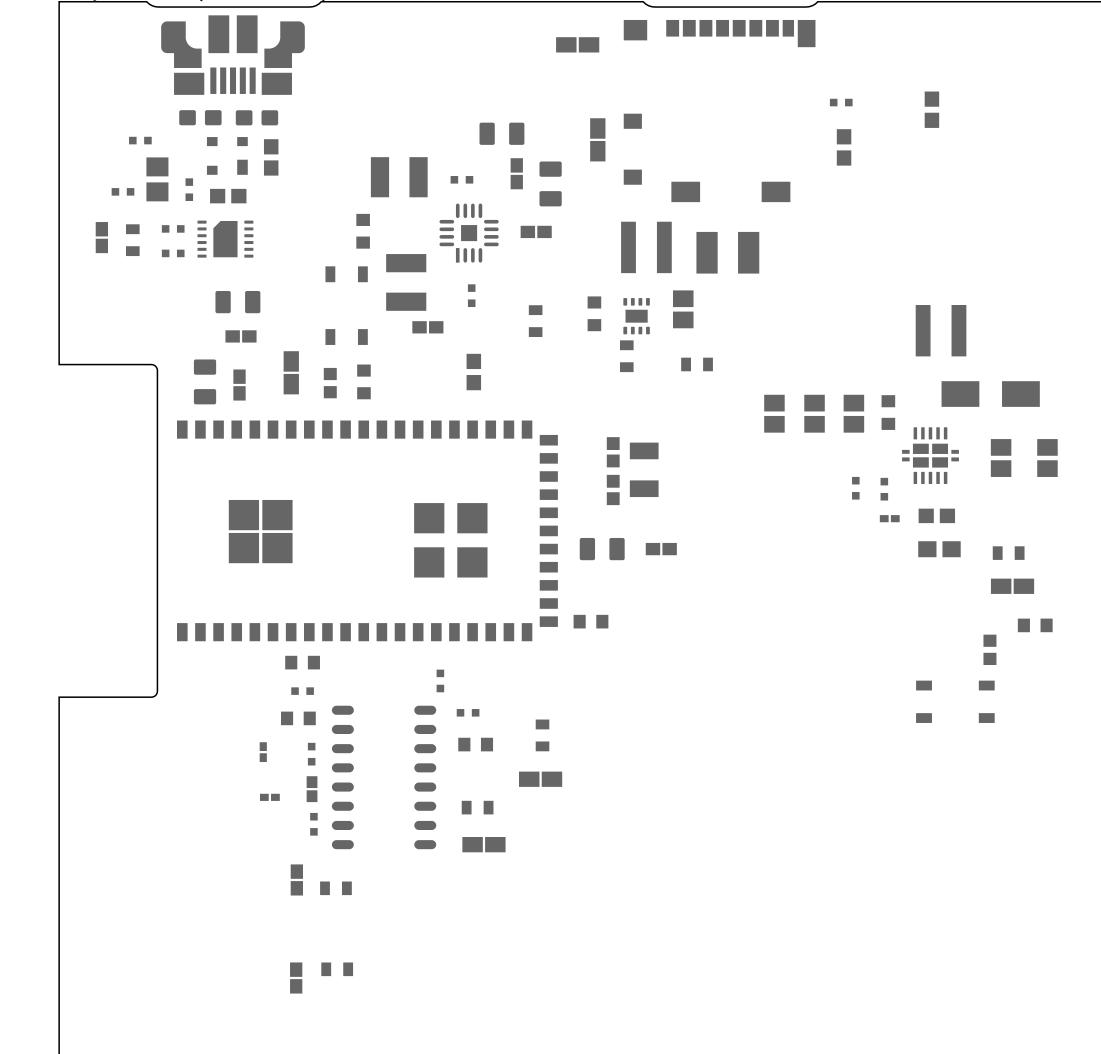
PART NO.: -PCB PART NUMBER			
APPROVALS	DATE		
ENGINEER:	CHENWEI TANG		
DESIGNER:	LIHONG ZHAO		
CHECKER:	YIANG GONG		
Reference Documents			
BOM DOC:	ESE516_ExampleProject.		
ASSY DOC:	=DOC_NO_FAB_DWG		
SCH DOC:	MAIN.SchDoc		
PCB DOC:	ESE516_PCB.PcbDoc		
DESIGN ITEM:		.Item	DESIGN ITEM REVISION:
TITLE:		=PCB_TITLE_1 =PCB_TITLE_2	
SIZE:	CAGE CODE: B =CAGE_CO		DWG NO:
SCALE:	FILE NAME: StarterBoardFabrication.PCDBdwf		REV: 4 OF 12



DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		
DESCRIPTION	DATE	APPROVED

Top Paste (Scale 2:1)



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	Altium ADDRESS 1 ADDRESS 2 ADDRESS 3 ADDRESS 4
ENGINEER: CHENWEI TANG	CHENWEI		
DESIGNER: LIHONG ZHAO	LIHONG		
CHECKER: YIANG GONG	YIANG		
Reference Documents			
BOM DOC: ESE516_ExampleProject.			DESIGN ITEM: .Item
ASSY DOC: =DOC_NO_FAB_DWG			DESIGN ITEM REVISION: .ItemRevision
SCH DOC: MAIN.SchDoc			TITLE: =PCB_TITLE_1 =PCB_TITLE_2
PCB DOC: ESE516_PCB.PcbDoc			SIZE: CAGE CODE: DWG NO: REV:
APPLICATION			B =CAGE_CO
NEXT ASSY	USED ON		SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 5 OF 12

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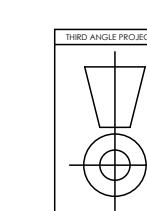
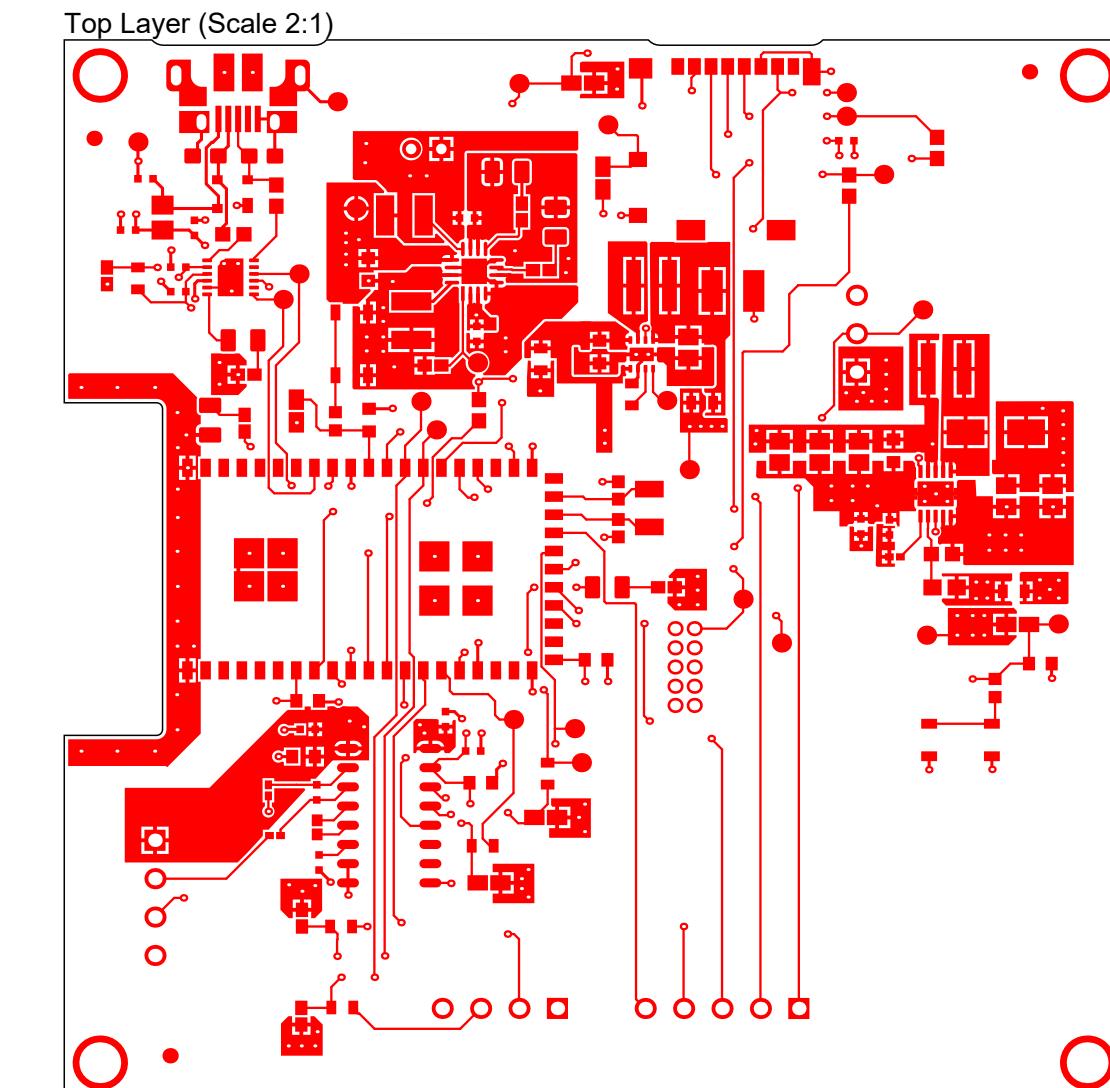
E

F

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DWG NO:	=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET		

REVISIONS		DESCRIPTION	DATE	APPROVED



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: CHENWEI TANG CHENWEI

DESIGNER: LIHONG ZHAO LIHONG

CHECKER: YIANG GONG YIANG

Reference Documents

BOM DOC: ESE516_ExampleProject.

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: MAIN.SchDoc

NEXT ASSY USED ON

PCB DOC: ESE516_PCB.PcbDoc

APPLICATION

Altium
TM

ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4

TITLE: .Item

DESIGN ITEM REVISION: .ItemRevision

=PCB_TITLE_1

=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO:

B =CAGE_CO

REV:

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf

SHEET: 6 OF 12

A

B

C

D

E

F

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DWG NO: =DOC_NO_ASSY_.lfe

4

A

B

C

D

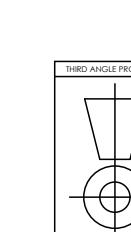
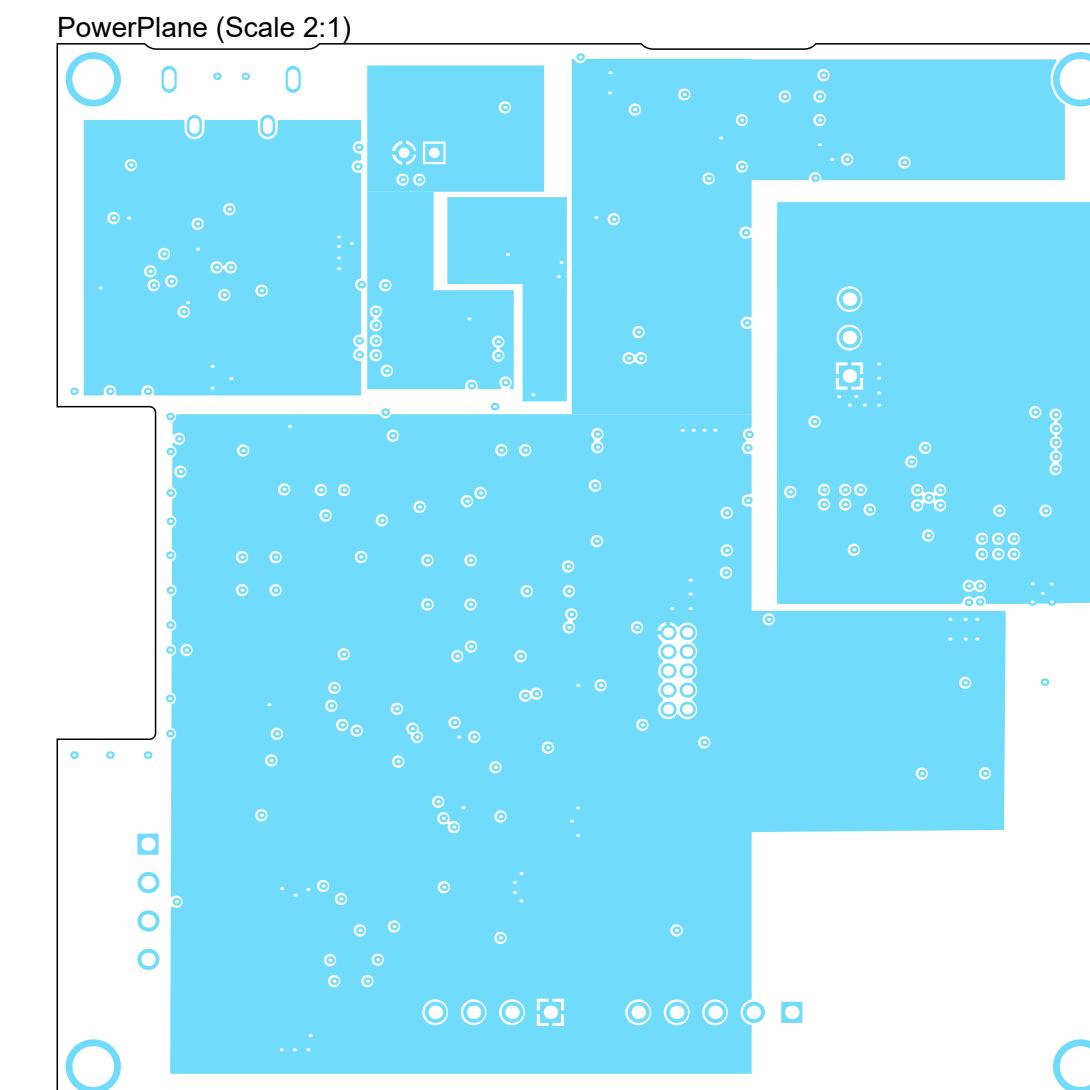
E

F

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DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		DESCRIPTION	DATE	APPROVED



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: CHENWEI TANG CHENWEI

DESIGNER: LIHONG ZHAO LIHONG

CHECKER: YIANG GONG YIANG

Reference Documents

BOM DOC: ESE516_ExampleProject.

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: MAIN.SchDoc

NEXT ASSY USED ON

PCB DOC: ESE516_PCB.PcbDoc

APPLICATION

AltiumTMADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: =PCB_TITLE_1

=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO:

B =CAGE_CO REV:

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 7 OF 12

A

B

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DWG NO:
=DOC_NO_ASSY_.lfe

REV:

.lfe

A

B

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D

E

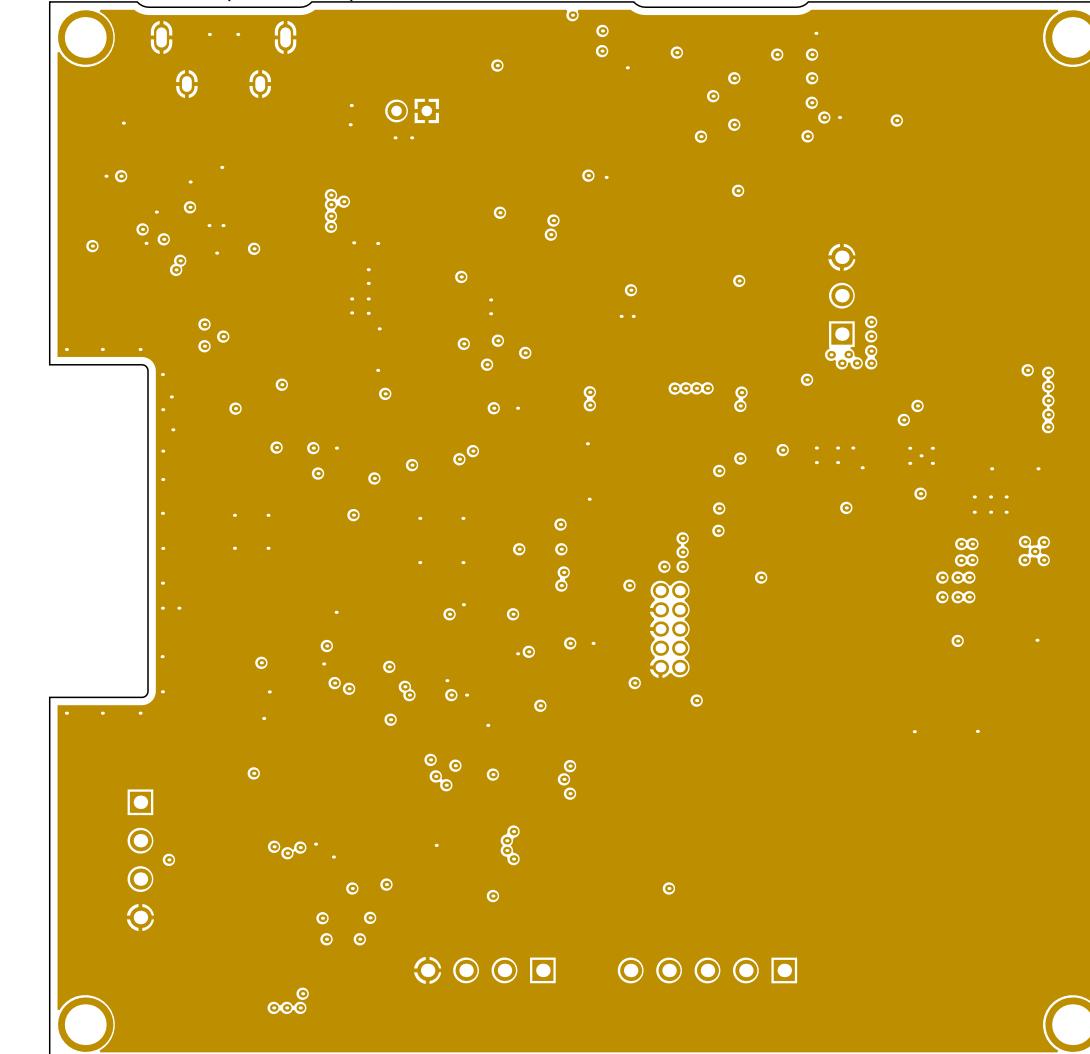
F

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DWG NO:	=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET		

REVISIONS		DESCRIPTION	DATE	APPROVED

GroundPlane (Scale 2:1)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: CHENWEI TANG CHENWEI

DESIGNER: LIHONG ZHAO LIHONG

CHECKER: YIANG GONG YIANG

Reference Documents

BOM DOC: ESE516_ExampleProject.

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: MAIN.SchDoc

NEXT ASSY PCB DOC: ESE516_PCB.PcbDoc

USED ON APPLICATION

AltiumTMADDRESS 1
ADDRESS 2

ADDRESS 3

ADDRESS 4

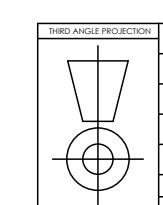
TITLE: .Item
=PCB_TITLE_1
=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO:

B =CAGE_CO REV:

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf

8 OF 12



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B

C

D

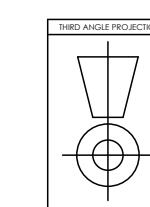
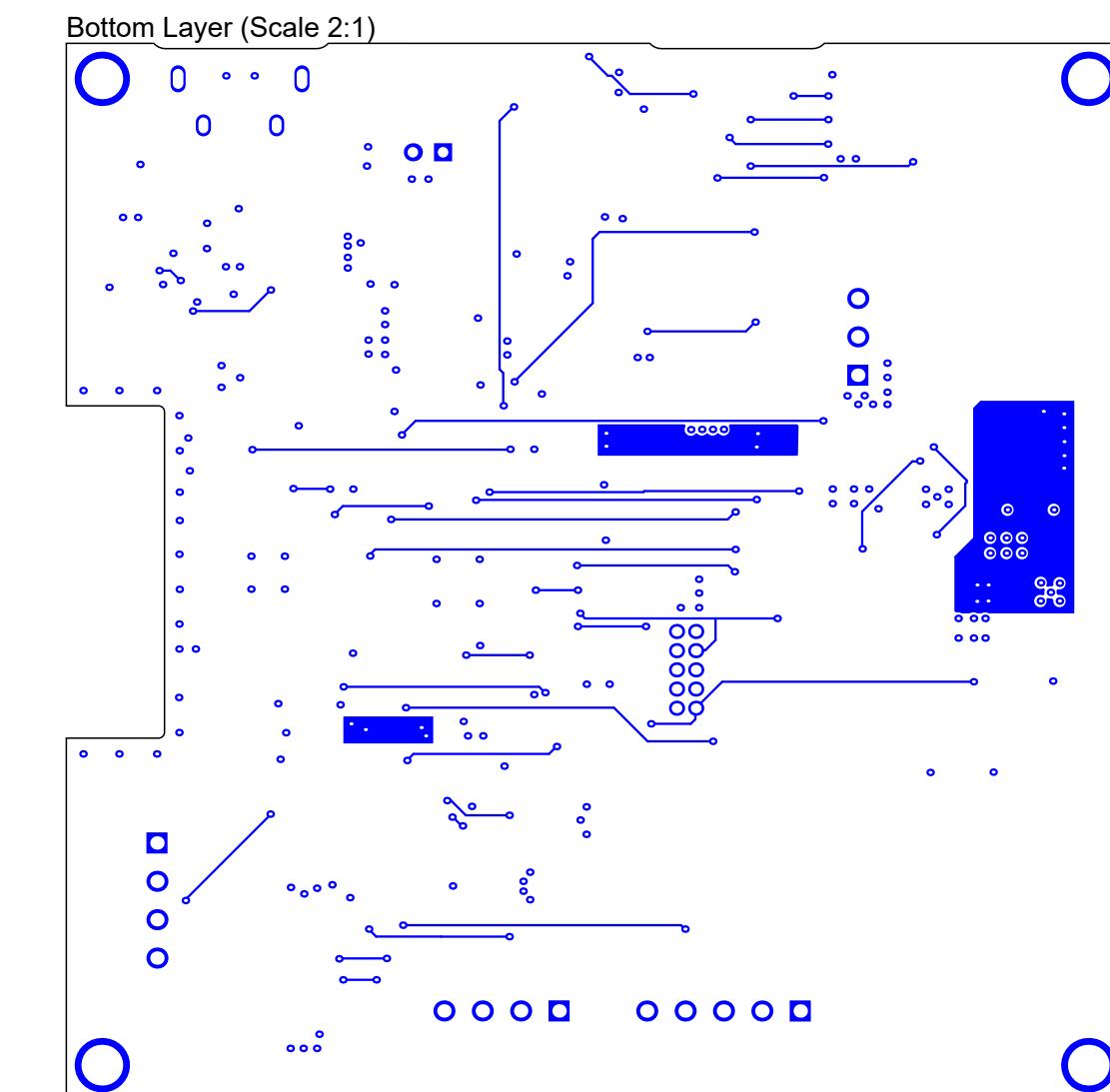
E

F

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REV STATUS OF SHEETS		REV						DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET									

REVISIONS		DESCRIPTION	DATE	APPROVED



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: CHENWEI TANG CHENWEI

DESIGNER: LIHONG ZHAO LIHONG

CHECKER: YIANG GONG YIANG

Reference Documents

BOM DOC: ESE516_ExampleProject.

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: MAIN.SchDoc

NEXT ASSY USED ON PCB DOC: ESE516_PCB.PcbDoc

APPLICATION

AltiumTMADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4

TITLE: .Item DESIGN ITEM REVISION: .ItemRevision

=PCB_TITLE_1

=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO:

B =CAGE_CO REV:

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 9 OF 12

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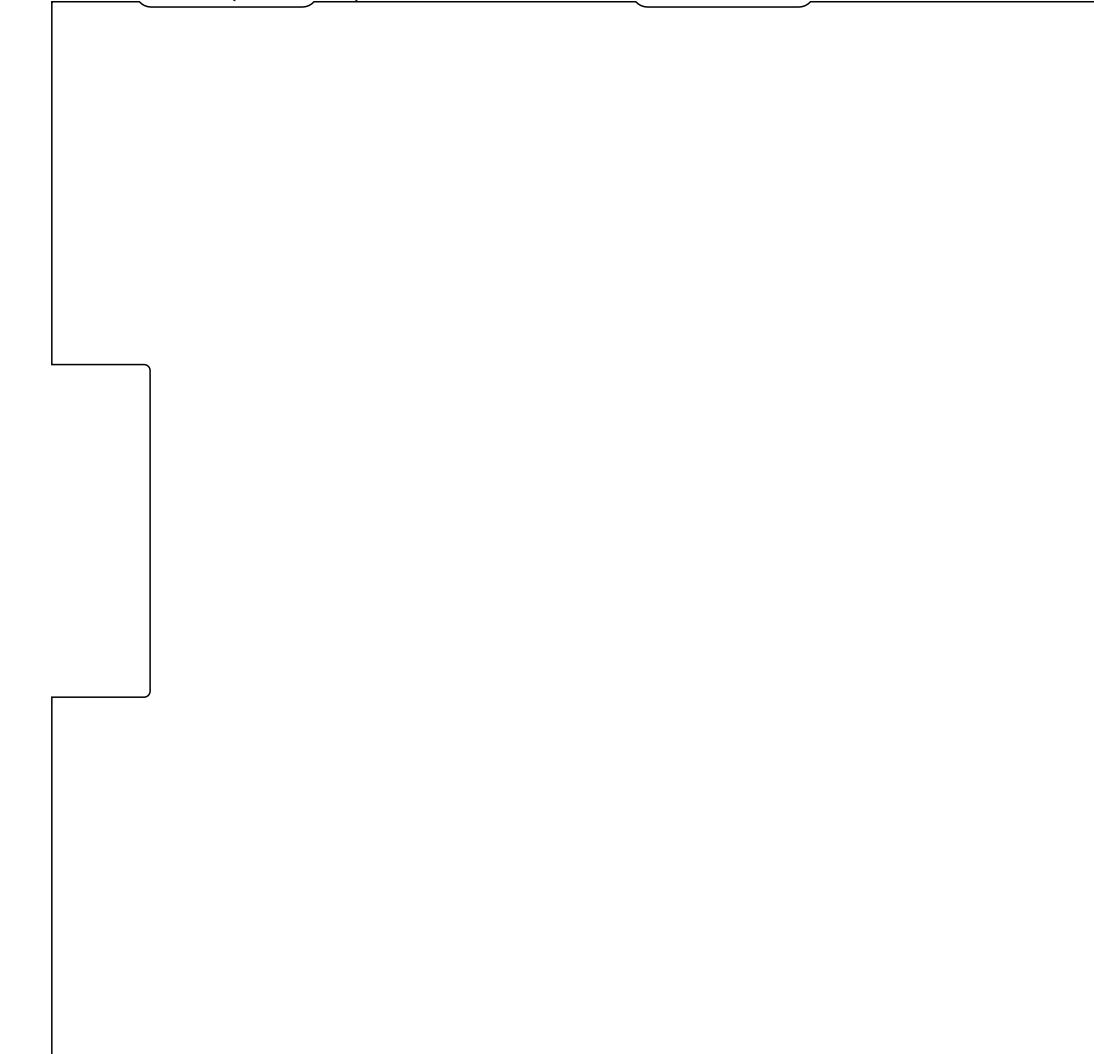
D

E

F

DWG NO: =DOC_NO_ASSY_DWG		REV: .lfe	REVISIONS		
REV STATUS OF SHEETS	SHEET	ZONE	REV	DESCRIPTION	DATE

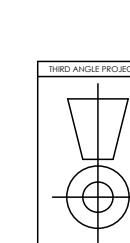
Bottom Paste (Scale 2:1)



.lt

DWG NO:
=DOC_NO_ASSY_

.lfe



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: CHENWEI TANG CHENWEI

DESIGNER: LIHONG ZHAO LIHONG

CHECKER: YIANG GONG YIANG

Reference Documents

BOM DOC: ESE516_ExampleProject.

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: MAIN.SchDoc

NEXT ASSY USED ON PCB DOC: ESE516_PCB.PcbDoc

APPLICATION

Altium
TM

ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: =PCB_TITLE_1

=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO:

B =CAGE_CO

REV:

10 OF 12

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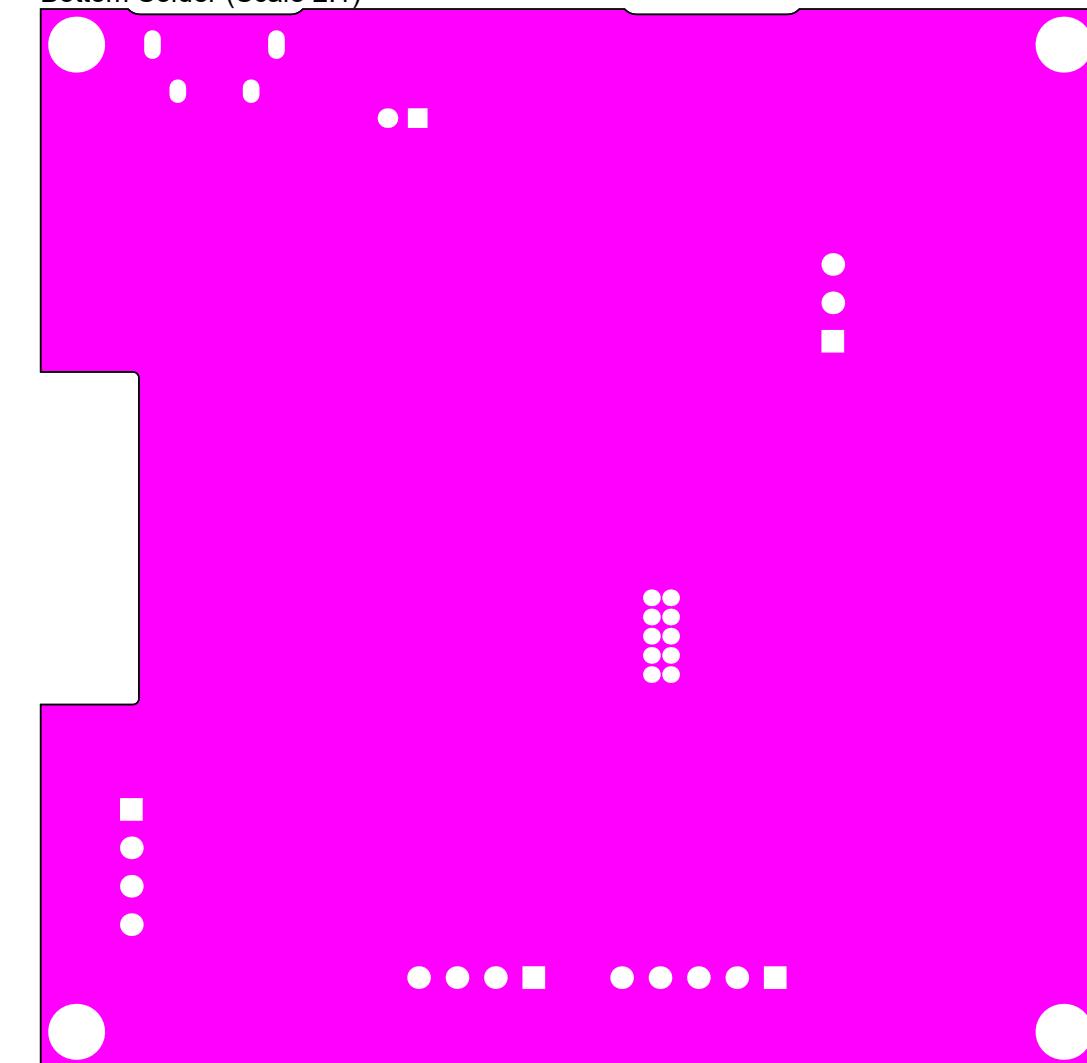
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Bottom Solder (Scale 2:1)

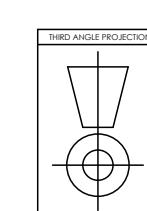


.It

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PART NO: =PCB PART NUMBER

PART NO.: =PCB_PART_NUMBER		Altium ™		ADDRESS 1 ADDRESS 2 ADDRESS 3 ADDRESS 4
APPROVALS	DATE			
ENGINEER:	CHENWEI TANG	CHENWEI		
DESIGNER:	LIHONG ZHAO	LIHONG		
CHECKER:	YIANG GONG	YIANG		
Reference Documents				
BOM DOC: ESE516_ExampleProject.				
ASSY DOC: =DOC_NO_FAB_DWG				
SCH DOC: MAIN.SchDoc				
PCB DOC: ESE516_PCB.PcbDoc				
DESIGN ITEM: .Item		DESIGN ITEM REVISION: .ItemRevision		
TITLE: =PCB_TITLE_1 =PCB_TITLE_2				
SIZE: B	CAGE CODE: =CAGE_CO	DWG NO:		REV:
SCALE:	FILE NAME: StarterBoardFabrication.PCDBdwf	SHEET: 11 OF 12		



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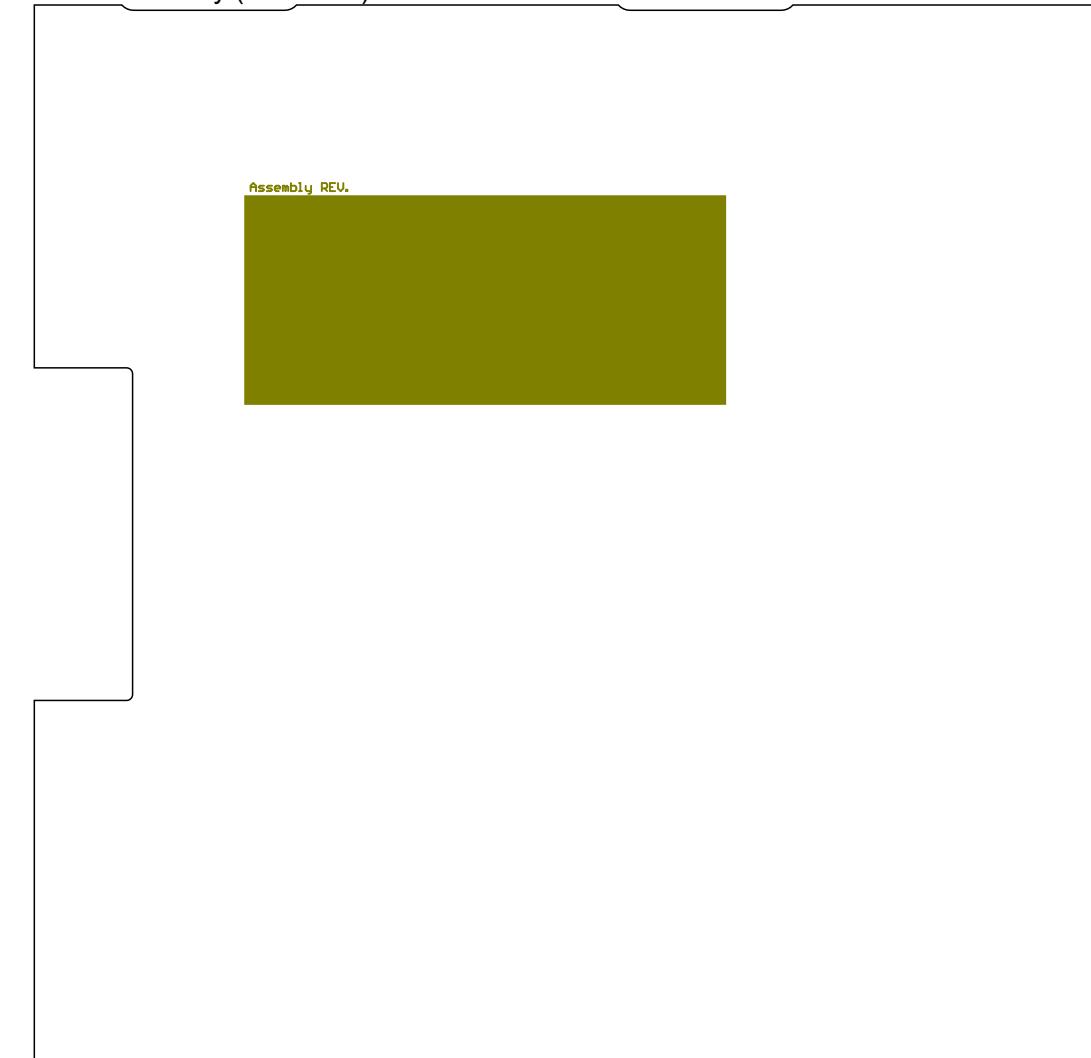
F

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DWG NO. =DOC_NO_ASSY_DWG	REV. .lfe

REVISIONS		
DESCRIPTION	DATE	APPROVED

Bottom Overlay (Scale 2:1)



PART NO: =PCB_PART_NUMBER	ADDRESS 1
APPROVALS	DATE
ENGINEER: CHENWEI TANG	CHENWEI
DESIGNER: LIHONG ZHAO	LIHONG
CHECKER: YIANG GONG	YIANG
DESIGN ITEM: .Item	
DESIGN ITEM REVISION: .ItemRevision	
TITLE: =PCB_TITLE_1	
=PCB_TITLE_2	
SIZE: CAGE CODE: B	DWG NO: =CAGE_CO
REV: .lfe	
SCALE: 1:1	FILE NAME: StarterBoardFabrication.PCBDwf
SHOOT: 12 OF 12	

Altium

TM

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DWG NO.
=DOC_NO_ASSY_

.lfe

DWG NO.
=DOC_NO_FAB_DWG

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