OPT3001 环境光传感器 (ALS)

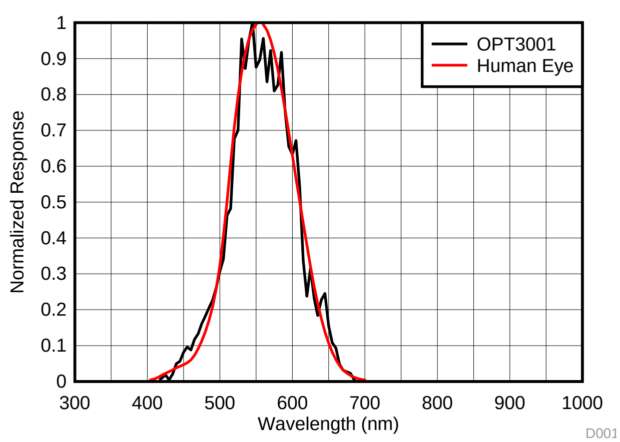
1 特性

- 采用精密光学滤波，可与人眼相匹配：
  – 可阻隔 99%（典型值）以上的红外线 (IR)
- 自动满量程设置功能可简化软件并确保进行适当配置
- 测量范围：0.01 Lux 至 83,000 Lux
- 23 位有效动态范围，
  支持自动设置增益范围
- 12 种二进制权满量程范围设置：范围间匹配程度 < 0.2%（典型值）
- 低工作电流：1.8μA（典型值）
- 工作温度范围：-40°C 至 +85°C
- 宽电源范围：1.6V 至 3.6V
- 可耐受 5.5V 电压的 I/O
- 灵活的中断系统
- 小封装尺寸：2.0mm x 2.0mm x 0.65mm

2 应用

- 显示屏背光控制
- 照明控制系统
- 平板电脑和笔记本电脑
- 温度调节装置和家庭自动化电器
- 销售点终端
- 室外的交通灯和街灯
- 摄像机

频谱响应：**OPT3001** 和人眼



3 说明

OPT3001 传感器用于测量可见光的密度。传感器的光谱响应与人眼的视觉响应紧密匹配，其中具有很高的红外线阻隔。

OPT3001 是一款可如人眼般测量光强的单芯片照度计。OPT3001 器件兼具精密的频谱响应和较强的 IR 阻隔功能，因此能够如人眼般准确测量光强且不受光源影响。对于为追求美观效果而需要将传感器安装在深色玻璃下的工业设计而言，较强的 IR 阻隔功能还有助于保持高精度。OPT3001 专门针对构建基于光线的人眼般体验的系统而设计，是人眼匹配度低且红外阻隔能力差的光电二极管、光敏电阻或其它环境光传感器的首选理想替代产品。

测量范围可达 0.01lux 至 83k lux，且内置有满量程设置功能，无需手动选择满量程范围。此功能允许在 23 位有效动态范围内进行光测量。

数字操作可灵活用于系统集成。测量既可连续进行也可单次触发。控制和中断系统 具有 自主操作功能，允许处理器在传感器搜索相应唤醒事件并通过中断引脚进行报告时处于休眠状态。数字输出通过 I^2C 以及 SMBus 兼容的两线制串口报告。

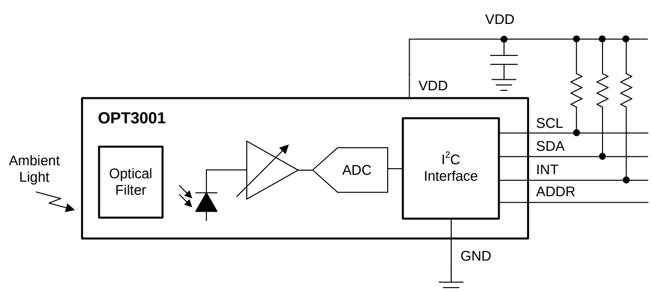
OPT3001 兼具低功耗和低电源电压特性，可延长电池供电系统的电池寿命。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPT3001	USON (6)	2.00mm x 2.00mm

(1) 要了解所有可用封装，请见数据表末尾的封装选项附录。

框图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (December 2014) to Revision C — **Page**

- 已添加 *接收文档更新通知和社区资源* 34

Changes from Revision A (October 2014) to Revision B — **Page**

- Changed Handling Ratings table to ESD Ratings table 4
- Added missing link to *Electrical Interface* section in *Serial Interface* section 12
- Added application information to *Application and Implementation* section 27
- 向相关文档 部分添加了新文档 34
- 添加了*关于焊接和处理的相关建议*部分 34

Changes from Original (July 2014) to Revision A — **Page**

- 将数据表从产品预览更改成了生产数据 1

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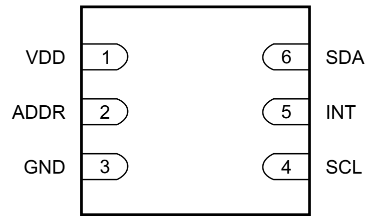
5 Pin Configuration and Functions

DNP Package
6-Pin USON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VDD	Power	设备电源。 连接到1.6V 至3.6V 电源。
2	ADDR	Digital input	地址引脚。 该引脚设置I2C 地址的LSB 。
3	GND	Power	Ground
4	SCL	Digital input	I2C 时钟。 使用10k 电阻器连接到1.6V 至5.5V 电源。
5	INT	Digital output	中断输出开漏。 使用10k 电阻器连接到1.6V 至5.5V 电源。
6	SDA	Digital input/output	I2C 数据。 使用10k 电阻器连接到1.6V 至5.5V 电源。

6 Specifications

6.1 Absolute Maximum Ratings

See [1]

		MIN	MAX	UNIT
Voltage	VDD to GND	–0.5	6	V
	SDA, SCL, INT, and ADDR to GND	–0.5	6	V
Current into any pin			10	mA
Temperature	Junction		150	°C
	Storage, T_{stg}	–65	+150 [2]	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Long exposure to temperatures higher than 105°C can cause package discoloration, spectral distortion, and measurement inaccuracy.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Operating temperature	–40		85	°C
Operating power-supply voltage	1.6		3.6	V

6.4 Thermal Information

THERMAL METRIC [1]		OPT3001 DNP (USON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	17.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CT = 1)[1], automatic full-scale range (RN[3:0] = 1100b[1]), white LED, and normal-angle incidence of light, unless otherwise specified.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPTICAL							
	Peak irradiance spectral responsivity				550		nm
	Resolution (LSB)	Lowest full-scale range, RN[3:0] = 0000b[1]			0.01		lux
	Full-scale illuminance				83865.6		lux
	Measurement output result	0.64 lux per ADC code, 2620.80 lux full-scale (RN[3:0] = 0110)[1], 2000 lux input[2]		2812	3125	3437	ADC codes
				1800	2000	2200	lux
	Relative accuracy between gain ranges[3]				0.2%		
	Infrared response (850 nm)[2]				0.2%		
	Light source variation (incandescent, halogen, fluorescent)	Bare device, no cover glass			4%		
	Linearity	Input illuminance > 40 lux			2%		
		Input illuminance < 40 lux			5%		
	Measurement drift across temperature	Input illuminance = 2000 lux			0.01		%/°C
	Dark condition, ADC output	0.01 lux per ADC code			0	3	ADC codes
					0	0.03	lux
	Half-power angle	50% of full-power reading			47		degrees
PSRR	Power-supply rejection ratio	V_{DD} at 3.6 V and 1.6 V			0.1		%/V[4]
POWER SUPPLY							
V_{DD}	Operating range			1.6		3.6	V
V_{I^2C}	Operating range of I^2C pull-up resistor	I^2C pull-up resistor, $V_{DD} \leq V_{I^2C}$		1.6		5.5	V
I_Q	Quiescent current	Dark	Active, V_{DD} = 3.6 V		1.8	2.5	µA
			Shutdown (M[1:0] = 00)[1], V_{DD} = 3.6 V		0.3	0.47	µA
		Full-scale lux	Active, V_{DD} = 3.6 V		3.7		µA
			Shutdown, (M[1:0] = 00)[1]		0.4		µA
POR	Power-on-reset threshold	T_A = 25°C			0.8		V
DIGITAL							
	I/O pin capacitance				3		pF
	Total integration time[5]	(CT = 1)[1], 800-ms mode, fixed lux range		720	800	880	ms
		(CT = 0)[1], 100-ms mode, fixed lux range		90	100	110	ms
V_{IL}	Low-level input voltage (SDA, SCL, and ADDR)			0		0.3 × V_{DD}	V
V_{IH}	High-level input voltage (SDA, SCL, and ADDR)			0.7 × V_{DD}		5.5	V
I_{IL}	Low-level input current (SDA, SCL, and ADDR)				0.01	0.25[6]	µA
V_{OL}	Low-level output voltage (SDA and INT)	I_{OL}= 3 mA				0.32	V
I_{ZH}	Output logic high, high-Z leakage current (SDA, INT)	Pin at V_{DD}			0.01	0.25[6]	µA
TEMPERATURE							
	Specified temperature range			–40		85	°C

(1) Refers to a control field within the configuration register.
(2) Tested with the white LED calibrated to 2k lux and an 850-nm LED.
(3) Characterized by measuring fixed near-full-scale light levels on the higher adjacent full-scale range setting.
(4) PSRR is the percent change of the measured lux output from its current value, divided by the change in power supply voltage, as characterized by results from 3.6-V and 1.6-V power supplies.
(5) The conversion time, from start of conversion until the data are ready to be read, is the integration time plus 3 ms.
(6) The specified leakage current is dominated by the production test equipment limitations. Typical values are much smaller.

6.6 Timing Requirements[1]

		MIN	TYP	MAX	UNIT
I^2C FAST MODE					
f_{SCL}	SCL operating frequency	0.01		0.4	MHz
t_{BUF}	Bus free time between stop and start	1300			ns
t_{HDSTA}	Hold time after repeated start	600			ns
t_{SUSTA}	Setup time for repeated start	600			ns
t_{SUSTO}	Setup time for stop	600			ns
t_{HDDAT}	Data hold time	20		900	ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_{RC} and t_{FC}	Clock rise and fall time			300	ns
t_{RD} and t_{FD}	Data rise and fall time			300	ns
t_{TIMEO}	Bus timeout period. If the SCL line is held low for this duration of time, the bus state machine is reset.		28		ms
I^2C HIGH-SPEED MODE					
f_{SCL}	SCL operating frequency	0.01		2.6	MHz
t_{BUF}	Bus free time between stop and start	160			ns
t_{HDSTA}	Hold time after repeated start	160			ns
t_{SUSTA}	Setup time for repeated start	160			ns
t_{SUSTO}	Setup time for stop	160			ns
t_{HDDAT}	Data hold time	20		140	ns
t_{SUDAT}	Data setup time	20			ns
t_{LOW}	SCL clock low period	240			ns
t_{HIGH}	SCL clock high period	60			ns
t_{RC} and t_{FC}	Clock rise and fall time			40	ns
t_{RD} and t_{FD}	Data rise and fall time			80	ns
t_{TIMEO}	Bus timeout period. If the SCL line is held low for this duration of time, the bus state machine is reset.		28		ms

(1) All timing parameters are referenced to low and high voltage thresholds of 30% and 70%, respectively, of final settled value.

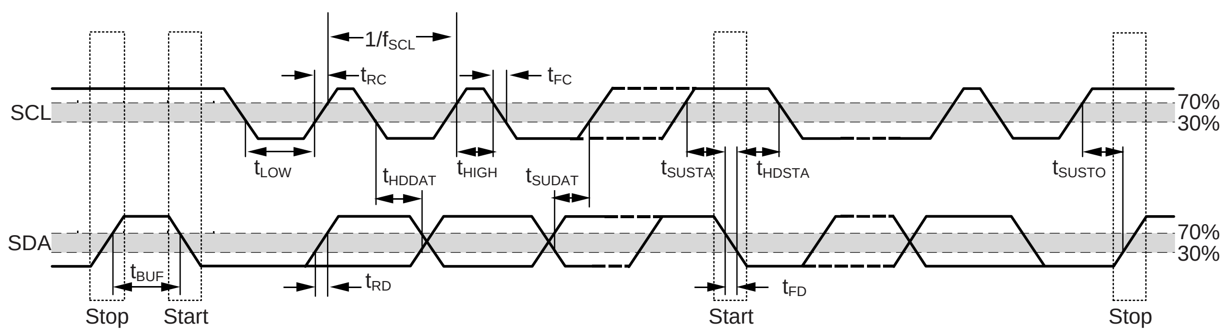

Figure 1. I^2C Detailed Timing Diagram

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6.7 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CT = 1), automatic full-scale range (RN[3:0] = 1100b), white LED, and normal-angle incidence of light, unless otherwise specified.

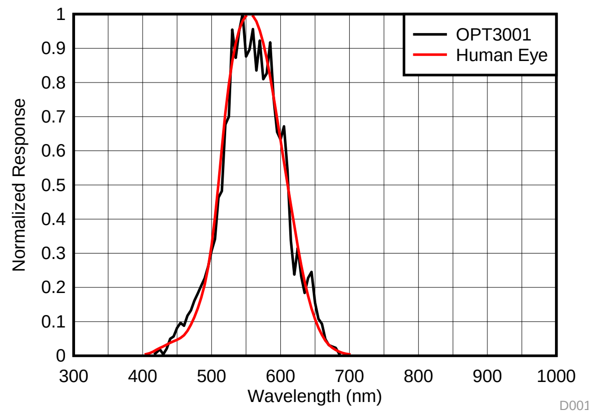


Figure 2. Spectral Response vs Wavelength

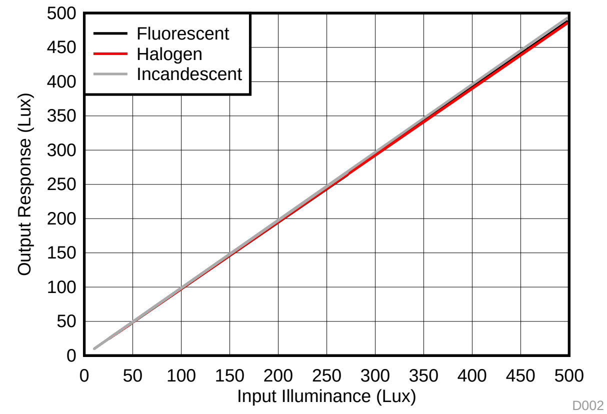


Figure 3. Output Response vs Input Illuminance, Multiple Light Sources (Fluorescent, Halogen, Incandescent)

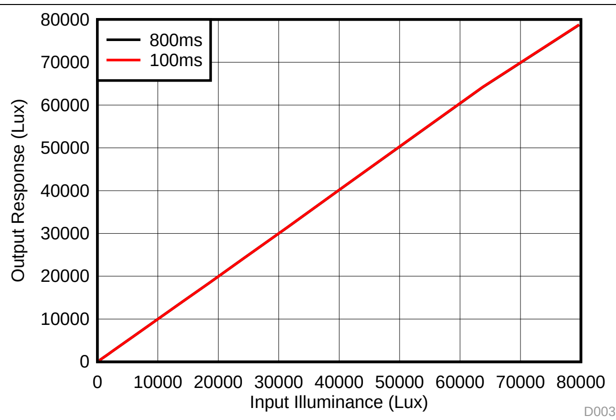


Figure 4. Output Response vs Input Illuminance (Entire Range = 0 lux to 83k lux)

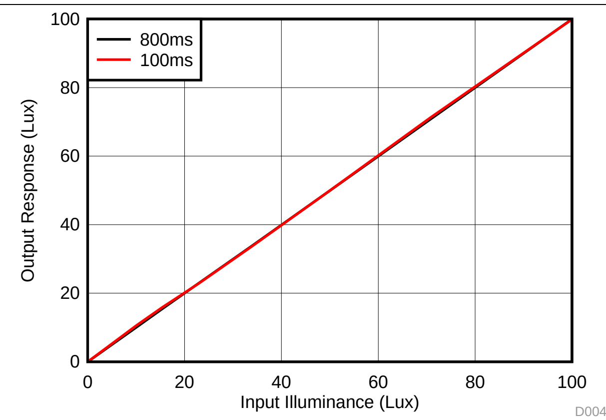


Figure 5. Output Response vs Input Illuminance (Mid Range = 0 lux to 100 lux)

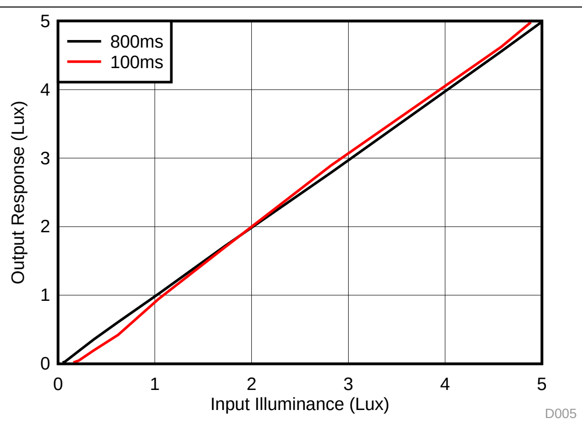
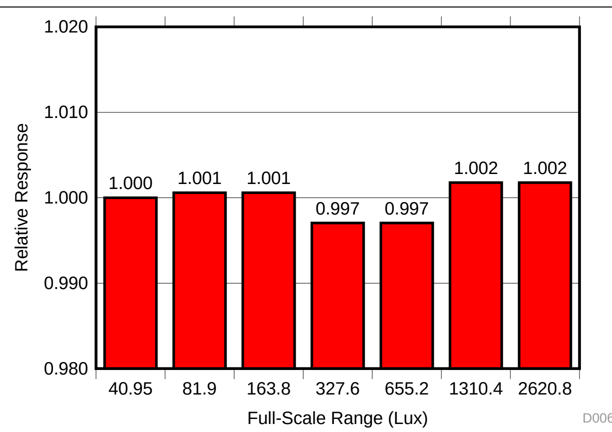


Figure 6. Output Response vs Input Illuminance (Low Range = 0 lux to 5 lux)

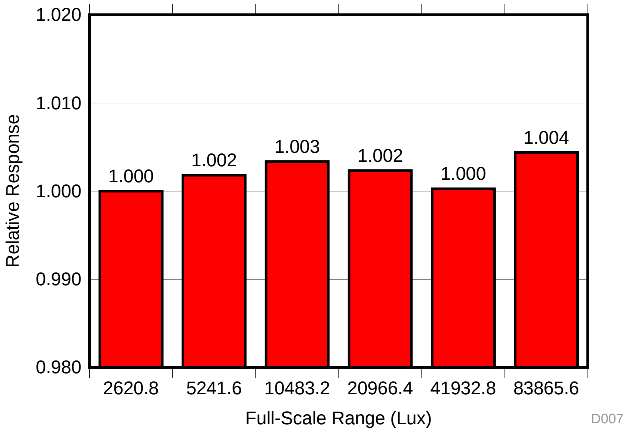


Input illuminance = 33 lux,
normalized to response of 40.95 lux full-scale

Figure 7. Full-Scale-Range Matching (Lowest 7 Ranges)

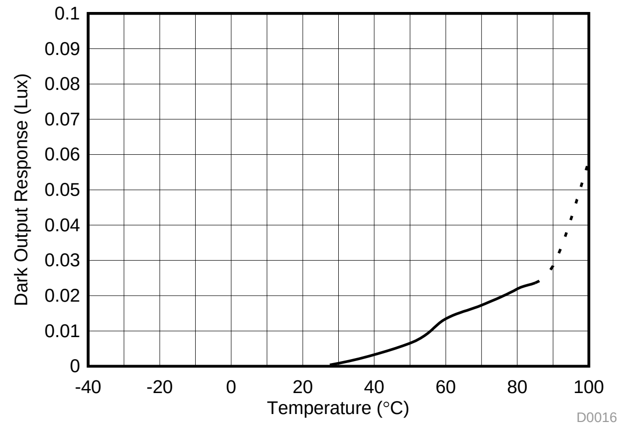
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CT = 1), automatic full-scale range (RN[3:0] = 1100b), white LED, and normal-angle incidence of light, unless otherwise specified.



Input illuminance = 2490 lux,
normalized to response of 2560 lux full-scale

Figure 8. Full-Scale-Range Matching (Highest 6 Ranges)



Average of 30 devices

Figure 9. Dark Response vs Temperature

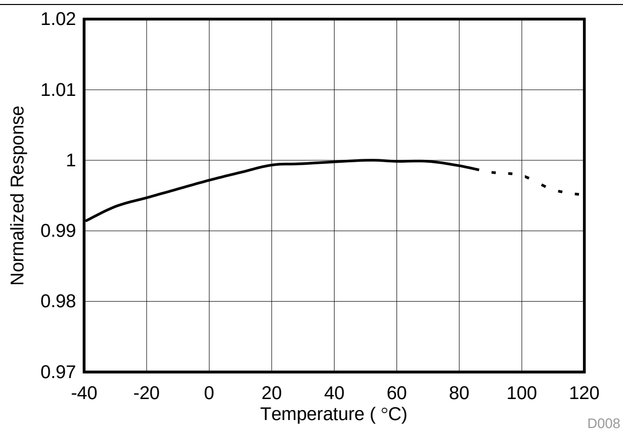


Figure 10. Normalized Response vs Temperature

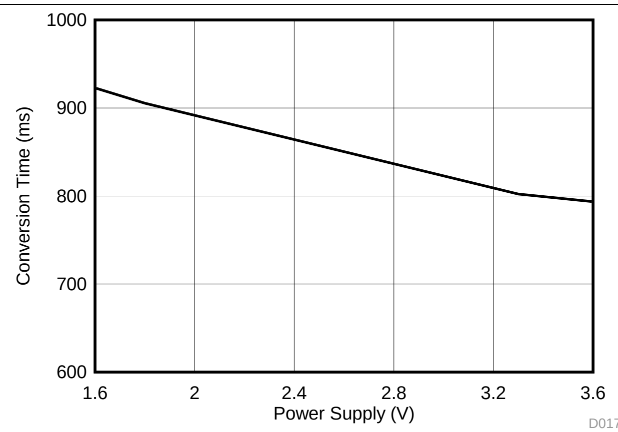


Figure 11. Conversion Time vs Power Supply

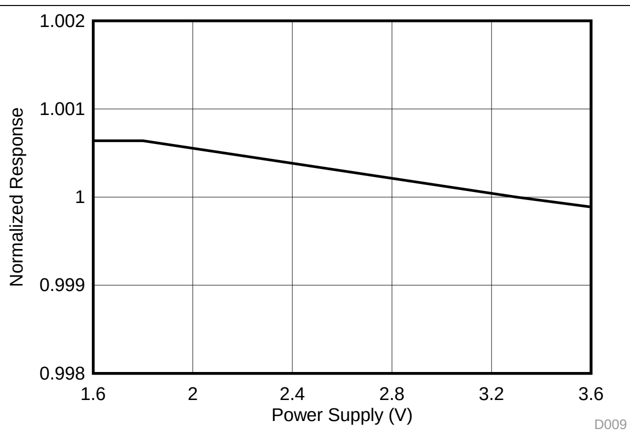


Figure 12. Normalized Response vs Power-Supply Voltage

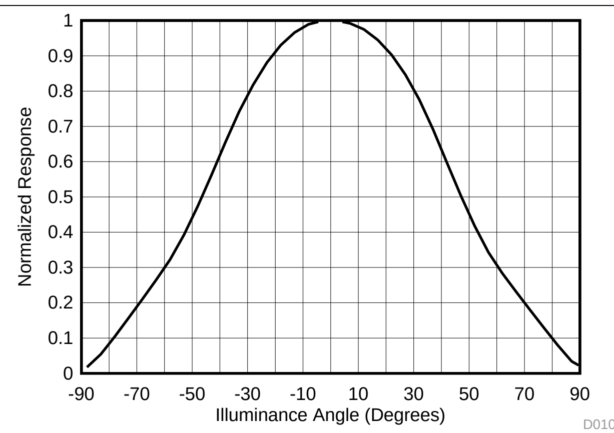


Figure 13. Normalized Response vs Illuminance Angle

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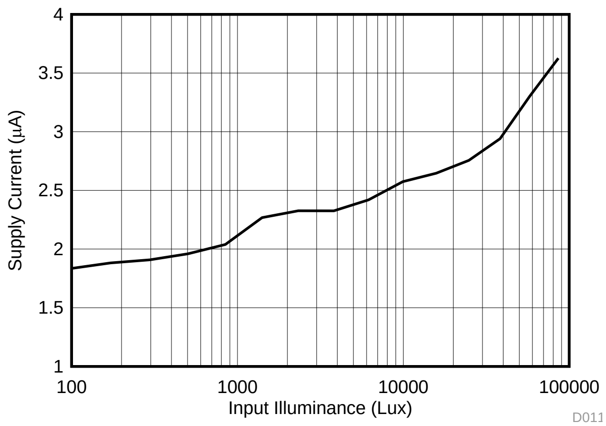
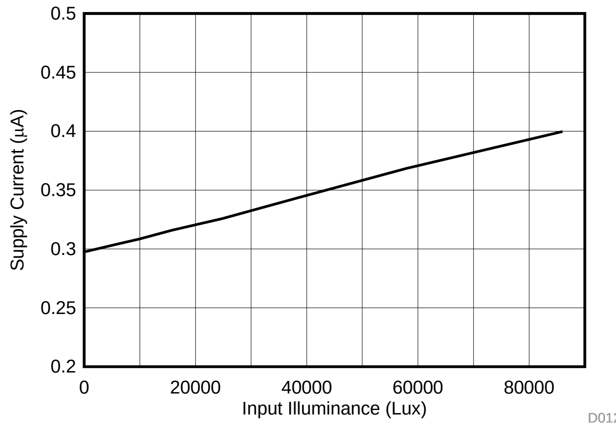
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CT = 1), automatic full-scale range (RN[3:0] = 1100b), white LED, and normal-angle incidence of light, unless otherwise specified.



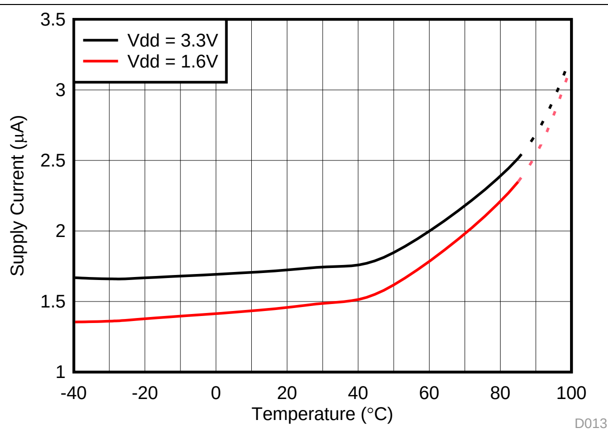
M[1:0] = 10b

Figure 14. Supply Current vs Input Illuminance



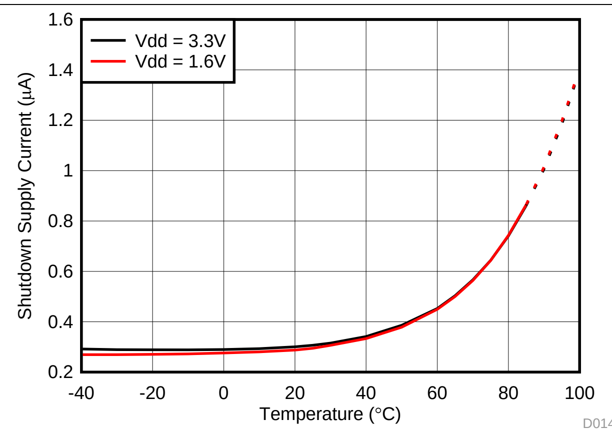
M[1:0] = 00b

Figure 15. Shutdown Current vs Input Illuminance



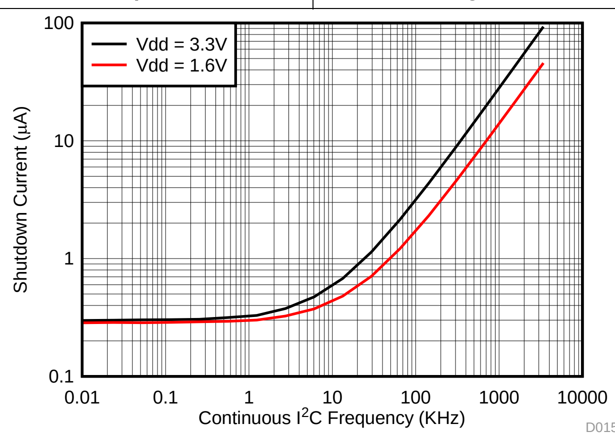
M[1:0] = 10b

Figure 16. Supply Current vs Temperature



M[1:0] = 00b, input illuminance = 0 lux

Figure 17. Shutdown Current vs Temperature



Input illuminance = 80 lux, SCL = SDA,
continuously toggled at I^2C frequency
Note: A typical application runs at a lower duty cycle and thus consumes a lower current.

Figure 18. Supply Current vs Continuous I^2C Frequency

7 Detailed Description

7.1 概述

OPT3001 测量照亮设备的环境光。该设备测量光谱响应与人眼非常接近的光，并且具有非常好的红外抑制。

将传感器光谱响应与人眼响应的光谱响应相匹配至关重要，因为环境光传感器用于测量和帮助创造理想的人类照明体验。对人类看不到的红外线的强烈抑制是这种匹配的关键组成部分。这种匹配使 OPT3001 特别适合在明显黑暗但可透射红外线的窗户下操作。

OPT3001 完全独立，可测量环境光并通过 I2C 总线以勒克斯数字形式报告结果。结果还可用于警告系统并通过 INT 引脚中断处理器。结果还可以通过可编程窗口比较进行汇总，并与INT 引脚进行通信。

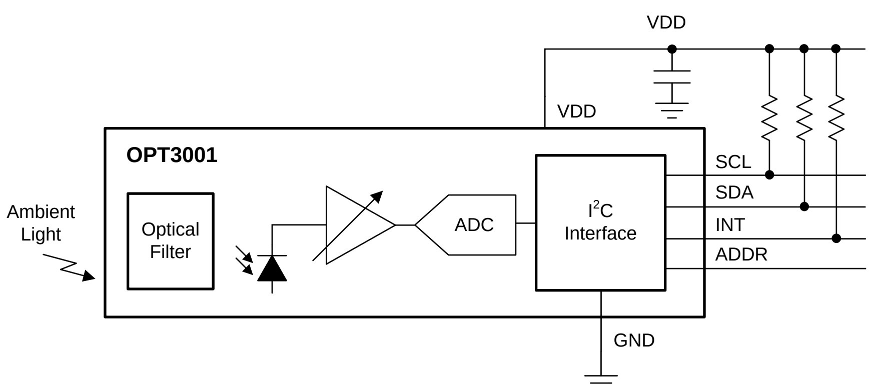
OPT3001 可配置为自动满量程范围设置模式，该模式始终为照明条件选择最佳满量程范围设置。这种模式使用户不必为潜在的测量迭代循环和满量程范围的重新调整编程他们的软件，直到对于任何给定的测量达到最佳。可以命令设备以连续或单次测量模式运行。

该设备在 100 毫秒或 800 毫秒内对其结果进行积分，因此来自典型灯泡的 50-Hz 和 60-Hz 噪声源的影响在名义上被降至最低。

该器件在低功耗关断状态下启动，因此OPT3001 仅在被编程为活动状态后才消耗活动运行功率。

OPT3001光学过滤系统对光学表面的非理想粒子和微阴影不会过于敏感。这种降低的灵敏度是由于设备对红外抑制的传感器区域的均匀密度光学照明的依赖性相对较小。为了在所有光学设备上获得最佳效果，始终建议保持适当的光学表面清洁度。

7.2 功能框图



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7.3 功能描述

7.3.1 人眼匹配

OPT3001 光谱响应与人眼的光谱响应非常匹配。如果环境光传感器测量用于帮助创造良好的人类体验，或创造最适合人类的光学条件，则传感器必须测量人类看到的相同光谱。

该器件还具有出色的红外光 (IR) 抑制能力。这种 IR 抑制尤为重要，因为许多现实世界的光源都具有人类看不到的大量红外成分。如果传感器测量人眼看不到的红外光，则无法准确呈现真实的人类体验。

此外，如果环境光传感器隐藏在暗窗下（这样最终产品用户看不到传感器），OPT3001 的红外抑制变得更加重要，因为许多暗窗衰减可见光但传输红外光。可见光的这种衰减和红外光的不衰减放大了红外光与照亮传感器的可见光的比率。由于OPT3001 的高红外线抑制能力，在这种情况下，结果仍然可以很好地与人眼匹配。

7.3.2 自动满量程范围设置

OPT3001 具有自动满量程范围设置功能，无需预测和设置设备的最佳范围。 在此模式下，OPT3001 会自动为给定的照明条件选择最佳的满量程范围。 OPT3001 在满量程范围设置之间具有高度的结果匹配。 此匹配消除了不同级别范围选择不同的结果或特定于范围的用户校准增益因子的问题。 有关更多详细信息，请参阅“自动满量程设置模式”部分。

7.3.3 中断操作、INT 引脚和中断报告机制

该器件具有中断报告系统，允许连接到I2C 总线的处理器进入睡眠状态，或以其他方式忽略器件结果，直到发生需要可能采取的操作的用户定义事件。或者，这种相同的机制也可以用于任何可以利用单个数字信号的系统，该信号指示光是高于还是低于感兴趣的水平。

中断事件条件由上限和下限寄存器以及配置寄存器锁存器和故障计数字段控制。将结果寄存器与上限寄存器和下限寄存器进行比较的结果称为故障事件。故障计数寄存器指示需要多少连续的相同结果故障事件来触发中断事件并随后更改中断报告机制的状态，即 INT 引脚、标志高字段和标志低字段。闩锁字段允许在闩锁窗口式比较和透明滞后式比较之间进行选择。

INT 引脚为开漏输出，需要使用上拉电阻。这种开漏输出允许具有开漏 INT 引脚的多个器件连接到同一条线上，从而在器件之间创建逻辑 NOR 或 AND 功能。 INT 引脚的极性可以通过配置寄存器中中断域的极性来控制。当 POL 字段设置为 0 时，引脚以低电平有效行为运行，当 INT 引脚变为有效时，将引脚拉低。当 POL 字段设置为 1 时，该引脚以高电平有效行为运行并变为高阻抗，从而允许该引脚在 INT 引脚变为活动状态时变为高电平。

中断报告机制模式和内部寄存器部分描述了中断报告寄存器的更多细节。

Feature Description (continued)

7.3.4 I2C 总线概述

OPT3001 提供与 I2C 和 SMBus 接口的兼容性。 I2C 和 SMBus 协议本质上是相互兼容的。 I2C 接口在本文档中用作主要示例，仅在讨论两种协议之间的差异时才指定SMBus 协议。

OPT3001 通过两个引脚连接到总线：一个 SCL 时钟输入引脚和一个 SDA 开漏双向数据引脚。总线必须由生成串行时钟 (SCL)、控制总线访问以及生成启动和停止条件的主设备控制。为了寻址特定器件，主机通过在 SCL 为高电平时将数据信号线 (SDA) 从高逻辑电平拉到低逻辑电平来启动启动条件。总线上的所有从机在 SCL 上升沿移位从机地址字节，最后一位指示是要进行读操作还是写操作。在第 9 个时钟脉冲期间，被寻址的从设备通过拉低 SDA 产生一个确认位来响应主设备。

然后启动数据传输并发送八位数据，然后是确认位。在数据传输期间，SDA 必须保持稳定，而 SCL 为高电平。SCL 为高时 SDA 的任何变化都被解释为开始或停止条件。当所有数据传输完毕后，主机产生一个停止条件，通过在 SCL 为高电平时将 SDA 从低电平拉高到高电平来指示。 OPT3001 在 I2C 接口上包含 28 毫秒的超时，以防止锁定总线。如果SCL 线在这段时间内保持低电平，则总线状态机将复位。

7.3.4.1 Serial Bus Address

To communicate with the OPT3001, the master must first initiate an I^{2}C start command. Then, the master must address slave devices via a slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

Four I^{2}C addresses are possible by connecting the ADDR pin to one of four pins: GND, VDD, SDA, or SCL. Table 1 summarizes the possible addresses with the corresponding ADDR pin configuration. The state of the ADDR pin is sampled on every bus communication and must be driven or connected to the desired level before any activity on the interface occurs.

Table 1. Possible I^{2}C Addresses with Corresponding ADDR Configuration

DEVICE I^{2}C ADDRESS	ADDR PIN
1000100	GND
1000101	VDD
1000110	SDA
1000111	SCL

7.3.4.2 Serial Interface

The OPT3001 operates as a slave device on both the I^{2}C bus and SMBus. Connections to the bus are made via the SCL clock input line and the SDA open-drain I/O line. The OPT3001 supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). All data bytes are transmitted most-significant bits first.

The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. See the *Electrical Interface* section for further details of the I^{2}C bus noise immunity.

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7.4 设备功能模式

7.4.1 自动满量程设置模式

OPT3001具有自动满量程范围设置模式，用户无需预测和设置设备的最佳范围。当配置寄存器范围编号字段 (RN[3:0]) 设置为1100b 时，将进入此模式。

设备在自动量程模式下进行的第一次测量是10毫秒的量程评估测量。然后设备确定适当的满量程范围以进行第一次完整测量。

对于后续测量，满量程范围由上次测量的结果设置。如果测量接近满量程的低端，则满量程范围会减少一个或两个设置以进行下一次测量。如果测量接近满量程的上侧，则满量程范围增加一个设置以进行下一次测量。

如果由于快速增加的光学瞬态事件导致测量超出满量程范围，则当前测量将中止。不报告此无效测量。进行 10 ms 测量以评估和正确重置满量程范围。然后，使用此适当的满量程范围进行新的测量。因此，在此模式下快速增加的光瞬态期间，完成和报告测量可能需要比配置寄存器转换时间字段(CT) 指示的更长的时间。

7.4.2 中断报告机制模式

中断报告机制模式主要有两大类：锁存窗口式比较模式和透明滞后式比较模式。 配置寄存器锁存字段 (L)（参见配置寄存器，位 4）控制使用这两种模式中的哪一种。 转换结束模式也与每个主要模式类型相关联。 当阈值低寄存器的两个最高有效位设置为 11b 时，转换结束模式处于活动状态。 该机制通过标志高和标志低字段、转换就绪字段和 INT 引脚报告。

7.4.2.1 锁窗式比较模式

使用 OPT3001 中断外部处理器时，通常选择锁存窗口式比较模式。 在这种模式下，当输入信号高于上限寄存器或低于下限寄存器时，就会识别出故障。 当连续的故障事件触发中断报告机制时，这些机制被锁存，从而报告故障是高电平比较还是低电平比较的结果。 这些机制保持锁存，直到读取配置寄存器，这会清除 INT 引脚和标志高位和标志低位字段。 SMBus 警报响应协议（在 SMBus 警报响应部分中有详细描述）清除引脚但不清除标志高和标志低字段。 此模式的行为以及转换就绪标志汇总在表 2 中。请注意，当两个阈值低寄存器 MSB（有关 MSB 的说明请参见透明迟滞式比较模式部分）是时，表2 不适用 设置为11b 。

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Device Functional Modes (continued)

Table 2. 锁窗式比较模式：标志设置和清除汇总(1)(2)

OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(3)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	X	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	X	1	Active	1
The conversion is complete with fault count criterion not met	X	X	X	1
Configuration register read(4)	0	0	Inactive	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	X	0
SMBus alert response protocol	X	X	Inactive	X

(1) X = no change from the previous state.
(2) The high-limit register is assumed to be greater than the low-limit register. If this assumption is incorrect, the flag high field and flag low field can take on different behaviors.
(3) The INT pin depends on the setting of the polarity field (POL). The INT pin is low when the pin state is active and POL = 0 (active low) or when the pin state is inactive and POL = 1 (active high).
(4) Immediately after the configuration register is read, the device automatically resets the conversion ready field to its 0 state. Thus, if two configuration register reads are performed immediately after a conversion completion, the first reads 1 and the second reads 0.

7.4.2.2 透明滞后式比较模式

当需要指示输入光是高于还是低于感兴趣的光水平的单个数字信号时，通常使用透明滞后式比较模式。如果故障计数字段设置的连续事件数的结果寄存器高于上限寄存器，则 INT 线设置为活动状态，标志高字段设置为 1，标志低字段设置为0. 如果在故障计数字段设置的连续事件数内，结果寄存器低于下限寄存器，则将 INT 线设置为无效，将标志低字段设置为 1，将标志高字段设置为设置为 0。INT 引脚和标志高和标志低字段不会随着配置读取和写入而改变状态。 INT 引脚和标志字段不断报告光与下限和上限寄存器的适当比较。在两种透明比较模式（配置寄存器，锁存字段 = 0）中的任何一种时，器件不响应 SMBus 警报响应协议。表 3 中总结了该模式的行为以及转换就绪。请注意，当两个阈值低寄存器MSB （表11 中的LE[3:2] ）设置为11 时，表3 不适用。

Table 3. Transparent Hysteresis-Style Comparison Mode: Flag Setting and Clearing Summary(1)(2)

OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(3)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	0	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	0	1	Inactive	1
The conversion is complete with fault count criterion not met	X	X	X	1
Configuration register read(4)	X	X	X	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	X	0
SMBus alert response protocol	X	X	X	X

(1) X = no change from the previous state.
(2) The high-limit register is assumed to be greater than the low-limit register. If this assumption is incorrect, the flag high field and flag low field can take on different behaviors.
(3) The INT pin depends on the setting of the polarity field (POL). The INT pin is low when the pin state is active and POL = 0 (active low) or when the pin state is inactive and POL = 1 (active high).
(4) Immediately after the configuration register is read, the device automatically resets the conversion ready field to its 0 state. Thus, if two configuration register reads are performed immediately after a conversion completion, the first reads 1 and the second reads 0.

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7.4.2.3 转换结束模式

当每次测量都需要处理器读取每个测量值时，可以使用转换结束指示器模式，每次测量完成时 INT 引脚都会激活。通过将下限寄存器（来自下限寄存器的 LE[3:2]）的最高两位设置为 11b 来进入该模式。 这种转换结束模式通常与锁存窗口式比较模式结合使用。 当读取配置寄存器或使用非关断参数写入配置寄存器或响应 SMBus 警报响应时，INT 引脚变为无效。 表4 总结了各种操作导致的中断报告机制。

Table 4. 处于锁定窗口样式比较模式时的转换结束模式：标志设置和清除摘要(1)

OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(2)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	X	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	X	1	Active	1
The conversion is complete with fault count criterion not met	X	X	Active	1
Configuration register read(3)	0	0	Inactive	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	X	0
SMBus alert response protocol	X	X	Inactive	X

(1) X = no change from the previous state.
(2) The INT pin depends on the setting of the polarity field (POL). The INT pin is low when the pin state is active and POL = 0 (active low) or when the pin state is inactive and POL = 1 (active high).
(3) Immediately after the configuration register is read, the device automatically resets the conversion ready field to its 0 state. Thus, if two configuration register reads are performed immediately after a conversion completion, the first reads 1 and the second reads 0.

Note that when transitioning from end-of-conversion mode to the standard comparison modes (that is, programming LE[3:2] from 11b to 00b) while the configuration register latch field (L) is 1, a subsequent write to the configuration register latch field (L) to 0 is necessary in order to properly clear the INT pin. The latch field can then be set back to 1 if desired.

7.4.2.4 转换结束和透明滞后式比较模式

The combination of end-of-conversion mode and transparent hysteresis-style comparison mode can also be programmed simultaneously. The behavior of this combination is shown in Table 5.

Table 5. End-Of-Conversion Mode while in Transparent Hysteresis-Style Comparison Mode: Flag Setting and Clearing Summary(1)

OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(2)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	0	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	0	1	Active	1
The conversion is complete with fault count criterion not met	X	X	Active	1
Configuration register read(3)	X	X	Inactive	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	Inactive	0
SMBus alert response protocol	X	X	X	X

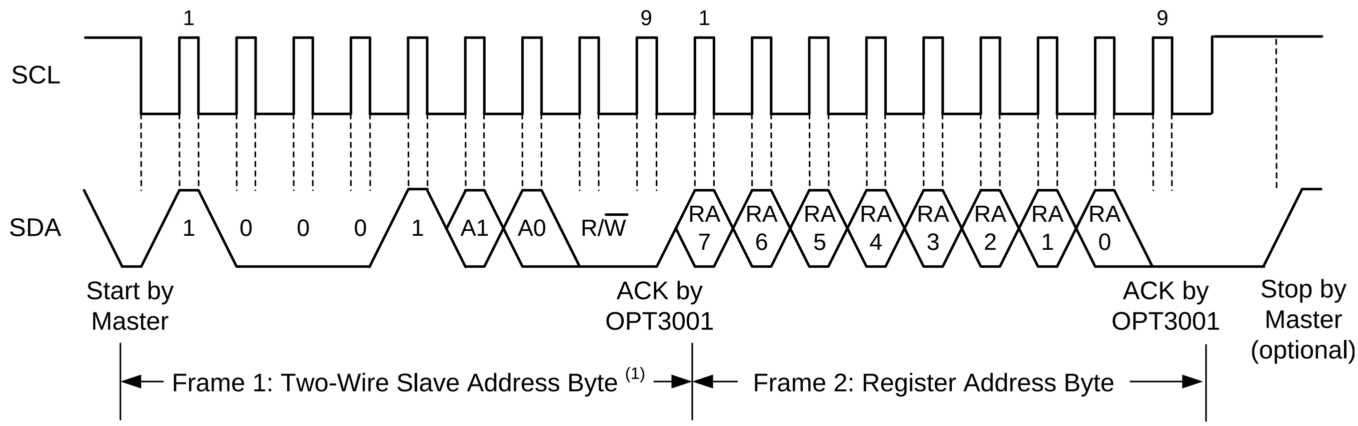
(1) X = no change from the previous state.
(2) The INT pin depends on the setting of the polarity field (POL). The INT pin is low when the pin state is active and POL = 0 (active low) or when the pin state is inactive and POL = 1 (active high).
(3) Immediately after the configuration register is read, the device automatically resets the conversion ready field to its 0 state. Thus, if two configuration register reads are performed immediately after a conversion completion, the first reads 1 and the second reads 0.

7.5 编程

OPT3001 支持标准模式（最高 100 kHz）、快速模式（最高 400 kHz）和高速模式（最高 2.6 MHz）的传输协议。快速和标准模式被描述为默认协议，称为F/S 。 高速I2C 模式部分介绍了高速模式。

7.5.1 写入和读取

访问 OPT3001 上的特定寄存器是通过在 I2C 事务序列期间写入适当的寄存器地址来完成的。 有关寄存器及其相应寄存器地址的完整列表，请参阅表 6。 寄存器地址的值（如图 19 所示）是在 R/W 位为低的从地址字节之后传输的第一个字节。



(1) The value of the slave address byte is determined by the ADDR pin setting; see Table 1.

Figure 19. 设置I2C 寄存器地址

从主机发送的第一个字节开始写入寄存器。该字节是 R/W 位为低的从地址。然后 OPT3001 确认收到有效地址。主机传输的下一个字节是要写入数据的寄存器的地址。接下来的两个字节被写入由寄存器地址寻址的寄存器。OPT3001 确认收到每个数据字节。主机可以通过生成开始或停止条件来终止数据传输。

从 OPT3001 读取时，写入操作存储在寄存器地址中的最后一个值决定了读取操作期间读取的寄存器。要更改读操作的寄存器地址，必须启动新的部分 I2C 写事务。该部分写入是通过发出一个 R/W 位为低电平的从地址字节来完成的，然后是寄存器地址字节和一个停止命令。然后主机产生一个起始条件并发送具有 R/W 位高电平的从机地址字节以启动读命令。下一个字节由从机发送，是寄存器地址所指示的寄存器的最高有效字节。该字节之后是来自主机的确认；然后从设备传输最低有效字节。主机确认收到数据字节。主机可以通过在接收到任何数据字节后产生一个不确认，或者通过产生一个开始或停止条件来终止数据传输。如果需要重复读取同一个寄存器，则不需要连续发送寄存器地址字节； OPT3001 会保留寄存器地址，直到下一次写操作更改该数字为止。

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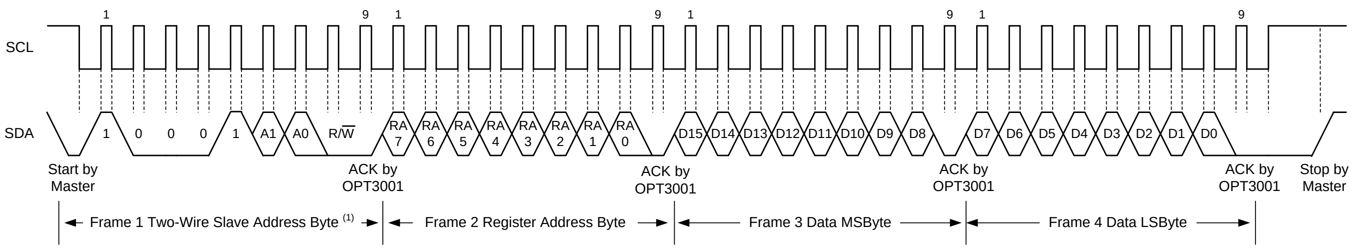
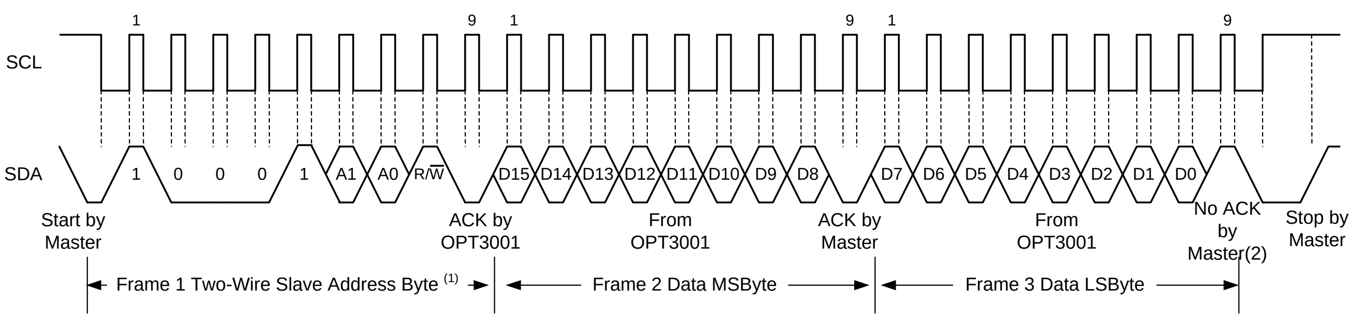
Programming (continued)

图20 和图21 分别显示了写和读操作时序图。 请注意，寄存器字节首先发送最高有效字节，然后是最低有效字节。



(1)从机地址字节的值由ADDR引脚的设置决定； 见表1 。

Figure 20. I2C 写示例



(1) 从机地址字节的值由ADDR 引脚设置决定； 见表1 。
(2) 也可以发送主机的 ACK。

Figure 21. I2C 读取示例

7.5.1.1 高速 I2C 模式

当总线空闲时，SDA 和 SCL 线都被上拉电阻或有源上拉器件拉高。 主机产生一个起始条件，后跟一个包含高速 (HS) 主机代码 0000 1XXXb 的有效串行字节。 这种传输以标准模式或快速模式（高达 400 kHz）进行。 OPT3001 不确认HS 主代码，但会识别代码并切换其内部滤波器以支持2.6-MHz 操作。

然后主机产生一个重复启动条件（重复启动条件与启动条件具有相同的时序）。 在此重复启动条件之后，协议与 F/S 模式相同，但允许高达 2.6 MHz 的传输速度。 不使用停止条件，而是使用重复的启动条件来确保总线处于 HS 模式。 停止条件会结束HS 模式并切换OPT3001 的所有内部滤波器以支持F/S 模式。

7.5.1.2 广播呼叫复位命令

I2C 通用调用复位允许主机控制器在一个命令中复位总线上响应通用调用复位命令的所有设备。 通用调用通过写入 I2C 地址 0 (0000 0000b) 来启动。 当随后的第二个地址字节为 06h (0000 0110b) 时，将启动复位命令。 通过此事务，设备会发出一个确认位并将其所有寄存器设置为上电复位默认条件。

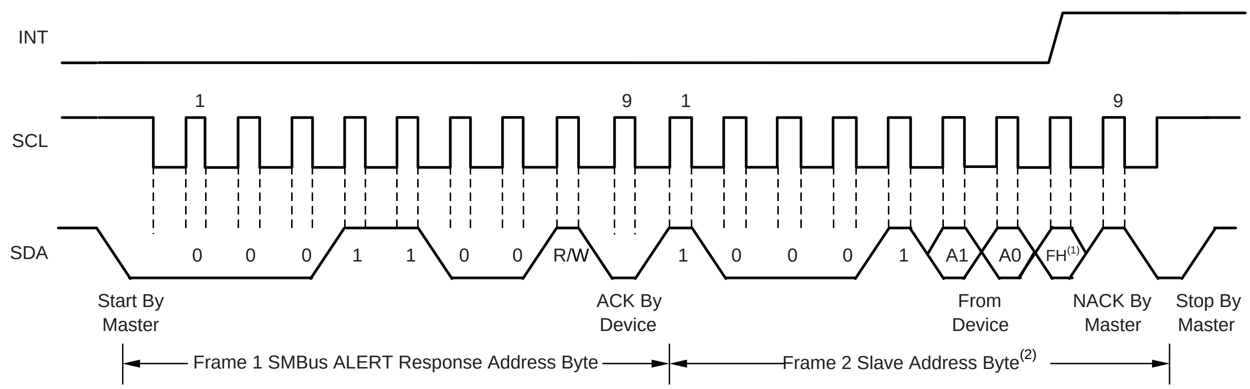
Programming (continued)

7.5.1.3 SMBus Alert Response

The SMBus alert response provides a quick identification for which device issued the interrupt. Without this alert response capability, the processor does not know which device pulled the interrupt line when there are multiple slave devices connected.

The OPT3001 is designed to respond to the SMBus alert response address, when in the latched window-style comparison mode (configuration register, latch field = 1). The OPT3001 does not respond to the SMBus alert response when in transparent mode (configuration register, latch field = 0).

The response behavior of the OPT3001 to the SMBus alert response is shown in Figure 22. When the interrupt line to the processor is pulled to active, the master can broadcast the alert response slave address (0001 1001b). Following this alert response, any slave devices that generated an alert identify themselves by acknowledging the alert response and sending their respective I^{2}C address on the bus. The alert response can activate several different slave devices simultaneously. If more than one slave attempts to respond, bus arbitration rules apply. The device with the lowest address wins the arbitration. If the OPT3001 loses the arbitration, the device does not acknowledge the I^{2}C transaction and its INT pin remains in an active state, prompting the I^{2}C master processor to issue a subsequent SMBus alert response. When the OPT3001 wins the arbitration, the device acknowledges the transaction and sets its INT pin to inactive. The master can issue that same command again, as many times as necessary to clear the INT pin. See the *Interrupt Reporting Mechanism Modes* section for additional details of how the flags and INT pin are controlled. The master can obtain information about the source of the OPT3001 interrupt from the address broadcast in the above process. The flag high field (configuration register, bit 6) is sent as the final LSB of the address to provide the master additional information about the cause of the OPT3001 interrupt. If the master requires additional information, the result register or the configuration register can be queried. The flag high and flag low fields are not cleared upon an SMBus alert response.



(1) FH is the flag high field (FH) in the configuration register (see Table 10).

(2) A1 and A0 are determined by the ADDR pin; see Table 1.

Figure 22. Timing Diagram for SMBus Alert Response

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7.6 Register Maps

7.6.1 Internal Registers

The device is operated over the I^2C bus with registers that contain configuration, status, and result information. All registers are 16 bits long.

There are four main registers: result, configuration, low-limit, and high-limit. There are also two ID registers: manufacturer ID and device ID. Table 6 lists these registers.

Table 6. Register Map

REGISTER	ADDRESS (Hex)(1)	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Result	00h	E3	E2	E1	E0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
Configuration	01h	RN3	RN2	RN1	RN0	CT	M1	M0	OVF	CRF	FH	FL	L	POL	ME	FC1	FC0
Low Limit	02h	LE3	LE2	LE1	LE0	TL11	TL10	TL9	TL8	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
High Limit	03h	HE3	HE2	HE1	HE0	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
Manufacturer ID	7Eh	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Device ID	7Fh	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0

(1) Register offset and register address are used interchangeably.

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7.6.1.1 寄存器说明

NOTE
Register offset and register address are used interchangeably.

7.6.1.1.1 结果登记表(offset = 00h)

这个寄存器包含了最近一次光-数转换的结果。这个16位的寄存器有两个字段：一个4位的指数和一个12位的尾数。

Figure 23. 结果寄存器（只读）。

15	14	13	12	11	10	9	8
E3	E2	E1	E0	R11	R10	R9	R8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	R1	R0
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 7. 结果寄存器字段描述

Bit	Field	Type	Reset	Description
15:12	E[3:0]	R	0h	**Exponent.** 这些位是指数位。表8提供了进一步的细节。
11:0	R[11:0]	R	000h	**Fractional result.** 这些位是直接二进制编码的结果（零到满分）。

Table 8. 满刻度范围和LSB大小与指数水平的关系

E3	E2	E1	E0	满刻度范围 (lux)	LSB SIZE (lux per LSB)
0	0	0	0	40.95	0.01
0	0	0	1	81.90	0.02
0	0	1	0	163.80	0.04
0	0	1	1	327.60	0.08
0	1	0	0	655.20	0.16
0	1	0	1	1310.40	0.32
0	1	1	0	2620.80	0.64
0	1	1	1	5241.60	1.28
1	0	0	0	10483.20	2.56
1	0	0	1	20966.40	5.12
1	0	1	0	41932.80	10.24
1	0	1	1	83865.60	20.48

将该寄存器转换为勒克斯的公式在公式1中给出。

$$\text{lux} = \text{LSB\_Size} \times \text{R}[11:0] \quad (1)$$

其中:

$$\text{LSB\_Size} = 0.01 \times 2^{\text{E}[3:0]} \quad (2)$$

LSB_Size也可以从表8中获取。完整的勒克斯方程显示在方程3中。

$$\text{lux} = 0.01 \times (2^{\text{E}[3:0]}) \times \text{R}[11:0] \quad (3)$$

表9中给出了一系列结果寄存器的输出例子，以及相应的LSB权重和结果Lux。请注意，许多指数（E[3:0]）和分数结果（R[11:0]）的组合可以映射到同一个Lux结果上，如表9的例子所示。

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Table 9. 将结果寄存器解码为勒克斯的例子

RESULT REGISTER (Bits 15:0, Binary)	EXPONENT (E[3:0], Hex)	FRACTIONAL RESULT (R[11:0], Hex)	LSB WEIGHT (lux, Decimal)	RESULTING LUX (Decimal)
0000 0000 0000 0001b	00h	001h	0.01	0.01
0000 1111 1111 1111b	00h	FFFh	0.01	40.95
0011 0100 0101 0110b	03h	456h	0.08	88.80
0111 1000 1001 1010b	07h	89Ah	1.28	2818.56
1000 1000 0000 0000b	08h	800h	2.56	5242.88
1001 0100 0000 0000b	09h	400h	5.12	5242.88
1010 0010 0000 0000b	0Ah	200h	10.24	5242.88
1011 0001 0000 0000b	0Bh	100h	20.48	5242.88
1011 0000 0000 0001b	0Bh	001h	20.48	20.48
1011 1111 1111 1111b	0Bh	FFFh	20.48	83865.60

请注意，通过启用指数屏蔽（配置寄存器，ME字段=1）和手动编程满量程（配置寄存器，RN[3:0]<1100b (0Ch)），可以禁用（设置为零）指数字段，允许在手动编程的满量程模式下更简单地操作。从结果寄存器的内容计算勒克斯，只需要将结果寄存器乘以与特定编程的满刻度范围相关的LSB权重（以勒克斯为单位）（见表8）。详见低限值寄存器。
关于勒克斯分辨率与转换时间的关系，请参阅配置寄存器转换时间字段（CT，位11）的描述。

7.6.1.1.2 配置寄存器 (offset = 01h) [reset = C810h]

这个寄存器控制设备的主要操作模式。这个寄存器有11个字段，下面有详细说明。如果配置寄存器被写入时，一个测量转换正在进行中，那么正在进行的测量转换将立即中止。如果新的配置寄存器指示一个新的转换，该转换将随后开始。

Figure 24. 配置寄存器

15	14	13	12	11	10	9	8
RN3	RN2	RN1	RN0	CT	M1	M0	OVF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRF	FH	FL	L	POL	ME	FC1	FC0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only

Table 10. 配置寄存器字段描述

Bit	Field	Type	Reset	Description
15:12	RN[3:0]	R/W	1100b	**范围号码字段 (read or write).** 范围号字段选择设备的满量程勒克斯范围。该字段的格式与结果寄存器的指数字段（E[3:0]）相同，见表8。当RN[3:0]被设置为1100b(0Ch)时，器件在自动满量程设置模式下工作，如自动满量程设置模式部分所述。在这种模式下，自动选择的范围在结果指数中报告（寄存器00h，E[3:0]）。 在自动满量程设置模式下，器件通电后为1100。代码1101b、1110b和1111b（0Dh、0Eh和0Fh）保留给将来使用。

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Table 10. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CT	R/W	1b	**转换时间领域 (read or write).** 转换时间字段决定了光到数字转换过程的长度。选择是100ms和800ms。较长的积分时间可以使测量的噪音更低。 转换时间也与数据转换过程的有效分辨率有关。800毫秒的转换时间可以达到完全规定的勒克斯分辨率。在结果和配置寄存器中E[3:0]的满量程高于0101b时，100毫秒的转换时间也可以达到完全规定的勒克斯分辨率。E[3:0]的满量程低于0101b（包括0101b）时，100毫秒的转换时间可使有效的结果分辨率减少多达3位，是所选满量程的一个函数。范围0101b减少一个比特。范围0100b、0011b、0010b和0001b减少两个位。范围0000b减少3位。结果寄存器格式和相关的LSB权重不随转换时间的变化而变化。 0 = 100 ms 1 = 800 ms
10:9	M[1:0]	R/W	00b	**转换操作的模式领域 (read or write).** 转换操作模式字段控制器件是在连续转换、单次拍摄或低功率关机模式下运行。默认值是00b（关机模式），这样在上电时，在对器件进行适当编程后，器件只消耗操作级别的功率。 当通过向该字段写入01b来选择单发模式时，该字段在器件主动转换时继续读取01b。当单次转换完成后，转换操作模式字段被自动设置为00b，器件被关闭。 当器件进入关机模式时，无论是通过完成单次转换还是通过对配置寄存器的手动写入，报告标志（转换就绪、标志高、标志低）或INT引脚的状态都没有变化。当器件处于关机模式时，这些信号将被保留用于后续的读操作。 00 = 关机 (default) 01 = 单次拍摄 10, 11 = 连续转换
8	OVF	R	0b	**溢出标志字段 (read-only).** 溢出标志字段表示在数据转换过程中发生溢出情况时，通常是因为照亮设备的光线超过了设备的编程满刻度范围。在这种情况下，OVF被设置为1，否则OVF保持为0。该字段在每次测量时都会重新评估。 如果满量程是手动设置的（RN[3:0]字段<1100b），溢出标志字段可以被设置，同时结果寄存器报告的值小于满量程。如果输入光有一个临时的高尖峰水平，暂时超过了集成ADC转换器电路的负荷，但在转换完成前又返回到范围内的水平，就会出现这种结果。因此，溢出标志报告了转换过程中可能出现的错误。这种行为在积分式转换器中很常见。 如果自动设置了满量程（RN[3:0]字段=1100b），那么设置溢出标志字段的唯一条件是输入光超出整个器件的满量程电平。当出现溢出条件且满量程未达到最大值时，OPT3001中止其当前转换，将满量程设置为更高的水平，并开始新的转换。该标志在该过程结束时被设置。这个过程重复进行，直到没有溢出条件或满量程被设置到最大范围。
7	CRF	R	0b	**准备转换的区域(read-only).** 转换准备字段表示转换完成的时间。该字段在转换结束时被设置为1，当配置寄存器随后被读取或写入任何数值时，除了包含关机模式（操作模式字段，M[1:0]=00b）外，该字段被清除（设置为0）。写入关机模式并不影响这个字段的状态，更多的细节见中断报告机制模式部分。
6	FH	R	0b	**高标志位 (read-only).** 高位标志字段(FH)确定转换的结果大于指定的关注水平。当结果大于高限值寄存器中的电平时，FH被设置为1。 (寄存器地址03h)中的电平时，FH被设置为1，而故障计数字段(FC[1:0])定义的连续测量次数。关于这个字段的清零和其他行为的更多细节，请参见中断报告机制模式部分。
5	FL	R	0b	**低标志位(read-only).** 标志低域（FL）识别转换的结果小于指定的关注水平。当结果小于低限寄存器中的电平时，FL被设置为1。 (寄存器地址02h)中的电平时，FL被设置为1，其连续测量次数由故障计数字段(FC[1:0])定义。关于这个字段的清零和其他行为的更多细节，请参见中断报告机制模式部分。

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Table 10. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	L	R/W	1b	**锁定领域 (read or write).** 闩锁字段控制中断报告机制的功能：INT引脚、标志高字段（FH）和标志低字段（FL）。该位在锁存窗口式比较和透明磁滞式比较之间选择报告方式。 0= 器件在透明的滞后式比较操作中发挥作用，其中三个中断报告机制直接反映了结果寄存器与高限和低限寄存器的比较，没有用户控制的清零事件。更多细节请参见中断操作、INT引脚和中断报告机制部分。 1= 器件在锁存窗口式比较操作中起作用，锁存中断报告机制，直到发生用户控制的清除事件。
3	POL	R/W	0b	**极性场Polarity field (read or write).** 极性字段控制INT引脚的极性或有效状态。 0=INT 引脚报告低电平，在发生中断事件时将引脚拉低。 1=INT 引脚的操作是反转的，INT引脚报告高电平，成为高阻抗，允许INT引脚在中断事件中被拉高。
2	ME	R/W	0b	**掩码指数字段Mask exponent field (read or write).** 当手动设置满量程时，屏蔽指数字段强制结果寄存器的指数字段（寄存器00h，位E[3:0]）为0000b，这可以简化手动编程满量程时对结果寄存器的处理。当屏蔽指数字段被设置为1，并且量程号字段（RN[3:0]）被设置为小于1100b时，会出现这种行为。注意，屏蔽只对结果寄存器执行。当使用中断报告机制时，与低限和高限寄存器的结果比较不受ME字段的影响。
1:0	FC[1:0]	R/W	00b	**故障计数字段Fault count field (read or write).** 故障计数字段指示器件需要多少个连续的故障事件来触发中断报告机制：INT引脚、标志高字段（FH）和标志低字段（FL）。故障事件在锁存器字段（L）、标志高字段（FH）和标志低字段（FL）的描述中。 00= 一个故障计数(默认) 01= 两个故障计数 10= 四个故障计数 11= 八个故障计数

7.6.1.1.3 低限值寄存器 (offset = 02h) [reset = C0000h]

该寄存器为中断报告机制设置比较下限：INT引脚、标志高域（FH）和标志低域（FL），如中断报告机制模式部分所述。

Figure 25. Low-Limit Register

15	14	13	12	11	10	9	8
LE3	LE2	LE1	LE0	TL11	TL10	TL9	TL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 11. Low-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	LE[3:0]	R/W	0h	**Exponent.** 这些位是指数位。表12提供了进一步的细节。
11:0	TL[11:0]	R/W	000h	**Result.** 这些位是直接二进制编码的结果（零到满分）。

这个寄存器的格式与结果寄存器的格式几乎相同，在结果寄存器中描述。低限值寄存器的指数（LE[3:0]）与结果寄存器的指数（E[3:0]）相似。低限值寄存器的结果（TL[11:0]）与结果寄存器的结果（R[11:0]）类似。

公式4给出了将该寄存器转化为勒克斯阈值的方程式，它与结果寄存器的方程式相似，即方程3。

$$lux = 0.01 \times (2^{LE[3:0]}) \times TL[11:0] \tag{4}$$

Table 12 gives the full-scale range and LSB size as it applies to the low-limit register. The detailed discussion and examples given in for the Result Register apply to the low-limit register as well.

Table 12. Full-Scale Range and LSB Size as a Function of Exponent Level

LE3	LE2	LE1	LE0	FULL-SCALE RANGE (lux)	LSB SIZE (lux per LSB)
0	0	0	0	40.95	0.01
0	0	0	1	81.90	0.02
0	0	1	0	163.80	0.04
0	0	1	1	327.60	0.08
0	1	0	0	655.20	0.16
0	1	0	1	1310.40	0.32
0	1	1	0	2620.80	0.64
0	1	1	1	5241.60	1.28
1	0	0	0	10483.20	2.56
1	0	0	1	20966.40	5.12
1	0	1	0	41932.80	10.24
1	0	1	1	83865.60	20.48

NOTE

The result and limit registers are all converted into lux values internally for comparison. These registers can have different exponent fields. However, when using a manually-set full-scale range (configuration register, RN < 0Ch, with mask enable (ME) active), programming the manually-set full-scale range into the LE[3:0] and HE[3:0] fields can simplify the choice of programming the register. This simplification results in the user only having to think about the fractional result and not the exponent part of the result.

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7.6.1.1.4 高限值寄存器 (offset = 03h) [reset = BFFFh]

高限寄存器为中断报告机制设置比较上限：INT引脚、标志高域（FH）和标志低域（FL），如中断操作、INT引脚和中断报告机制部分所述。这个寄存器的格式与低限寄存器（在低限寄存器中描述）和结果寄存器（在结果寄存器中描述）的格式几乎相同。为了更详细地解释这种相似性，高限值寄存器的指数（HE[3:0]）与低限值寄存器的指数（LE[3:0]）和结果寄存器的指数（E[3:0]）相似。高限值寄存器结果（TH[11:0]）与低限值结果（TH[11:0]）和结果寄存器结果（R[11:0]）类似。请注意，高限值寄存器与结果寄存器的比较不受ME位的影响。

当使用手动设置的满量程和屏蔽使能（ME）激活时，将手动设置的满量程编程到HE[3:0]位可以简化编程到该寄存器所需的数值选择。将该寄存器转换为勒克斯的公式与公式4相似。满刻度值与表8类似。

Figure 26. High-Limit Register

15	14	13	12	11	10	9	8
HE3	HE2	HE1	HE0	TH11	TH10	TH9	TH8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 13. High-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	HE[3:0]	R/W	Bh	**Exponent.** These bits are the exponent bits.
11:0	TH[11:0]	R/W	FFFh	**Result.** These bits are the result in straight binary coding (zero to full-scale).

7.6.1.1.5 制造商ID注册 (offset = 7Eh) [reset = 5449h]

这个寄存器的目的是帮助唯一地识别设备。

Figure 27. 制造商ID注册

15	14	13	12	11	10	9	8
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 14. Manufacturer ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ID[15:0]	R	5449h	**Manufacturer ID.** 制造商ID读作5449h。在ASCII码中，该寄存器的读数为TI。

7.6.1.1.6 设备ID寄存器 (offset = 7Fh) [reset = 3001h]

这个寄存器也是为了帮助唯一地识别设备。

Figure 28. Device ID Register

15	14	13	12	11	10	9	8
DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 15. Device ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DID[15:0]	R	3001h	**Device ID.** 设备ID读作3001h。

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Ambient light sensors are used in a wide variety of applications that require control as a function of ambient light. Because ambient light sensors nominally match the human eye spectral response, they are superior to photodiodes when the goal is to create an experience for human beings. Very common applications include display optical-intensity control and industrial or home lighting control.

There are two categories of interface to the OPT3001: electrical and optical.

8.1.1 Electrical Interface

The electrical interface is quite simple, as illustrated in Figure 29. Connect the OPT3001 I^2C SDA and SCL pins to the same pins of an applications processor, microcontroller, or other digital processor. If that digital processor requires an interrupt resulting from an event of interest from the OPT3001, then connect the INT pin to either an interrupt or general-purpose I/O pin of the processor. There are multiple uses for this interrupt, including signaling the system to wake up from low-power mode, processing other tasks while waiting for an ambient light event of interest, or alerting the processor that a sample is ready to be read. Connect pullup resistors between a power supply appropriate for digital communication and the SDA and SCL pins (because they have open-drain output structures). If the INT pin is used, connect a pullup resistor to the INT pin. A typical value for these pullup resistors is 10 kΩ. The resistor choice can be optimized in conjunction to the bus capacitance to balance the system speed, power, noise immunity, and other requirements.

The power supply and grounding considerations are discussed in the *Power-Supply Recommendations* section.

Although spike suppression is integrated in the SDA and SCL pin circuits, use proper layout practices to minimize the amount of coupling into the communication lines. One possible introduction of noise occurs from capacitively coupling signal edges between the two communication lines themselves. Another possible noise introduction comes from other switching noise sources present in the system, especially for long communication lines. In noisy environments, shield communication lines to reduce the possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted.

8.1.2 Optical Interface

The optical interface is physically located within the package, facing away from the PCB, as specified by the *Sensor Area* in 图 37.

Physical components, such as a plastic housing and a window that allows light from outside of the design to illuminate the sensor (see Figure 30), can help protect the OPT3001 and neighboring circuitry. Sometimes, a dark or opaque window is used to further enhance the visual appeal of the design by hiding the sensor from view. This window material is typically transparent plastic or glass.

Any physical component that affects the light that illuminates the sensing area of a light sensor also affects the performance of that light sensor. Therefore, for optimal performance, make sure to understand and control the effect of these components. Design a window width and height to permit light from a sufficient field of view to illuminate the sensor. For best performance, use a field of view of at least ±35°, or ideally ±45° or more. Understanding and designing the field of view is discussed further in application report SBEA002, *OPT3001: Ambient Light Sensor Application Guide*.

Application Information (continued)

The visible-spectrum transmission for dark windows typically ranges between 5% to 30%, but can be less than 1%. Specify a visible-spectrum transmission as low as, but no more than, necessary to achieve sufficient visual appeal because decreased transmission decreases the available light for the sensor to measure. The windows are made dark by either applying an ink to a transparent window material, or including a dye or other optical substance within the window material itself. This attenuating transmission in the visible spectrum of the window creates a ratio between the light on the outside of the design and the light that is measured by the OPT3001. To accurately measure the light outside of the design, compensate the OPT3001 measurement for this ratio; an example is given in Dark Window Selection and Compensation.

Ambient light sensors are used to help create ideal lighting experiences for humans; therefore, the matching of the sensor spectral response to that of the human eye response is vital. Infrared light is not visible to the human eye, and can interfere with the measurement of visible light when sensors lack infrared rejection. Therefore, the ratio of visible light to interfering infrared light affects the accuracy of any practical system that represents the human eye. The strong rejection of infrared light by the OPT3001 allows measurements consistent with human perception under high-infrared lighting conditions, such as from incandescent, halogen, or sunlight sources.

Although the inks and dyes of dark windows serve their primary purpose of being minimally transmissive to visible light, some inks and dyes can also be very transmissive to infrared light. The use of these inks and dyes further decreases the ratio of visible to infrared light, and thus decreases sensor measurement accuracy. However, because of the excellent infrared rejection of the OPT3001, this effect is minimized, and good results are achieved under a dark window with similar spectral responses to those shown in Figure 31.

For best accuracy, avoid grill-like window structures, unless the designer understands the optical effects sufficiently. These grill-like window structures create a nonuniform illumination pattern at the sensor that make light measurement results vary with placement tolerances and angle of incidence of the light. If a grill-like structure is desired, the OPT3001 is an excellent sensor choice because it is minimally sensitive to illumination uniformity issues disrupting the measurement process.

Light pipes can appear attractive for aiding in the optomechanical design that brings light to the sensor; however, do not use light pipes with any ambient light sensor unless the system designer fully understands the ramifications of the optical physics of light pipes within the full context of his design and objectives.

8.2 Typical Application

Measuring the ambient light with the OPT3001 in a product case and under a dark window is described in this section. The schematic for this design is shown in Figure 29.

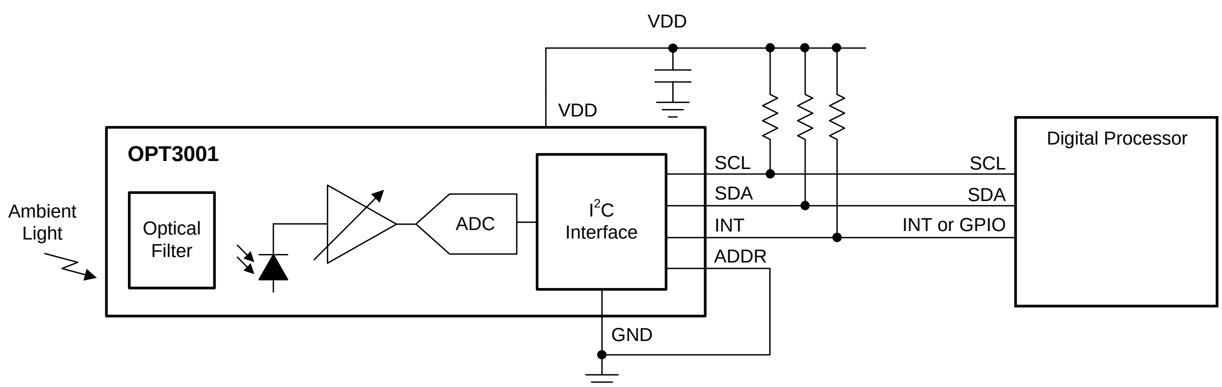

Figure 29. Measuring Ambient Light in a Product Case Behind a Dark Window

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Typical Application (continued)

8.2.1 设计要求

这种设计的基本要求是。

- 传感器隐藏在深色玻璃下，这样传感器就不明显了。请注意，这一要求是由设计者的主观偏好决定的。
- 荧光灯的测量精度为15%。
- 荧光灯、卤素灯和白炽灯之间的测量差异（也称为光源差异）要尽可能小。

8.2.2 详细设计程序

8.2.2.1 光学机械设计

完成电气设计后，下一个任务是光学财务设计。如图30所示，设计一个产品外壳，其中包括一个窗口，将产品外部的光线传输到传感器上。设计窗口的宽度和高度，使其具有±45°的视场。严格的视场设计要考虑到传感器区域的位置，如图37所示。OPT3001有源传感器区域沿封装顶视图的一个轴线居中，但在顶视图的另一个轴线上有一个小的偏移。窗口的大小和位置在应用报告SBEA002，OPT3001：环境光传感器应用指南中有更严格的讨论。

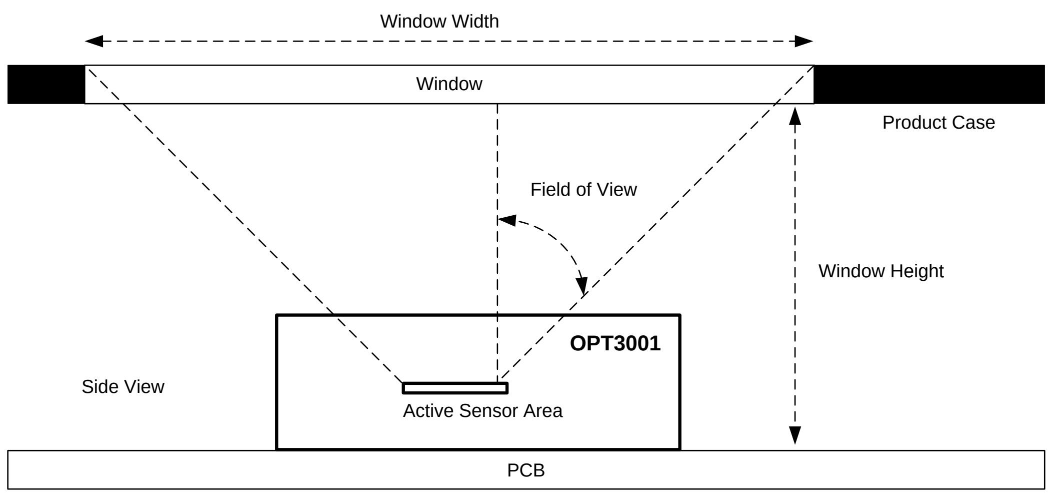

Figure 30. Product Case and Window Over the OPT3001

8.2.2.2 Dark Window Selection and Compensation

There are several approaches to selecting and compensating for a dark window. One of many approaches is the method described here.

Sample several different windows with various levels of darkness. Choose a window that is dark enough to optimize the balance between the aesthetics of the device and sensor performance. Note that the aesthetic evaluation is the subjective opinion of the designer; therefore, it is more important to see the window on the physical design rather than refer to window transmission specifications on paper. Make sure that the chosen window is not darker than absolutely necessary because a darker window allows less light to illuminate the sensor and therefore impedes sensor accuracy.

The window chosen for this application example is dark and has less than 7% transmission at 550 nm.Figure 31 shows the normalized response of the spectrum. Note that the equipment used to measure the transmission spectrum is not capable of measuring the absolute accuracy (non-normalized) of the dark window sample, but only the relative normalized spectrum. Also note that the window is much more transmissive to infrared wavelengths longer than 700 nm than to visible wavelengths between 400 nm and 650 nm. This imbalance between infrared and visible light decreases the ratio of visible light to infrared light at the sensor. Although it is preferable to have the window decrease this ratio as little as possible (by having a window with a close ratio of visible transmission to infrared transmission), the OPT3001 still performs well as shown in Figure 34.

Typical Application (continued)

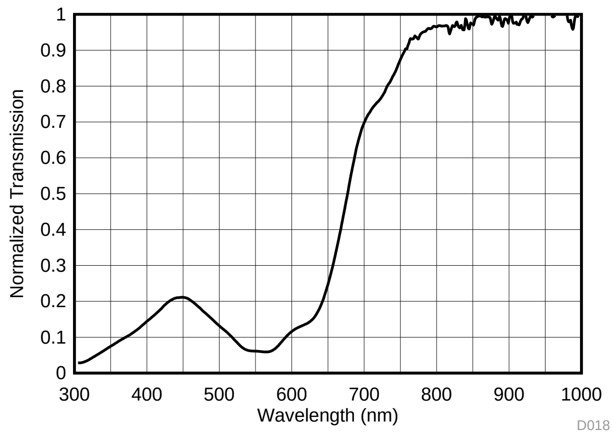

Figure 31. Normalized Transmission Spectral Response of the Chosen Dark Window

After choosing the dark window, measure the attenuating effect of the dark window for later compensation. In order to measure this attenuation, measure a fluorescent light source with a lux meter, then measure that same light with the OPT3001 under the dark window. To measure accurately, it is important to use a fixture that can accommodate either the lux meter or the design containing the OPT3001 and dark window, with the center of each of the sensing areas being in exactly the same *X, Y, Z* location, as shown in Figure 32. The *Z* placement of the design (distance from the light source) is the top of the window, and not the OPT3001 itself.

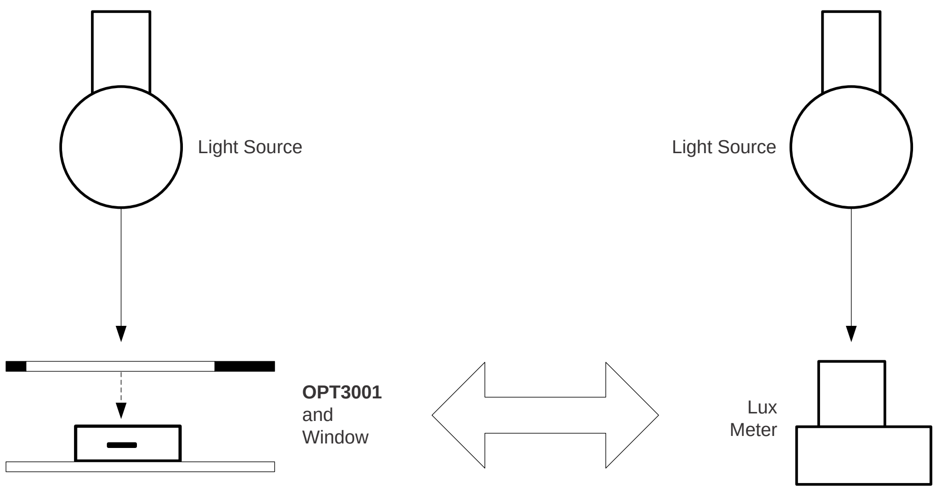

Figure 32. Fixture with One Light Source Accommodating Either a Lux Meter or the Design (Window and OPT3001) in the Exact Same X,Y,Z Position

The fluorescent light in this location measures 1000 lux with the lux meter, and 73 lux with the OPT3001 under the dark window within the application. Therefore, the window has an effective transmission of 7.3% for the fluorescent light. This 7.3% is the weighted average attenuation across the entire spectrum, weighted by the spectral response of the lux meter (or photopic response).

For all subsequent OPT3001 measurements under this dark window, the following formula is applied.

$$\text{Compensated Measurement} = \text{Uncompensated Measurement} / (7.3\%) \quad (5)$$

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Typical Application (continued)

8.2.3 Application Curves

To validate that the design example now measures correctly, create a sequential number of different light intensities with the fluorescent light by using neutral density filters to attenuate the light. Different light intensities can also be created by changing the distance between the light source, and the measurement devices. However, these two methods for changing the light level have minor accuracy tradeoffs that are beyond the scope of this discussion. Measure each intensity with both the lux meter and the OPT3001 under the window, and compensate using Equation 5. The results are displayed in Figure 33, and show that the application accurately reports results very similar to the lux meter.

To validate that the design measures a variety of light sources correctly, despite the large ratio of infrared transmission to visible light transmission of the window, measure the application with a halogen bulb and an incandescent bulb. Use the physical location and light attenuation procedures that were used for the fluorescent light. The results are shown in Figure 34.

The addition of the dark window changes the results as seen by comparing the results of the same measurement with a window (Figure 34) and without a window (Figure 3). Even after the expected change, the performance is still good. All data are both within 15% of the correct answer, and within 15% of the other bulb measurements.

Results can vary at different angles of light because the OPT3001 does not match the lux meter at all angles of light.

If the measurement variation between the light sources is not acceptable, choose a different window that has a closer ratio of visible light transmission to infrared light transmission.

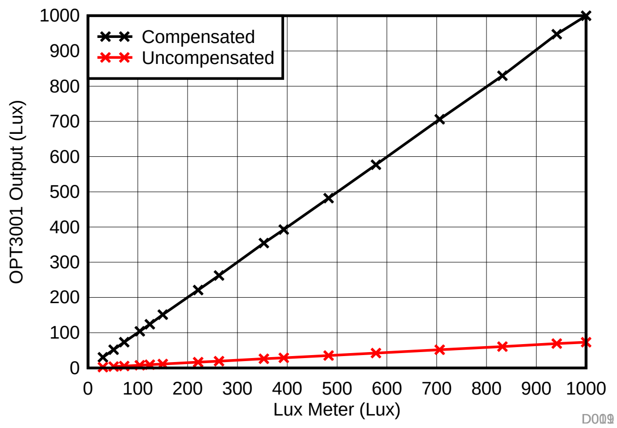

Figure 33. Uncompensated and Compensated Output of the OPT3001 Under a Dark Window Illuminated by Fluorescent Light Source

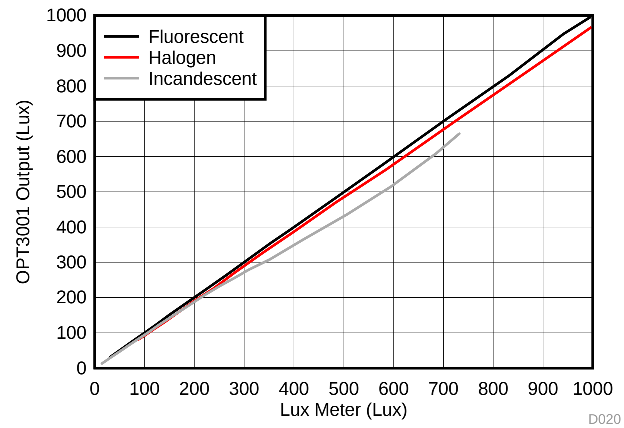

Figure 34. Compensated Output of the OPT3001 Under a Dark Window Illuminated by Fluorescent, Halogen, and Incandescent Light Sources

8.3 Do's and Don'ts

As with any optical product, special care must be taken into consideration when handling the OPT3001. Although the OPT3001 has low sensitivity to dust and scratches, proper optical device handling procedures are still recommended.

The optical surface of the device must be kept clean for optimal performance in both prototyping with the device and mass production manufacturing procedures. Tweezers with plastic or rubber contact surfaces are recommended to avoid scratches on the optical surface. Avoid manipulation with metal tools when possible. The optical surface must be kept clean of fingerprints, dust, and other optical-inhibiting contaminants.

If the device optical surface requires cleaning, the use of de-ionized water or isopropyl alcohol is recommended. A few gentile brushes with a soft swab are appropriate. Avoid potentially abrasive cleaning and manipulating tools and excessive force that can scratch the optical surface.

If the OPT3001 performs less than optimally, inspect the optical surface for dirt, scratches, or other optical artifacts.

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9 Power-Supply Recommendations

Although the OPT3001 has low sensitivity to power-supply issues, good practices are always recommended. For best performance, the OPT3001 V_{DD} pin must have a stable, low-noise power supply with a 100-nF bypass capacitor close to the device and solid grounding. There are many options for powering the OPT3001 because the device current consumption levels are very low.

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10 Layout

10.1 Layout Guidelines

The PCB layout design for the OPT3001 requires a couple of considerations. Bypass the power supply with a capacitor placed close to the OPT3001. Note that optically reflective surfaces of components also affect the performance of the design. The three-dimensional geometry of all components and structures around the sensor must be taken into consideration to prevent unexpected results from secondary optical reflections. Placing capacitors and components at a distance of at least twice the height of the component is usually sufficient. The most optimal optical layout is to place all close components on the opposite side of the PCB from the OPT3001. However, this approach may not be practical for the constraints of every design.

Electrically connecting the thermal pad to ground is recommended. This connection can be created either with a PCB trace or with vias to ground directly on the thermal pad itself. If the thermal pad contains vias, they are recommended to be of a small diameter (< 0.2 mm) to prevent them from wicking the solder away from the appropriate surfaces.

An example PCB layout with the OPT3001 is shown in Figure 35.

10.2 Layout Example

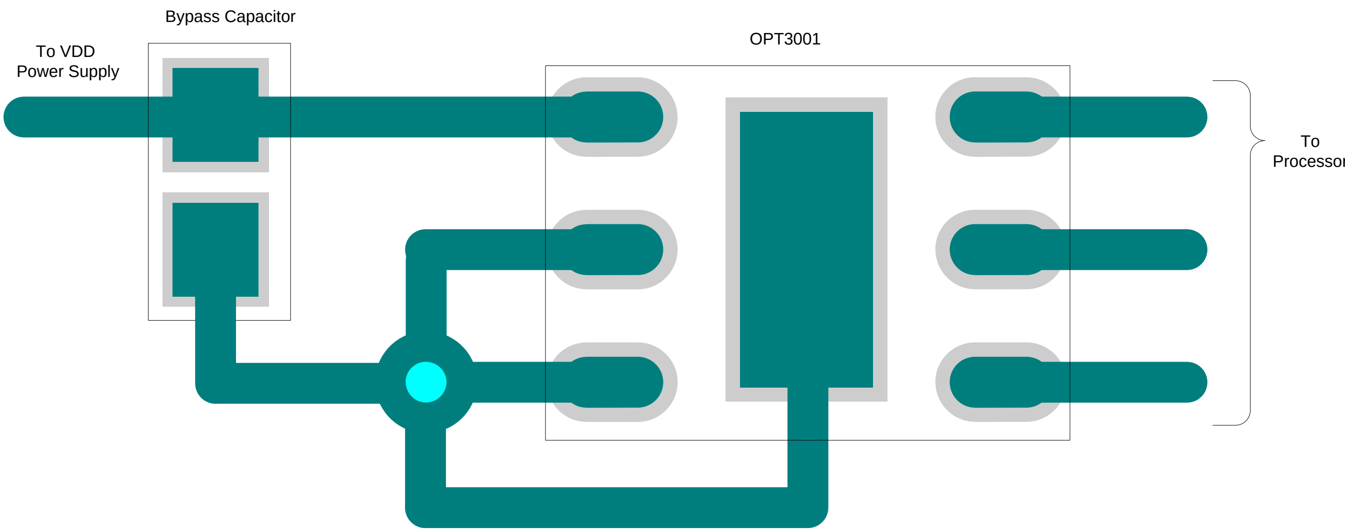

Figure 35. Example PCB Layout With the OPT3001

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- *《OPT3001：环境光传感器应用指南》*
- *《OPT3001EVM 用户指南》*
- *《QFN/SON PCB 连接 应用报告》*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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11.5 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

12.1 关于焊接和处理的相关建议

OPT3001 通过 JEDEC JSTD-020 认证，适用于三种回流焊操作。

请注意：温度过高会导致器件褪色并影响光学性能。

有关焊接热规范和其他详细信息，请参见应用报告*《QFN/SON PCB 连接》*(SLUA271)。如果必须从 PCB 上移除 OPT3001，请拆下此器件后不再重新连接。

处理 OPT3001 时需要像处理大多数光学器件那样谨慎操作，确保光学表面保持洁净无损伤。更多详细建议，请参见*Do's and Don'ts* 部分。为获得最优光学性能，完成焊接后必须清理焊剂和任何其他碎屑。

12.2 DNP (S-PDSO-N6) 机械制图

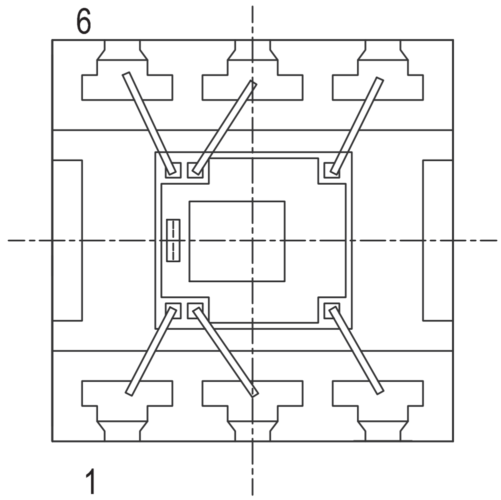

图 **36.** 引脚 **1** 的封装方向视觉基准
（顶视图）

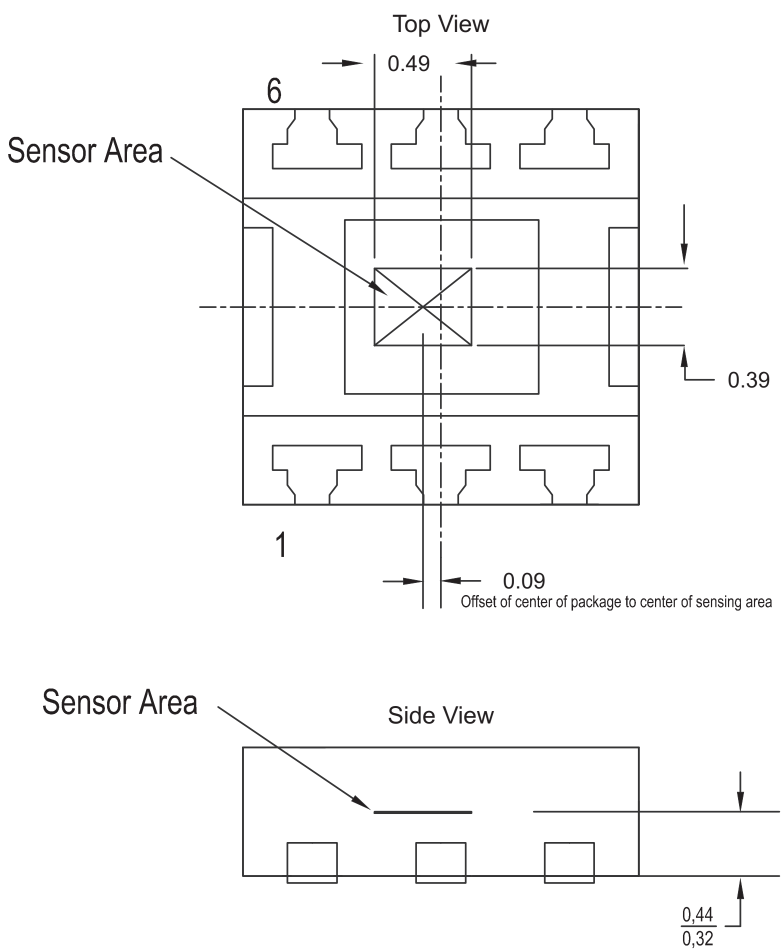

图 **37.** 显示感测区域位置的机械制图
（顶视图和侧视图）

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPT3001DNPR	ACTIVE	USON	DNP	6	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	ED	Samples
OPT3001DNPT	ACTIVE	USON	DNP	6	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	ED	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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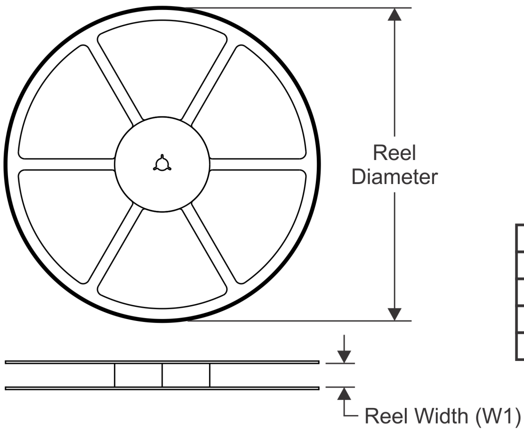
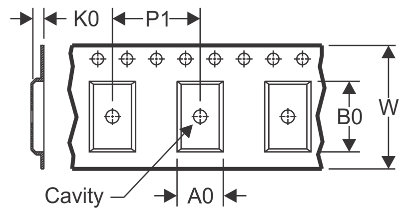
TAPE AND REEL INFORMATION

REEL DIMENSIONS

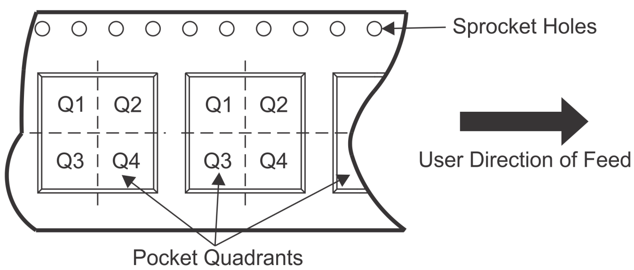


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

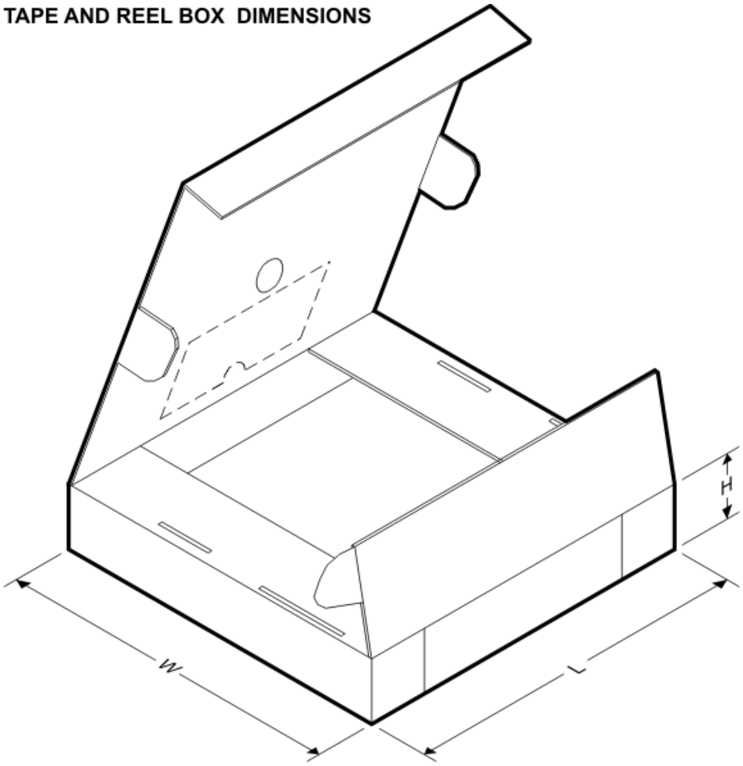
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

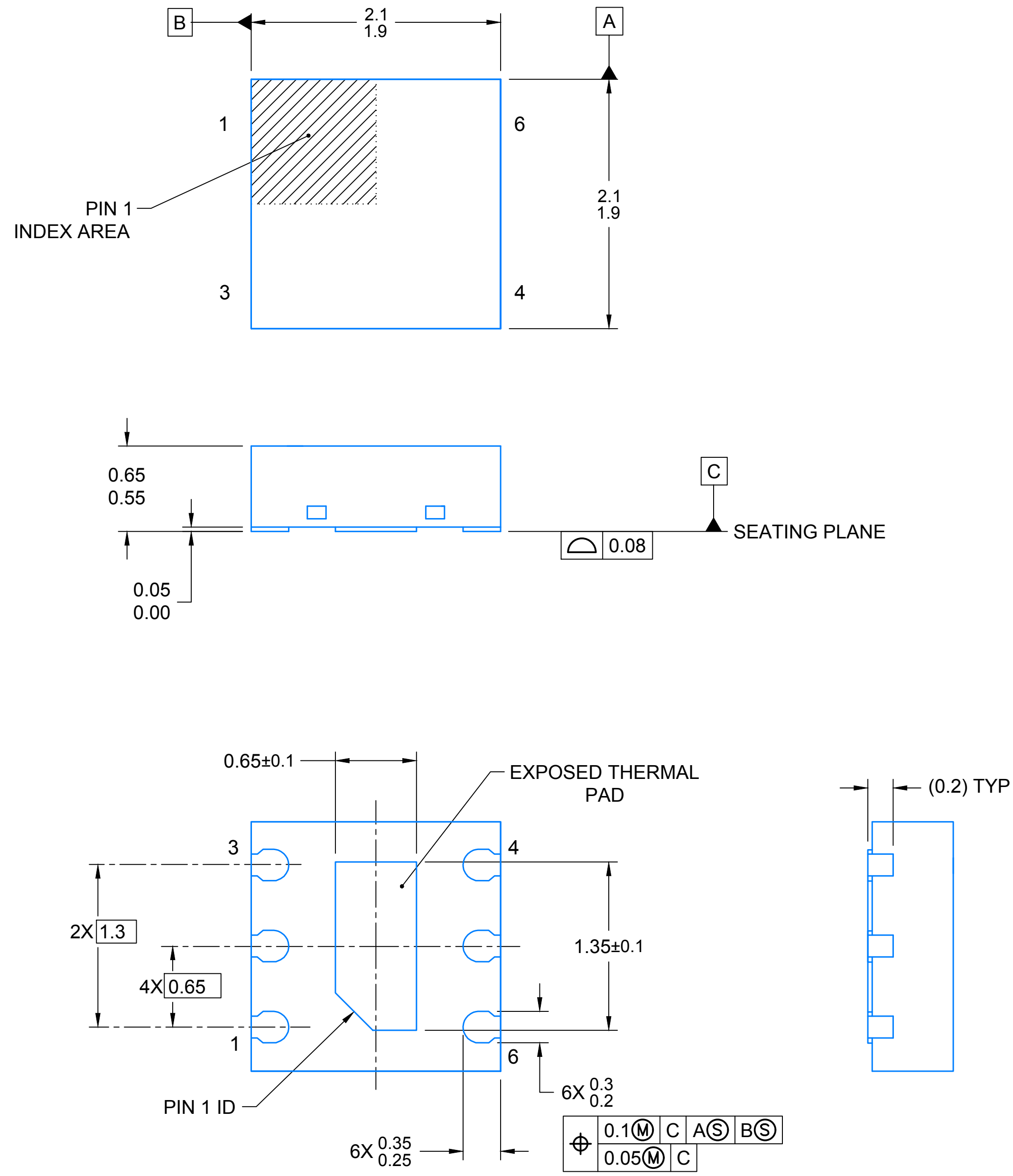
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPT3001DNPR	USON	DNP	6	3000	330.0	18.4	2.3	2.3	0.9	8.0	12.0	Q1
OPT3001DNPT	USON	DNP	6	250	180.0	12.4	2.3	2.3	0.9	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPT3001DNPR	USON	DNP	6	3000	356.0	338.0	48.0
OPT3001DNPT	USON	DNP	6	250	193.0	193.0	70.0



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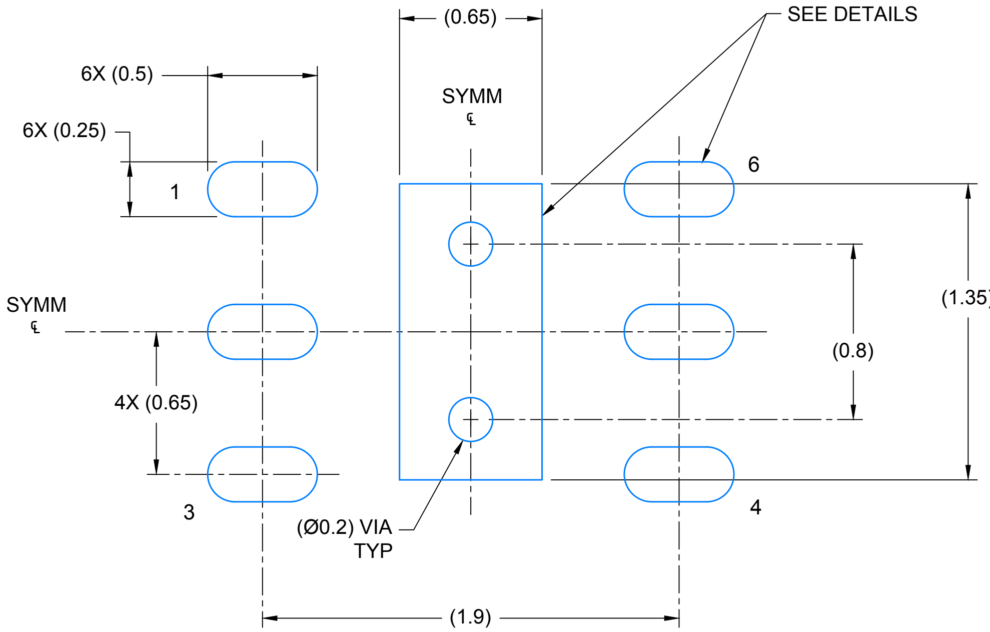
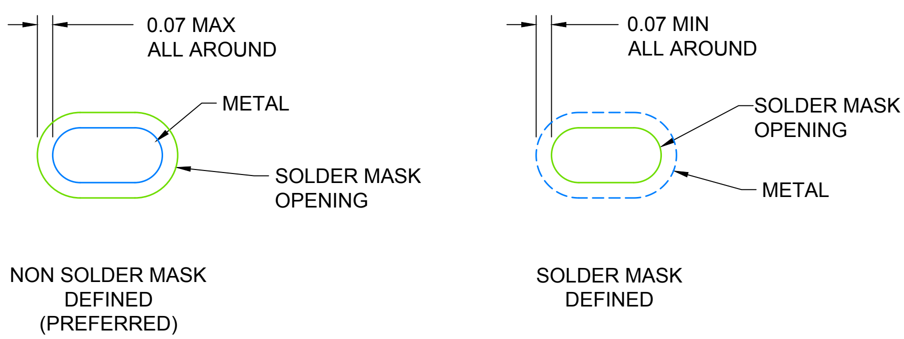
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Optical package with clear mold compound.



LAND PATTERN EXAMPLE
SCALE: 30X



SOLDER MASK DETAILS

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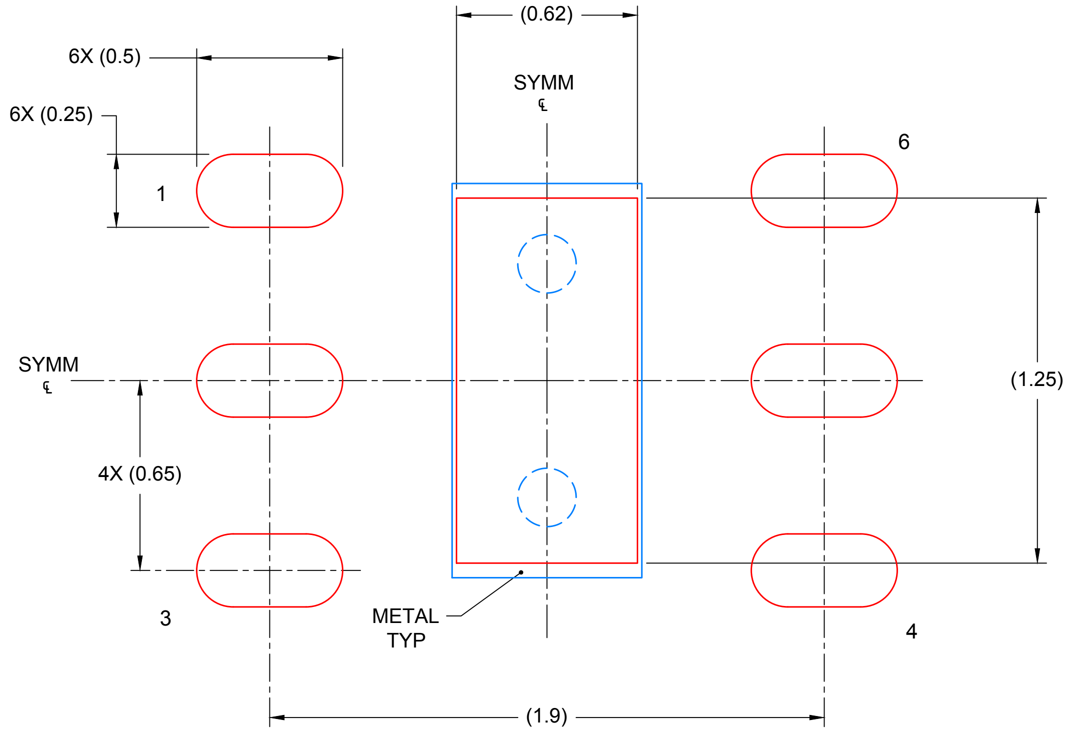
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 40X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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