Exhibit 103

EXHIBIT 103
Domestic Industry Claim Chart for Claims of U.S. Patent No. 12,675,407 (the "'407 Patent") Based on Samsung Practicing '407 Products

As shown in the chart below, the Samsung Practicing '407 Products, which include Samsung which include Samsung DDR5 RDIMMS and MRDIMMS, practice at least claim 1 of the '407 patent. It should be understood that Netlist's contentions are not limited to these products but instead encompass any and all reasonably similar products and components that practice the claims in the same or similar manner as discussed below. Netlist may supplement, modify or amend its contentions under the doctrine of equivalents based on any claim constructions, additional information obtained through formal discovery or other means, and/or based on other circumstances including any assertions by Respondents that the Samsung Practicing '407 Products do not practice the '407 patent as to any one or more of the limitations in the claim(s) below.

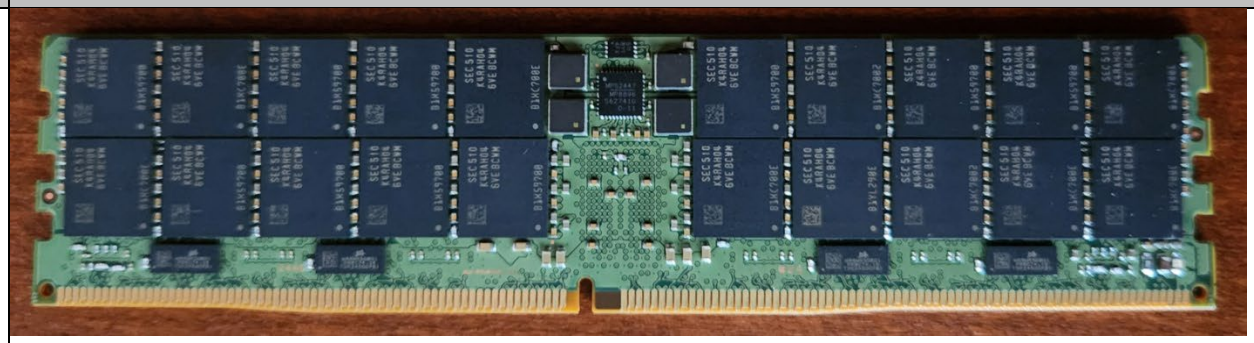
To the extent Respondents contend that any differences are alleged to exist between the asserted claims below and the Samsung Practicing '407 Products, such differences are insubstantial and the Samsung Practicing '407 Products perform substantially the same function, in substantially the same way, to yield substantially the same result, and therefore the Samsung Practicing '407 Products practice the claims below under the doctrine of equivalents. Netlist may supplement, modify or amend its contentions under the doctrine of equivalents based on any claim constructions, additional information obtained through formal discovery or other means, and/or based on other circumstances including any assertions that the Samsung Practicing '407 Products do not satisfy the technical domestic industry by Respondents as to any one or more of the limitations in the claims below.

Claim 1	Evidence of Use
[**1.pre**] A memory module operable in a computer system having a memory controller and a system bus, the system bus including one or more clock signal lines, control/address (C/A) signal lines and data signal lines, the memory module comprising:	To the extent the preamble is limiting, each of the Samsung Practicing '407 Products,[1] such as Samsung's imported Registered DIMMs ("RDIMMs") includes a memory module operable in a computer system having a memory controller and a system bus, the system bus including one or more clock signal lines, control/address (C/A) signal lines and data signal lines. Examples of Samsung DIMMs are shown below. The Samsung Practicing '407 Products each include a "memory module:" Ex. CC-116 (Samsung 4800MHz PC5-38400): Samsung 64GB DDR5 4800MHz PC5-38400 ECC RDIMM 2Rx4 (EC8 10x4) Dual Rank 1.1V Registered DIMM 288-Pin Server RAM Memory M321R8GA0BB0-CQK.

[1] Analysis for certain limitations below uses RDIMM format as an example, but based on currently available information MRDIMMs would operate in materially the same way in all relevant parts. *See* JEDEC Press Release (planned features for MRDIMMs include "Utilization of standard DDR5 DIMM components including DRAM, DIMM Form Factor & Pinout, SPD, PMIC, and TS for ease of adoption").

Claim 1	Evidence of Use
	 Ex. CC-117 (Samsung 5600MHz PC5-44800): Samsung 64GB DDR5 5600MHz PC5-44800 ECC RDIMM 2Rx4 (EC8 10x4) Dual Rank 1.1V Registered DIMM 288-Pin Server RAM Memory M321R8GA0PB0-CWM. Ex. CC-118 (Samsung 64GB DDR5 PC5-4800 EC8 RDIMM 2Rx4 M321R8GA0BB0-CQK).

Claim 1	Evidence of Use
	  Ex. CC-119 (Samsung 64GB DDR5 PC5-6400 EC8 RDIMM 2Rx4 M321R8GA0PB2-CCP).

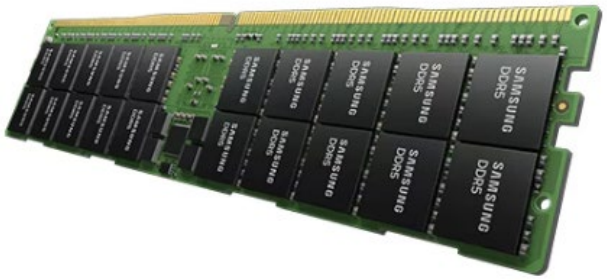
Claim 1	Evidence of Use
	 An image of a Samsung MRDIMM M327R8GA0EB0-CLVXB. *See* Exs. CC-111, CC-112, CC-113. "DIMM" in RDIMM and MRDIMM stands for dual inline ***memory module***. For example, Samsung's web pages for its RDIMM, LRDIMM, and UDIMM products are preceded by an overview page labeled "***memory modules*** for extensive use" that explains "Samsung's ***memory modules*** are designed for a wide range of applications to deliver the best performance with low power requirements." Ex. CC-95 (Samsung DRAM Modules). *See also* Ex. CC-114 ("Samsung has developed a Multi-Ranked Buffered Dual In-Line ***Memory Module*** (MCRDIMM) … . This ***module*** …."); Ex. CC-94 ("***Module*** Handling Guide" covering DDR5 UDIMMs, MRDIMMs, RDIMMs, and SO-DIMMs). The memory module of the Samsung Practicing '407 Products are further operable in a computer system having a memory controller and a system bus. For example:

Claim 1	Evidence of Use
	Samsung's web site advertises various dual in-line memory modules "for a wide range of applications." Ex. CC-95 (Samsung DRAM Modules). For instance, Samsung advertises registered DIMMs ("RDIMMs"), including ones with ECC capability, as suitable for server applications. *Id.*

RDIMM

Registered DIMM

Include a register for enhancing the clock, command and control signals
Error correction is available by adding 8-bit parity signals
Supports x4 / x8 Organization / up to 2 ranks per DIMM and 3DPC configuration
Application : Server



Additionally, the Samsung Practicing '407 Products are JEDEC compliant, further demonstrating they are memory modules operable in computer systems having memory controllers and system busses. *See, e.g.:*

> Samsung first entered the DDR5 PMIC market in 2017. After making this move, the company released its first PMIC for DDR5 DRAM modules in 2021. Previously, the mainboard supplied power to the module through the PMIC. With the transition to DDR5, however, JEDEC has mandated that the PMIC must be embedded internally within the module. As a leader in the field, Samsung manufactures products that abide by JEDEC standards and consistently aims for the best efficiency in the industry, as well as robust design. This approach is not limited to PMICs, however. The company is also expanding the lineup of products necessary for DDR5 modules, making the goal of providing customers with a total solution a top priority.

Ex. CC-104 (Samsung Optimized DDR5 DIMM Solutions) at 1.

Claim 1	Evidence of Use

1.0 DDR5 REGISTERED DIMM ORDERING INFORMATION

[Table 1] Ordering Information

Part Number [1]	Density	Organization	Component Composition[2]	Number of Rank	Height
M321R2GA3BB0-CQK##	16GB	2Gx80	2Gx8(K4RAH086VB-BCQK) * 10	1	31.25mm±0.15mm
M321R4GA3BB0-CQK##	32GB	4Gx80	2Gx8(K4RAH086VB-BCQK) * 20	2	31.25mm±0.15mm
M321R4GA0BB0-CQK##	32GB	4Gx80	4Gx4(K4RAH046VB-BCQK) * 20	1	31.25mm±0.15mm
M321R8GA0BB0-CQK##	64GB	8Gx80	4Gx4(K4RAH046VB-BCQK) * 40	2	31.25mm±0.15mm

NOTE :
1) "##"- Bucket field for PMIC/RCD information.
2) "QK" - 4400Mbps 36-36-36, 4800Mbps 40-39-39.

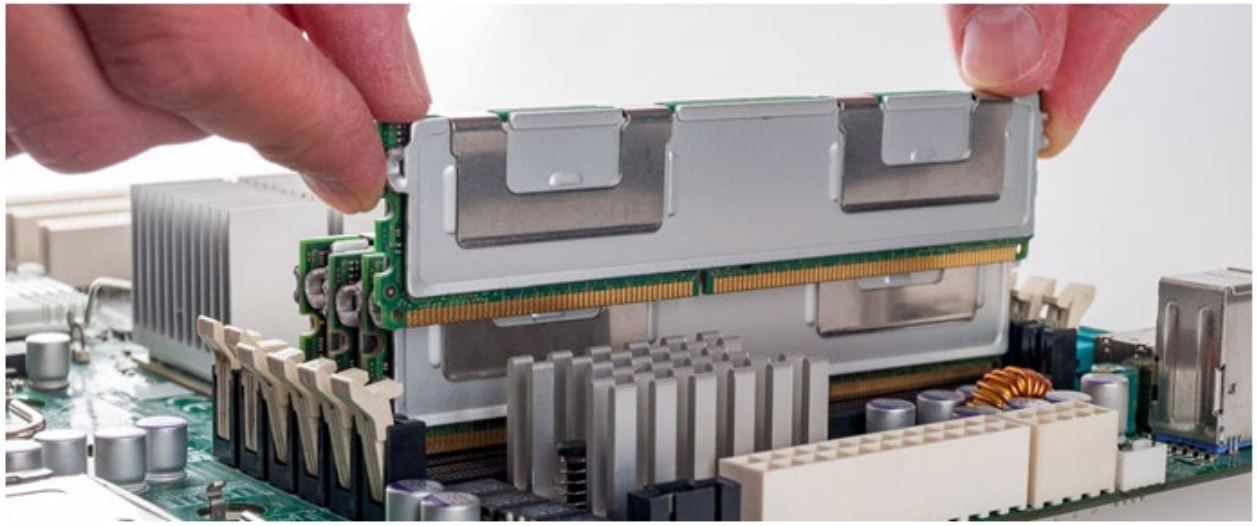
2.0 KEY FEATURES

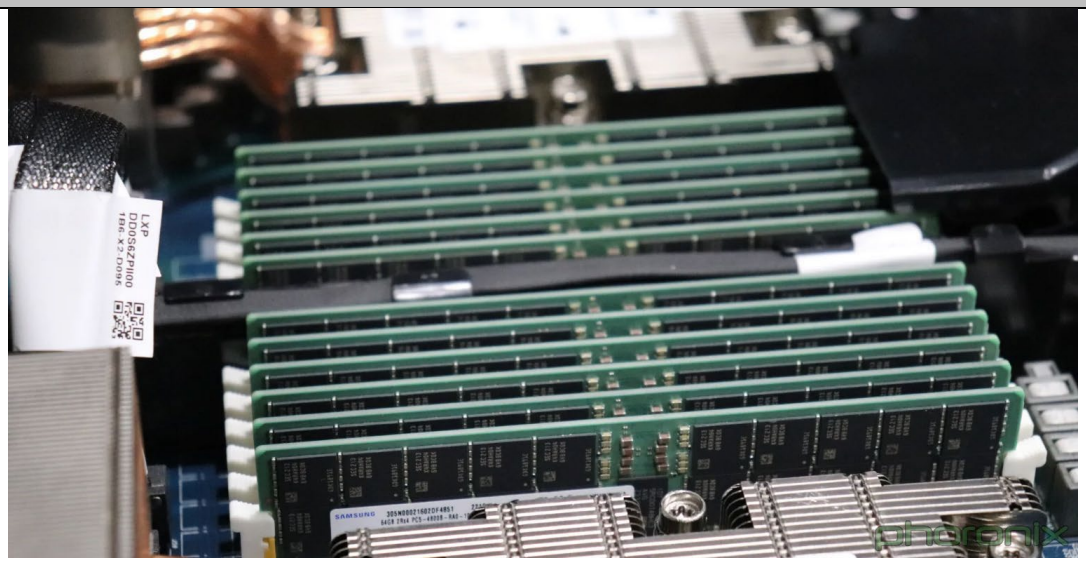
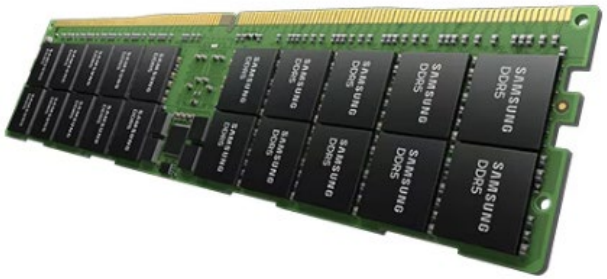
[Table 2] Key Parameters for 4800Mbps Speed Bin

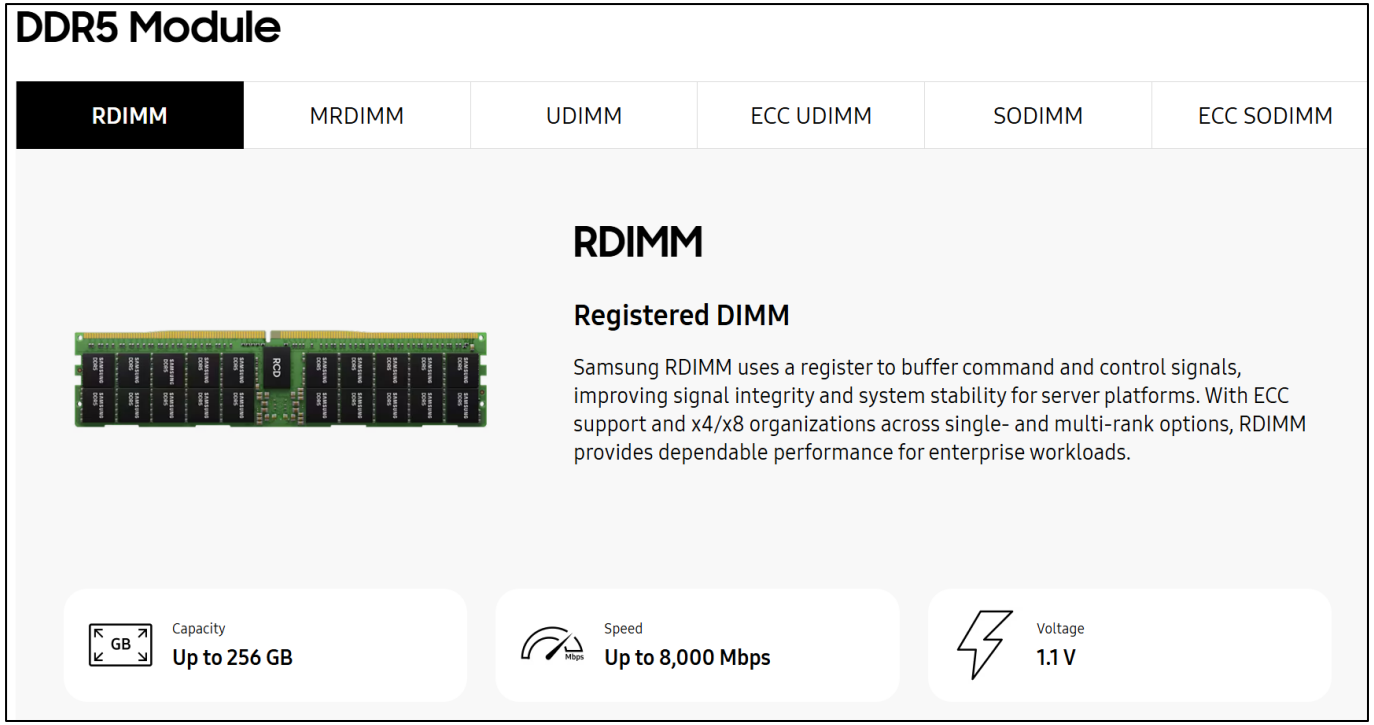
Speed	DDR5-4400	DDR5-4800	Unit
	36-36-36	40-39-39	
tCK(min)	0.454	0.416	ns
CAS Latency	36	40	nCK
tRCD(min)	16.000	16.000	ns
tRP(min)	16.000	16.000	ns
tRAS(min)	32.000	32.000	ns
tRC(min)	48.000	48.000	ns

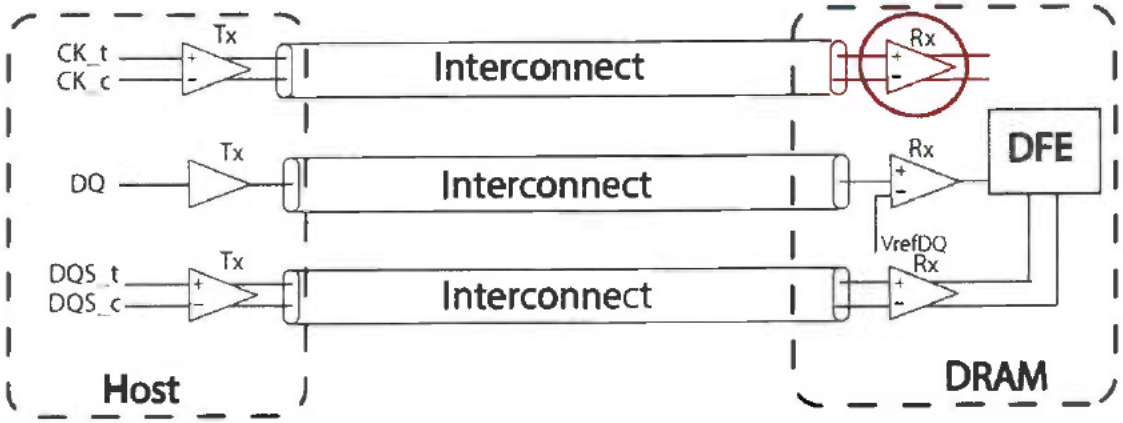
- JEDEC standard compliant.
- VDD = VDDQ = 1.1V (1.067V(- 3%) ~ 1.166V(+6%)).
- VPP = 1.8V (1.746 (-3%) ~ 1.908 (+6%).
- 2200MHz f_{CK} for 4400Mb/sec/pin, 2400MHz f_{CK} for 4800Mb/sec/pin.
- 32 Banks (8 Bank Groups).
- Programmable CAS Latency (posted CAS): 22,26,28,30,32,36,40,42.
- Programmable CAS Write Latency (CWL) = RL-2.
- 16-bit prefetch.
- Burst Length: 16 by default. 8 with tCCD=8, which does not allow gapless READ or WRITE, where BC8 and BL32 refer to CA5 BL*=L.
- Bi-directional Differential Data-Strobe.
- Internal ZQ calibration via Multi-Purpose Command (MPC) - ZQcal start and ZQcal Latch.
- On Die Termination (ODT) via Mode Register setting : RTT_PARK, RTT_WR, RTT_NOM_WR, RTT_NOM_RD.
- Average Refresh period 3.9us at lower than T_{CASE} 85°C, 1.95us at 85°C < T_{CASE} ≤ 95 °C.
- Connectivity Test Mode (TEN) is supported.
- Asynchronous Reset.

Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 5.

Claim 1	Evidence of Use
	This standard defines the electrical and mechanical requirements for 288-position, 1.1 Volt (VDD and VDDQ), DDR5 Registered (RDIMM), Double Data Rate (DDR), Synchronous DRAM Dual In-Line Memory Modules (DIMM). These Registered DDR5 SDRAM DIMMs are intended for use in server, workstation, and database environments. Ex. CC-88 DDR5 Registered Dual Inline Memory Module (RDIMM) Common Standard, JESD305B.01 v. 3.00, JEDEC, (Feb. 2026) ("JEDEC 305B") at 1. As seen above, Samsung's RDIMMs each include edge connections with gold fingers which are configured to fit into a memory slot connector of a server computer's motherboard (system board) for communication with a memory controller via a system bus. *See also*, *e.g.*,  Ex. CC-120 (Samsung, "Memory VR changes in the system by DDR5 adoption") (showing a DIMM being inserted into a memory slot having a system bus on a motherboard of a computer system).

Claim 1	Evidence of Use
	 Ex. CC-70 (DDR5 Memory Channel Scaling Performance). System busses with which the Samsung Practicing ’407 Products are operable each include one or more clock signal lines, control/address (C/A) signal lines and data signal lines. For example, Samsung’s web site described its RDIMMs as each “[i]nclud[ing] a register for enhancing the clock, command and control signals.” *See* Ex. CC-95 (Samsung DRAM Modules): **RDIMM** **Registered DIMM** Include a register for enhancing the clock, command and control signals Error correction is available by adding 8-bit parity signals Supports x4 / x8 Organization / up to 2 ranks per DIMM and 3DPC configuration Application : Server 

Claim 1	Evidence of Use
	This indicates that the system bus includes clock, command and control signals. *See also*, *e.g.*, Ex. CC-95 (Samsung DRAM Modules):  The system bus also includes data signal lines, as illustrated by an exemplary Samsung's RDIMM datasheet, showing interconnects between a host (memory system's memory controller) and a DRAM device (*e.g.*, one on an RDIMM) for DQ (data) signals, as well as clock and data strobe (DQS) signals:

Claim 1	Evidence of Use
	 Figure 10. Example of DDR5 Memory Interconnect (Ex. CC-89 at 42, Fig. 10). As another example, a representative Samsung RDIMM datasheet show that the RDIMM includes CA and CS control/address signal pins, CK_t/c clock signal pins, and DQ and CB data signal pins:

Claim 1	Evidence of Use

[Table 5] PIN Description

Pin Name	Description
CA[6:0]_A CA[6:0]_B	SDRAM Address and Command Bus
CS[1:0]_A CS[1:0]_B	SDRAM Chip Select
PAR_A PAR_B	SDRAM Parity input
CK_t	SDRAM Clocks (true/positive)
CK_c	SDRAM Clocks (complement/negative)
ALERT_n	SDRAM alert for CRC error
RESET_n	Set DRAM to known state
PCAMP	Control and Monitor Port
HSCL	I2C/I3C-Basic Host Sideband Bus Clock
HSDA	I2C/I3C-Basic Host Sideband Bus Data
HSA	I2C/I3C-Basic Host Sideband Bus Address
LBDQ	Loopback data output:

Pin Name	Description
DQ[31:0]_A DQ[31:0]_B	DIMM memory data bus channel A and B
CB[7:0]_A CB[7:0]_B	DIMM ECC check bits(CB) channel A and B
DQS[9:0]_A_t DQS[9:0]_B_t	SDRAM data strobes (positive line of differential pair)
DQS[9:0]_A_c DQS[9:0]_B_c	SDRAM data strobes (negative line of differential pair)
TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
VIN_BULK	DIMM Power Supply from system to PMIC
VIN_MGMT	DIMM Power Supply from system to PMIC
VSS	Power supply return (ground)
RFU	Reserved for future use
LBDQS	Loopback data strobe output

Ex. CC-89 at 9.

[Table 4] PIN Configuration

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VIN_BULK	145	VIN_BULK	50	VSS	194	DQ31_A	96	CB0_B	240	VSS
2	RFU	146	VIN_BULK	51	CB0_A	195	VSS	97	VSS	241	CB2_B
3	VIN_MGMT	147	PWR_GOOD/FAIL_n	52	VSS	196	CB2_A	98	CB1_B	242	VSS
4	SCL	148	SAA	53	CB1_A	197	VSS	99	VSS	243	CB3_B
5	SDA	149	RFU	54	VSS	198	CB3_A	100	DQ0_B	244	VSS
6	VSS	150	RFU	55	DQS4_A_t	199	VSS	101	VSS	245	DQ2_B
7	DQ0_A	151	VSS	56	DQS4_A_c	200	DQS9_A_c,TDQS9_A_c	102	DQ1_B	246	VSS
8	VSS	152	DQ2_A	57	VSS	201	DQS9_A_t,TDQS9_A_t	103	VSS	247	DQ3_B
9	DQ1_A	153	VSS	58	CB4_A	202	VSS	104	DQS0_B_t	248	VSS
10	VSS	154	DQ3_A	59	VSS	203	CB6_A	105	DQS0_B_c	249	DQS5_B_c,TDQS5_B_c
11	DQS0_A_t	155	VSS	60	CB5_A	204	VSS	106	VSS	250	DQS5_B_t,TDQS5_B_t
12	DQS0_A_c	156	DQS5_A_c, TDQS5_A_c	61	VSS	205	CB7_A	107	DQ4_B	251	VSS
13	VSS	157	DQS5_A_t, TDQS5_A_t	62	ALERT_n	206	VSS	108	VSS	252	DQ6_B
14	DQ4_A	158	VSS	63	VSS	207	RESET_n	109	DQ5_B	253	VSS
15	VSS	159	DQ5_A	64	CS0_A_n	208	VSS	110	VSS	254	DQ7_B
16	DQ5_A	160	VSS	65	VSS	209	CS1_A_n	111	DQ6_B	255	VSS
17	VSS	161	DQ7_A	66	CA0_A	210	VSS	112	VSS	256	DQ10_B
18	DQ8_A	162	VSS	67	VSS	211	CA1_A	113	DQ9_B	257	VSS
19	VSS	163	DQ10_A	68	CA2_A	212	VSS	114	VSS	258	DQ11_B
20	DQ9_A	164	VSS	69	VSS	213	CA3_A	115	DQS1_B_t	259	VSS
21	VSS	165	DQ11_A	70	CA4_A	214	VSS	116	DQS1_B_c	260	DQS6_B_c,TDQS6_B_c
22	DQS1_A_t	166	VSS	71	VSS	215	CA5_A	117	VSS	261	DQS6_B_t,TDQS6_B_t
23	DQS1_A_c	167	DQS6_A_c,TDQS6_A_c	72	CA6_A	216	VSS	118	DQ12_B	262	VSS
24	VSS	168	DQS6_A_t,TDQS6_A_t	73	VSS	217	CK_t	119	VSS	263	DQ14_B
25	DQ12_A	169	VSS	74	PAR_A	218	CK_c	120	DQ13_B	264	VSS
26	VSS	170	DQ14_A	75	VSS	219	VSS	121	VSS	265	DQ15_B
27	DQ13_A	171	VSS	KEY				122	DQ16_B	266	VSS
28	VSS	172	DQ15_A					123	VSS	267	DQ18_B
29	DQ16_A	173	VSS					124	DQ17_B	268	VSS
30	VSS	174	DQ18_A	76	CA0_B	220	RFU	125	VSS	269	DQ19_B
31	DQ17_A	175	VSS	77	VSS	221	CA1_B	126	DQS2_B_t	270	VSS
32	VSS	176	DQ19_A	78	CA2_B	222	VSS	127	DQS2_B_c	271	DQS7_B_c,TDQS7_B_c
33	DQS2_A_t	177	VSS	79	VSS	223	CA3_B	128	VSS	272	DQS7_B_t,TDQS7_B_t
34	DQS2_A_c	178	DQS7_A_c,TDQS7_A_c	80	CA4_B	224	VSS	129	DQ20_B	273	VSS
35	VSS	179	DQS7_A_t, TDQS7_A_t	81	VSS	225	CA5_B	130	VSS	274	DQ22_B
36	DQ20_A	180	VSS	82	CA6_B	226	VSS	131	DQ21_B	275	VSS
37	VSS	181	DQ22_A	83	VSS	227	PAR_B	132	VSS	276	DQ23_B
38	DQ21_A	182	VSS	84	CS0_B_n	228	VSS	133	DQ24_B	277	VSS
39	VSS	183	DQ23_A	85	VSS	229	CS1_B_n	134	VSS	278	DQ26_B
40	DQ24_A	184	VSS	86	LBD, RSP_A_n	230	VSS	135	DQ25_B	279	VSS
41	VSS	185	DQ26_A	87	LBS, RSP_B_n	231	RFU	136	VSS	280	DQ27_B
42	DQ25_A	186	VSS	88	VSS	232	RFU	137	DQS3_B_t	281	VSS
43	VSS	187	DQ27_A	89	CB4_B	233	VSS	138	DQS3_B_c	282	DQS8_B_c,TDQS8_B_c
44	DQS3_A_t	188	VSS	90	VSS	234	CB6_B	139	VSS	283	DQS8_B_t,TDQS8_B_t
45	DQS3_A_c	189	DQS8_A_c,TDQS8_A_c	91	CB5_B	235	VSS	140	DQ28_B	284	VSS
46	VSS	190	DQS8_A_t, TDQS8_A_t	92	VSS	236	CB7_B	141	VSS	285	DQ30_B
47	DQ28_A	191	VSS	93	DQS9_B_t, TDQS9_B_t	237	VSS	142	DQ29_B	286	VSS
48	VSS	192	DQ30_A	94	DQS9_B_c,TDQS9_B_c	238	DQS4_B_c	143	VSS	287	DQ31_B
49	DQ29_A	193	VSS	95	VSS	239	DQS4_B_t	144	RFU	288	VSS

Claim 1	Evidence of Use
	Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 6 (illustrating clock signal lines (e.g., “CK_t” and “CK_c”), control/address (C/A) signal lines (e.g., “CA[]_A,” “CA[]_B,” “CS[]_A_n,” and “CS[]_B_n”), and data signal lines (e.g., “DQ[]_A” and “DQ[]_B”)).

Front Side Pin Label	Pin	Pin	Back side Pin Label
VIN_BULK	1	145	VIN_BULK
RFU	2	146	VIN_BULK
VIN_MGMT	3	147	PWR_GOOD/FAIL_n
HSCL	4	148	HSA
HSDA	5	149	RFU
VSS	6	150	RFU
DQ0_A	7	151	VSS
VSS	8	152	DQ2_A
DQ1_A	9	153	VSS
VSS	10	154	DQ3_A
DQS0_A_t	11	155	VSS
DQS0_A_c	12	156	DQS5_A_c, TDQS5_A_c
VSS	13	157	DQS5_A_t, TDQS5_A_t DBI0_A_n
DQ4_A	14	158	VSS
VSS	15	159	DQ6_A
DQ5_A	16	160	VSS
VSS	17	161	DQ7_A
DQ8_A	18	162	VSS
VSS	19	163	DQ10_A
DQ9_A	20	164	VSS
VSS	21	165	DQ11_A
DQS1_A_t	22	166	VSS
DQS1_A_c	23	167	DQS6_A_c, TDQS6_A_c
VSS	24	168	DQS6_A_t, TDQS6_A_t DBI1_A_n
DQ12_A	25	169	VSS
VSS	26	170	DQ14_A
DQ13_A	27	171	VSS
VSS	28	172	DQ15_A
DQ16_A	29	173	VSS
VSS	30	174	DQ18_A
DQ17_A	31	175	VSS
VSS	32	176	DQ19_A
DQS2_A_t	33	177	VSS
DQS2_A_c	34	178	DQS7_A_c, TDQS7_A_c
VSS	35	179	DQS7_A_t, TDQS7_A_t DBI2_n
DQ20_A	36	180	VSS
VSS	37	181	DQ22_A
DQ21_A	38	182	VSS

Front Side Pin Label	Pin	Pin	Back side Pin Label
PAR_A	74	218	CK_c
V33	75	219	V33
	Key		
CA0_B	76	220	RFU
VSS	77	221	CA1_B
CA2_B	78	222	VSS
VSS	79	223	CA3_B
CA4_B	80	224	VSS
VSS	81	225	CA5_B
CA6_B	82	226	VSS
VSS	83	227	PAR_B
CS0_B_n	84	228	VSS
VSS	85	229	CS1_B_n
LBD, RSP_A_n	86	230	VSS
LBS, RSP_B_n	87	231	RFU
VSS	88	232	RFU
CB4_B	89	233	VSS
VSS	90	234	CB6_B
CB5_B	91	235	VSS
VSS	92	236	CB7_B
DQS9_B_t, TDQS9_B_t DBI4_B_n	93	237	VSS
DQS9_B_c, TDQS9_B_c	94	238	DQS4_B_c
VSS	95	239	DQS4_B_t
CB0_B	96	240	VSS
V33	97	241	CB2_B
CB1_B	98	242	VSS
VSS	99	243	CB3_B
DQ0_B	100	244	VSS
VSS	101	245	DQ2_B
DQ1_B	102	246	VSS
VSS	103	247	DQ3_BDQ3_B
DQS0_B_t	104	248	VSS
DQS0_B_c	105	249	DQS5_B_c, TDQS5_B_c
VSS	106	250	DQS5_B_t, TDQS5_B_t DBI0_B_n
DQ4_B	107	251	VSS
VSS	108	252	DQ6_B
DQ5_B	109	253	VSS

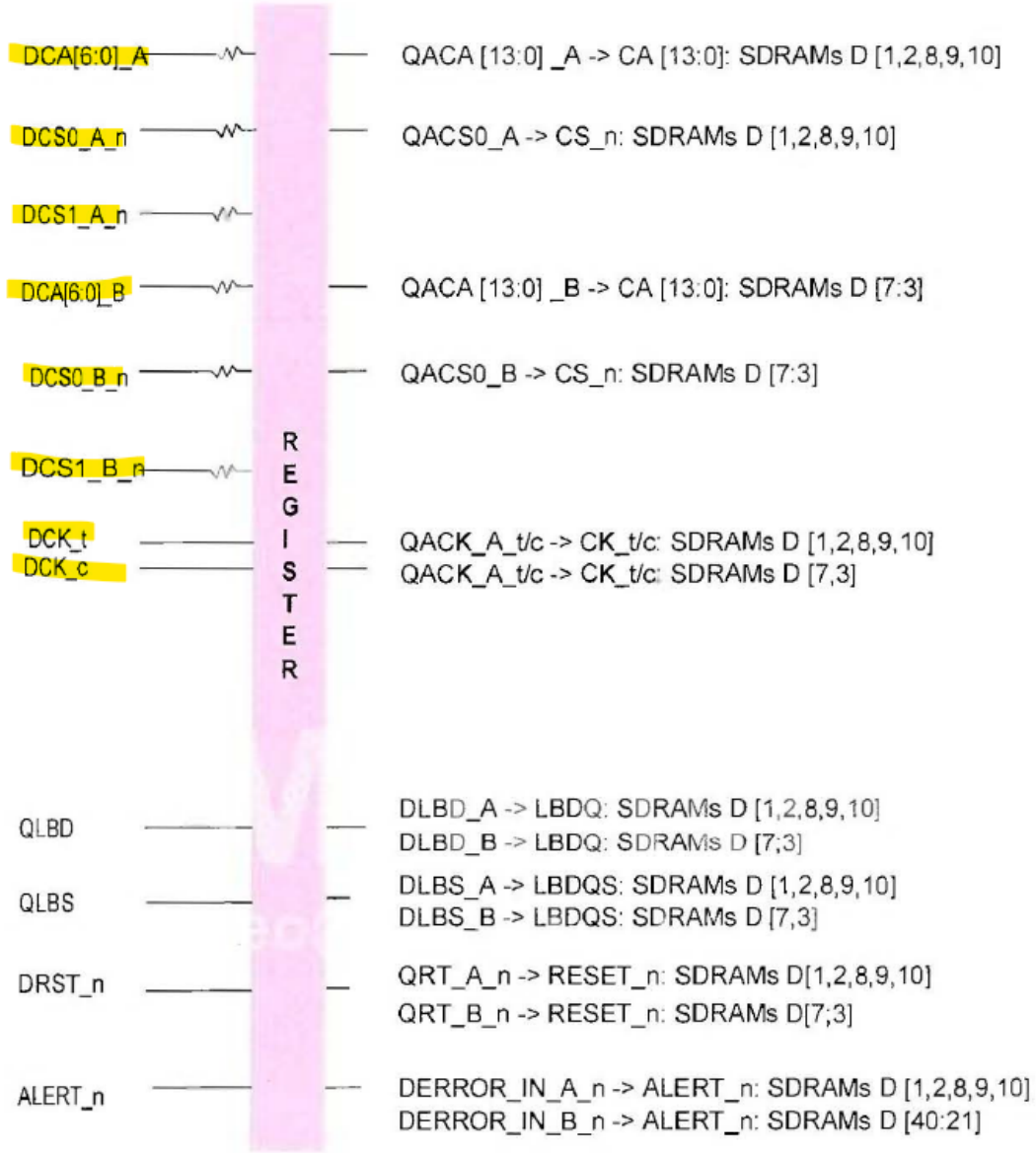
Claim 1	Evidence of Use

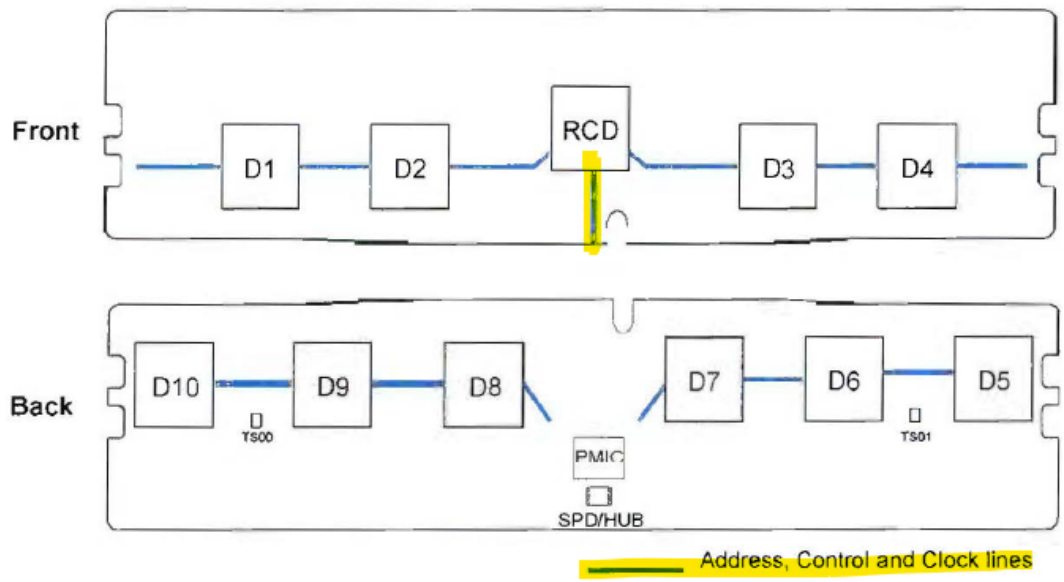
Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	39	183	DQ23_A
DQ24_A	40	184	V33
VSS	41	185	DQ26_A
DQ25_A	42	186	VSS
VSS	43	187	DQ27_A
DQS3_A_t	44	188	VSS
DQS3_A_c	45	189	DQS8_A_c, TDQS8_A_c
VSS	46	190	DQS8_A_t, TDQS8_A_t DBI3_A_n
DQ28_A	47	191	VSS
VSS	48	192	DQ30_A
DQ29_A	49	193	VSS
VSS	50	194	DQ31_A
CB0_A	51	195	VSS
VSS	52	196	CB2_A
CB1_A	53	197	VSS
VSS	54	198	CB3_A
DQS4_A_t	55	199	VSS
DQS4_A_c	56	200	DQS9_A_c, TDQS9_A_c
VSS	57	201	DQS9_A_t, TDQS9_A_t DBI4_A_n
CB4_A	58	202	VSS
VSS	59	203	CB6_A
CB5_A	60	204	VSS
VSS	61	205	CB7_A
ALERT_n	62	206	VSS
VSS	63	207	RESET_n
CS0_A_n	64	208	VSS
VSS	65	209	CS1_A_n
CA0_A	66	210	VSS
VSS	67	211	CA1_A
CA2	68	212	VSS
VSS	69	213	CA3_A
CA4_A	70	214	VSS
VSS	71	215	CA5_A
CA6_A	72	216	VSS
VSS	73	217	CK_t

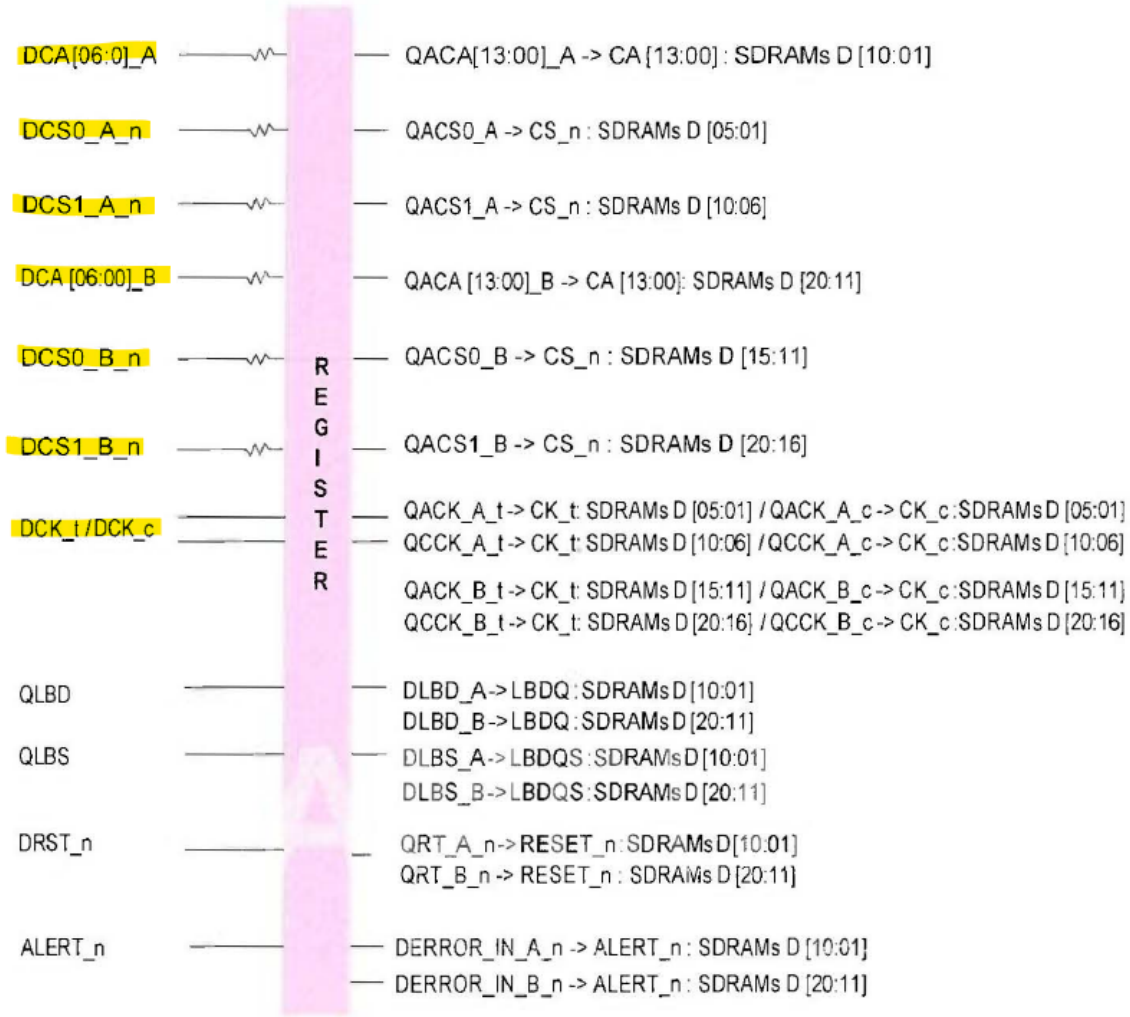
Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	110	254	DQ7_B
DQ8_B	111	255	VSS
VSS	112	256	DQ10_B
DQ9_B	113	257	VSS
VSS	114	258	DQ11_B
DQS1_B_t	115	259	VSS
DQS1_B_c	116	260	DQS6_B_c, TDQS6_B_c
VSS	117	261	DQS6_B_t, TDQS6_B_t DBI1_B_n
DQ12_B	118	262	VSS
VSS	119	263	DQ14_B
DQ13_B	120	264	VSS
VSS	121	265	DQ15_B
DQ16_B	122	266	VSS
VSS	123	267	DQ18_B
DQ17_B	124	268	VSS
VSS	125	269	DQ19_B
DQS2_B_t	126	270	V33
DQS2_B_c	127	271	DQS7_B_c, TDQS7_B_c
VSS	128	272	DQS7_B_t, TDQS7_B_t DBI2_B_n
DQ20_B	129	273	VSS
VSS	130	274	DQ22_B
DQ21_B	131	275	VSS
VSS	132	276	DQ23_B
DQ24_B	133	277	VSS
VSS	134	278	DQ26_B
DQ25_B	135	279	VSS
VSS	136	280	DQ27_B
DQS3_B_t	137	281	VSS
DQS3_B_c	138	282	DQS8_B_c, TDQS8_B_c
VSS	139	283	DQS8_B_t, TDQS8_B_t DBI3_B_n
DQ28_B	140	284	VSS
VSS	141	285	DQ30_B
DQ29_B	142	286	VSS
VSS	143	287	DQ31_B
RFU	144	288	VSS

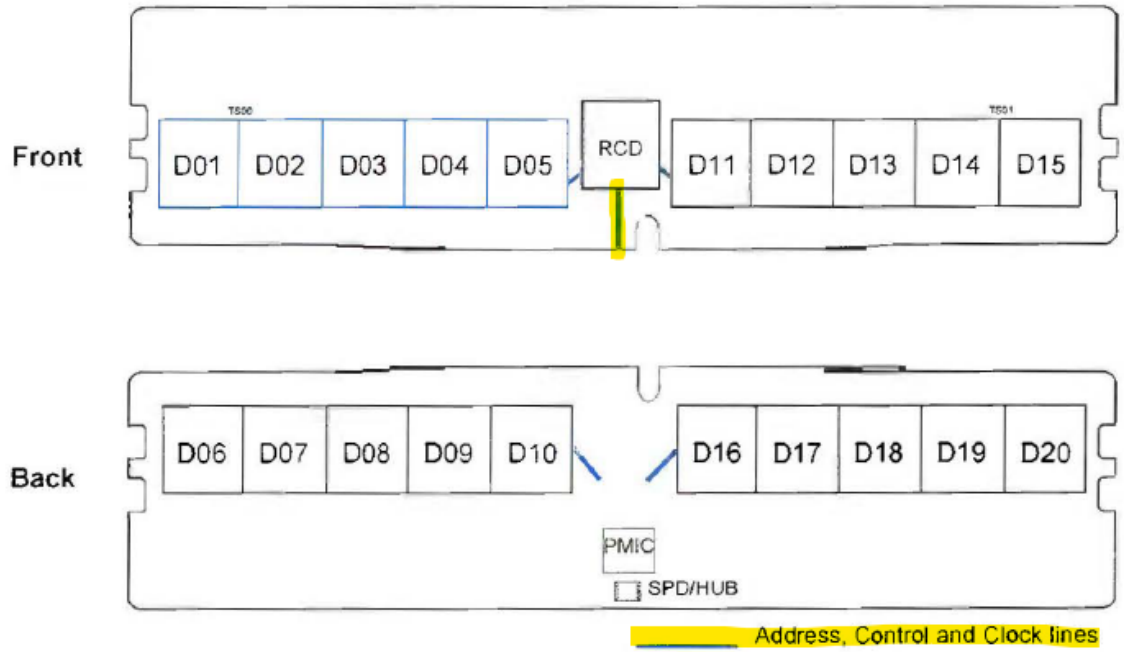
Figure 1. Wiring Assignments

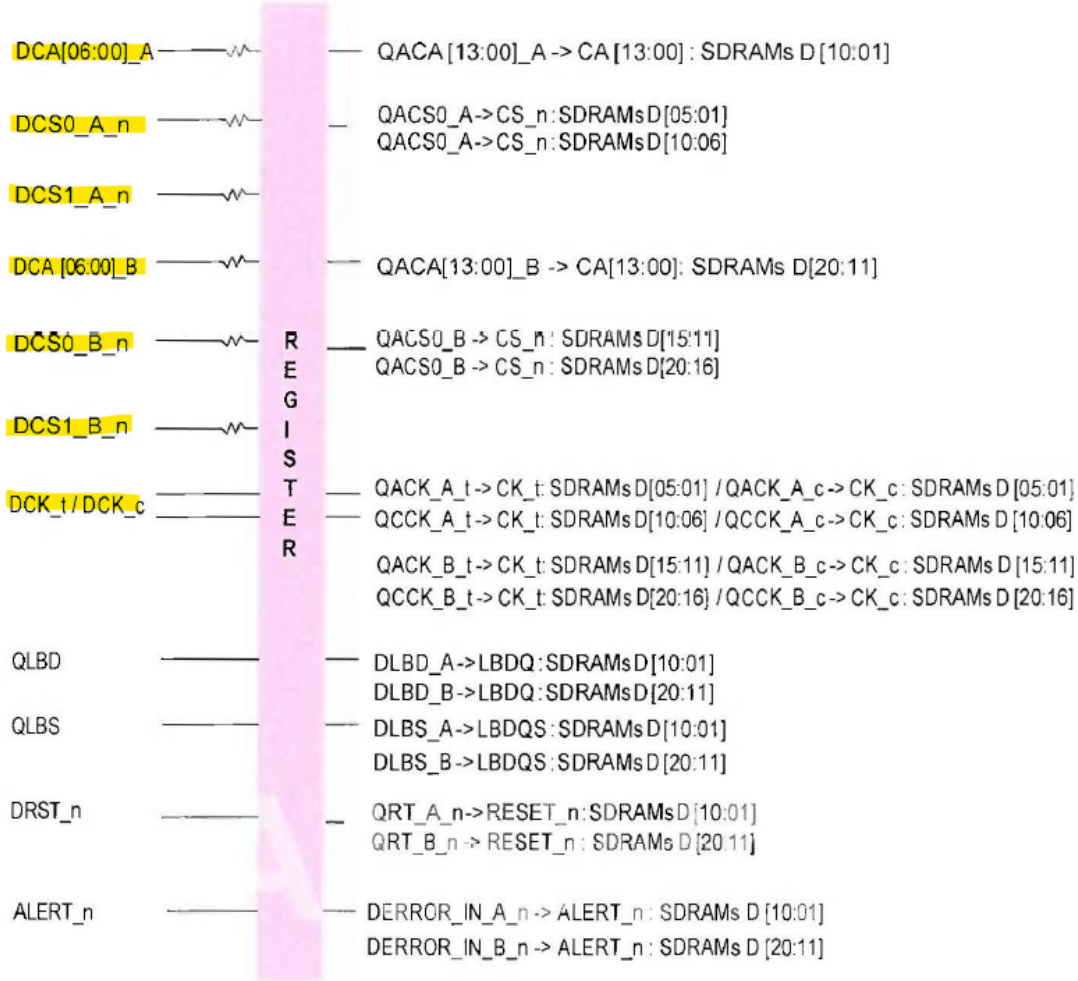
Claim 1	Evidence of Use
	Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 7-8 (illustrating clock signal lines (e.g., “CK_t” and “CK_c”), control/address (C/A) signal lines (e.g., “CA[]_A,” “CA[]_B,” “CS[]_A_n,” and “CS[]_B_n”), and data signal lines (e.g., “DQ[]_A” and “DQ[]_B”)).

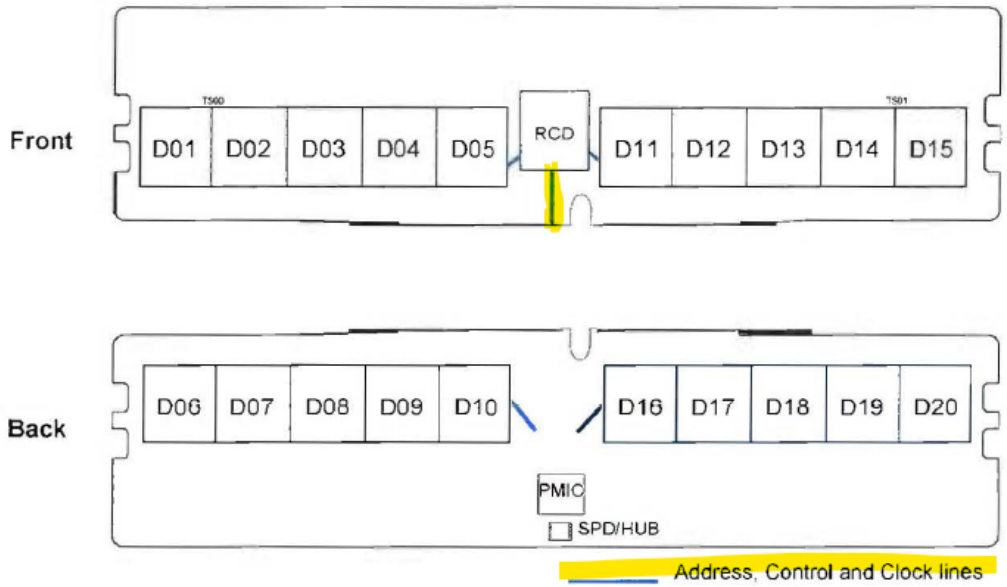

DCA[6:0]_A
DCS0_A_n
DCS1_A_n
DCA[6:0]_B
DCS0_B_n
DCS1_B_n
DCK_t
DCK_c
QLBD
QLBS
DRST_n
ALERT_n
REGISTER
QACA [13:0] _A -> CA [13:0]: SDRAMs D [1,2,8,9,10]
QACS0_A -> CS_n: SDRAMs D [1,2,8,9,10]
QACA [13:0] _B -> CA [13:0]: SDRAMs D [7:3]
QACS0_B -> CS_n: SDRAMs D [7:3]
QACK_A_t/c -> CK_t/c: SDRAMs D [1,2,8,9,10]
QACK_A_t/c -> CK_t/c: SDRAMs D [7,3]
DLBD_A -> LBDQ: SDRAMs D [1,2,8,9,10]
DLBD_B -> LBDQ: SDRAMs D [7;3]
DLBS_A -> LBDQS: SDRAMs D [1,2,8,9,10]
DLBS_B -> LBDQS: SDRAMs D [7,3]
QRT_A_n -> RESET_n: SDRAMs D[1,2,8,9,10]
QRT_B_n -> RESET_n: SDRAMs D[7;3]
DERROR_IN_A_n -> ALERT_n: SDRAMs D [1,2,8,9,10]
DERROR_IN_B_n -> ALERT_n: SDRAMs D [40:21]

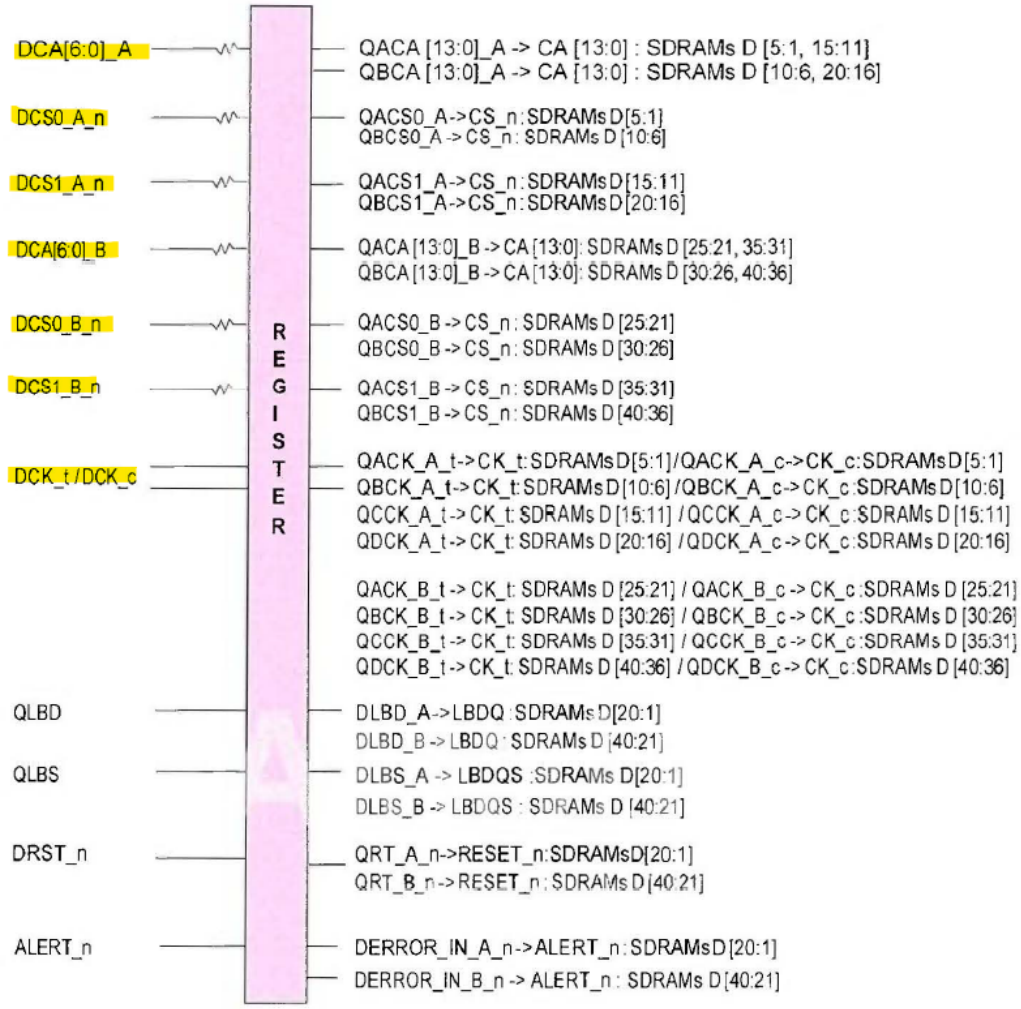
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 21.

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 25.

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 29.

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 33. As explained *supra*, the Samsung Practicing ’407 Products are JEDEC compliant, including the use of a JEDEC compliant 288-pin edge connector used to connect to the system bus. The JEDEC DDR5 RDIMM standard connector pinout and signal description further indicates the system bus of the computer system includes one or more clock signal lines, control/address (C/A) signal lines, and data signal lines. *See, e.g.,*

Claim 1	Evidence of Use
	Table 3 — Pin Definitions Ex. CC-88 (JEDEC 305B) at 3 (illustrating clock signal lines (*e.g.,* "CK_t" and "CK_c"), control/address (C/A) signal lines (*e.g.,* "CA[]_A," "CA[]_B," "CS[]_A_n," and "CS[]_B_n"), and data signal lines (*e.g.,* "DQ[]_A" and "DQ[]_B")). **Table 4 — Input/Output Functional Description** Ex. CC-88 (JEDEC 305B) at 4 (illustrating clock signal lines (*e.g.,* "CK_t" and "CK_c") and control/address (C/A) signal lines (*e.g.,* "CA[]_A" and "CA[]_B")).

Table 3 — Pin Definitions

Pin Name	Description	Pin Name	Description
CA[6:0]_A CA[6:0]_B	Command and Address (CA) Bus	DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A and B
CS[1:0]_A_n CS[1:0]_B_n	Control (Chip Select) (CS_n)	CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A and B
PAR_A PAR_B	Parity input	DQS[9:0]_A_t DQS[9:0]_B_t	Data Strobes (positive line of differential pair)
CK_t	Clock (true/positive)	DQS[9:0]_A_c DQS[9:0]_B_c	Data Strobes (negative line of differential pair)
CK_c	Clock (complement/negative)	TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.

Table 4 — Input/Output Functional Description

Symbol	Type	I/O Levels	Function
CK_t, CK_c,	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All CA and CS_n input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[6:0]_A CA[6:0]_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during Mode Register Set commands.

Claim 1	Evidence of Use

DQ[31:0]_A DQ[31:0]_B	Input/ Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	Input/ Output	VDD	ECC Checkbits Input/ Output: Bi-directional data bus - for 8-bit ECC (EC8) all 8 bits are used - for 4-bit ECC (EC4) [3:0] bits are used; [7:4] bits are floating

Ex. CC-88 (JEDEC 305B) at 4 (illustrating data signal lines (*e.g.,* "DQ[]_A" and "DQ[]_B")).

Table 4 — Input/Output Functional Description (cont'd)

Symbol	Type	I/O Levels	Function
DQS[9:0]_A_t DQS[9:0]_B_t DQS[9:0]_A_c DQS[9:0]_B_c	Input/ Output	VDD	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The Data Strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential Data Strobe only and does not support single-ended.
TDQS[9:5]_A_t TDQS[9:5]_B_t	Input	VDD	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs.
TDQS[9:5]_A_c TDQS[9:5]_B_c	Input	VDD	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs.

Ex. CC-88 (JEDEC 305B) at 5.

Claim 1	Evidence of Use

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
VIN_BULK	1	145	VIN_BULK	PAR_A	74	218	CK_c
RFU	2	146	VIN_BULK	VSS	75	219	VSS
VIN_MGMT	3	147	PCAMP		Key		
HSCL	4	148	HSA				
HSDA	5	149	RFU	CA0_B	76	220	RFU / No Pin Present
VSS	6	150	RFU	VSS	77	221	CA1_B
DQ0_A	7	151	VSS	CA2_B	78	222	VSS
VSS	8	152	DQ2_A	VSS	79	223	CA3_B
DQ1_A	9	153	VSS	CA4_B	80	224	VSS
VSS	10	154	DQ3_A	VSS	81	225	CA5_B
DQS0_A_t	11	155	VSS	CA6_B	82	226	VSS
DQS0_A_c	12	156	DQS5_A_c, TDQS5_A_c	VSS	83	227	PAR_B
VSS	13	157	DQS5_A_t, TDQS5_A_t	CS0_B_n	84	228	VSS
DQ4_A	14	158	VSS	VSS	85	229	CS1_B_n
VSS	15	159	DQ6_A	DLBDQ	86	230	VSS
DQ5_A	16	160	VSS	DLBDQS	87	231	RFU
VSS	17	161	DQ7_A	VSS	88	232	RFU
DQ8_A	18	162	VSS	CB4_B	89	233	VSS
VSS	19	163	DQ10_A	VSS	90	234	CB6_B
DQ9_A	20	164	VSS	CB5_B	91	235	VSS
VSS	21	165	DQ11_A	VSS	92	236	CB7_B
DQS1_A_t	22	166	VSS	DQS9_B_t, TDQS9_B_t	93	237	VSS
DQS1_A_c	23	167	DQS6_A_c, TDQS6_A_c	DQS9_B_c, TDQS9_B_c	94	238	DQS4_B_c
VSS	24	168	DQS6_A_t, TDQS6_A_t	VSS	95	239	DQS4_B_t
DQ12_A	25	169	VSS	CB0_B	96	240	VSS
VSS	26	170	DQ14_A	VSS	97	241	CB2_B
DQ13_A	27	171	VSS	CB1_B	98	242	VSS
VSS	28	172	DQ15_A	VSS	99	243	CB3_B
DQ16_A	29	173	VSS	DQ0_B	100	244	VSS
VSS	30	174	DQ18_A	VSS	101	245	DQ2_B
DQ17_A	31	175	VSS	DQ1_B	102	246	VSS
VSS	32	176	DQ19_A	VSS	103	247	DQ3_B
DQS2_A_t	33	177	VSS	DQS0_B_t	104	248	VSS
DQS2_A_c	34	178	DQS7_A_c, TDQS7_A_c	DQS0_B_c	105	249	DQS5_B_c, TDQS5_B_c
VSS	35	179	DQS7_A_t, TDQS7_A_t	VSS	106	250	DQS5_B_t, TDQS5_B_t
DQ20_A	36	180	VSS	DQ4_B	107	251	VSS
VSS	37	181	DQ22_A	VSS	108	252	DQ6_B
DQ21_A	38	182	VSS	DQ5_B	109	253	VSS

Cravath & Wa

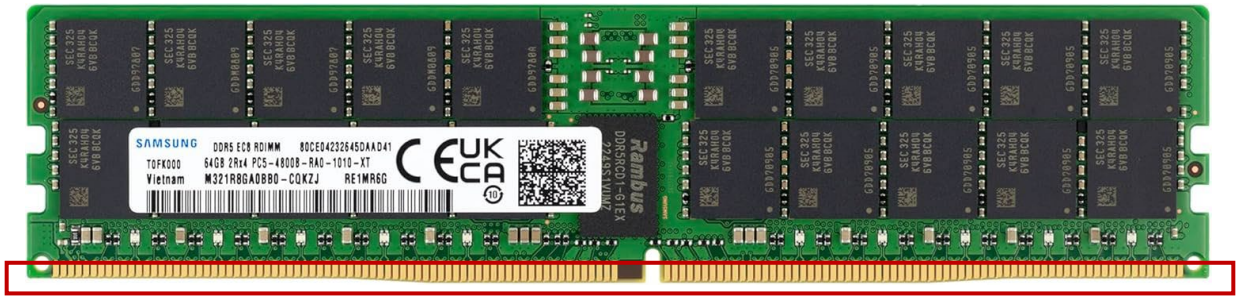
Claim 1	Evidence of Use
	Ex. CC-88 (JEDEC 305B) at 6 (illustrating clock signal lines (*e.g.,* "CK_t" and "CK_c"), control/address (C/A) signal lines (*e.g.,* "CA[]_A," "CA[]_B," "CS[]_A_n," and "CS[]_B_n"), and data signal lines (*e.g.,* "DQ[]_A" and "DQ[]_B")).

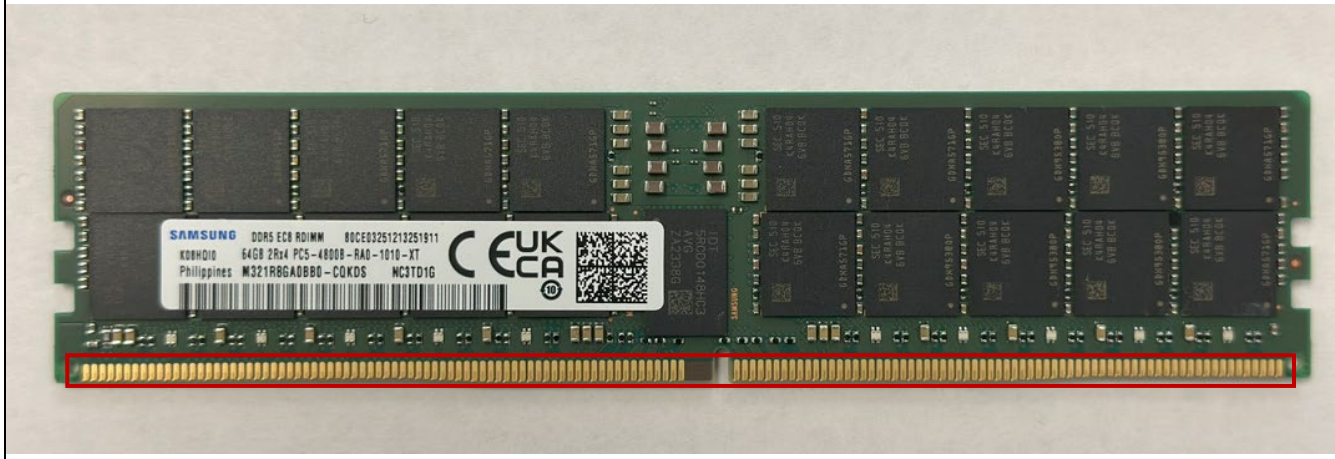
Claim 1	Evidence of Use

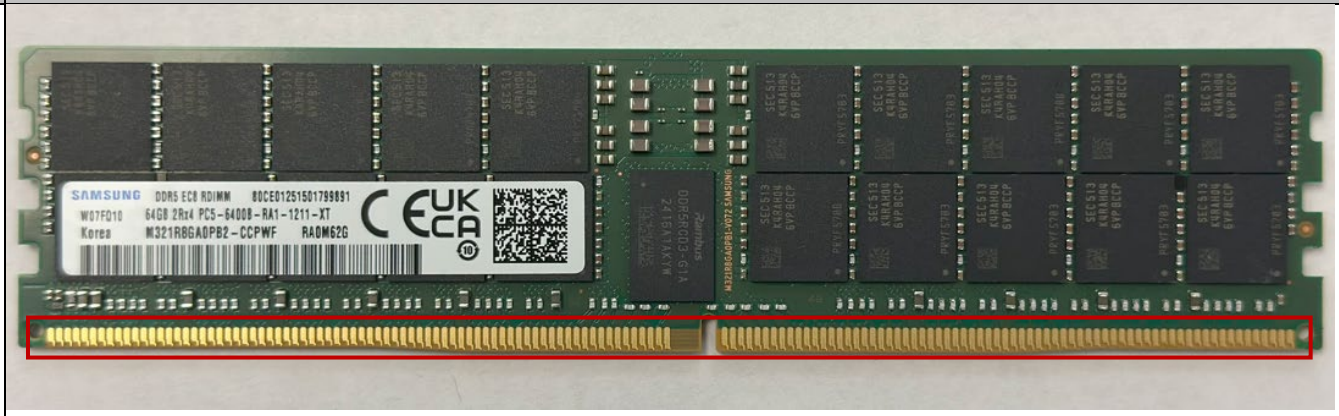
Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	39	183	DQ23_A	VSS	110	254	DQ7_B
DQ24_A	40	184	VSS	DQ8_B	111	255	VSS
VSS	41	185	DQ26_A	VSS	112	256	DQ10_B
DQ25_A	42	186	VSS	DQ9_B	113	257	VSS
VSS	43	187	DQ27_A	VSS	114	258	DQ11_B
DQS3_A_t	44	188	VSS	DQS1_B_t	115	259	VSS
DQS3_A_c	45	189	DQS8_A_c, TDQS8_A_c	DQS1_B_c	116	260	DQS6_B_c, TDQS6_B_c
VSS	46	190	DQS8_A_t, TDQS8_A_t	VSS	117	261	DQS6_B_t, TDQS6_B_t
DQ28_A	47	191	VSS	DQ12_B	118	262	VSS
VSS	48	192	DQ30_A	VSS	119	263	DQ14_B
DQ29_A	49	193	VSS	DQ13_B	120	264	VSS
VSS	50	194	DQ31_A	VSS	121	265	DQ15_B
CB0_A	51	195	VSS	DQ16_B	122	266	VSS
VSS	52	196	CB2_A	VSS	123	267	DQ18_B
CB1_A	53	197	VSS	DQ17_B	124	268	VSS
VSS	54	198	CB3_A	VSS	125	269	DQ19_B
DQS4_A_t	55	199	VSS	DQS2_B_t	126	270	VSS
DQS4_A_c	56	200	DQS9_A_c, TDQS9_A_c	DQS2_B_c	127	271	DQS7_B_c, TDQS7_B_c
VSS	57	201	DQS9_A_t, TDQS9_A_t	VSS	128	272	DQS7_B_t, TDQS7_B_t
CB4_A	58	202	VSS	DQ20_B	129	273	VSS
VSS	59	203	CB6_A	VSS	130	274	DQ22_B
CB5_A	60	204	VSS	DQ21_B	131	275	VSS
VSS	61	205	CB7_A	VSS	132	276	DQ23_B
ALERT_n	62	206	VSS	DQ24_B	133	277	VSS
VSS	63	207	RESET_n	VSS	134	278	DQ26_B
CS0_A_n	64	208	VSS	DQ25_B	135	279	VSS
VSS	65	209	CS1_A_n	VSS	136	280	DQ27_B
CA0_A	66	210	VSS	DQS3_B_t	137	281	VSS
VSS	67	211	CA1_A	DQS3_B_c	138	282	DQS8_B_c, TDQS8_B_c
CA2_A	68	212	VSS	VSS	139	283	DQS8_B_t, TDQS8_B_t
VSS	69	213	CA3_A	DQ28_B	140	284	VSS
CA4_A	70	214	VSS	VSS	141	285	DQ30_B
VSS	71	215	CA5_A	DQ29_B	142	286	VSS
CA6_A	72	216	VSS	VSS	143	287	DQ31_B
VSS	73	217	CK_t	RFU	144	288	VSS

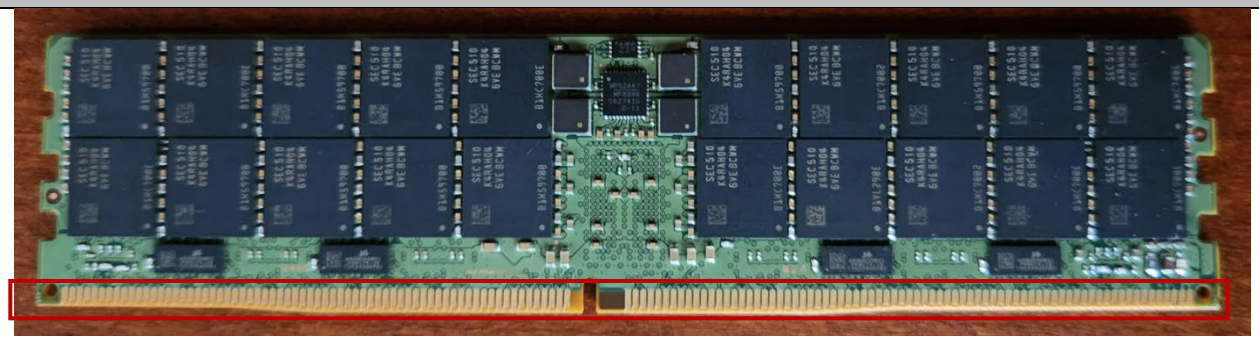
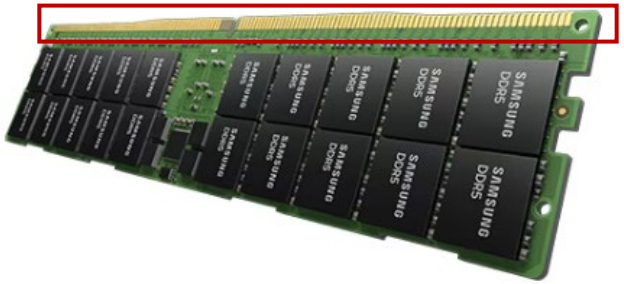
NOTE 1 Individual Annex standards for RDIMM define pin use where multiple functions are possible.
NOTE 2 Pin 220 for 8000 Mbps and faster RDIMM raw cards do not have the edge pin present.

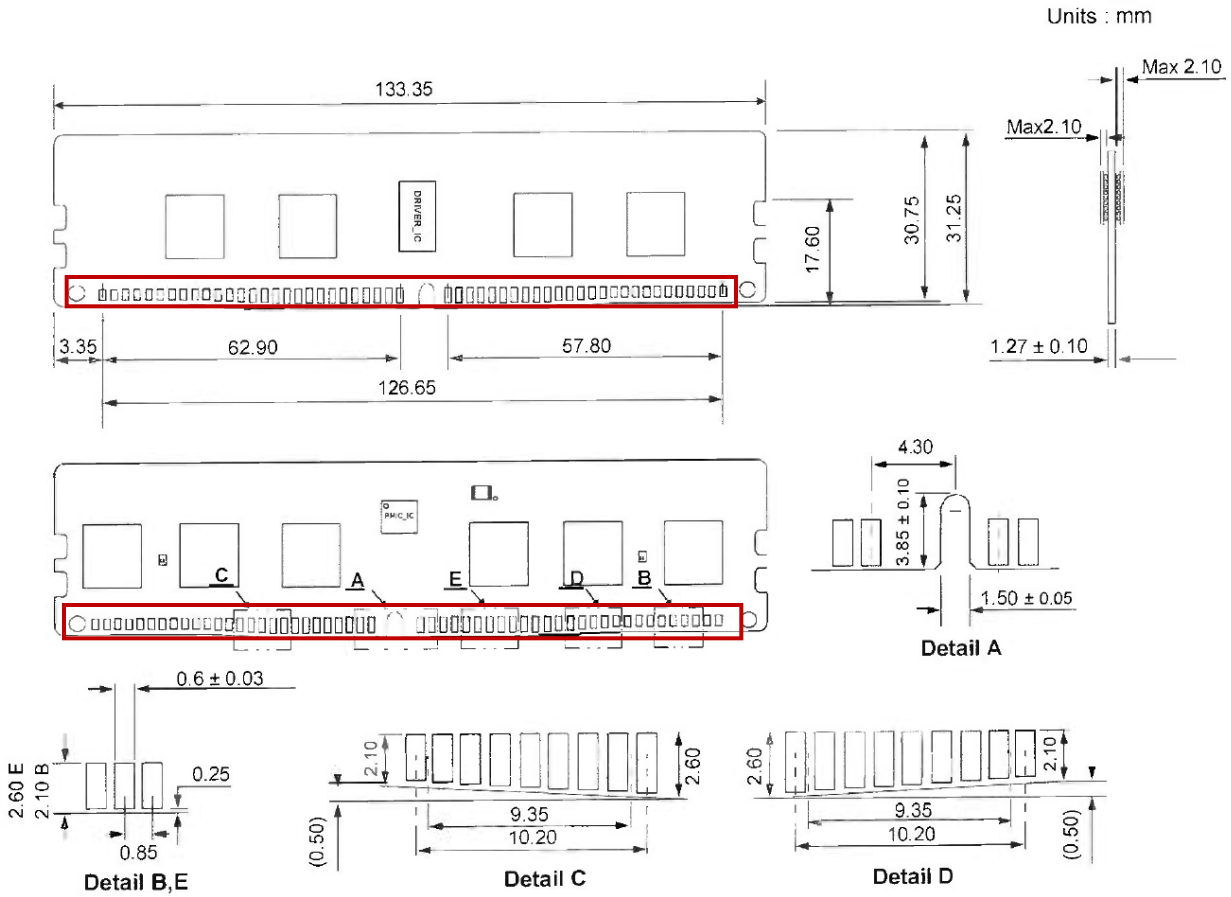
Williams & Wat

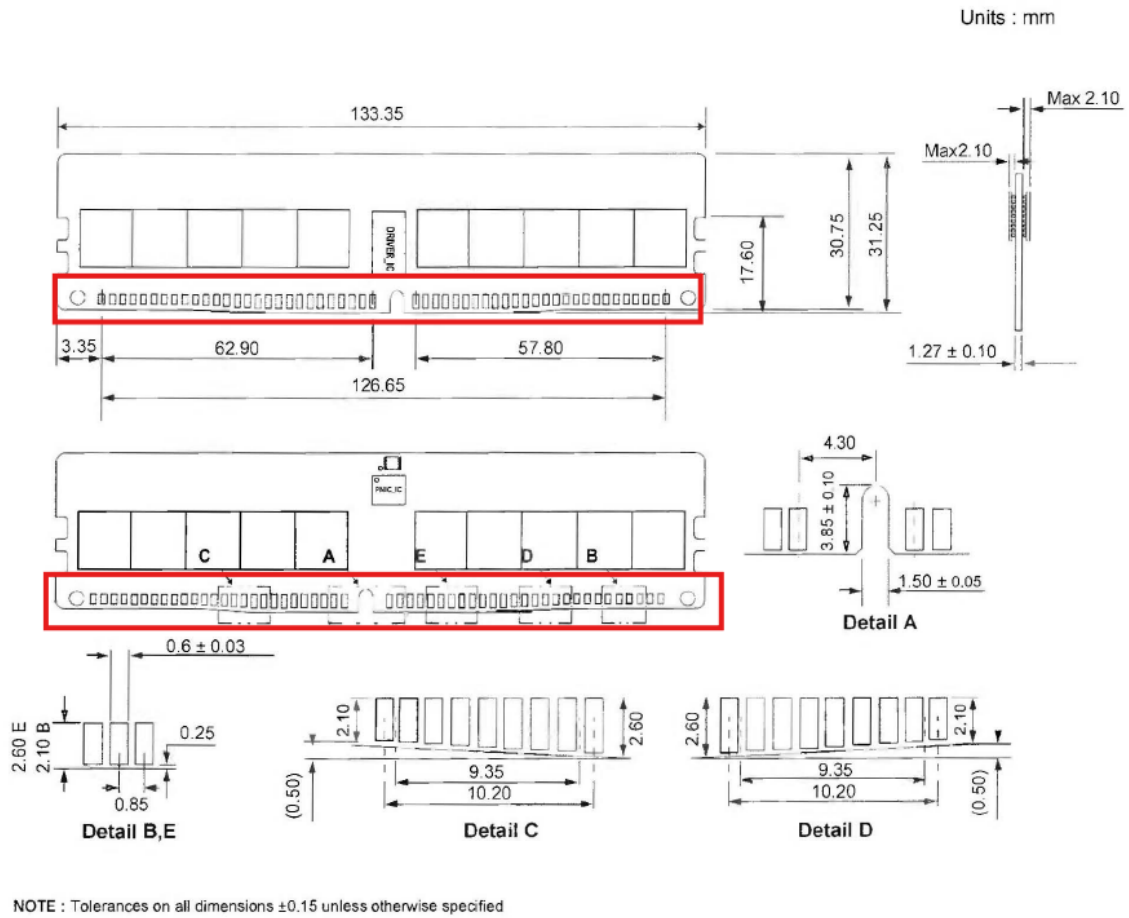
Claim 1	Evidence of Use
	Ex. CC-88 (JEDEC 305B) at 7 (illustrating clock signal lines (*e.g.,* "CK_t" and "CK_c"), control/address (C/A) signal lines (*e.g.,* "CA[]_A," "CA[]_B," "CS[]_A_n," and "CS[]_B_n"), and data signal lines (*e.g.,* "DQ[]_A" and "DQ[]_B")). These are the pins to be inserted and mated with the corresponding pins in the memory slot, thus indicating that the system bus includes one or more clock signal lines, control/address (C/A) signal lines and data signal lines.
[**1.a**] a printed circuit board (PCB) having connectors configured to provide electrical connections between the memory module and the system bus;	The Samsung Practicing '407 Products each comprise a printed circuit board (PCB) having connectors configured to provide electrical connections between the memory module and the system bus. For example, as shown in the below images, each Samsung RDIMM has a green printed circuit board, at the bottom of which there are two rows of gold fingers (connectors, annotated in red boxes):  Ex. ITC-1472 CC-116 (Samsung 4800MHz PC5-38400).

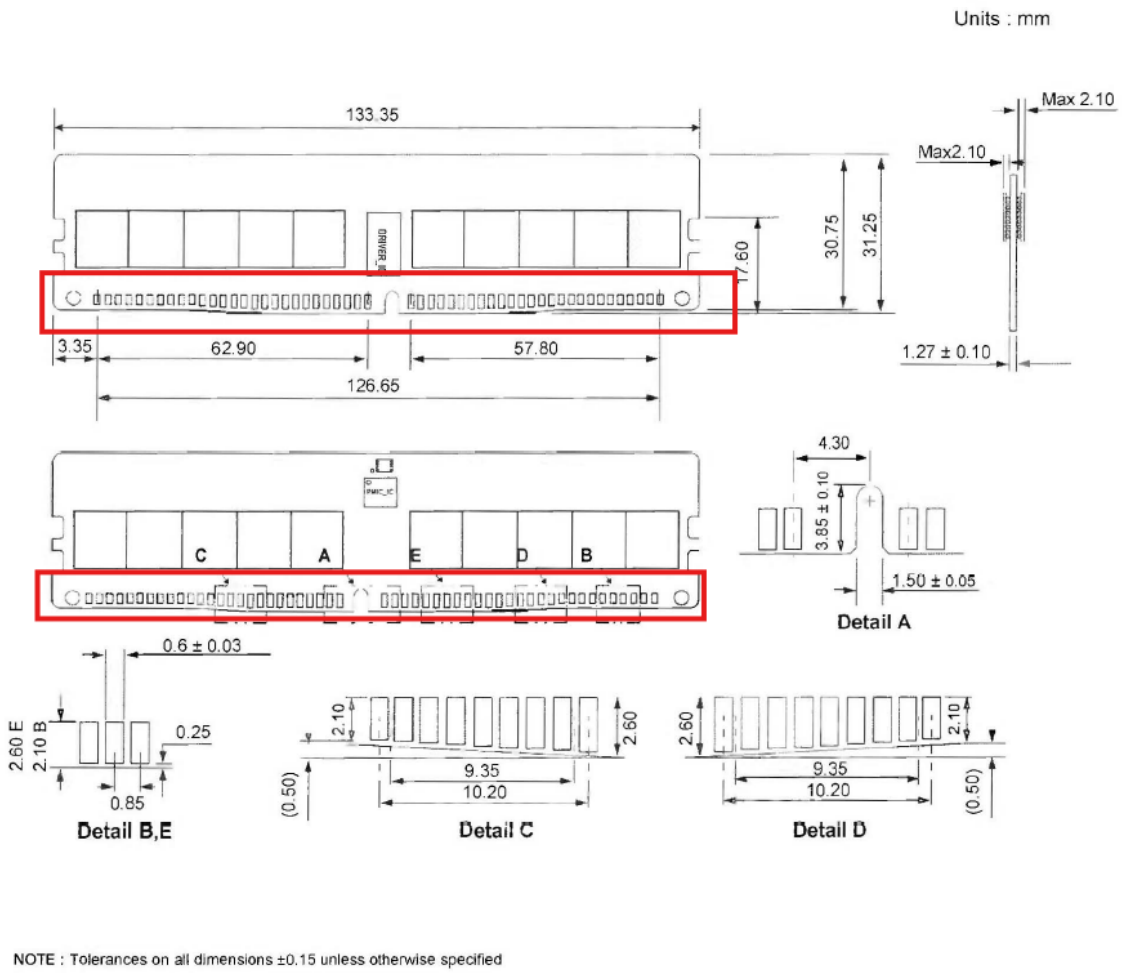
Claim 1	Evidence of Use
	 Ex. ITC-1472 CC-117 (Samsung 5600MHz PC5-44800).  Ex. CC-118 (Samsung 64GB DDR5 PC5-4800 EC8 RDIMM 2Rx4 M321R8GA0BB0-CQK).

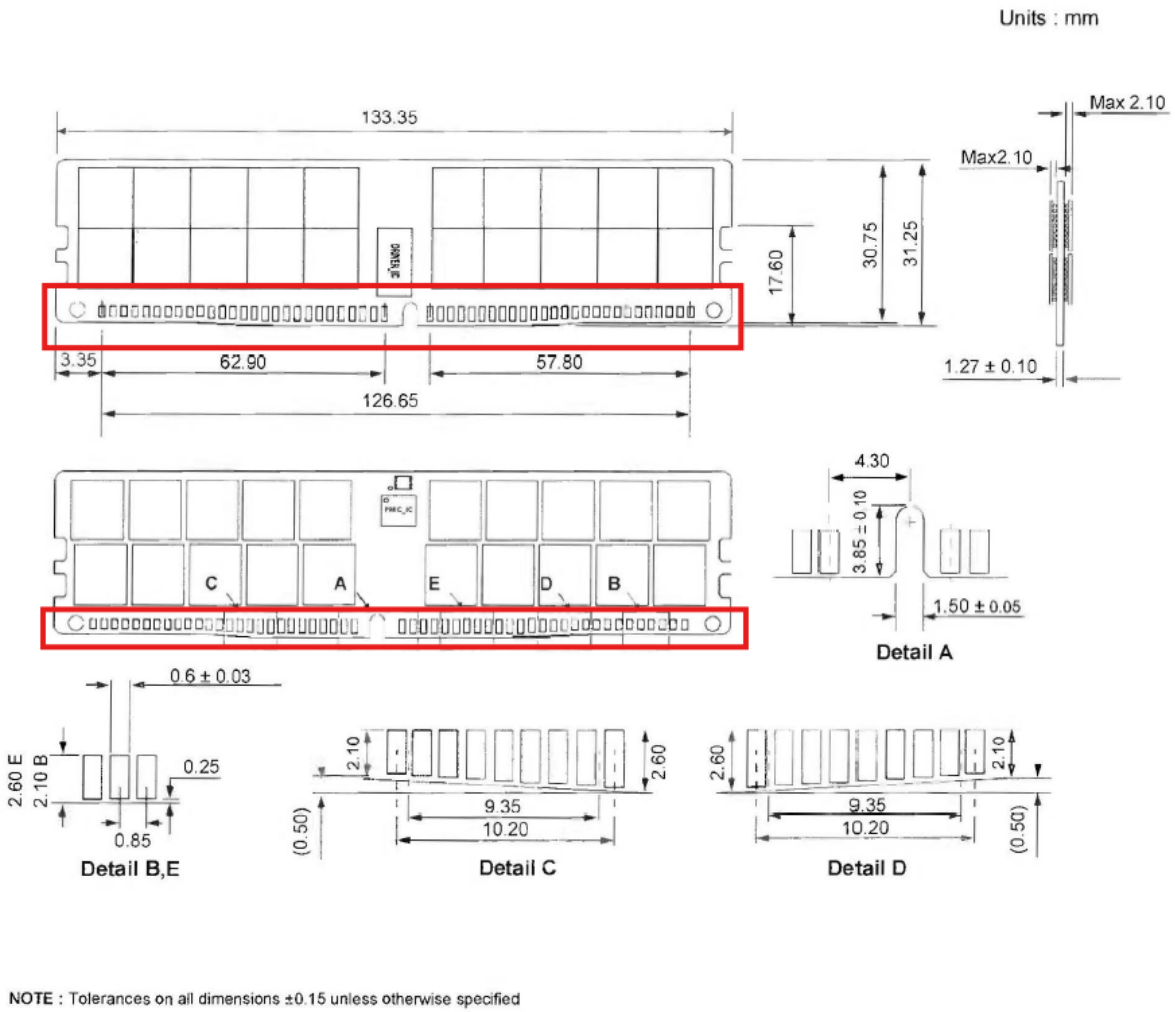
Claim 1	Evidence of Use
	 Ex. CC-119 (Samsung 64GB DDR5 PC5-6400 EC8 RDIMM 2Rx4 M321R8GA0PB2-CCP).

Claim 1	Evidence of Use
	 An image of a Samsung MRDIMM M327R8GA0EB0-CLVXB. *See* Exs. CC-111, CC-112. **RDIMM** **Registered DIMM** Include a register for enhancing the clock, command and control signals Error correction is available by adding 8-bit parity signals Supports x4 / x8 Organization / up to 2 ranks per DIMM and 3DPC configuration Application : Server  Ex. CC-95 (Samsung DDR DIMMs)

Claim 1	Evidence of Use
	19.0 PHYSICAL DIMENSIONS **19.1 2Gx8 based x80 Module (1 Rank) - M321R2GA3BB0**  Ex. CC-89 at 93

Claim 1	Evidence of Use
	19.2 2Gx8 based x80 Module (2 Ranks) - M321R4GA3BB0  Ex. CC-89 at 94

Claim 1	Evidence of Use
	19.3 4Gx4 based x80 Module (1 Rank) - M321R4GA0BB0  Ex. CC-89 at 95.

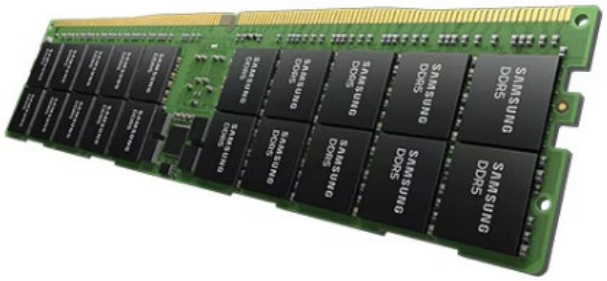
Claim 1	Evidence of Use
	19.4 4Gx4 based x80 Module (2 Ranks) - M321R8GA0BB0  Ex. CC-89 at 96.

Claim 1	Evidence of Use
	Furthermore, the connectors are configured to provide electrical connections between the memory module and the system bus. For example, the connectors in the Samsung Practicing ’407 Products are assigned to pin assignments for connecting with lines in the system bus, including clock signal lines, control/address (C/A) signal lines and data signal lines. *See, e.g.,*

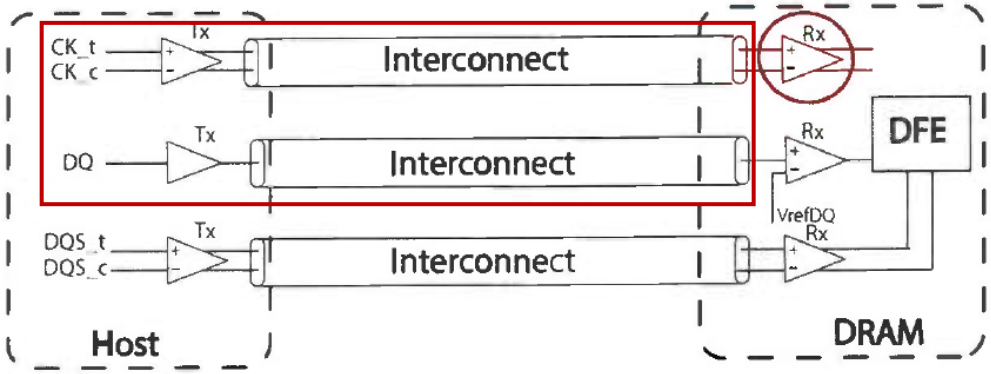
RDIMM

Registered DIMM

Include a register for enhancing the clock, command and control signals
Error correction is available by adding 8-bit parity signals
Supports x4 / x8 Organization / up to 2 ranks per DIMM and 3DPC configuration
Application : Server



Ex. CC-95 (Samsung DDR DIMMs)

Claim 1	Evidence of Use
	 Figure 10. Example of DDR5 Memory Interconnect (Ex. CC-89 at 42, Fig. 10).

Claim 1	Evidence of Use

[Table 5] PIN Description

Pin Name	Description
CA[6:0]_A CA[6:0]_B	SDRAM Address and Command Bus
CS[1:0]_A CS[1:0]_B	SDRAM Chip Select
PAR_A PAR_B	SDRAM Parity input
CK_t	SDRAM Clocks (true/positive)
CK_c	SDRAM Clocks (complement/negative)
ALERT_n	SDRAM alert for CRC error
RESET_n	Set DRAM to known state
PCAMP	Control and Monitor Port
HSCL	I2C/I3C-Basic Host Sideband Bus Clock
HSDA	I2C/I3C-Basic Host Sideband Bus Data
HSA	I2C/I3C-Basic Host Sideband Bus Address
LBDQ	Loopback data output:

Pin Name	Description
DQ[31:0]_A DQ[31:0]_B	DIMM memory data bus channel A and B
CB[7:0]_A CB[7:0]_B	DIMM ECC check bits(CB) channel A and B
DQS[9:0]_A_t DQS[9:0]_B_t	SDRAM data strobes (positive line of differential pair)
DQS[9:0]_A_c DQS[9:0]_B_c	SDRAM data strobes (negative line of differential pair)
TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
VIN_BULK	DIMM Power Supply from system to PMIC
VIN_MGMT	DIMM Power Supply from system to PMIC
VSS	Power supply return (ground)
RFU	Reserved for future use
LBDQS	Loopback data strobe output

Ex. CC-89 at 9.

[Table 4] PIN Configuration

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VIN_BULK	145	VIN_BULK	50	VSS	194	DQ31_A	96	CB0_B	240	VSS
2	RFU	146	VIN_BULK	51	CB0_A	195	VSS	97	VSS	241	CB2_B
3	VIN_MGMT	147	PWR_GOOD/FAIL_n	52	VSS	196	CB2_A	98	CB1_B	242	VSS
4	SCL	148	SAA	53	CB1_A	197	VSS	99	VSS	243	CB3_B
5	SDA	149	RFU	54	VSS	198	CB3_A	100	DQ0_B	244	VSS
6	VSS	150	RFU	55	DQS4_A_t	199	VSS	101	VSS	245	DQ2_B
7	DQ0_A	151	VSS	56	DQS4_A_c	200	DQS9_A_c,TDQS9_A_c	102	DQ1_B	246	VSS
8	VSS	152	DQ2_A	57	VSS	201	DQS9_A_t,TDQS9_A_t	103	VSS	247	DQ3_B
9	DQ1_A	153	VSS	58	CB4_A	202	VSS	104	DQS0_B_t	248	VSS
10	VSS	154	DQ3_A	59	VSS	203	CB6_A	105	DQS0_B_c	249	DQS5_B_c,TDQS5_B_c
11	DQS0_A_t	155	VSS	60	CB5_A	204	VSS	106	VSS	250	DQS5_B_t,TDQS5_B_t
12	DQS0_A_c	156	DQS5_A_c, TDQS5_A_c	61	VSS	205	CB7_A	107	DQ4_B	251	VSS
13	VSS	157	DQS5_A_t, TDQS5_A_t	62	ALERT_n	206	VSS	108	VSS	252	DQ6_B
14	DQ4_A	158	VSS	63	VSS	207	RESET_n	109	DQ5_B	253	VSS
15	VSS	159	DQ5_A	64	CS0_A_n	208	VSS	110	VSS	254	DQ7_B
16	DQ5_A	160	VSS	65	VSS	209	CS1_A_n	111	DQ6_B	255	VSS
17	VSS	161	DQ7_A	66	CA0_A	210	VSS	112	VSS	256	DQ10_B
18	DQ8_A	162	VSS	67	VSS	211	CA1_A	113	DQ9_B	257	VSS
19	VSS	163	DQ10_A	68	CA2_A	212	VSS	114	VSS	258	DQ11_B
20	DQ9_A	164	VSS	69	VSS	213	CA3_A	115	DQS1_B_t	259	VSS
21	VSS	165	DQ11_A	70	CA4_A	214	VSS	116	DQS1_B_c	260	DQS6_B_c,TDQS6_B_c
22	DQS1_A_t	166	VSS	71	VSS	215	CA5_A	117	VSS	261	DQS6_B_t,TDQS6_B_t
23	DQS1_A_c	167	DQS6_A_c,TDQS6_A_c	72	CA6_A	216	VSS	118	DQ12_B	262	VSS
24	VSS	168	DQS6_A_t,TDQS6_A_t	73	VSS	217	CK_t	119	VSS	263	DQ14_B
25	DQ12_A	169	VSS	74	PAR_A	218	CK_c	120	DQ13_B	264	VSS
26	VSS	170	DQ14_A	75	VSS	219	VSS	121	VSS	265	DQ15_B
27	DQ13_A	171	VSS	KEY				122	DQ16_B	266	VSS
28	VSS	172	DQ15_A					123	VSS	267	DQ18_B
29	DQ16_A	173	VSS					124	DQ17_B	268	VSS
30	VSS	174	DQ18_A	76	CA0_B	220	RFU	125	VSS	269	DQ19_B
31	DQ17_A	175	VSS	77	VSS	221	CA1_B	126	DQS2_B_t	270	VSS
32	VSS	176	DQ19_A	78	CA2_B	222	VSS	127	DQS2_B_c	271	DQS7_B_c,TDQS7_B_c
33	DQS2_A_t	177	VSS	79	VSS	223	CA3_B	128	VSS	272	DQS7_B_t,TDQS7_B_t
34	DQS2_A_c	178	DQS7_A_c,TDQS7_A_c	80	CA4_B	224	VSS	129	DQ20_B	273	VSS
35	VSS	179	DQS7_A_t, TDQS7_A_t	81	VSS	225	CA5_B	130	VSS	274	DQ22_B
36	DQ20_A	180	VSS	82	CA6_B	226	VSS	131	DQ21_B	275	VSS
37	VSS	181	DQ22_A	83	VSS	227	PAR_B	132	VSS	276	DQ23_B
38	DQ21_A	182	VSS	84	CS0_B_n	228	VSS	133	DQ24_B	277	VSS
39	VSS	183	DQ23_A	85	VSS	229	CS1_B_n	134	VSS	278	DQ26_B
40	DQ24_A	184	VSS	86	LBD, RSP_A_n	230	VSS	135	DQ25_B	279	VSS
41	VSS	185	DQ26_A	87	LBS, RSP_B_n	231	RFU	136	VSS	280	DQ27_B
42	DQ25_A	186	VSS	88	VSS	232	RFU	137	DQS3_B_t	281	VSS
43	VSS	187	DQ27_A	89	CB4_B	233	VSS	138	DQS3_B_c	282	DQS8_B_c,TDQS8_B_c
44	DQS3_A_t	188	VSS	90	VSS	234	CB6_B	139	VSS	283	DQS8_B_t,TDQS8_B_t
45	DQS3_A_c	189	DQS8_A_c,TDQS8_A_c	91	CB5_B	235	VSS	140	DQ28_B	284	VSS
46	VSS	190	DQS8_A_t, TDQS8_A_t	92	VSS	236	CB7_B	141	VSS	285	DQ30_B
47	DQ28_A	191	VSS	93	DQS9_B_t, TDQS9_B_t	237	VSS	142	DQ29_B	286	VSS
48	VSS	192	DQ30_A	94	DQS9_B_c,TDQS9_B_c	238	DQS4_B_c	143	VSS	287	DQ31_B
49	DQ29_A	193	VSS	95	VSS	239	DQS4_B_t	144	RFU	288	VSS

Claim 1	Evidence of Use
	Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 6 (illustrating clock signal lines (e.g., “CK_t” and “CK_c”), control/address (C/A) signal lines (e.g., “CA[]_A,” “CA[]_B,” “CS[]_A_n,” and “CS[]_B_n”), and data signal lines (e.g., “DQ[]_A” and “DQ[]_B”)).

Front Side Pin Label	Pin	Pin	Back side Pin Label
VIN_BULK	1	145	VIN_BULK
RFU	2	146	VIN_BULK
VIN_MGMT	3	147	PWR_GOOD/FAIL_n
HSCL	4	148	HSA
HSDA	5	149	RFU
VSS	6	150	RFU
DQ0_A	7	151	VSS
VSS	8	152	DQ2_A
DQ1_A	9	153	VSS
VSS	10	154	DQ3_A
DQS0_A_t	11	155	VSS
DQS0_A_c	12	156	DQS5_A_c, TDQS5_A_c
VSS	13	157	DQS5_A_t, TDQS5_A_t DBI0_A_n
DQ4_A	14	158	VSS
VSS	15	159	DQ6_A
DQ5_A	16	160	VSS
VSS	17	161	DQ7_A
DQ8_A	18	162	VSS
VSS	19	163	DQ10_A
DQ9_A	20	164	VSS
VSS	21	165	DQ11_A
DQS1_A_t	22	166	VSS
DQS1_A_c	23	167	DQS6_A_c, TDQS6_A_c
VSS	24	168	DQS6_A_t, TDQS6_A_t DBI1_A_n
DQ12_A	25	169	VSS
VSS	26	170	DQ14_A
DQ13_A	27	171	VSS
VSS	28	172	DQ15_A
DQ16_A	29	173	VSS
VSS	30	174	DQ18_A
DQ17_A	31	175	VSS
VSS	32	176	DQ19_A
DQS2_A_t	33	177	VSS
DQS2_A_c	34	178	DQS7_A_c, TDQS7_A_c
VSS	35	179	DQS7_A_t, TDQS7_A_t DBI2_n
DQ20_A	36	180	VSS
VSS	37	181	DQ22_A
DQ21_A	38	182	VSS

Front Side Pin Label	Pin	Pin	Back side Pin Label
PAR_A	74	218	CK_c
V33	75	219	V33
	Key		
CA0_B	76	220	RFU
VSS	77	221	CA1_B
CA2_B	78	222	VSS
VSS	79	223	CA3_B
CA4_B	80	224	VSS
VSS	81	225	CA5_B
CA6_B	82	226	VSS
VSS	83	227	PAR_B
CS0_B_n	84	228	VSS
VSS	85	229	CS1_B_n
LBD, RSP_A_n	86	230	VSS
LBS, RSP_B_n	87	231	RFU
VSS	88	232	RFU
CB4_B	89	233	VSS
VSS	90	234	CB6_B
CB5_B	91	235	VSS
VSS	92	236	CB7_B
DQS9_B_t, TDQS9_B_t DBI4_B_n	93	237	VSS
DQS9_B_c, TDQS9_B_c	94	238	DQS4_B_c
VSS	95	239	DQS4_B_t
CB0_B	96	240	VSS
V33	97	241	CB2_B
CB1_B	98	242	VSS
VSS	99	243	CB3_B
DQ0_B	100	244	VSS
VSS	101	245	DQ2_B
DQ1_B	102	246	VSS
VSS	103	247	DQ3_BDQ3_B
DQS0_B_t	104	248	VSS
DQS0_B_c	105	249	DQS5_B_c, TDQS5_B_c
VSS	106	250	DQS5_B_t, TDQS5_B_t DBI0_B_n
DQ4_B	107	251	VSS
VSS	108	252	DQ6_B
DQ5_B	109	253	VSS

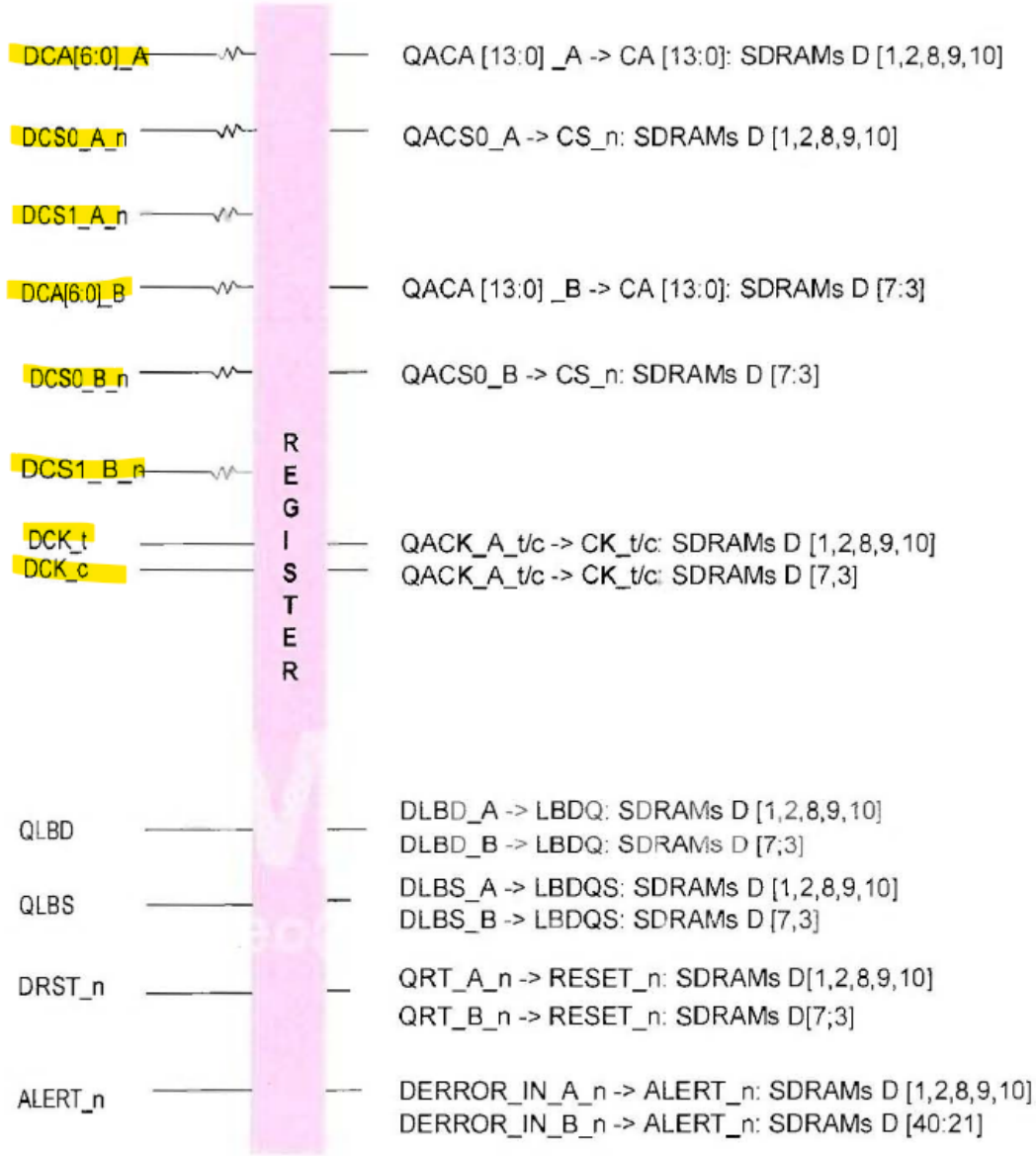
Claim 1	Evidence of Use

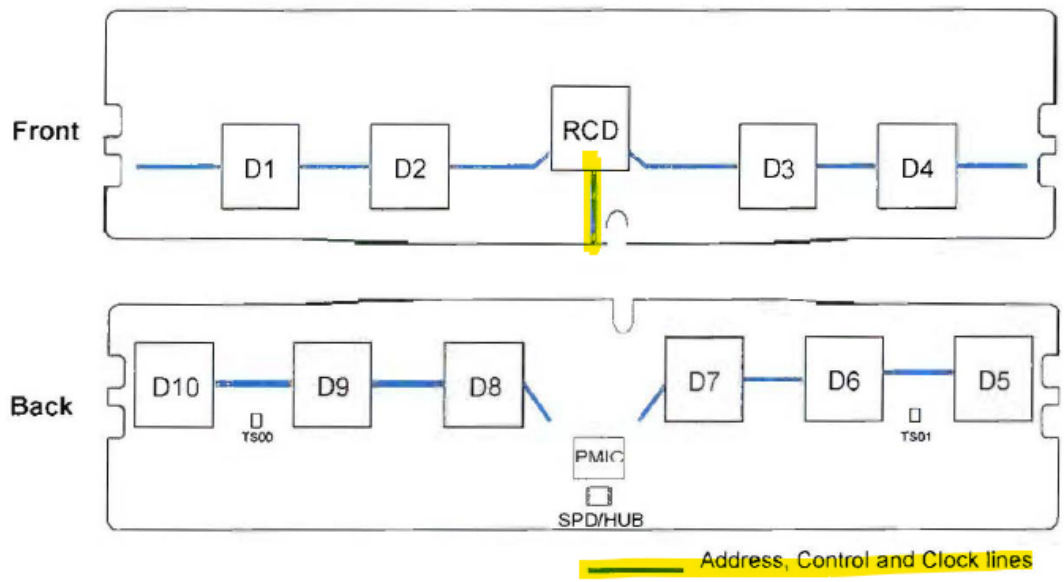
Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	39	183	DQ23_A
DQ24_A	40	184	VSS
VSS	41	185	DQ26_A
DQ25_A	42	186	VSS
VSS	43	187	DQ27_A
DQS3_A_t	44	188	VSS
DQS3_A_c	45	189	DQS8_A_c, TDQS8_A_c
VSS	46	190	DQS8_A_t, TDQS8_A_t DBI3_A_n
DQ28_A	47	191	VSS
VSS	48	192	DQ30_A
DQ29_A	49	193	VSS
VSS	50	194	DQ31_A
CB0_A	51	195	VSS
VSS	52	196	CB2_A
CB1_A	53	197	VSS
VSS	54	198	CB3_A
DQS4_A_t	55	199	VSS
DQS4_A_c	56	200	DQS9_A_c, TDQS9_A_c
VSS	57	201	DQS9_A_t, TDQS9_A_t DBI4_A_n
CB4_A	58	202	VSS
VSS	59	203	CB6_A
CB5_A	60	204	VSS
VSS	61	205	CB7_A
ALERT_n	62	206	VSS
VSS	63	207	RESET_n
CS0_A_n	64	208	VSS
VSS	65	209	CS1_A_n
CA0_A	66	210	VSS
VSS	67	211	CA1_A
CA2	68	212	VSS
VSS	69	213	CA3_A
CA4_A	70	214	VSS
VSS	71	215	CA5_A
CA6_A	72	216	VSS
VSS	73	217	CK_t

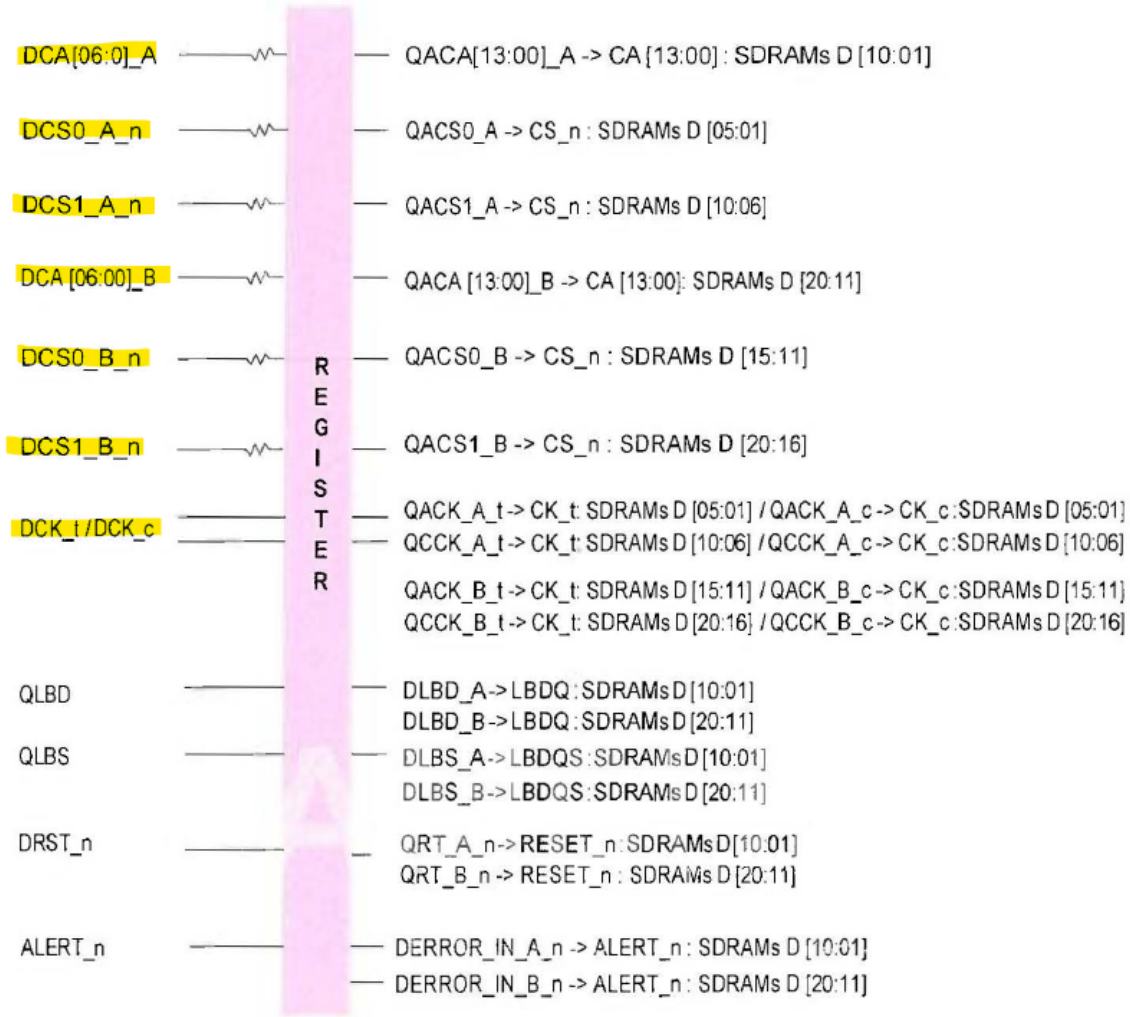
Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	110	254	DQ7_B
DQ8_B	111	255	VSS
VSS	112	256	DQ10_B
DQ9_B	113	257	VSS
VSS	114	258	DQ11_B
DQS1_B_t	115	259	VSS
DQS1_B_c	116	260	DQS6_B_c, TDQS6_B_c
VSS	117	261	DQS6_B_t, TDQS6_B_t DBI1_B_n
DQ12_B	118	262	VSS
VSS	119	263	DQ14_B
DQ13_B	120	264	VSS
VSS	121	265	DQ15_B
DQ16_B	122	266	VSS
VSS	123	267	DQ18_B
DQ17_B	124	268	VSS
VSS	125	269	DQ19_B
DQS2_B_t	126	270	VSS
DQS2_B_c	127	271	DQS7_B_c, TDQS7_B_c
VSS	128	272	DQS7_B_t, TDQS7_B_t DBI2_B_n
DQ20_B	129	273	VSS
VSS	130	274	DQ22_B
DQ21_B	131	275	VSS
VSS	132	276	DQ23_B
DQ24_B	133	277	VSS
VSS	134	278	DQ26_B
DQ25_B	135	279	VSS
VSS	136	280	DQ27_B
DQS3_B_t	137	281	VSS
DQS3_B_c	138	282	DQS8_B_c, TDQS8_B_c
VSS	139	283	DQS8_B_t, TDQS8_B_t DBI3_B_n
DQ28_B	140	284	VSS
VSS	141	285	DQ30_B
DQ29_B	142	286	VSS
VSS	143	287	DQ31_B
RFU	144	288	VSS

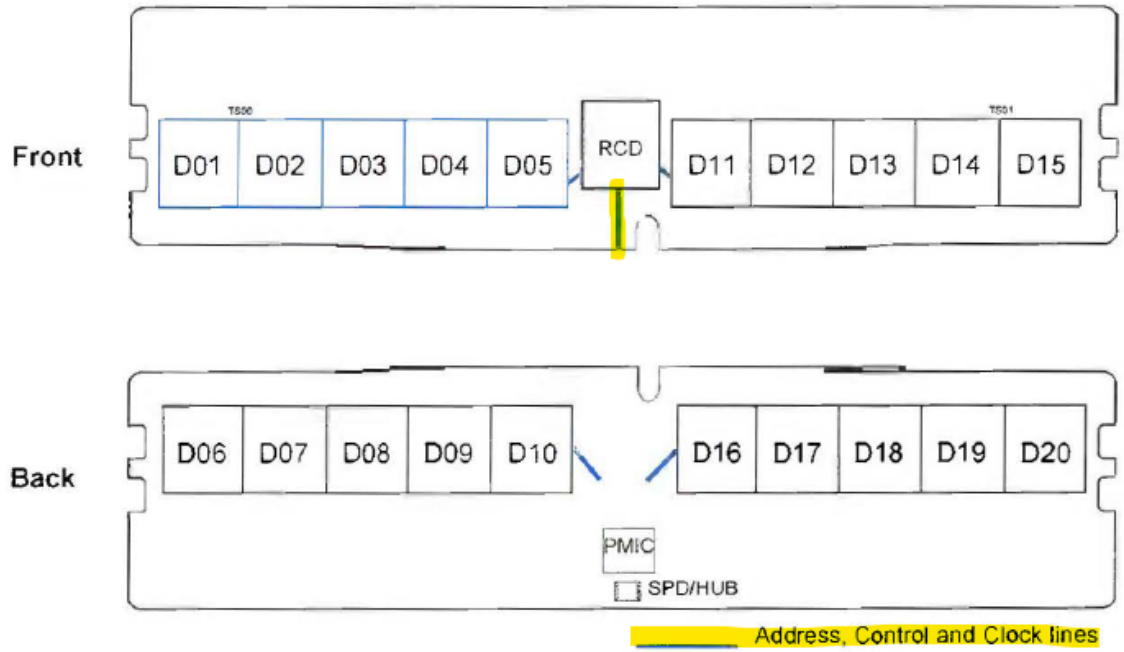
Figure 1. Wiring Assignments

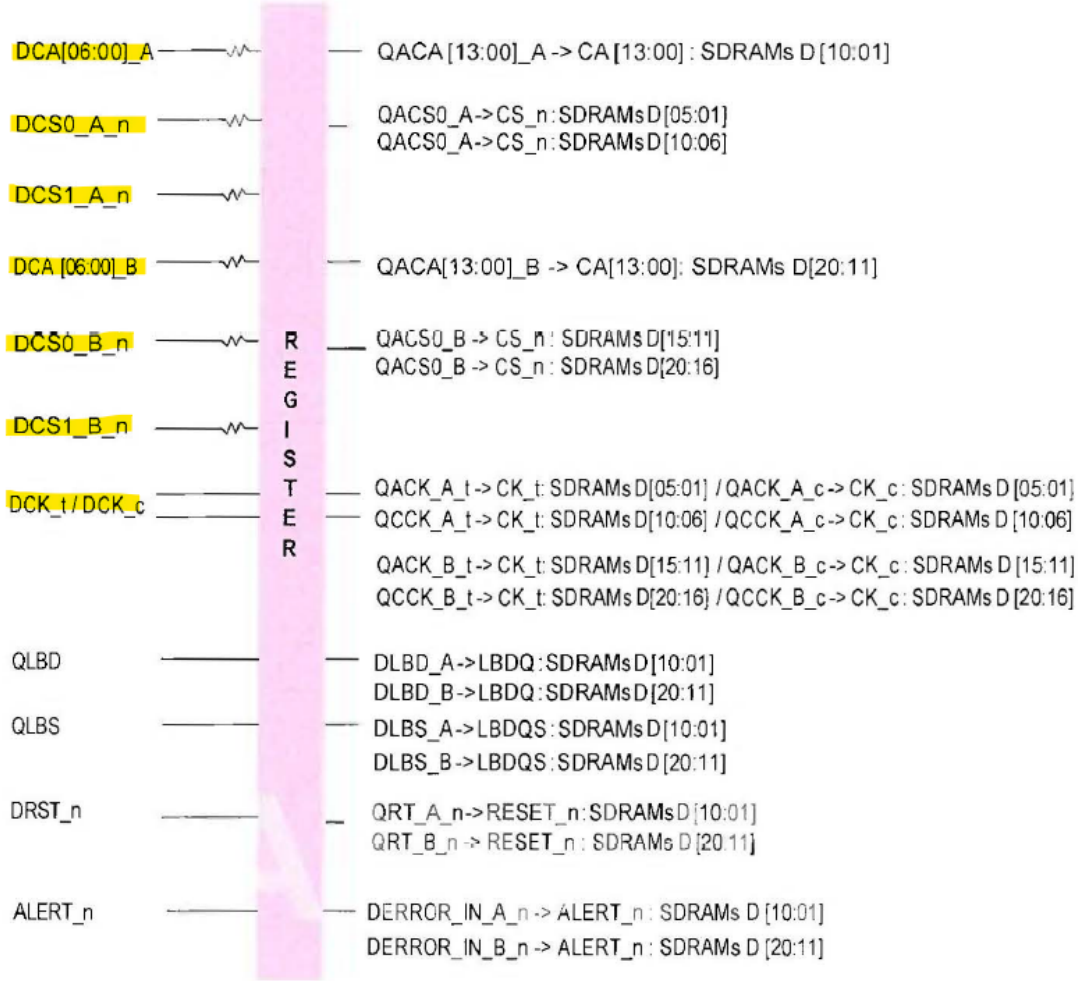
Claim 1	Evidence of Use
	Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 7-8 (illustrating clock signal lines (e.g., “CK_t” and “CK_c”), control/address (C/A) signal lines (e.g., “CA[]_A,” “CA[]_B,” “CS[]_A_n,” and “CS[]_B_n”), and data signal lines (e.g., “DQ[]_A” and “DQ[]_B”)).

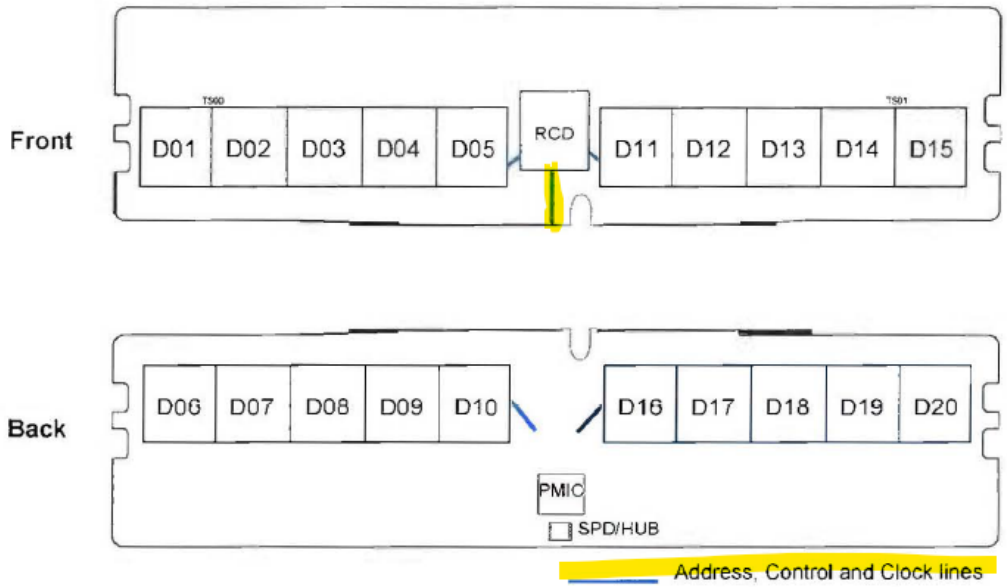

DCA[6:0]_A
DCS0_A_n
DCS1_A_n
DCA[6:0]_B
DCS0_B_n
DCS1_B_n
DCK_t
DCK_c
REGISTER
QACA [13:0] _A -> CA [13:0]: SDRAMs D [1,2,8,9,10]
QACS0_A -> CS_n: SDRAMs D [1,2,8,9,10]
QACA [13:0] _B -> CA [13:0]: SDRAMs D [7:3]
QACS0_B -> CS_n: SDRAMs D [7:3]
QACK_A_t/c -> CK_t/c: SDRAMs D [1,2,8,9,10]
QACK_A_t/c -> CK_t/c: SDRAMs D [7,3]
QLBD
QLBS
DRST_n
ALERT_n
DLBD_A -> LBDQ: SDRAMs D [1,2,8,9,10]
DLBD_B -> LBDQ: SDRAMs D [7;3]
DLBS_A -> LBDQS: SDRAMs D [1,2,8,9,10]
DLBS_B -> LBDQS: SDRAMs D [7,3]
QRT_A_n -> RESET_n: SDRAMs D[1,2,8,9,10]
QRT_B_n -> RESET_n: SDRAMs D[7;3]
DERROR_IN_A_n -> ALERT_n: SDRAMs D [1,2,8,9,10]
DERROR_IN_B_n -> ALERT_n: SDRAMs D [40:21]

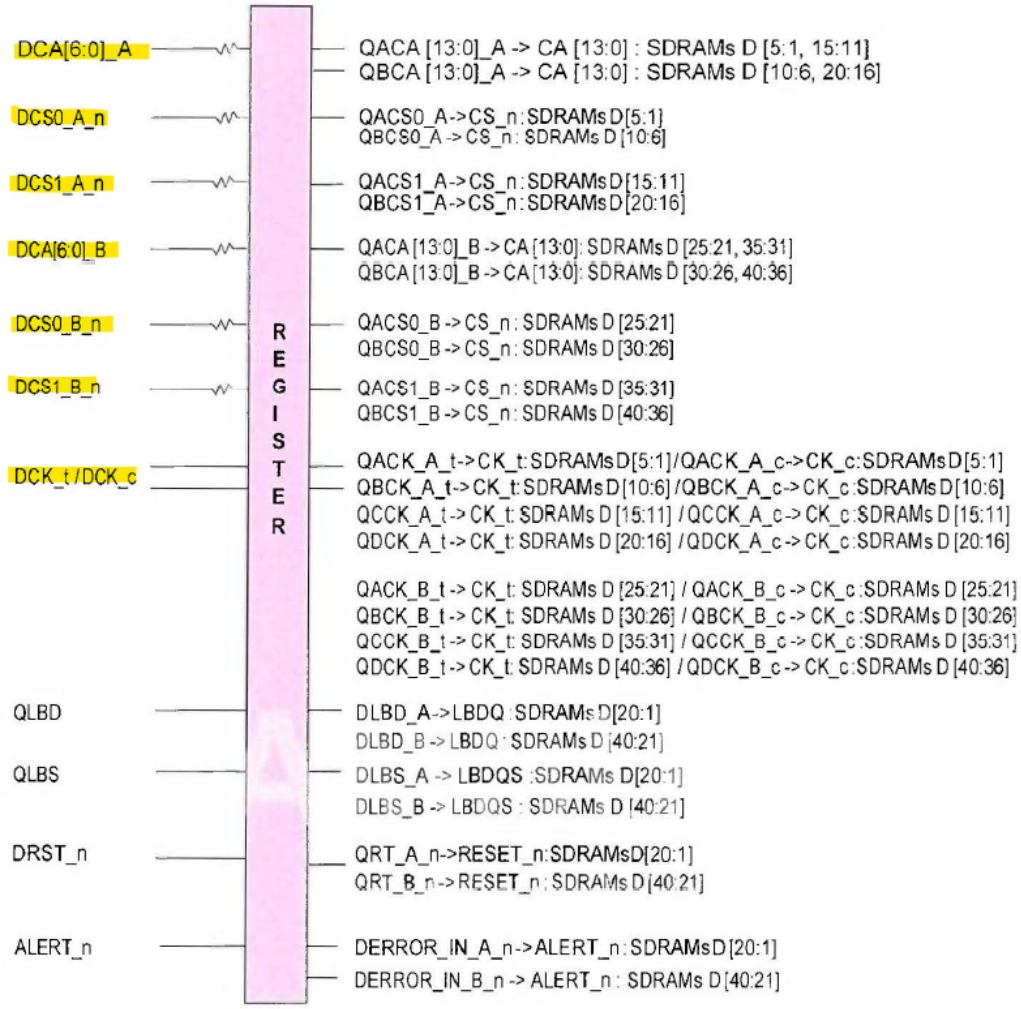
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 21.

Claim 1	Evidence of Use
	

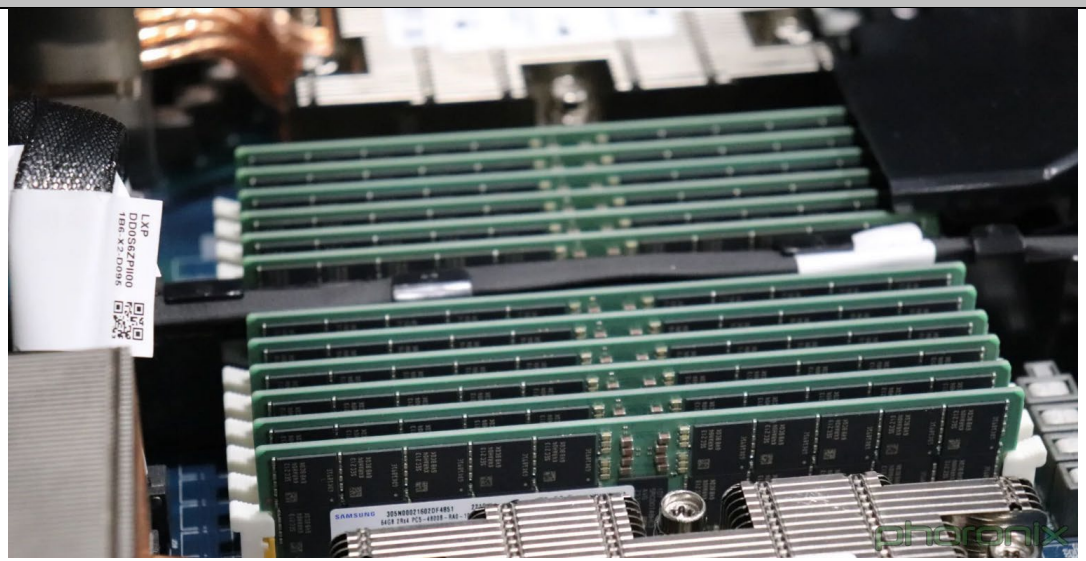
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 25.

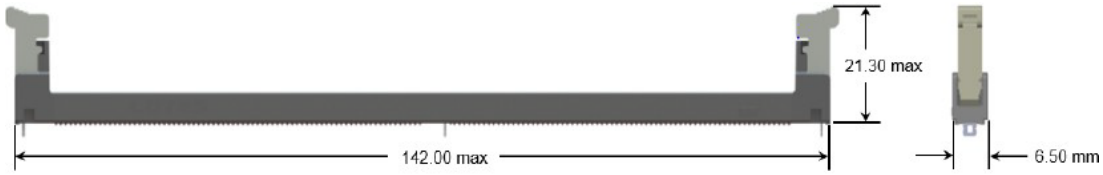
Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 29.

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 33. As explained *supra*, Samsung's RDIMMs are JEDEC standard compliant and are therefore configured to fit into a JEDEC-compliant memory slot, as illustrated below:

Claim 1	Evidence of Use
	 Ex. CC-70 (DDR5 Memory Channel Scaling Performance).

Claim 1	Evidence of Use
	 Figure 1 DDR5 socket and module (SMT)  **Figure 2 DDR5 U/R/LR DIMM Surface Mount (SMT) Connector Socket Outline** Ex. CC-73 (JEDEC PS-005B) at 6.

Claim 1	Evidence of Use
	Contacting the RDIMM's edge connectors with the corresponding pins in the memory slot forms electrical connections between the RDIMM and the system bus:

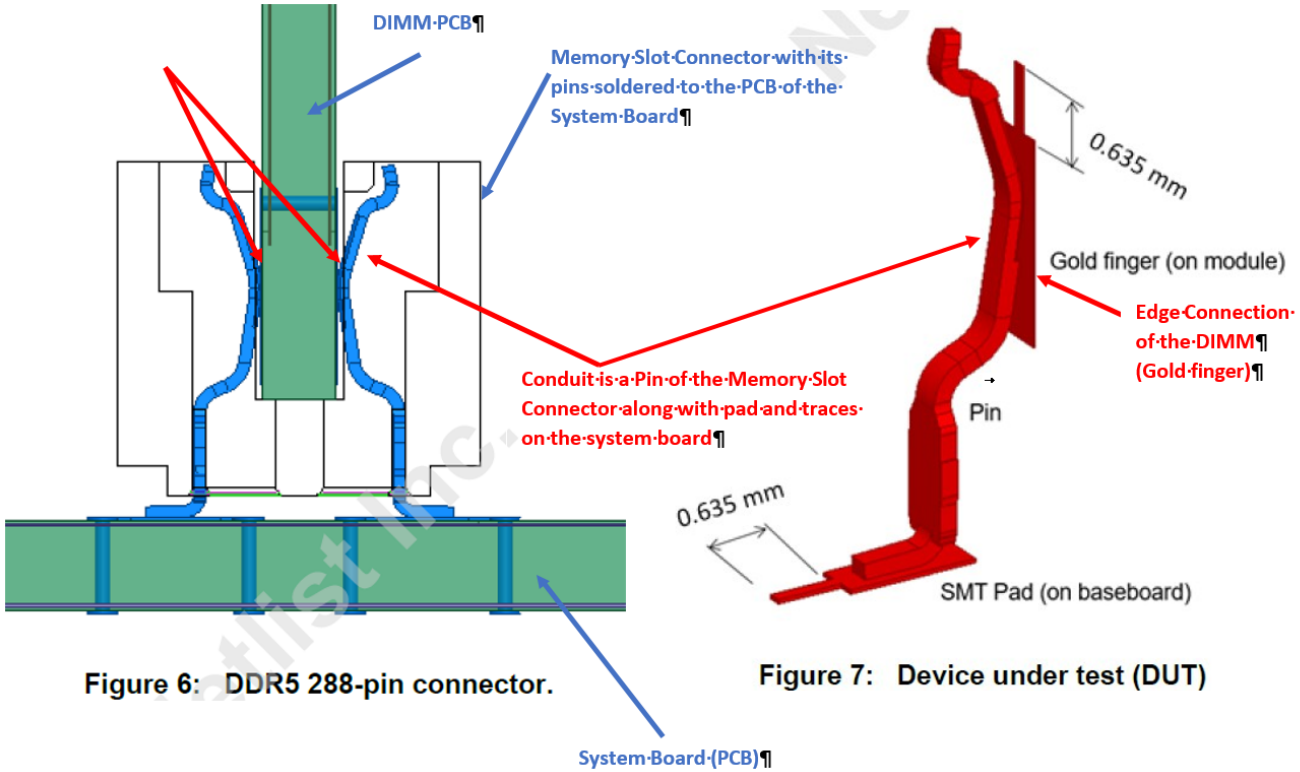


Figure 6: DDR5 288-pin connector.

Figure 7: Device under test (DUT)

Ex. CC-73 (JEDEC PS-005B) at 13, Figs. 6–7 (annotated) (illustrating an edge connection on a DIMM being electrically connected with a corresponding pin on the memory slot).

The JEDEC DDR5 RDIMM standard further demonstrates the Samsung Practicing '407 Products' edge connectors provide electrical connections between the memory module and the system bus because it includes connector pin assignments for clock signal lines, control/address (C/A) signal lines, and data signal lines included in the system bus. *See, e.g.,*

Claim 1	Evidence of Use

Table 3 — Pin Definitions

Pin Name	Description	Pin Name	Description
CA[6:0]_A CA[6:0]_B	Command and Address (CA) Bus	DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A and B
CS[1:0]_A_n CS[1:0]_B_n	Control (Chip Select) (CS_n)	CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A and B
PAR_A PAR_B	Parity input	DQS[9:0]_A_t DQS[9:0]_B_t	Data Strobes (positive line of differential pair)
CK_t	Clock (true/positive)	DQS[9:0]_A_c DQS[9:0]_B_c	Data Strobes (negative line of differential pair)
CK_c	Clock (complement/negative)	TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.

Ex. CC-88 (JEDEC 305B) at 3.

Table 4 — Input/Output Functional Description

Symbol	Type	I/O Levels	Function
CK_t, CK_c,	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All CA and CS_n input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[6:0]_A CA[6:0]_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during Mode Register Set commands.

Ex. CC-88 (JEDEC 305B) at 4.

DQ[31:0]_A DQ[31:0]_B	Input/ Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	Input/ Output	VDD	ECC Checkbits Input/ Output: Bi-directional data bus - for 8-bit ECC (EC8) all 8 bits are used - for 4-bit ECC (EC4) [3:0] bits are used; [7:4] bits are floating

Claim 1	Evidence of Use
	Ex. CC-88 (JEDEC 305B) at 4. **Table 4 — Input/Output Functional Description (cont'd)** **Symbol** / **Type** / **I/O Levels** / **Function** DQS[9:0]_A_t, DQS[9:0]_B_t, DQS[9:0]_A_c, DQS[9:0]_B_c — Input/Output — VDD — Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The Data Strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential Data Strobe only and does not support single-ended. TDQS[9:5]_A_t, TDQS[9:5]_B_t — Input — VDD — Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs. TDQS[9:5]_A_c, TDQS[9:5]_B_c — Input — VDD — Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs. Ex. CC-88 (JEDEC 305B) at 5.

Claim 1	Evidence of Use

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
VIN_BULK	1	145	VIN_BULK	PAR_A	74	218	CK_c
RFU	2	146	VIN_BULK	VSS	75	219	VSS
VIN_MGMT	3	147	PCAMP		Key		
HSCL	4	148	HSA				
HSDA	5	149	RFU	CA0_B	76	220	RFU / No Pin Present
VSS	6	150	RFU	VSS	77	221	CA1_B
DQ0_A	7	151	VSS	CA2_B	78	222	VSS
VSS	8	152	DQ2_A	VSS	79	223	CA3_B
DQ1_A	9	153	VSS	CA4_B	80	224	VSS
VSS	10	154	DQ3_A	VSS	81	225	CA5_B
DQS0_A_t	11	155	VSS	CA6_B	82	226	VSS
DQS0_A_c	12	156	DQS5_A_c, TDQS5_A_c	VSS	83	227	PAR_B
VSS	13	157	DQS5_A_t, TDQS5_A_t	CS0_B_n	84	228	VSS
DQ4_A	14	158	VSS	VSS	85	229	CS1_B_n
VSS	15	159	DQ6_A	DLBDQ	86	230	VSS
DQ5_A	16	160	VSS	DLBDQS	87	231	RFU
VSS	17	161	DQ7_A	VSS	88	232	RFU
DQ8_A	18	162	VSS	CB4_B	89	233	VSS
VSS	19	163	DQ10_A	VSS	90	234	CB6_B
DQ9_A	20	164	VSS	CB5_B	91	235	VSS
VSS	21	165	DQ11_A	VSS	92	236	CB7_B
DQS1_A_t	22	166	VSS	DQS9_B_t, TDQS9_B_t	93	237	VSS
DQS1_A_c	23	167	DQS6_A_c, TDQS6_A_c	DQS9_B_c, TDQS9_B_c	94	238	DQS4_B_c
VSS	24	168	DQS6_A_t, TDQS6_A_t	VSS	95	239	DQS4_B_t
DQ12_A	25	169	VSS	CB0_B	96	240	VSS
VSS	26	170	DQ14_A	VSS	97	241	CB2_B
DQ13_A	27	171	VSS	CB1_B	98	242	VSS
VSS	28	172	DQ15_A	VSS	99	243	CB3_B
DQ16_A	29	173	VSS	DQ0_B	100	244	VSS
VSS	30	174	DQ18_A	VSS	101	245	DQ2_B
DQ17_A	31	175	VSS	DQ1_B	102	246	VSS
VSS	32	176	DQ19_A	VSS	103	247	DQ3_B
DQS2_A_t	33	177	VSS	DQS0_B_t	104	248	VSS
DQS2_A_c	34	178	DQS7_A_c, TDQS7_A_c	DQS0_B_c	105	249	DQS5_B_c, TDQS5_B_c
VSS	35	179	DQS7_A_t, TDQS7_A_t	VSS	106	250	DQS5_B_t, TDQS5_B_t
DQ20_A	36	180	VSS	DQ4_B	107	251	VSS
VSS	37	181	DQ22_A	VSS	108	252	DQ6_B
DQ21_A	38	182	VSS	DQ5_B	109	253	VSS

Ex. CC-88 (JEDEC 305B) at 6.

Cravath & Wa

Claim 1	Evidence of Use

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	39	183	DQ23_A	VSS	110	254	DQ7_B
DQ24_A	40	184	VSS	DQ8_B	111	255	VSS
VSS	41	185	DQ26_A	VSS	112	256	DQ10_B
DQ25_A	42	186	VSS	DQ9_B	113	257	VSS
VSS	43	187	DQ27_A	VSS	114	258	DQ11_B
DQS3_A_t	44	188	VSS	DQS1_B_t	115	259	VSS
DQS3_A_c	45	189	DQS8_A_c, TDQS8_A_c	DQS1_B_c	116	260	DQS6_B_c, TDQS6_B_c
VSS	46	190	DQS8_A_t, TDQS8_A_t	VSS	117	261	DQS6_B_t, TDQS6_B_t
DQ28_A	47	191	VSS	DQ12_B	118	262	VSS
VSS	48	192	DQ30_A	VSS	119	263	DQ14_B
DQ29_A	49	193	VSS	DQ13_B	120	264	VSS
VSS	50	194	DQ31_A	VSS	121	265	DQ15_B
CB0_A	51	195	VSS	DQ16_B	122	266	VSS
VSS	52	196	CB2_A	VSS	123	267	DQ18_B
CB1_A	53	197	VSS	DQ17_B	124	268	VSS
VSS	54	198	CB3_A	VSS	125	269	DQ19_B
DQS4_A_t	55	199	VSS	DQS2_B_t	126	270	VSS
DQS4_A_c	56	200	DQS9_A_c, TDQS9_A_c	DQS2_B_c	127	271	DQS7_B_c, TDQS7_B_c
VSS	57	201	DQS9_A_t, TDQS9_A_t	VSS	128	272	DQS7_B_t, TDQS7_B_t
CB4_A	58	202	VSS	DQ20_B	129	273	VSS
VSS	59	203	CB6_A	VSS	130	274	DQ22_B
CB5_A	60	204	VSS	DQ21_B	131	275	VSS
VSS	61	205	CB7_A	VSS	132	276	DQ23_B
ALERT_n	62	206	VSS	DQ24_B	133	277	VSS
VSS	63	207	RESET_n	VSS	134	278	DQ26_B
CS0_A_n	64	208	VSS	DQ25_B	135	279	VSS
VSS	65	209	CS1_A_n	VSS	136	280	DQ27_B
CA0_A	66	210	VSS	DQS3_B_t	137	281	VSS
VSS	67	211	CA1_A	DQS3_B_c	138	282	DQS8_B_c, TDQS8_B_c
CA2_A	68	212	VSS	VSS	139	283	DQS8_B_t, TDQS8_B_t
VSS	69	213	CA3_A	DQ28_B	140	284	VSS
CA4_A	70	214	VSS	VSS	141	285	DQ30_B
VSS	71	215	CA5_A	DQ29_B	142	286	VSS
CA6_A	72	216	VSS	VSS	143	287	DQ31_B
VSS	73	217	CK_t	RFU	144	288	VSS

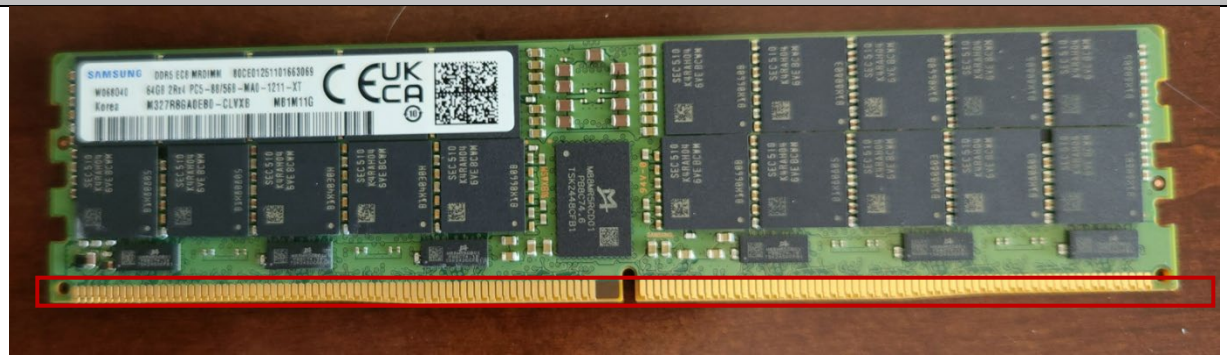
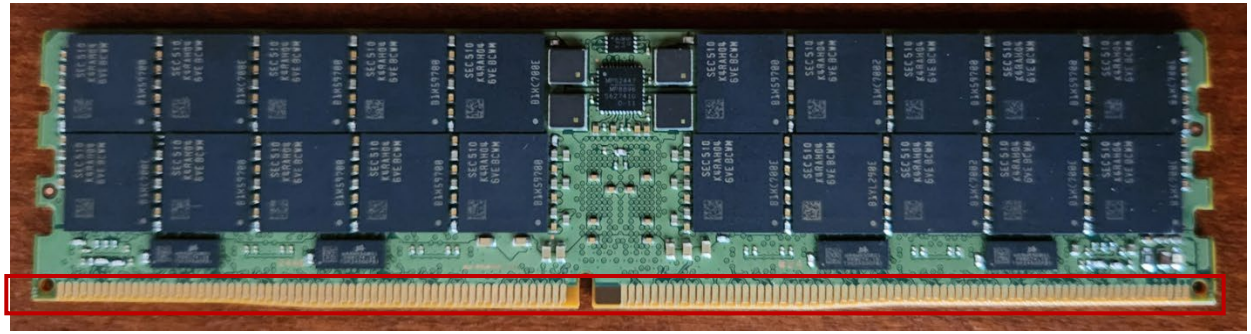
NOTE 1 Individual Annex standards for RDIMM define pin use where multiple functions are possible.
NOTE 2 Pin 220 for 8000 Mbps and faster RDIMM raw cards do not have the edge pin present.

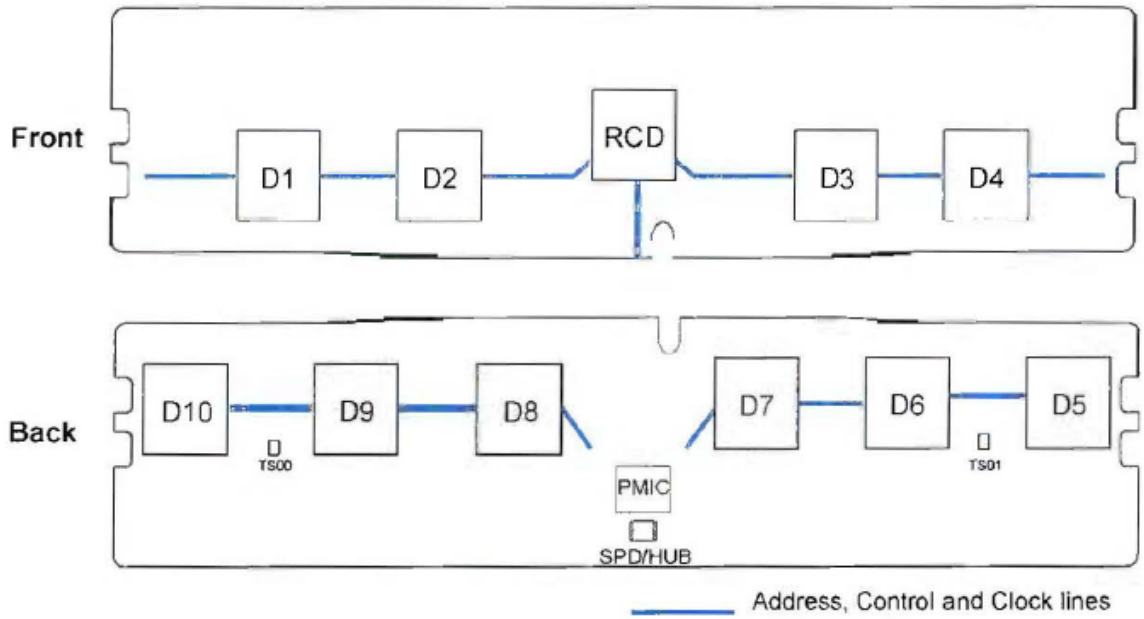
Ex. CC-88 (JEDEC 305B) at 7.

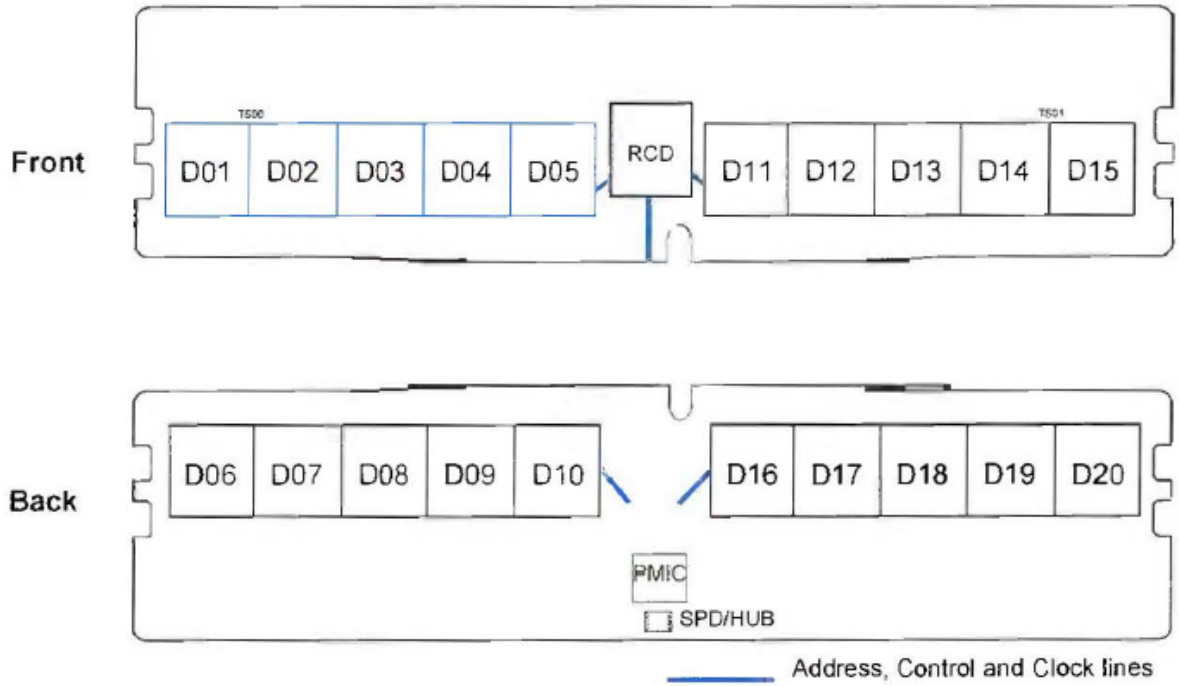
Quinn Emanuel Urquhart & Wa

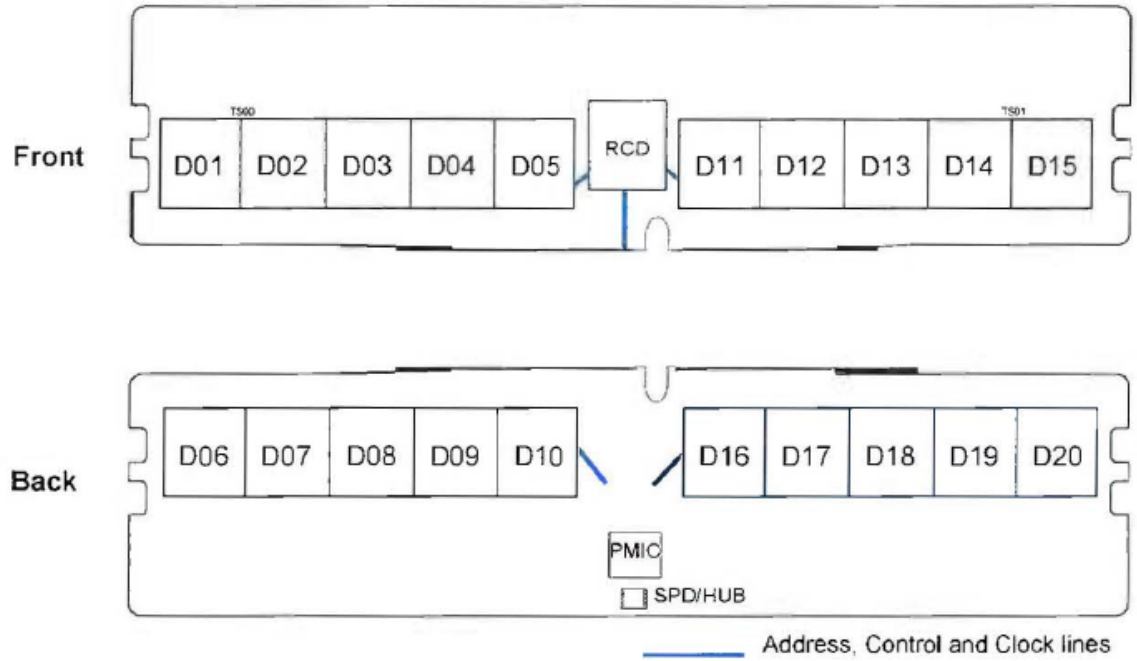
Claim 1	Evidence of Use
[**1.b**] memory devices mounted on the PCB and organized in a plurality of groups, wherein a respective group of the memory devices is configurable to communicate data with the memory controller via a corresponding subset of the data signal lines;	The Samsung Practicing '407 Products comprise memory devices mounted on the PCB and organized in a plurality of groups, wherein a respective group of the memory devices is configurable to communicate data with the memory controller via a corresponding subset of the data signal lines. For example, as seen below, each Samsung Practicing Product has multiple memory devices (there are one or more memory devices per DRAM package) mounted on the PCB and organized in a plurality of groups: Ex. ITC-1472 CC-116 (Samsung 4800MHz PC5-38400). Ex. ITC-1472 CC-117 (Samsung 5600MHz PC5-44800).

Claim 1	Evidence of Use
	 Ex. CC-118 (Samsung 64GB DDR5 PC5-4800 EC8 RDIMM 2Rx4 M321R8GA0BB0-CQK). Ex. CC-119 (Samsung 64GB DDR5 PC5-6400 EC8 RDIMM 2Rx4 M321R8GA0PB2-CCP).

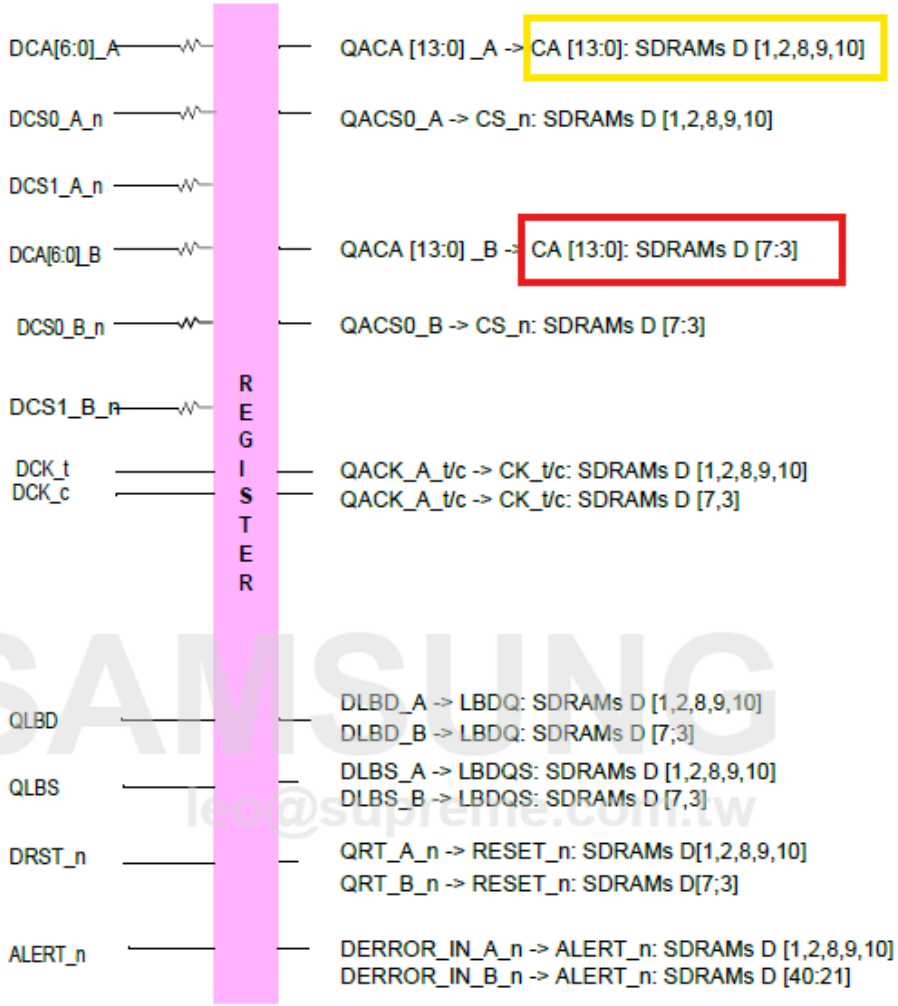
Claim 1	Evidence of Use
	  An image of a Samsung MRDIMM M327R8GA0EB0-CLVXB. *See* Exs. CC-5, CC-6.

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 21.

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 25.

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 29.

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 33. The memory devices are organized in a plurality of groups, and a respective group of the memory devices is configurable to communicate data with the memory controller via a corresponding subset of the data signal lines.

Claim 1	Evidence of Use
	 Ex. CC-89 at 21 (Samsung DDR5 RDIMM Datasheet)

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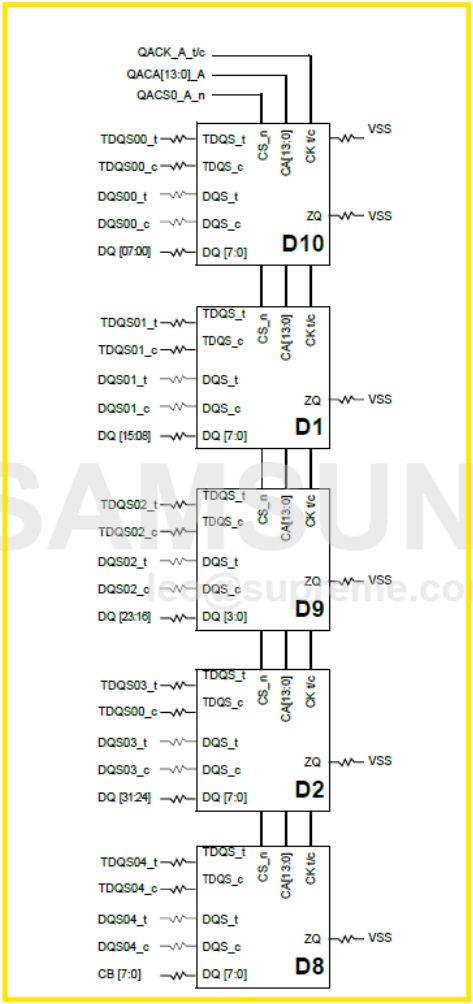
leo@supremic.com.tw

Claim 1	Evidence of Use
	Channel A  Ex. CC-89 at 22 (Samsung DDR5 RDIMM Datasheet)

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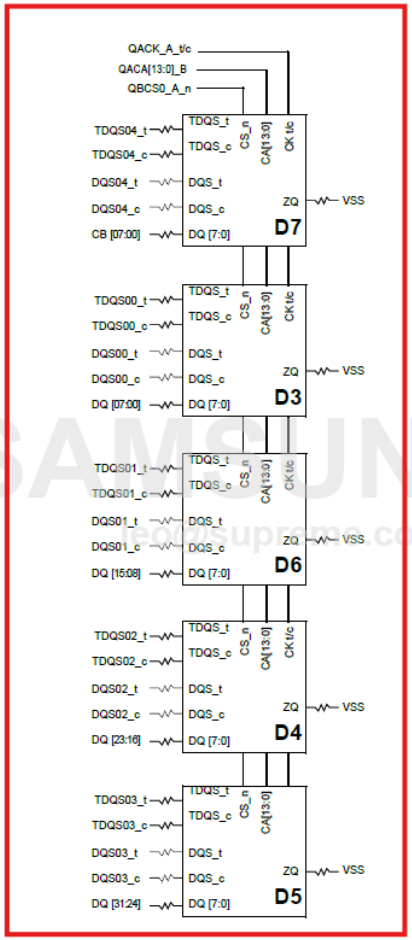
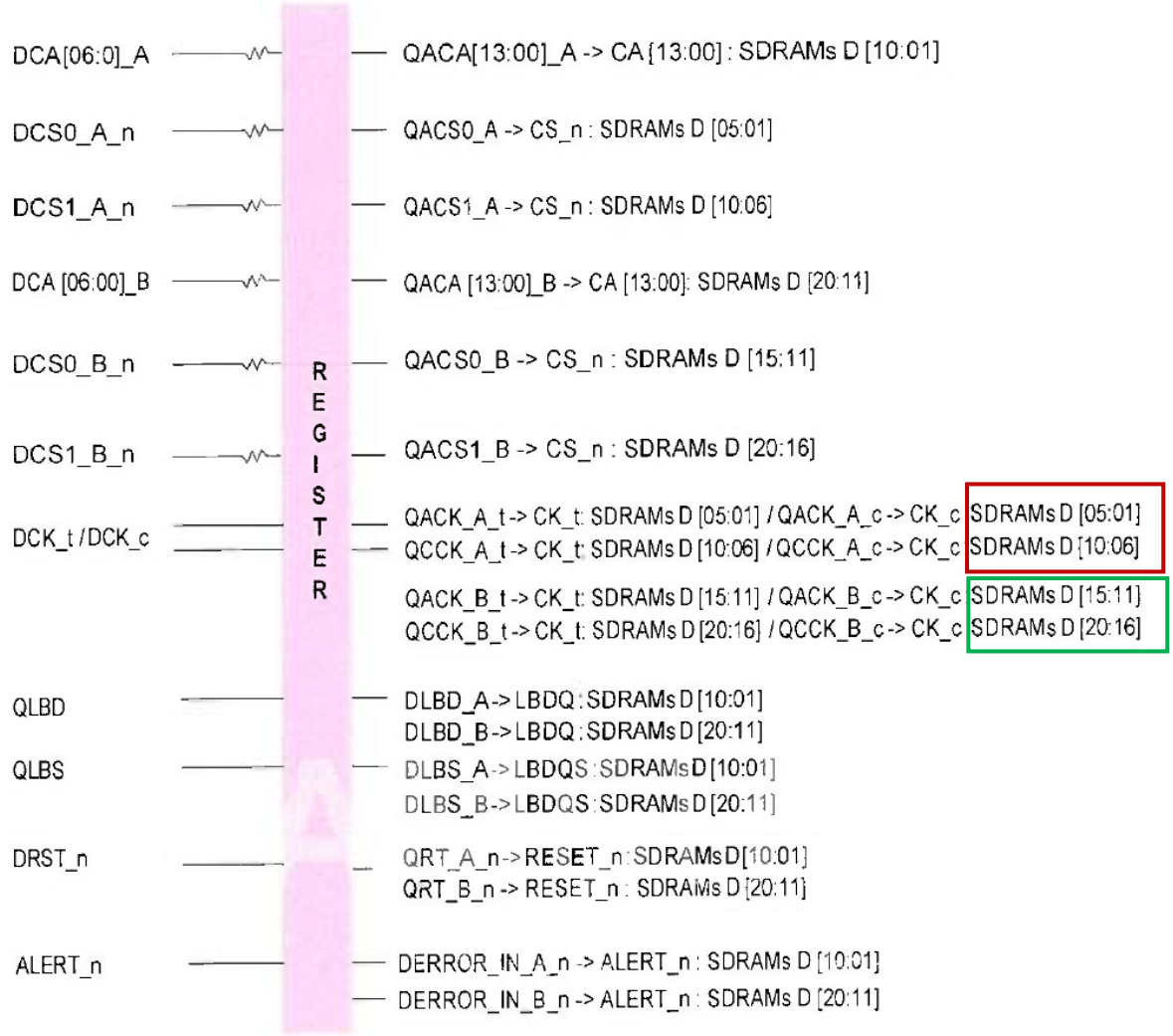
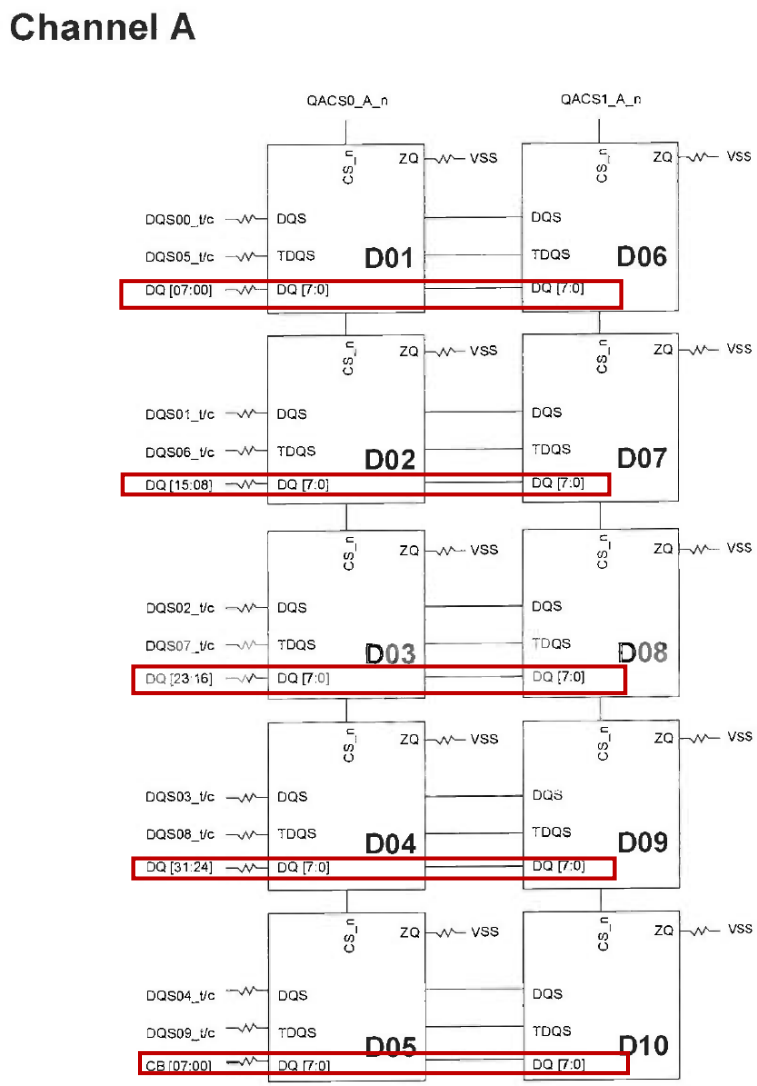
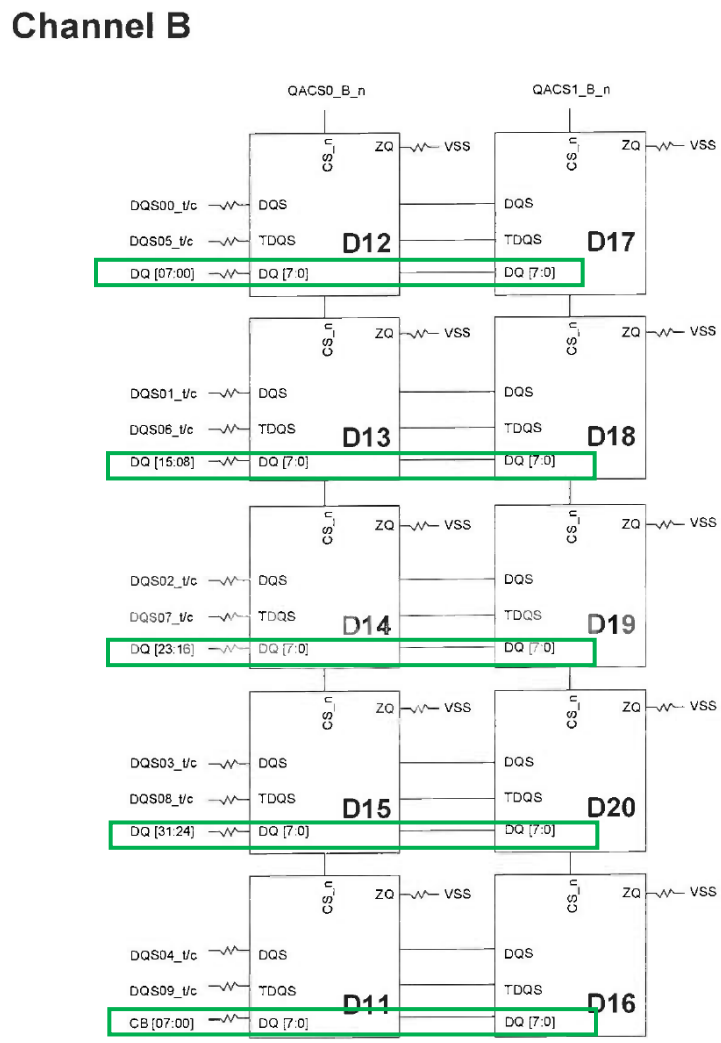
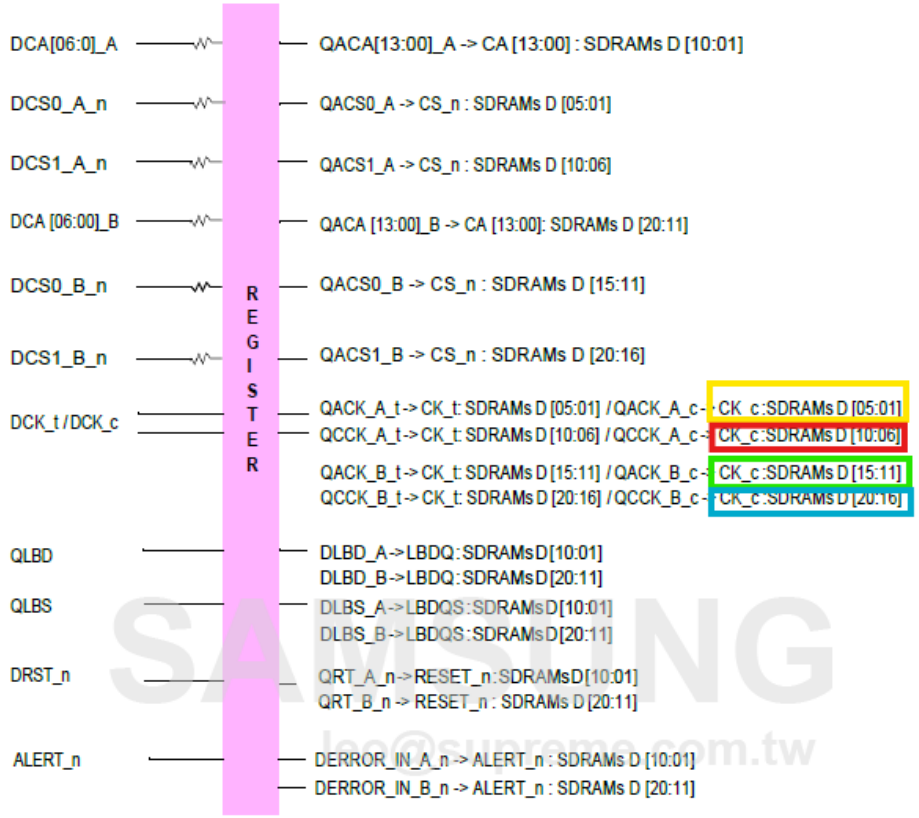
lee@supreme.com.tw

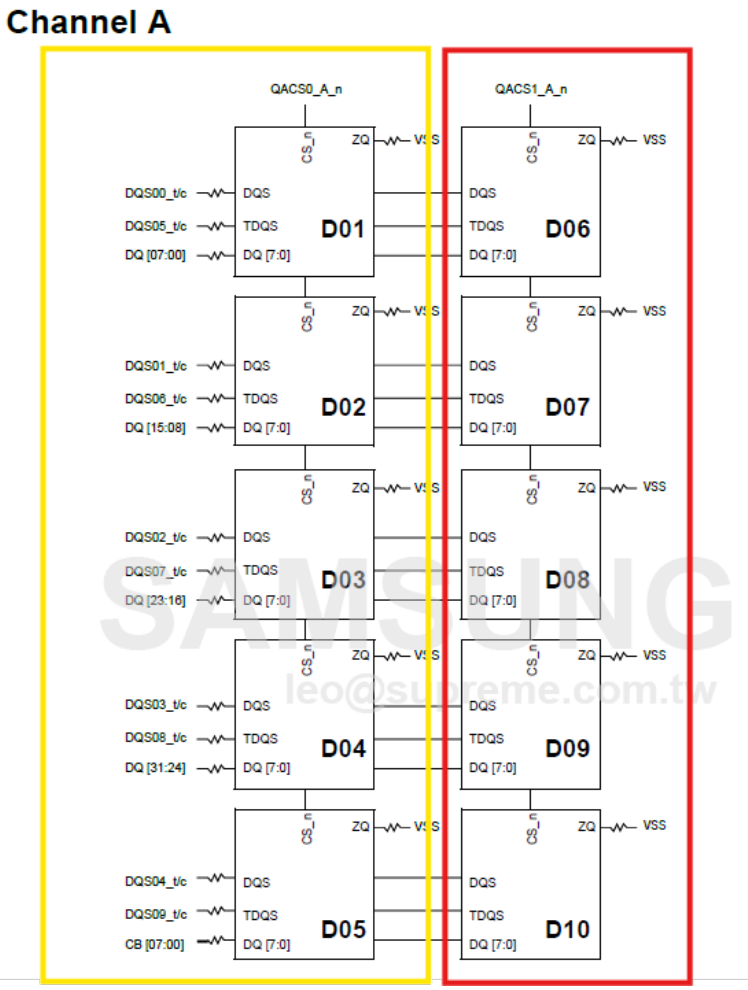
Claim 1	Evidence of Use
	Channel B  Ex. CC-89 at 23 (Samsung DDR5 RDIMM Datasheet)

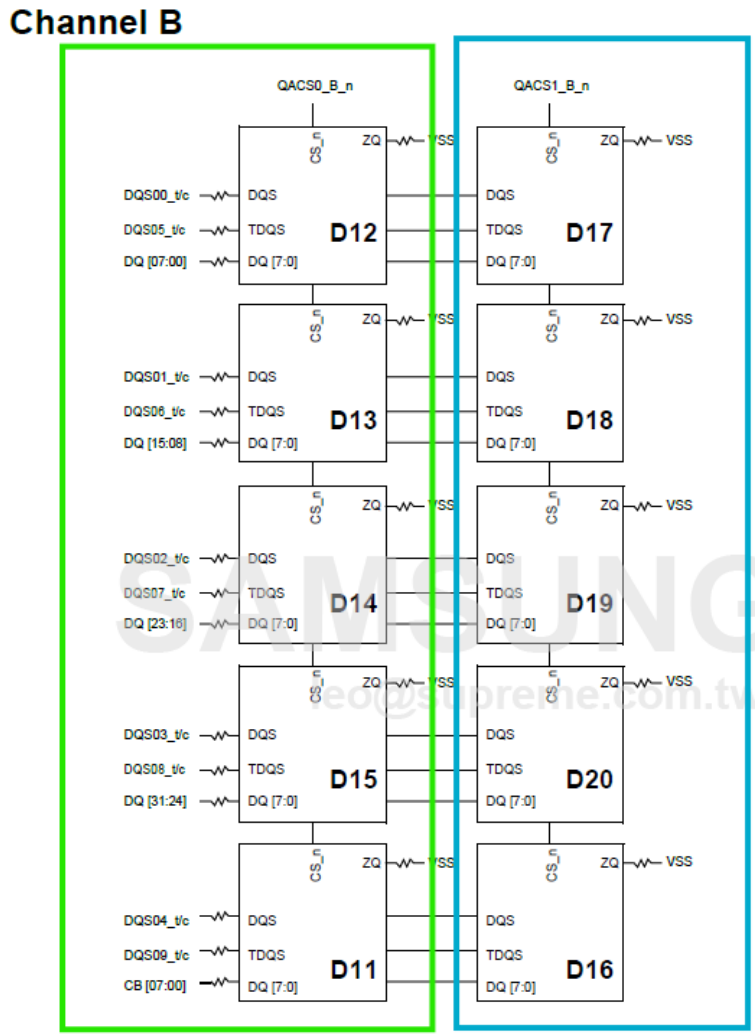
Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	Ex. CC-89 at 25 (Samsung DDR5 RDIMM Datasheet) 

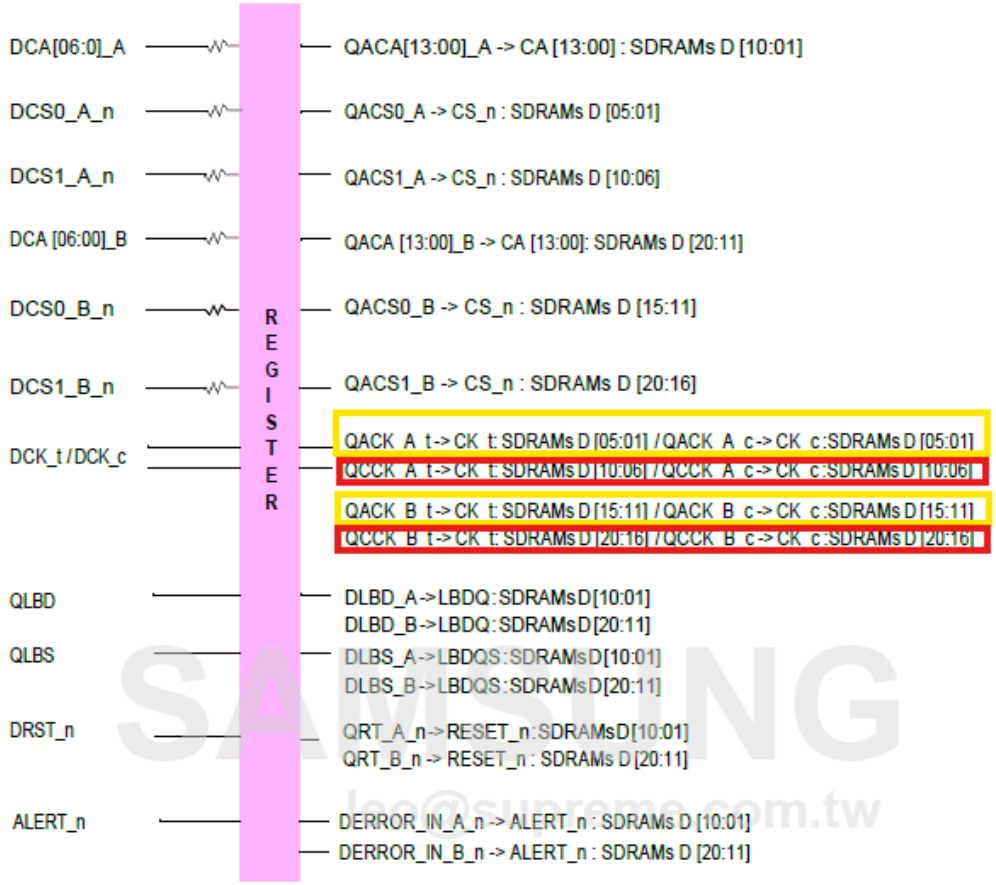
Claim 1	Evidence of Use
	Ex. CC-89 at 26 (Samsung DDR5 RDIMM Datasheet) 

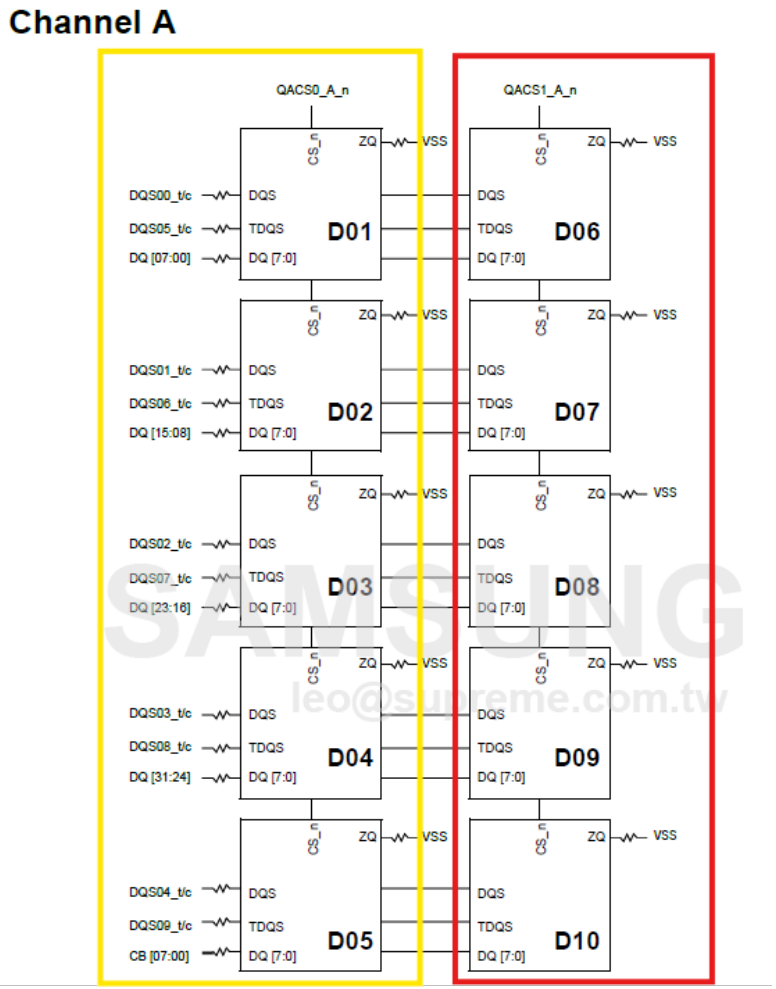
Claim 1	Evidence of Use
	Ex. CC-89 at 27 (Samsung DDR5 RDIMM Datasheet).  Ex. CC-89 at 25 (Samsung DDR5 RDIMM Datasheet).

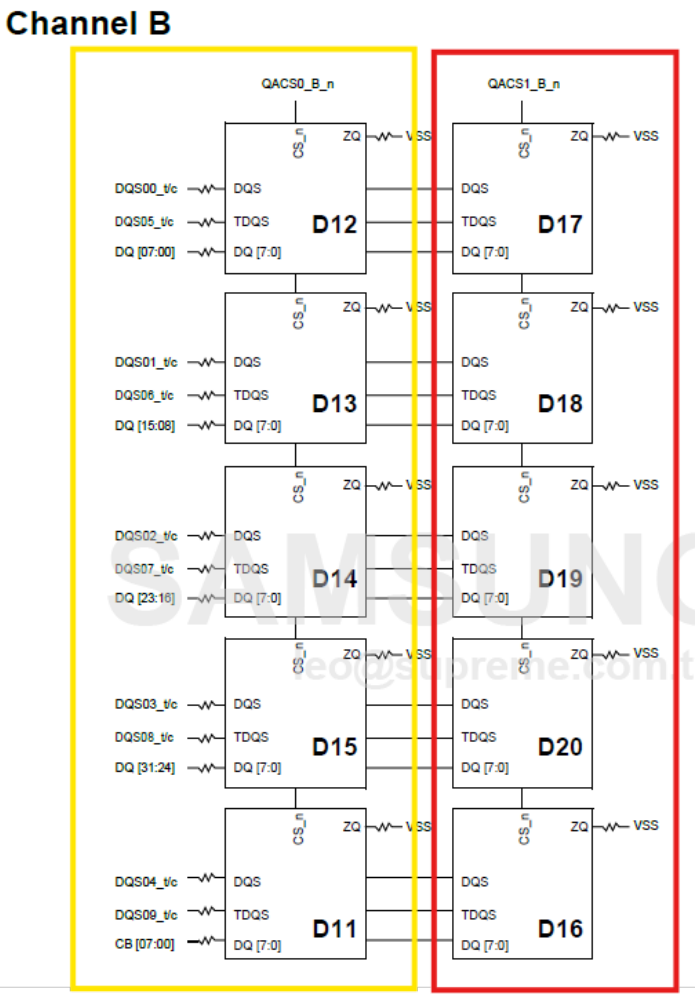
Claim 1	Evidence of Use
	 Ex. CC-89 at 26 (Samsung DDR5 RDIMM Datasheet).

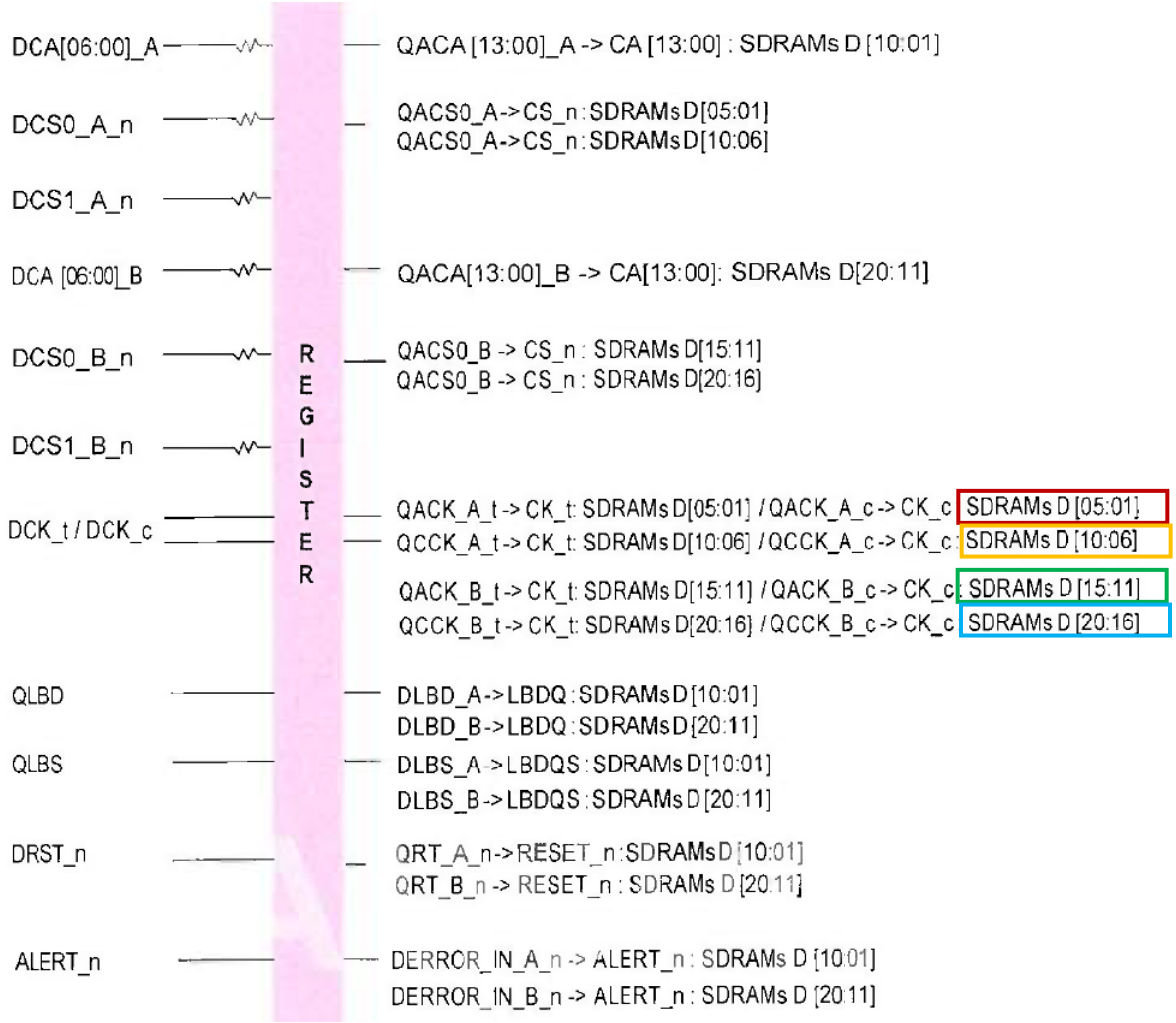
Claim 1	Evidence of Use
	 Ex. CC-89 at 27 (Samsung DDR5 RDIMM Datasheet).

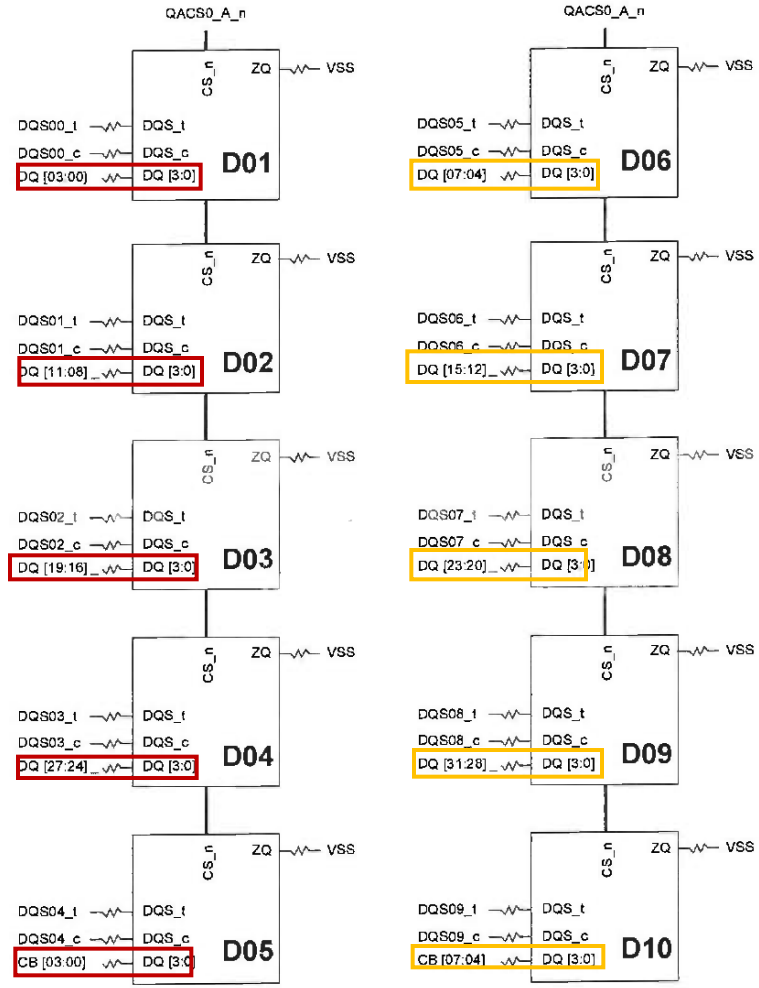
Claim 1	Evidence of Use
	SAMSUNG leo@supreme.com.tw

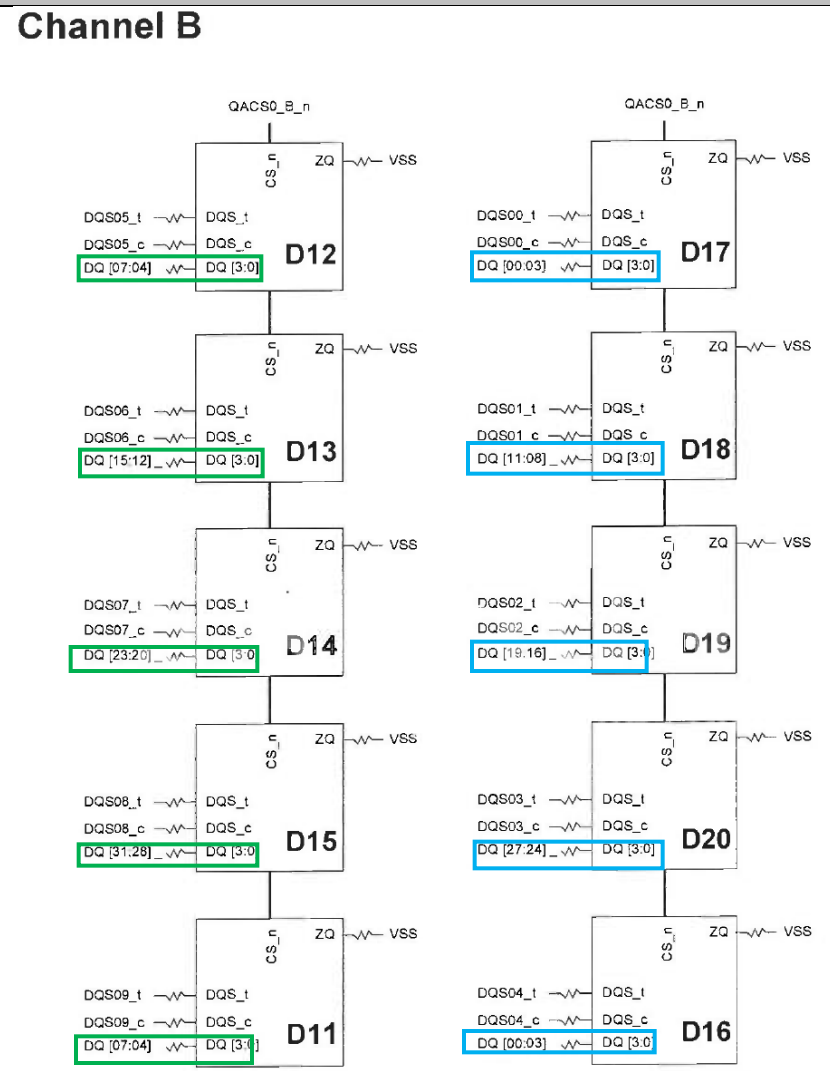
Claim 1	Evidence of Use
	Ex. CC-89 at 26 (Samsung DDR5 RDIMM Datasheet).  Ex. CC-89 at 25 (Samsung DDR5 RDIMM Datasheet).

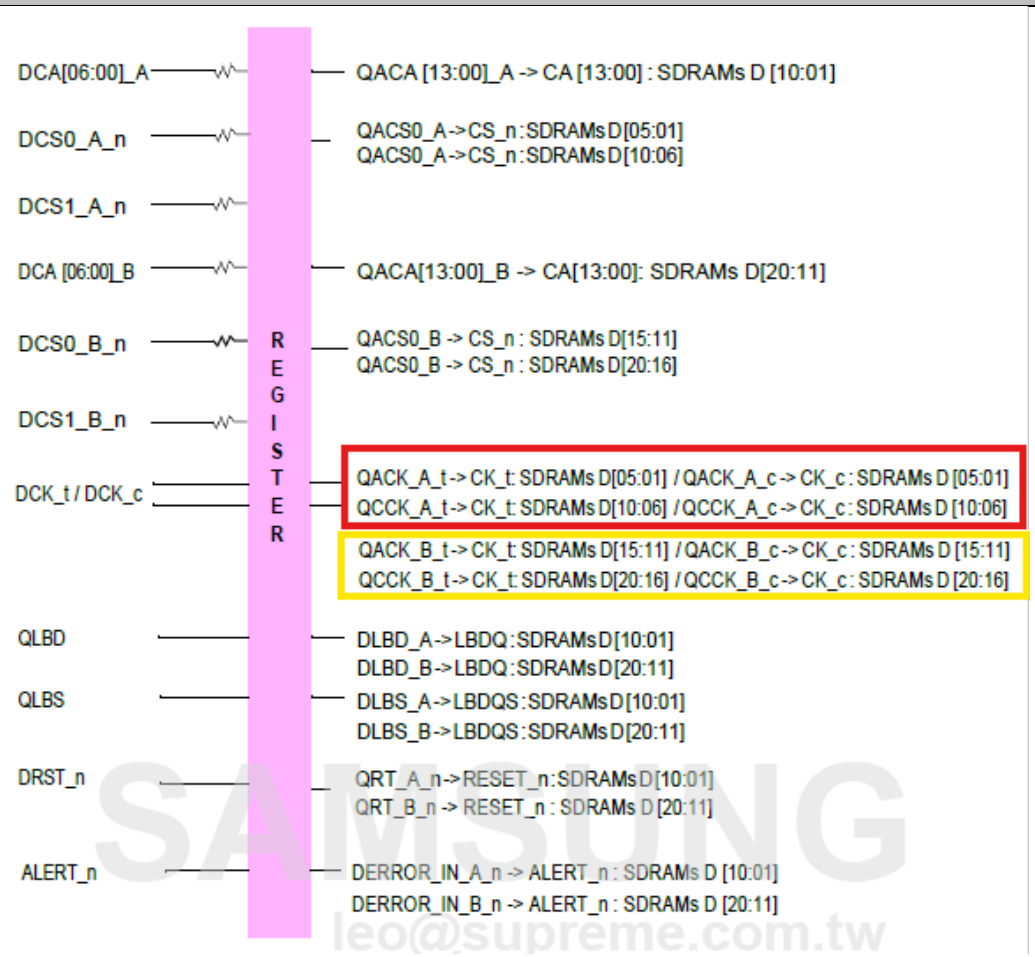
Claim 1	Evidence of Use
	 Ex. CC-89 at 26 (Samsung DDR5 RDIMM Datasheet).

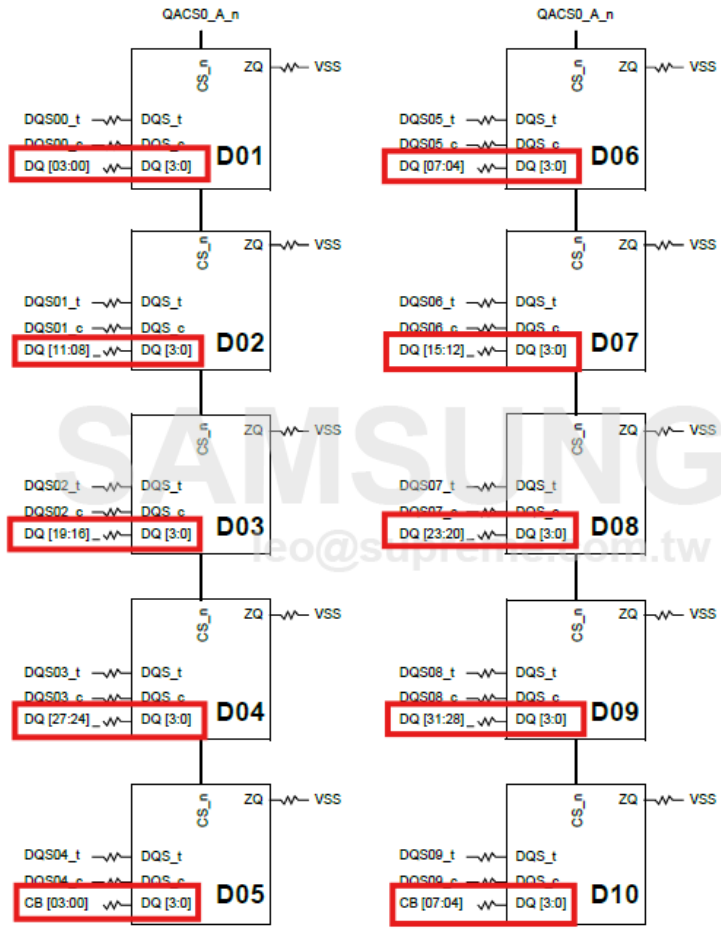
Claim 1	Evidence of Use
	 Ex. CC-89 at 27 (Samsung DDR5 RDIMM Datasheet).

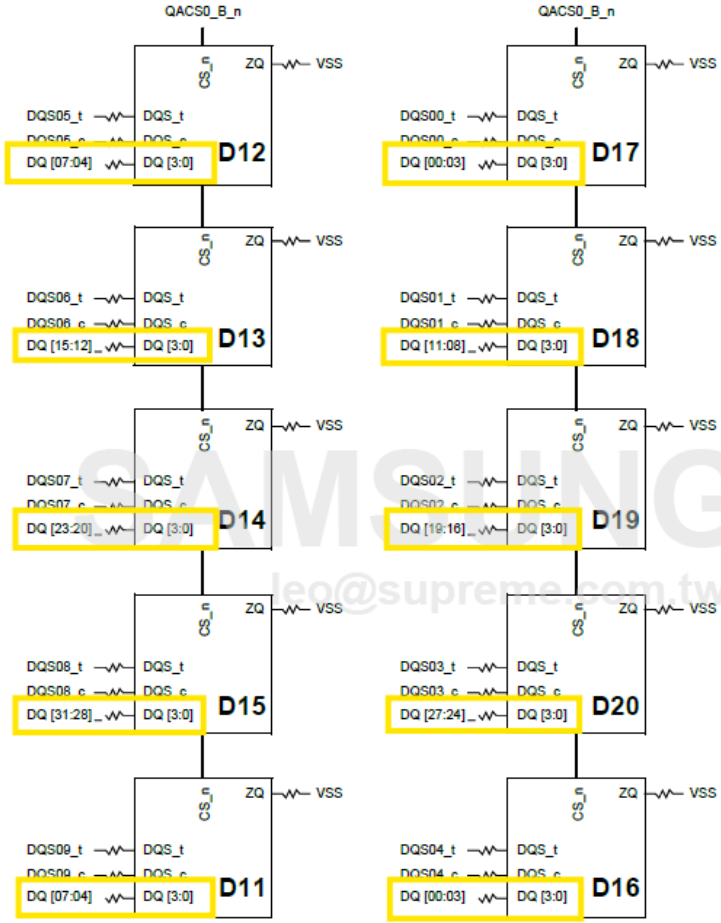
Claim 1	Evidence of Use
	 Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet).

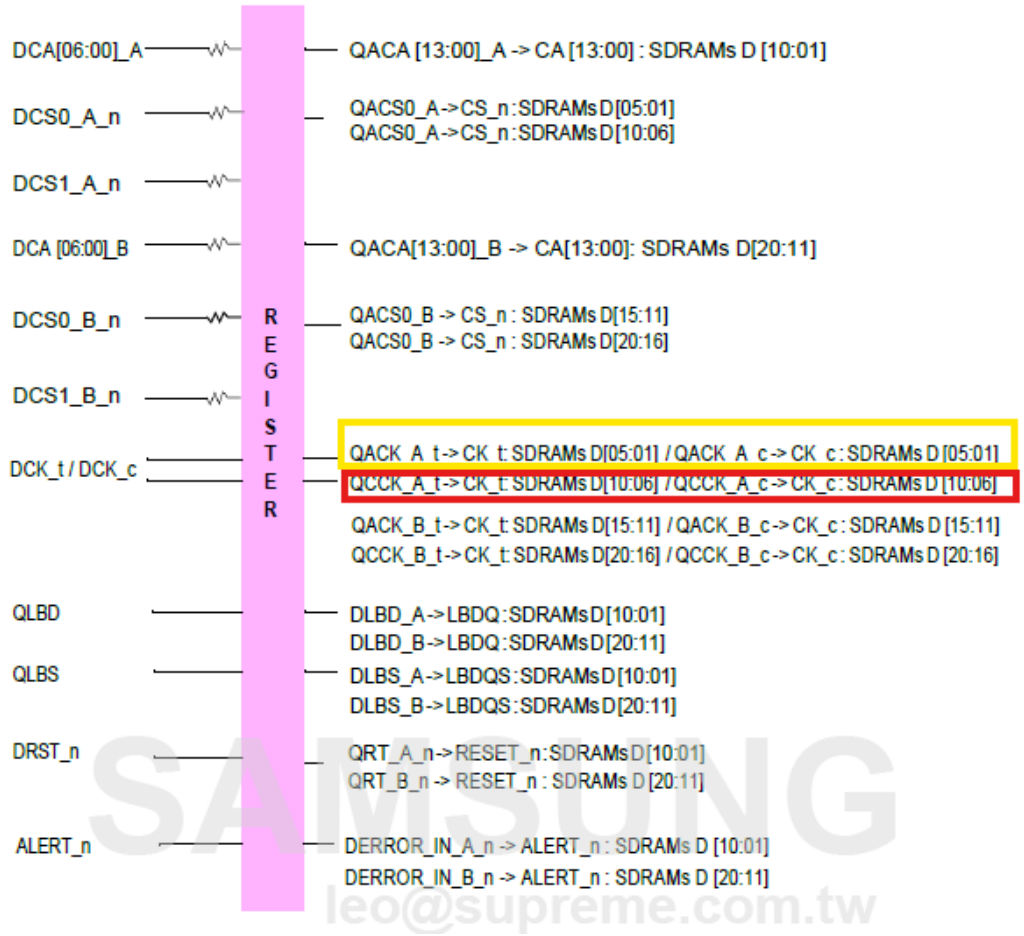
Claim 1	Evidence of Use
	Channel A  Ex. CC-89 at 30 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	 Ex. CC-89 at 31 (Samsung DDR5 RDIMM Datasheet)

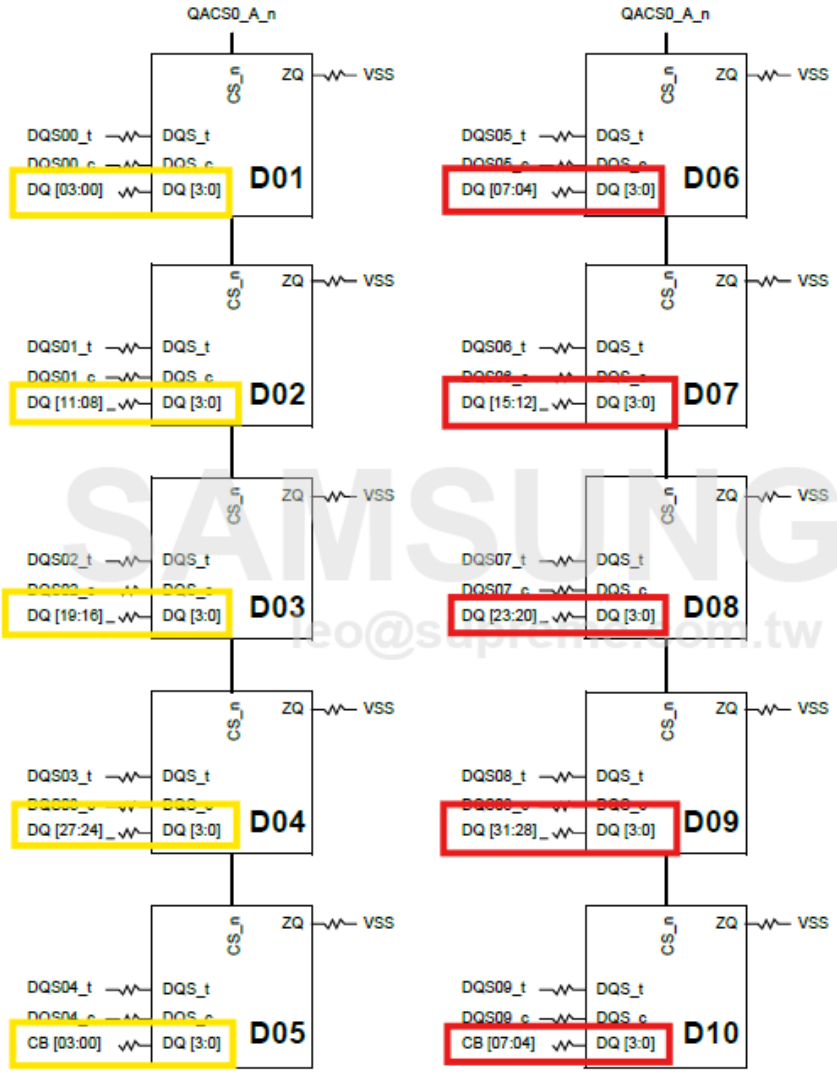
Claim 1	Evidence of Use
	 SAMSUNG leo@supreme.com.tw Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet).

Claim 1	Evidence of Use
	Channel A  Ex. CC-89 at 30 (Samsung DDR5 RDIMM Datasheet).

Claim 1	Evidence of Use
	Channel B  Ex. CC-89 at 31 (Samsung DDR5 RDIMM Datasheet).

Claim 1	Evidence of Use
	 SAMSUNG leo@supreme.com.tw Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet).

Channel A



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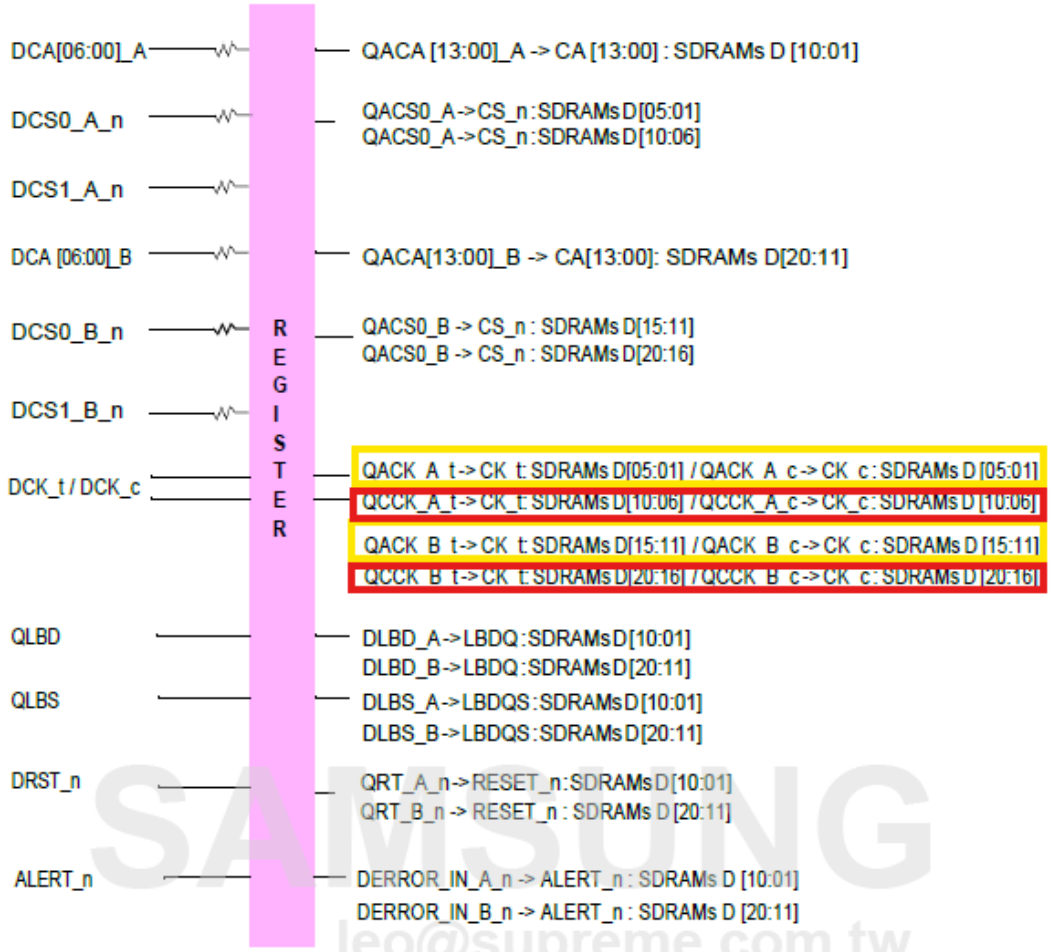
Claim 1	Evidence of Use
	Ex. CC-89 at 30 (Samsung DDR5 RDIMM Datasheet).



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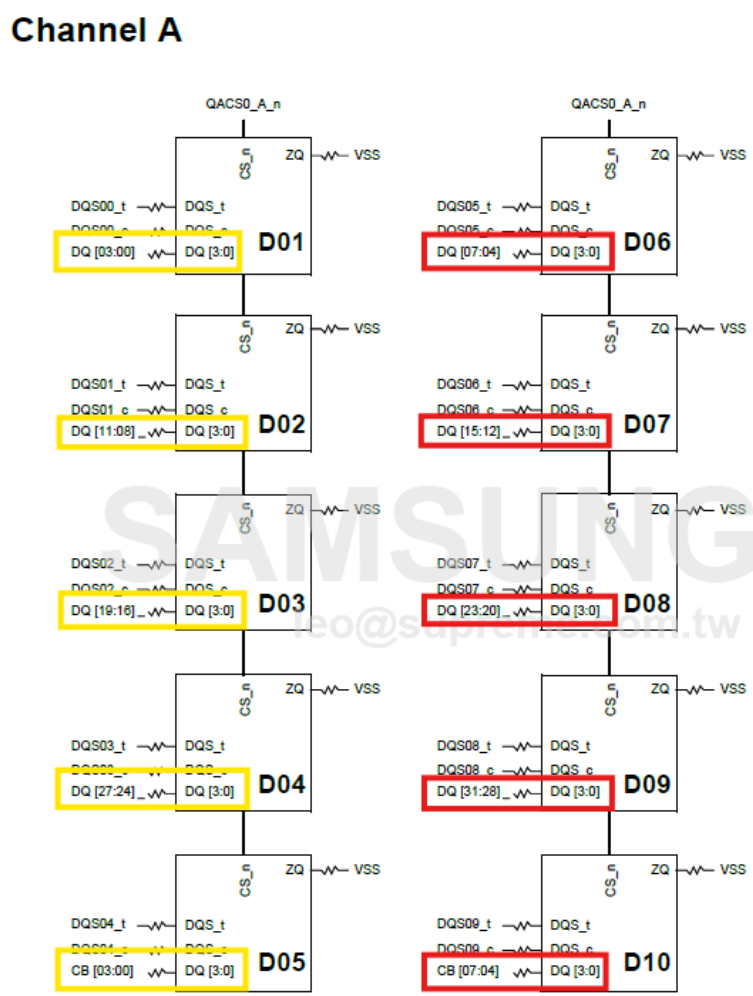
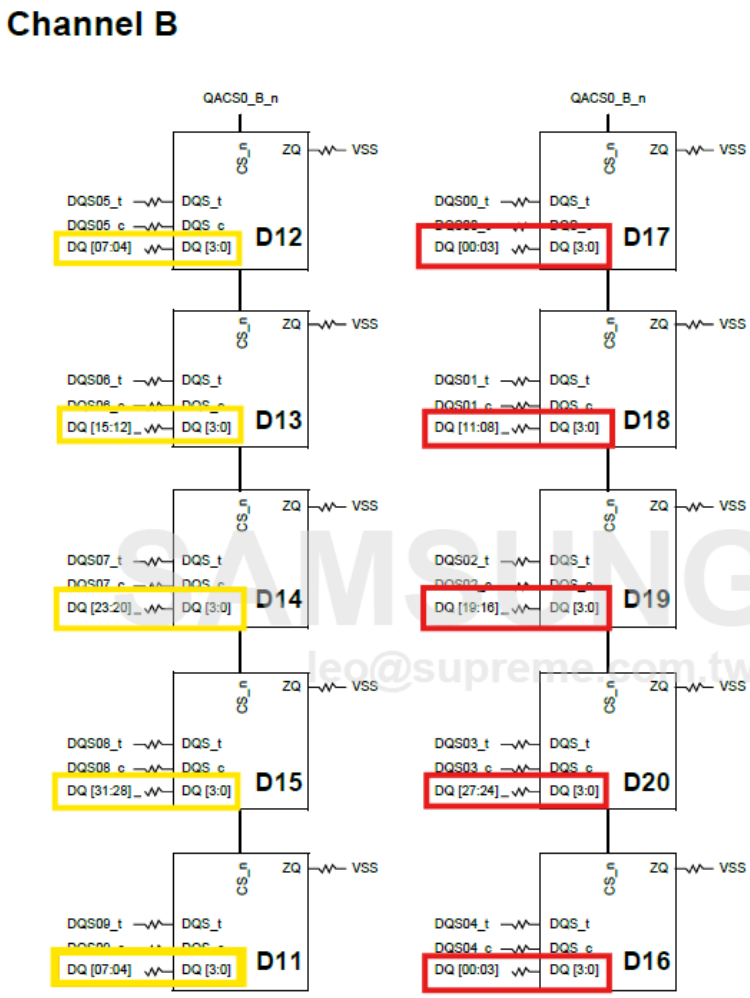
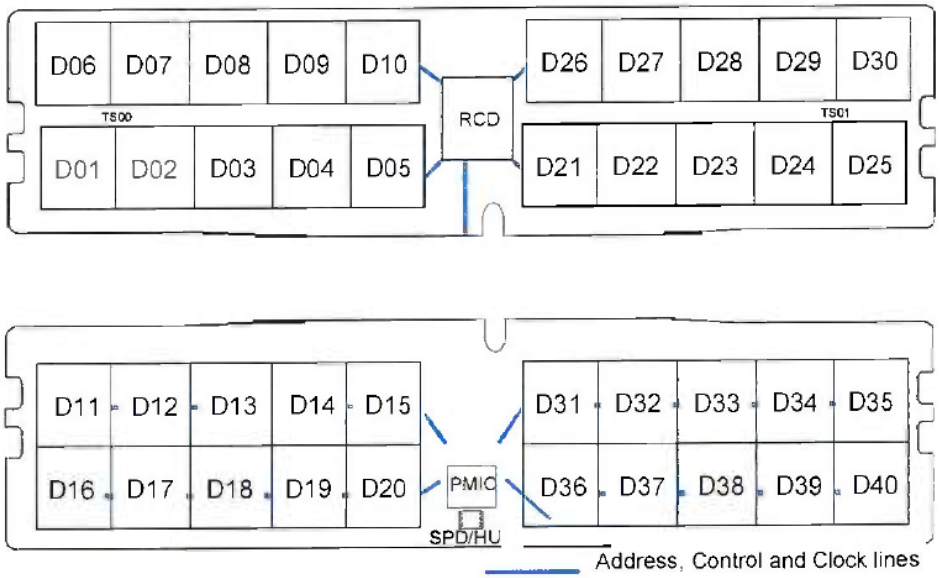
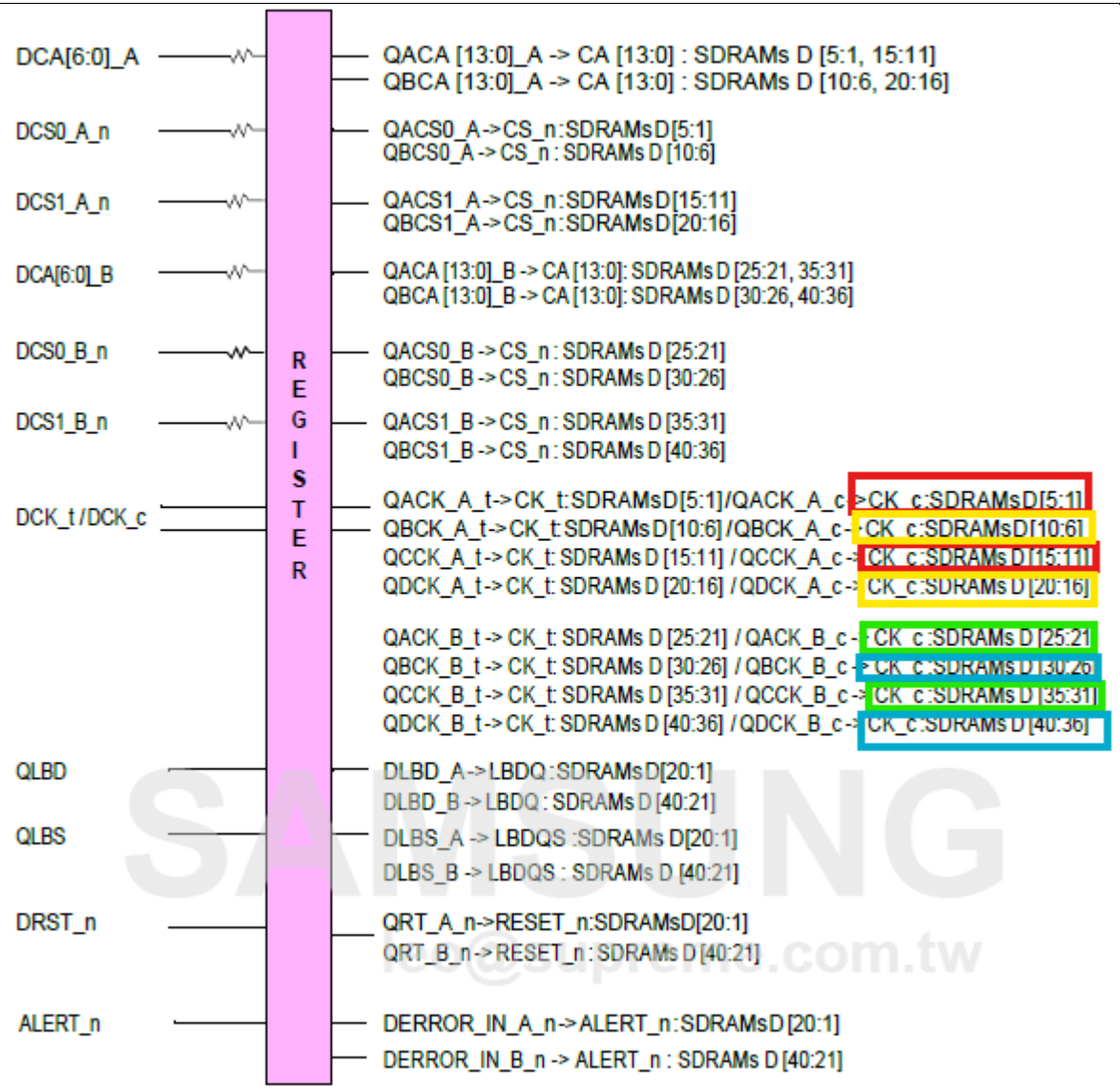
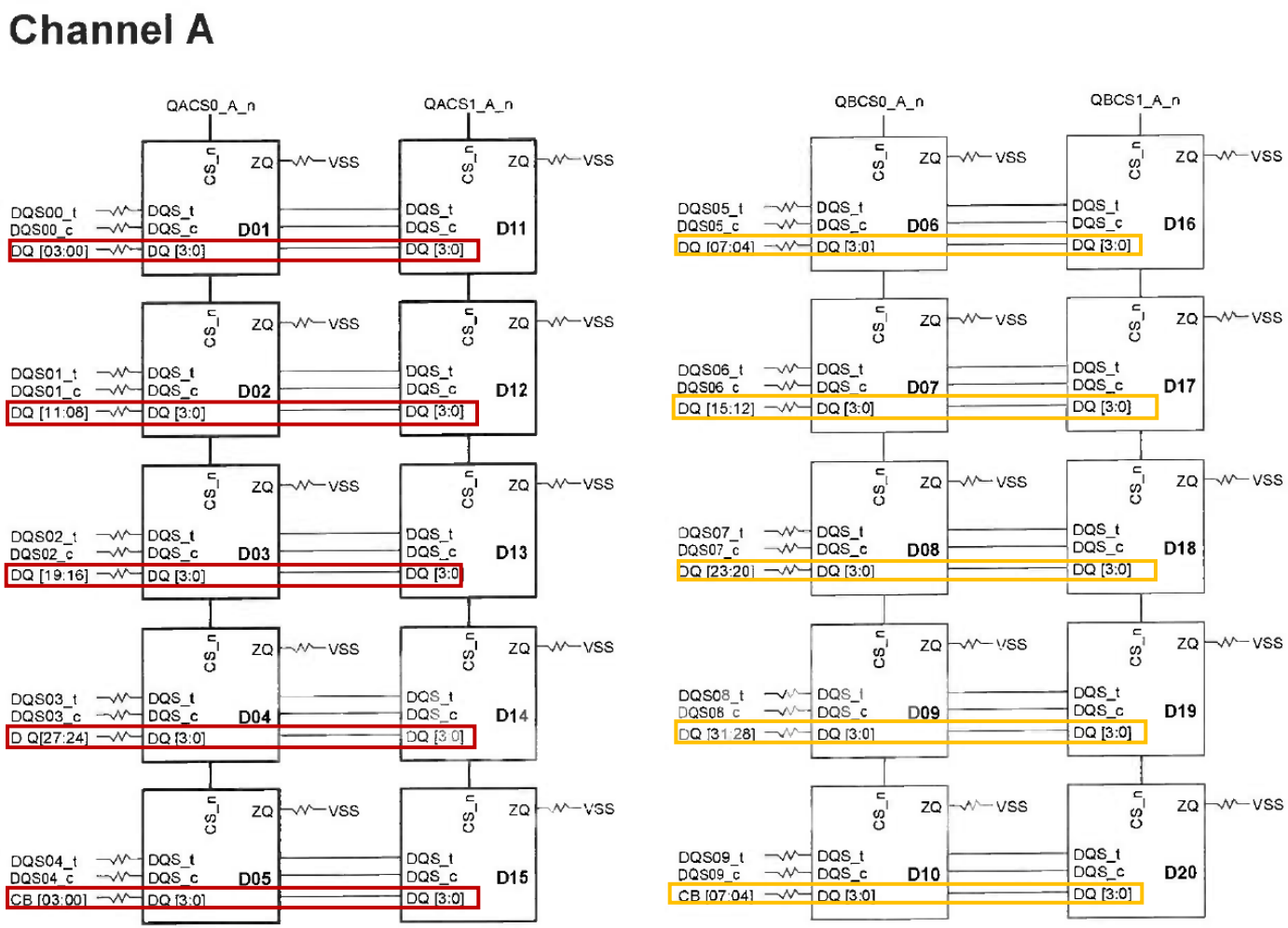
Claim 1	Evidence of Use
	Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet).

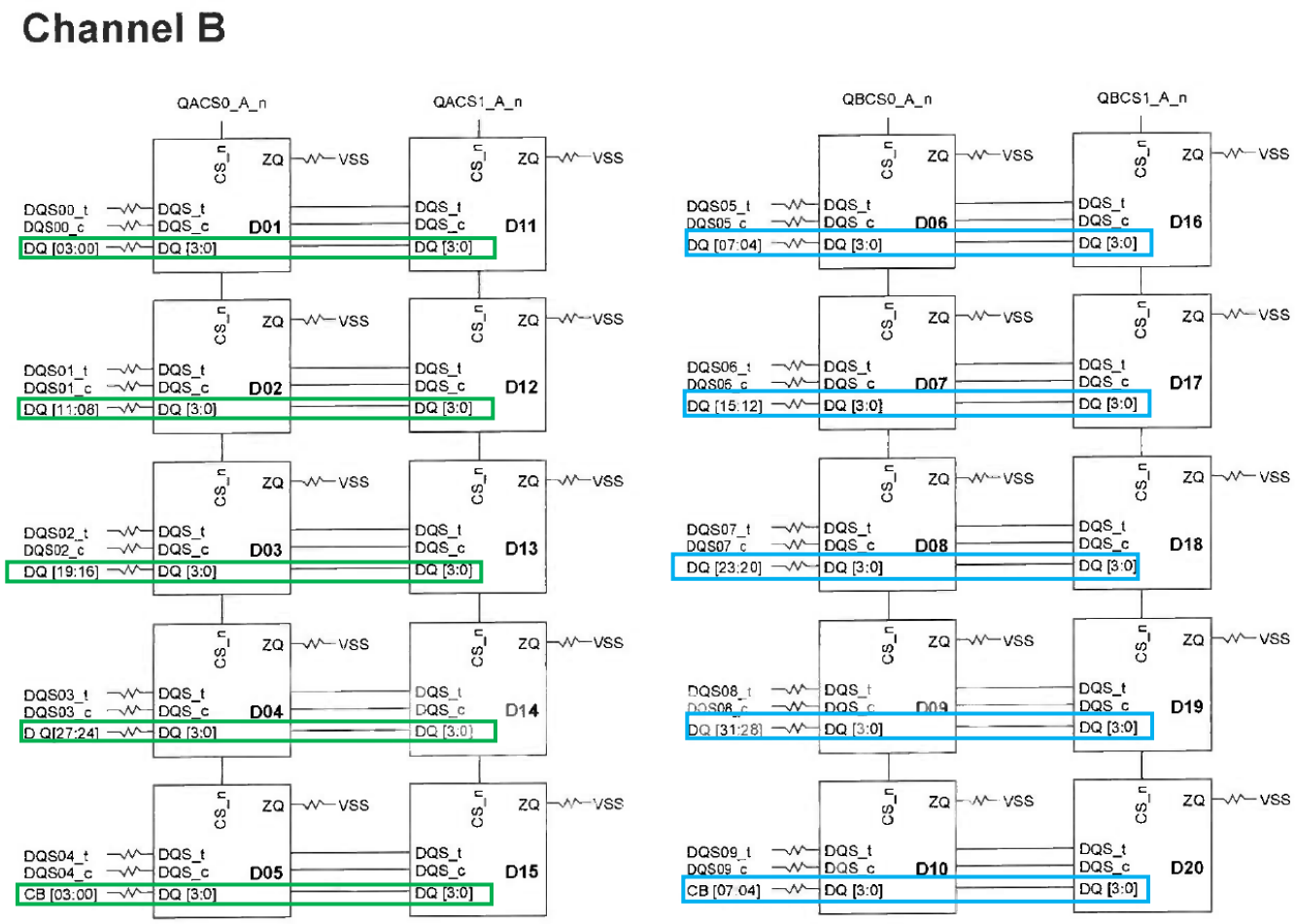


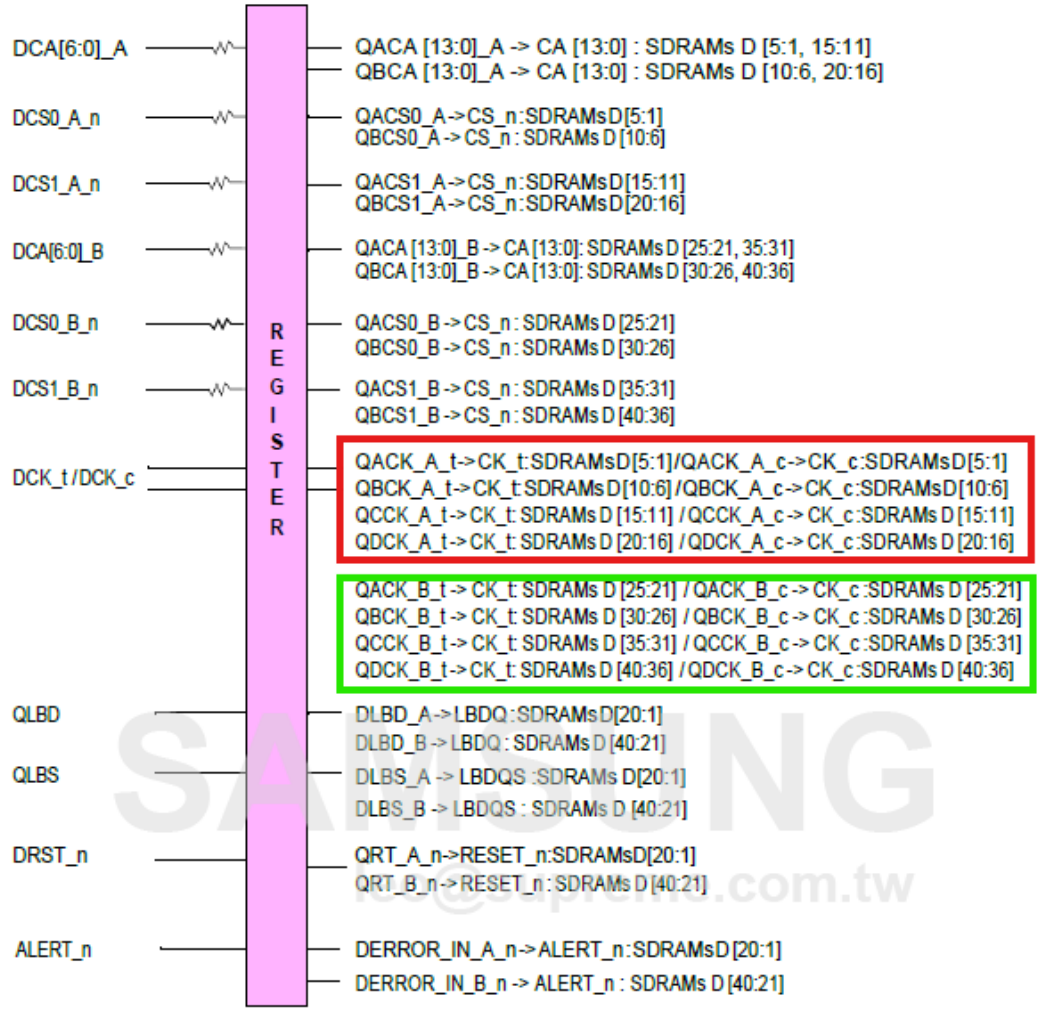
Claim 1	Evidence of Use
	Ex. CC-89 at 30 (Samsung DDR5 RDIMM Datasheet).  Ex. CC-89 at 31 (Samsung DDR5 RDIMM Datasheet).

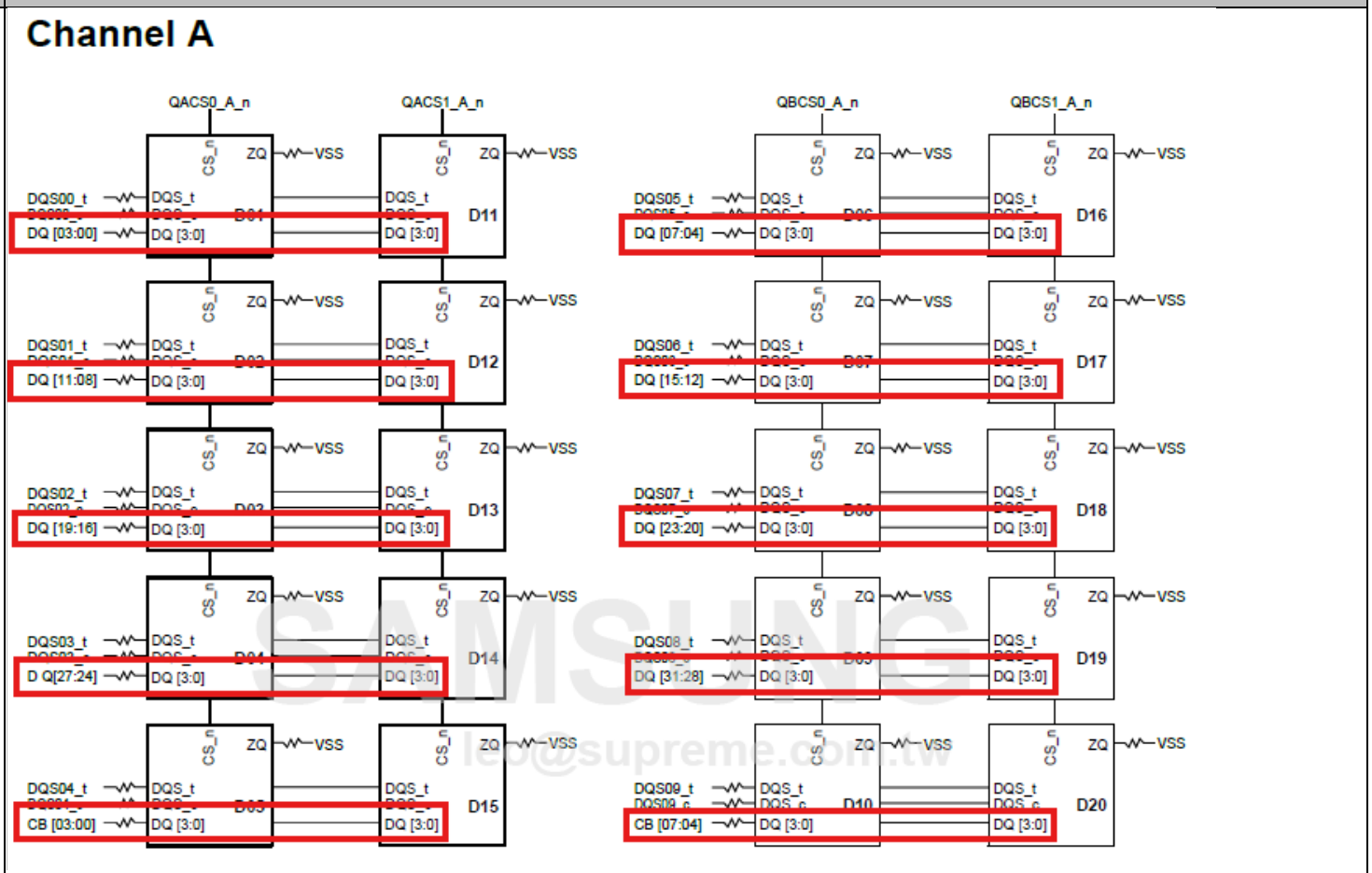
Claim 1	Evidence of Use
	

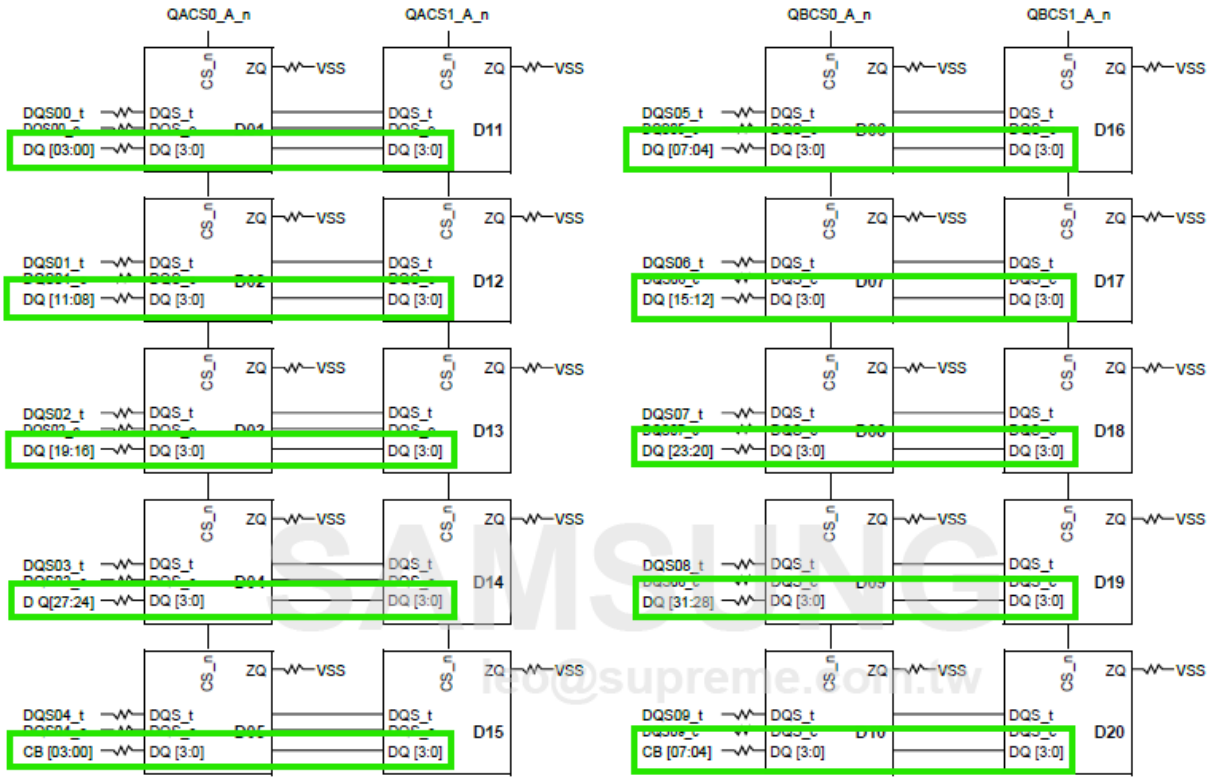

DCA[6:0]_A
DCS0_A_n
DCS1_A_n
DCA[6:0]_B
DCS0_B_n
DCS1_B_n
DCK_t/DCK_c
QLBD
QLBS
DRST_n
ALERT_n
REGISTER
QACA [13:0]_A -> CA [13:0] : SDRAMs D [5:1, 15:11]
QBCA [13:0]_A -> CA [13:0] : SDRAMs D [10:6, 20:16]
QACS0_A->CS_n:SDRAMs D[5:1]
QBCS0_A -> CS_n : SDRAMs D [10:6]
QACS1_A->CS_n:SDRAMs D[15:11]
QBCS1_A->CS_n:SDRAMs D[20:16]
QACA [13:0]_B -> CA [13:0]: SDRAMs D [25:21, 35:31]
QBCA [13:0]_B -> CA [13:0]: SDRAMs D [30:26, 40:36]
QACS0_B -> CS_n : SDRAMs D [25:21]
QBCS0_B -> CS_n : SDRAMs D [30:26]
QACS1_B -> CS_n : SDRAMs D [35:31]
QBCS1_B -> CS_n : SDRAMs D [40:36]
QACK_A_t->CK_t:SDRAMs D[5:1]/QACK_A_c->CK_c:SDRAMs D[5:1]
QBCK_A_t->CK_t:SDRAMs D[10:6]/QBCK_A_c->CK_c:SDRAMs D[10:6]
QCCK_A_t->CK_t: SDRAMs D [15:11] / QCCK_A_c->CK_c:SDRAMs D [15:11]
QDCK_A_t->CK_t: SDRAMs D [20:16] / QDCK_A_c->CK_c:SDRAMs D [20:16]
QACK_B_t -> CK_t: SDRAMs D [25:21] / QACK_B_c -> CK_c:SDRAMs D [25:21]
QBCK_B_t -> CK_t: SDRAMs D [30:26] / QBCK_B_c -> CK_c:SDRAMs D [30:26]
QCCK_B_t -> CK_t: SDRAMs D [35:31] / QCCK_B_c -> CK_c:SDRAMs D [35:31]
QDCK_B_t -> CK_t: SDRAMs D [40:36] / QDCK_B_c -> CK_c:SDRAMs D [40:36]
DLBD_A->LBDQ:SDRAMs D[20:1]
DLBD_B -> LBDQ : SDRAMs D [40:21]
DLBS_A -> LBDQS :SDRAMs D[20:1]
DLBS_B -> LBDQS : SDRAMs D [40:21]
QRT_A_n->RESET_n:SDRAMs D[20:1]
QRT_B_n -> RESET_n : SDRAMs D [40:21]
DERROR_IN_A_n->ALERT_n:SDRAMs D [20:1]
DERROR_IN_B_n -> ALERT_n : SDRAMs D [40:21]

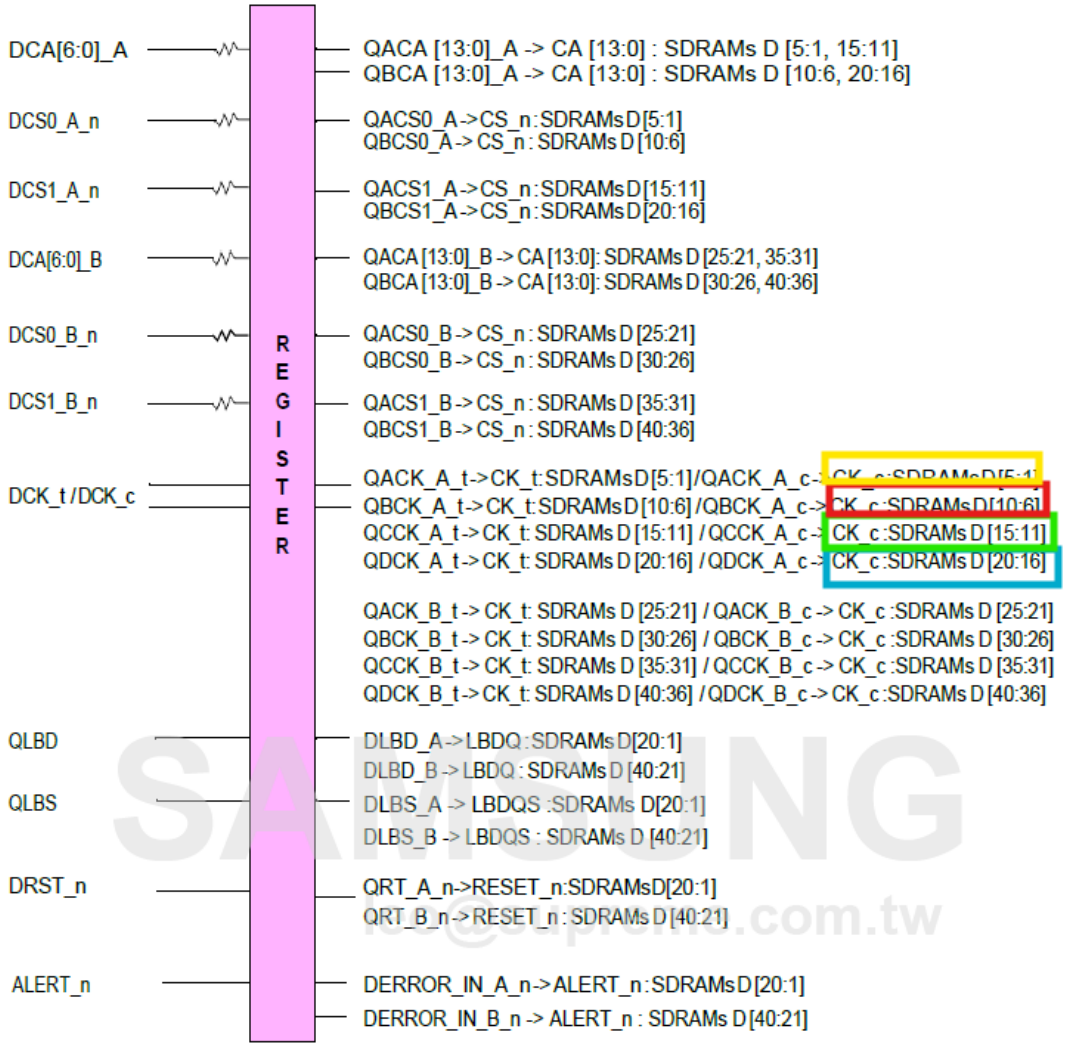
Claim 1	Evidence of Use
	Ex. CC-89 at 33 (Samsung DDR5 RDIMM Datasheet) 

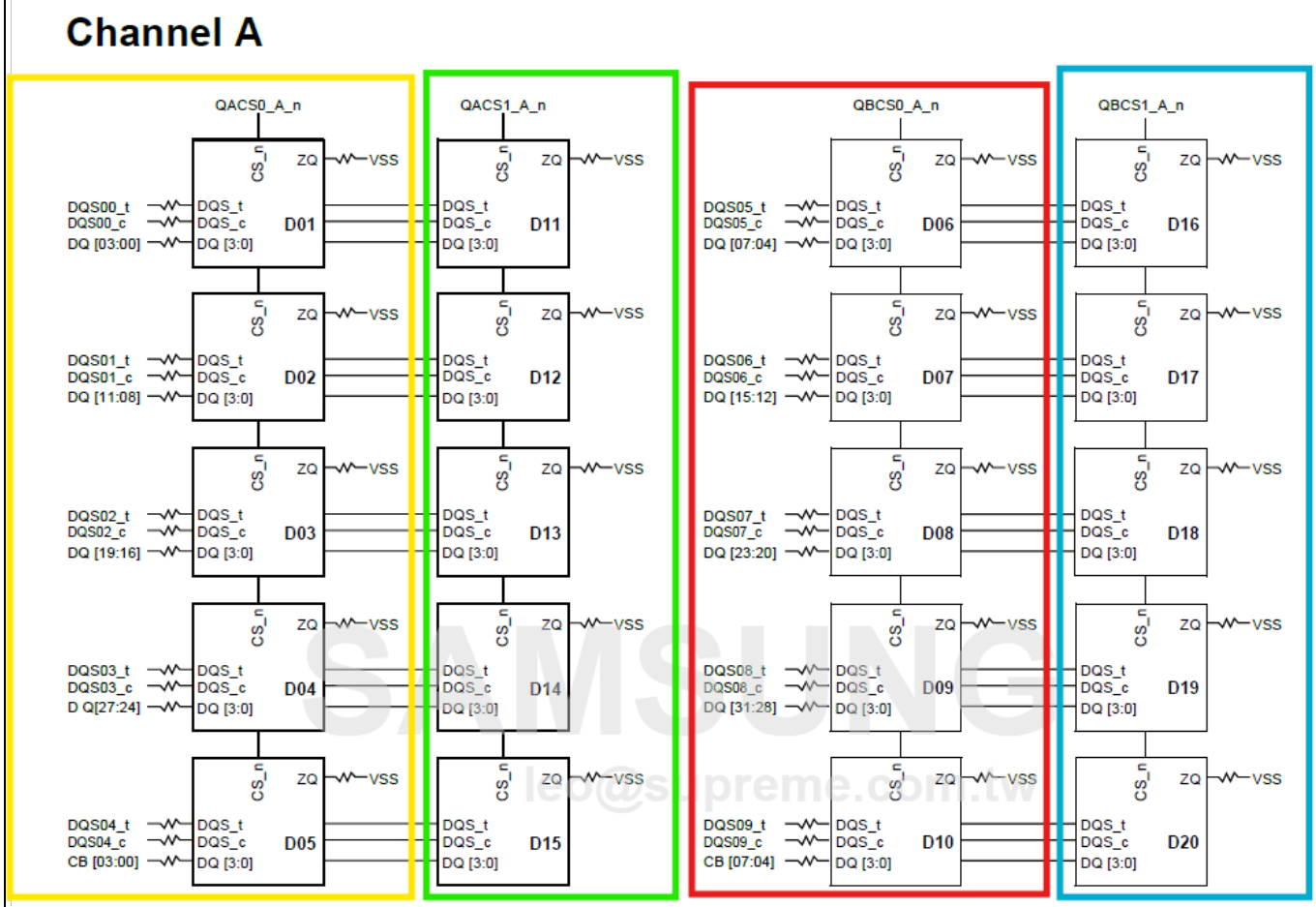
Claim 1	Evidence of Use
	Ex. CC-89 at 34 (Samsung DDR5 RDIMM Datasheet)  Ex. CC-89 at 35 (Samsung DDR5 RDIMM Datasheet)

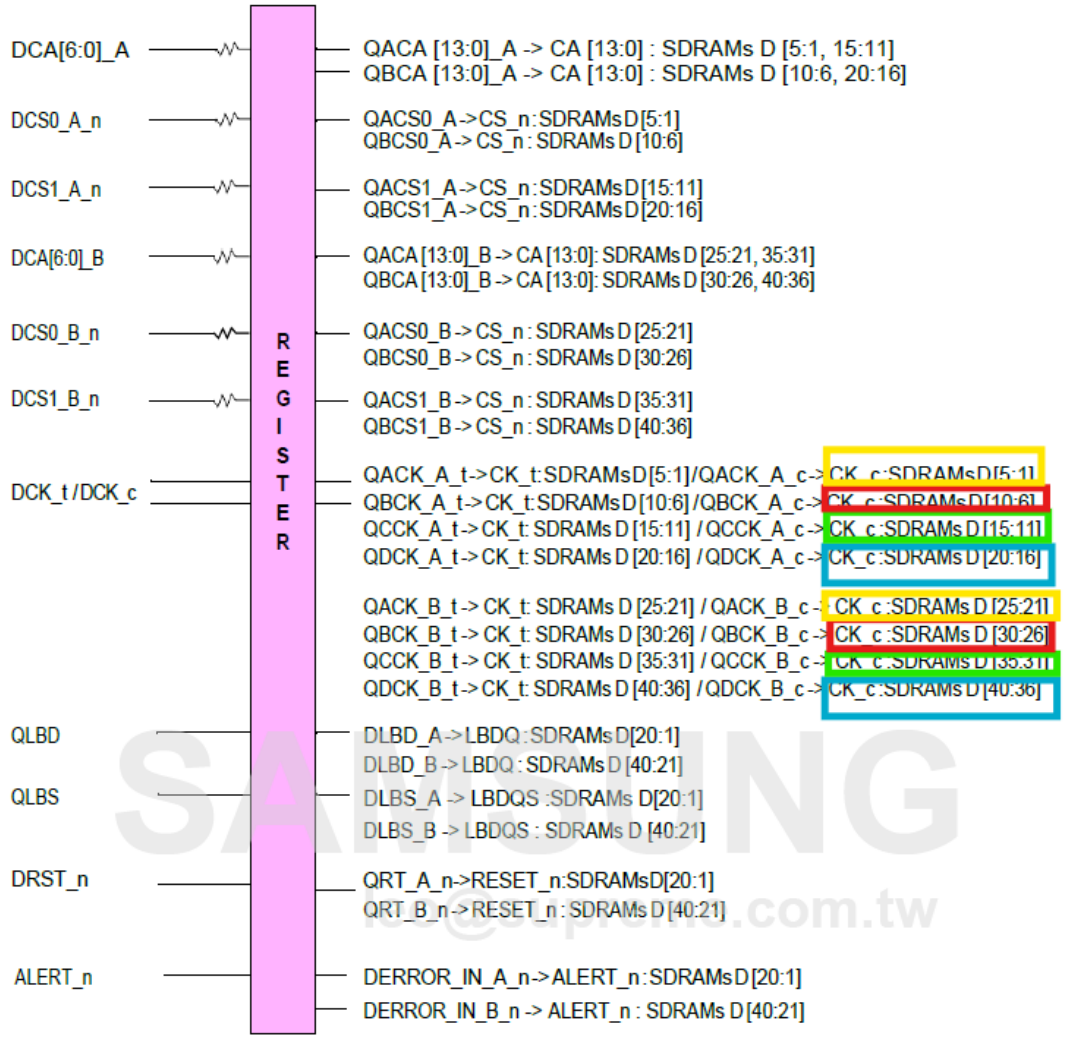
Claim 1	Evidence of Use
	 Ex. CC-89 at 33 (Samsung DDR5 RDIMM Datasheet)

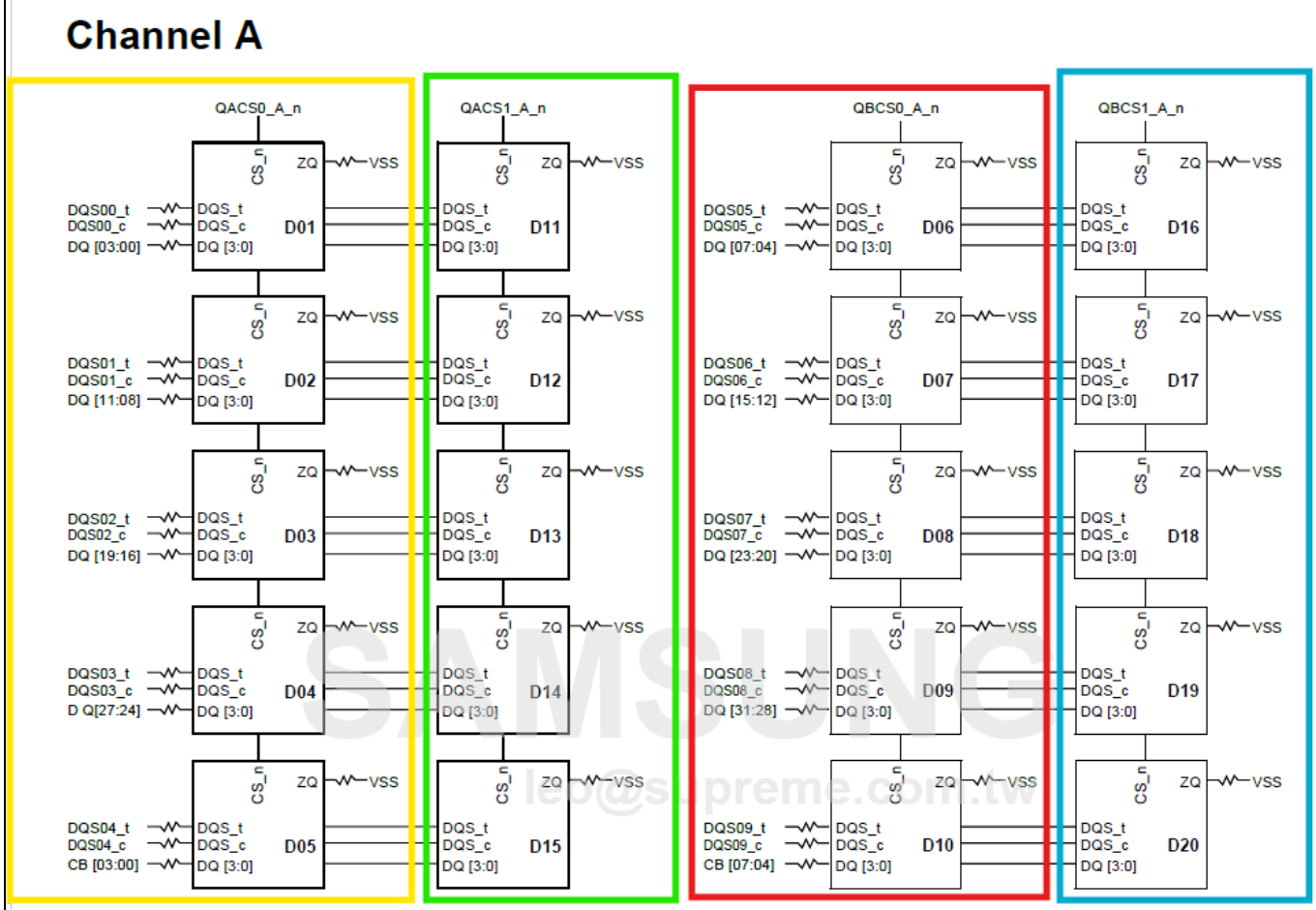
Claim 1	Evidence of Use
	 Ex. CC-89 at 34 (Samsung DDR5 RDIMM Datasheet)

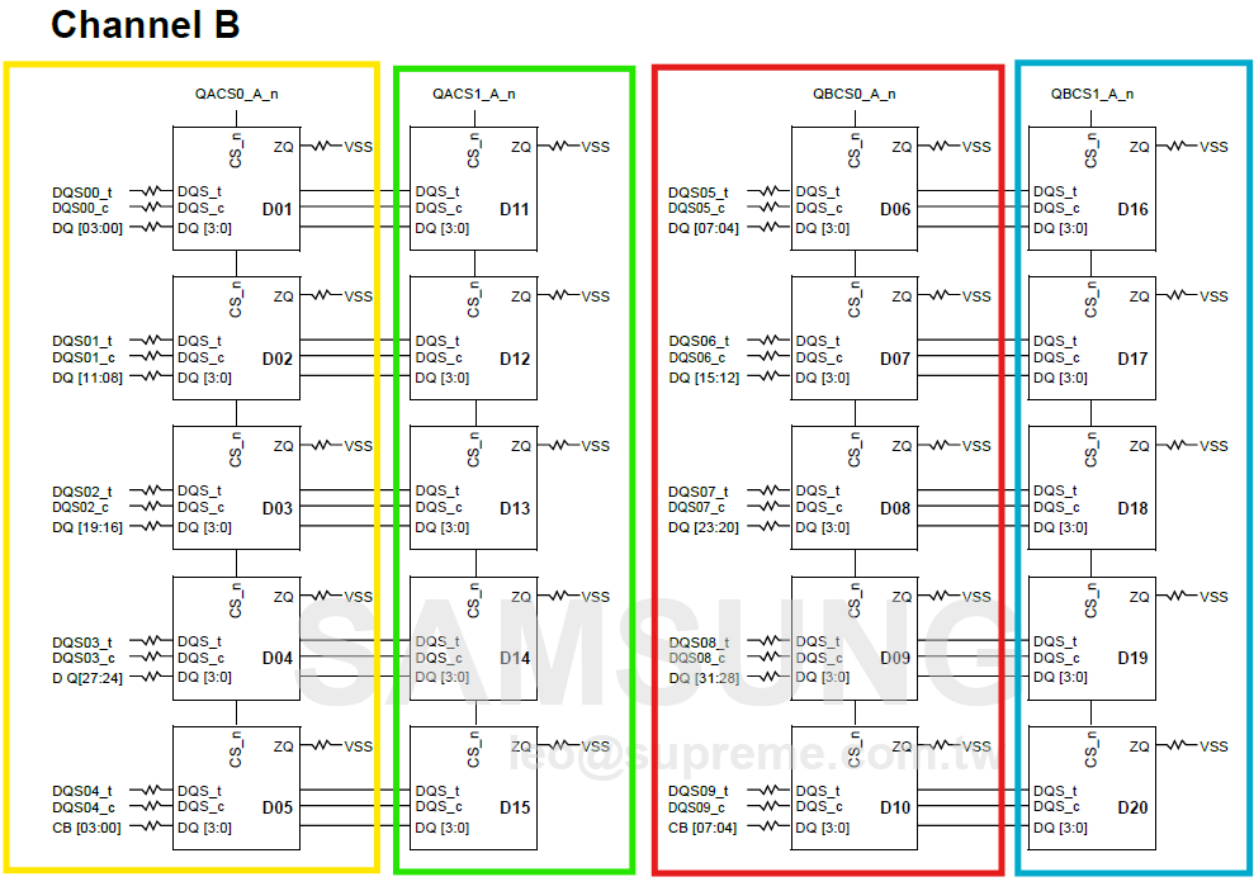
Claim 1	Evidence of Use
	Channel B  Ex. CC-89 at 35 (Samsung DDR5 RDIMM Datasheet)

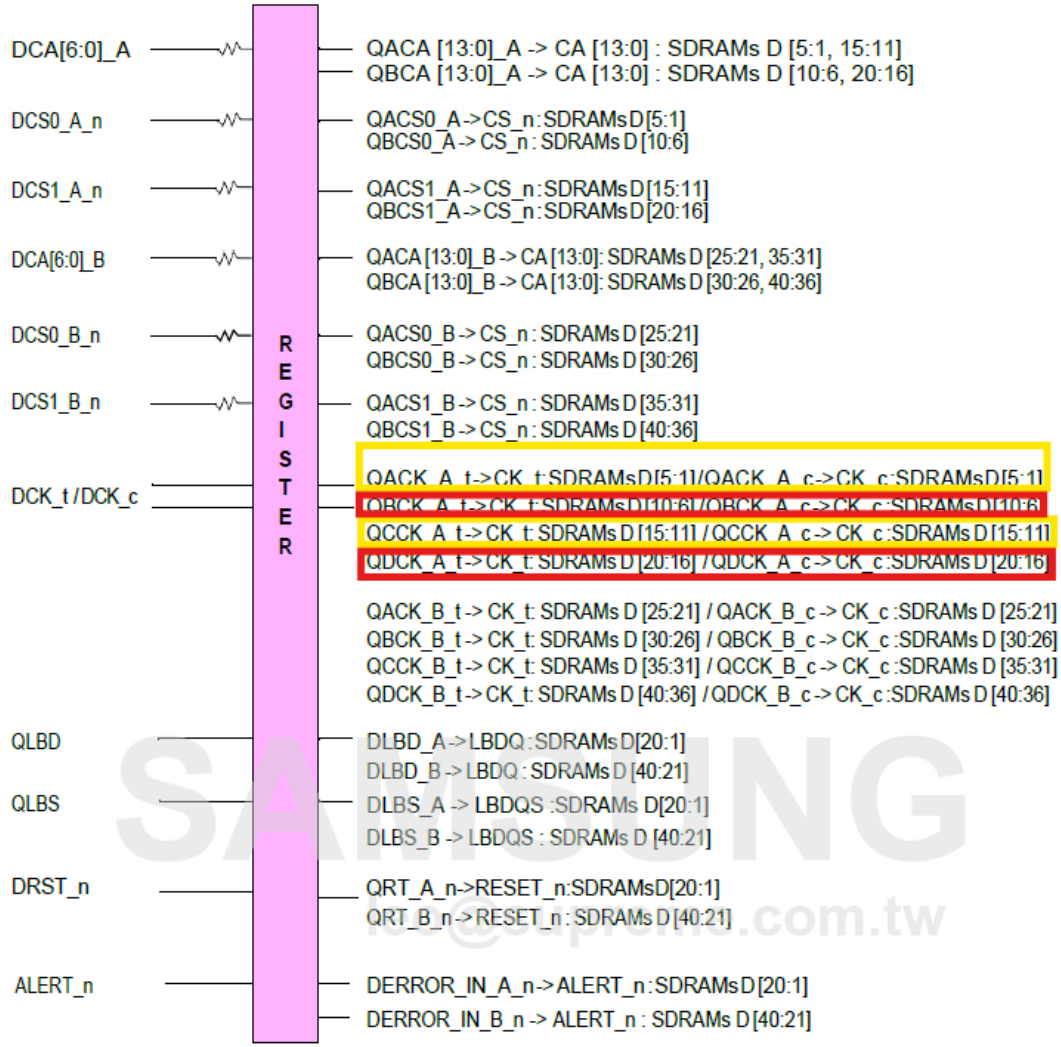
Claim 1	Evidence of Use
	 Ex. CC-89 at 33 (Samsung DDR5 RDIMM Datasheet)

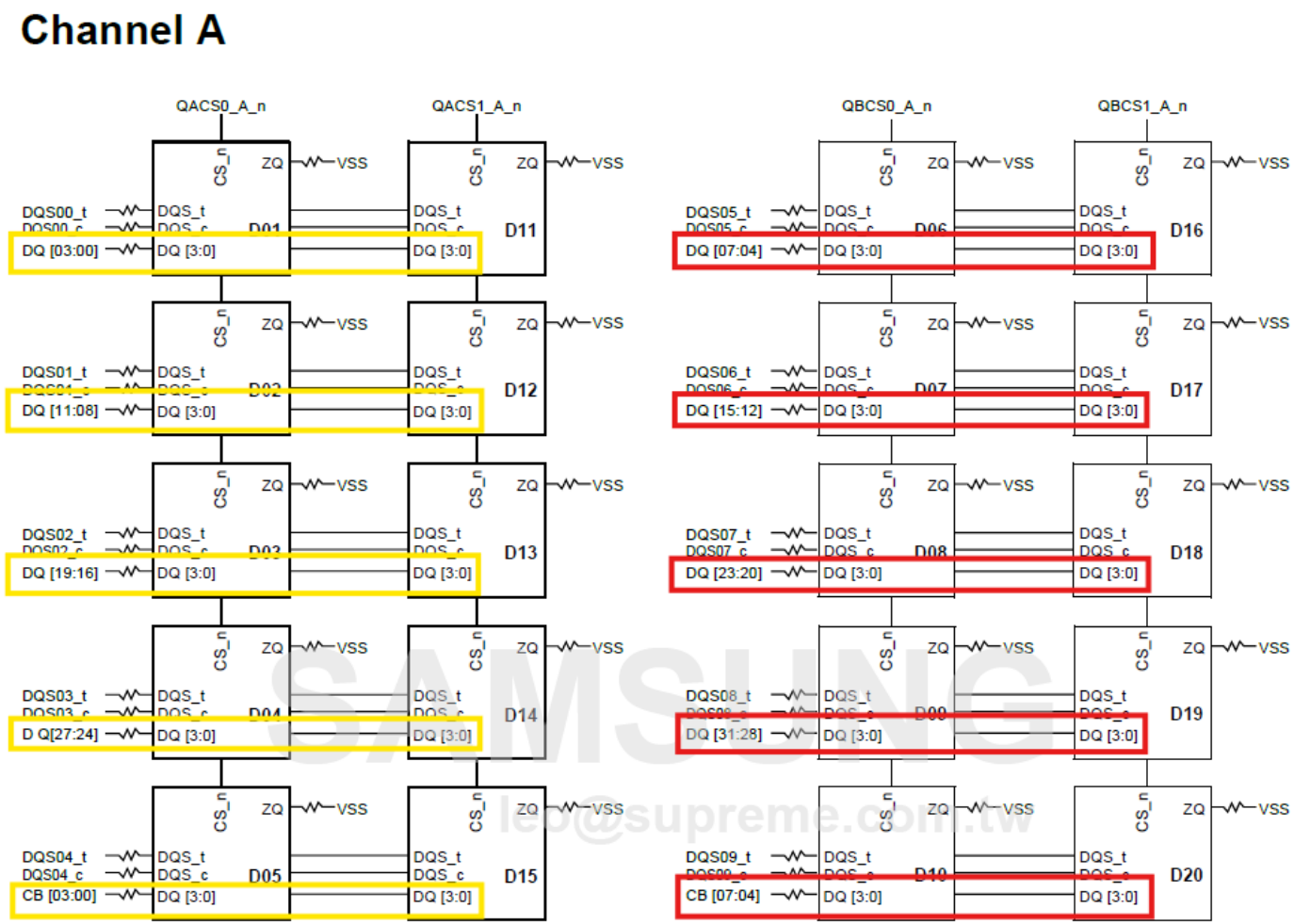
Claim 1	Evidence of Use
	 Ex. CC-89 at 34 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	 Ex. CC-89 at 33 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	 Ex. CC-89 at 34 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	 Ex. CC-89 at 35 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	 Ex. CC-89 at 33 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	 Ex. CC-89 at 33 (Samsung DDR5 RDIMM Datasheet)

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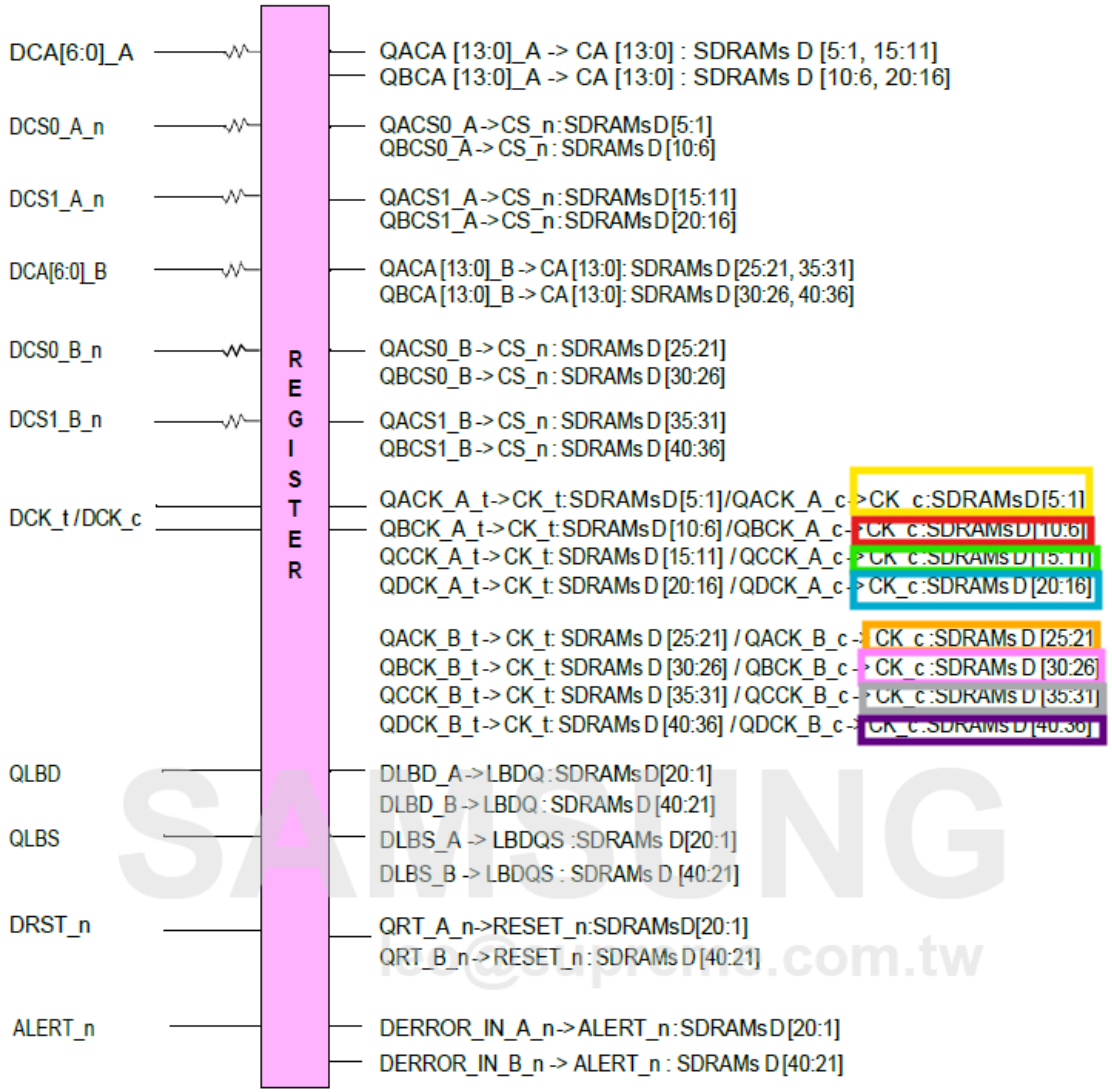
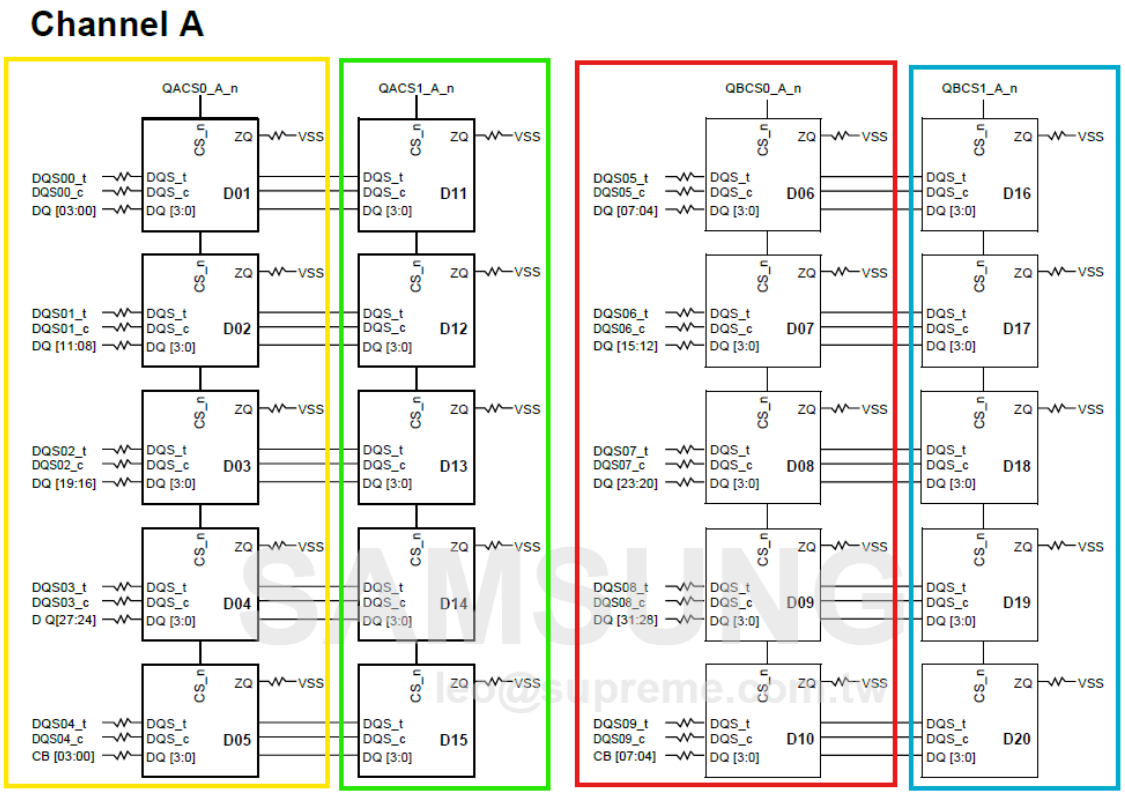
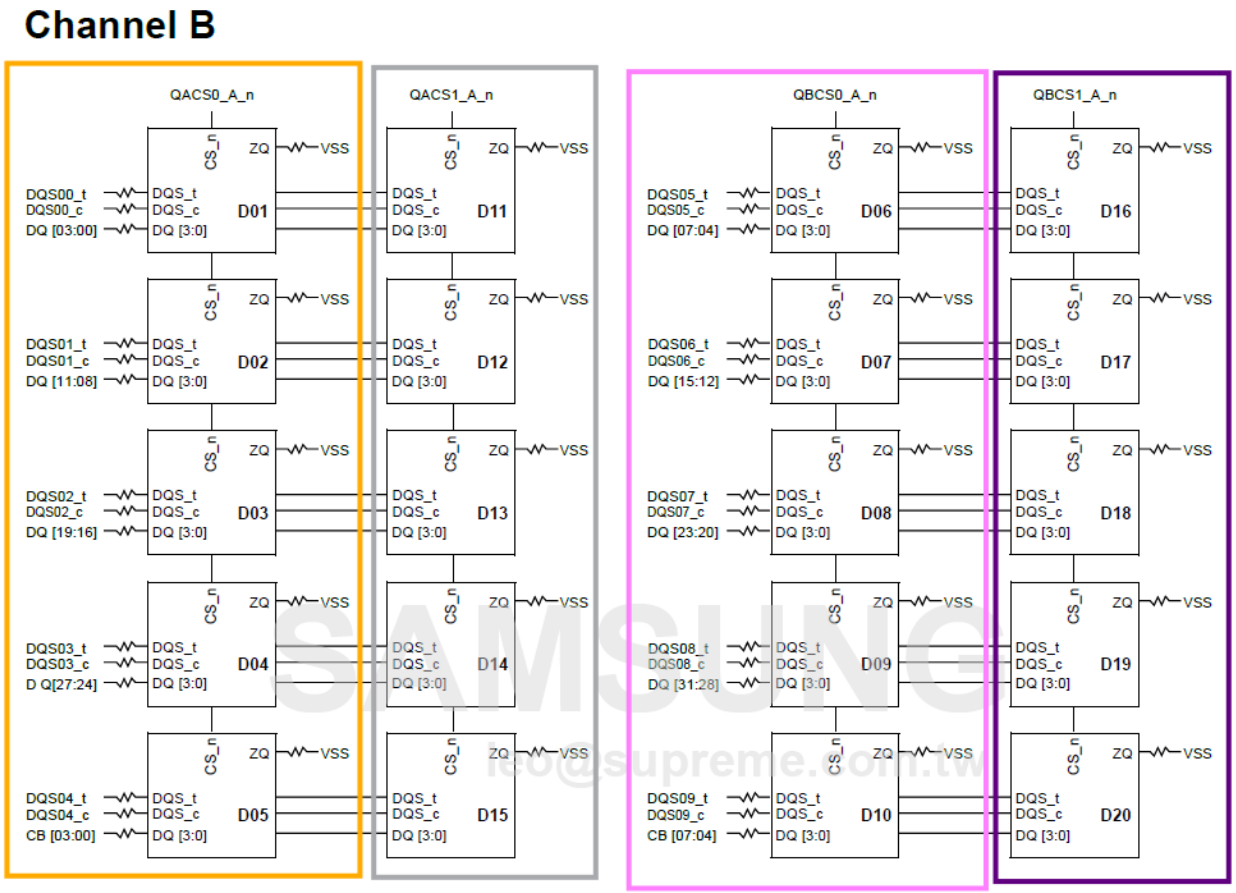
Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	Ex. CC-89 at 31 (Samsung DDR5 RDIMM Datasheet)  Ex. CC-89 at 32 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	 Ex. CC-89 at 33 (Samsung DDR5 RDIMM Datasheet) As explained *supra*, the Samsung Practicing ’407 Products use a JEDEC compliant 288-pin edge connector. The JEDEC DDR5 RDIMM standard further demonstrates the Samsung Practicing ’407 Products’ edge connectors

Claim 1	Evidence of Use
	allow each respective group of the memory devices to be configured to communicate data with the memory controller via a corresponding subset of the data signal lines. *See, e.g.,*

Table 3 — Pin Definitions

Pin Name	Description	Pin Name	Description
CA[6:0]_A CA[6:0]_B	Command and Address (CA) Bus	DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A and B
CS[1:0]_A_n CS[1:0]_B_n	Control (Chip Select) (CS_n)	CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A and B

Ex. CC-88 (JEDEC 305B) at 3 (showing each channel has separate CA Bus and CS commands).

DQ[31:0]_A DQ[31:0]_B	Input/ Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.

Ex. CC-88 (JEDEC 305B) at 4 (showing each channel has separate data lines).

Claim 1	Evidence of Use

6.9.1 DIMM Connectivity Wiring

2Rx4					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Top	Upper	QBCK	QBCS0	QBCA	0
Bottom	Lower	QCCK	QACS1	QACA	1
Bottom	Upper	QDCK	QBCS1	QBCA	1

2Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Top		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]
Bottom	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]

2Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Top	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]
Bottom		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

1Rx4					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QCCK	QBCS0	QACA	0

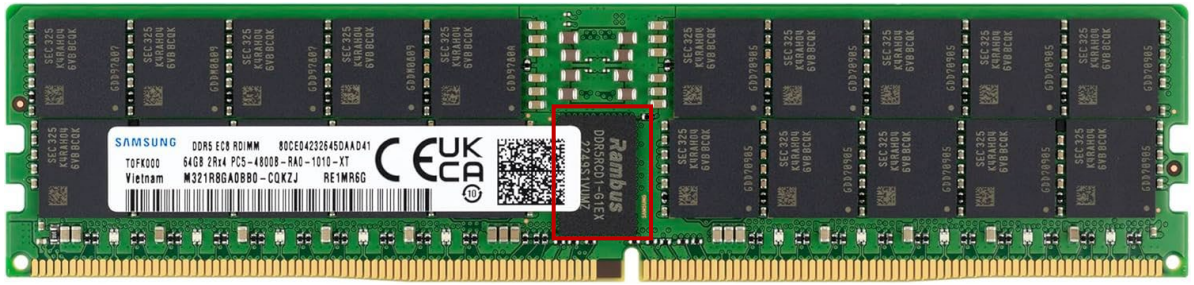
1Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]

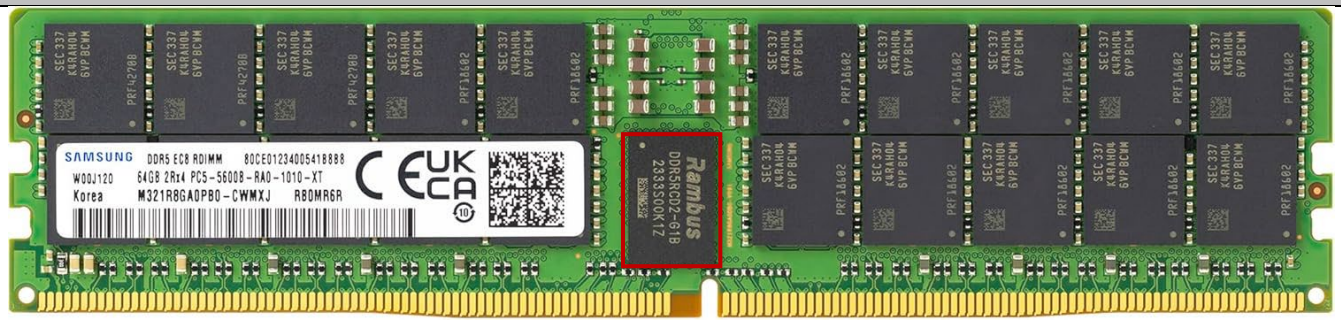
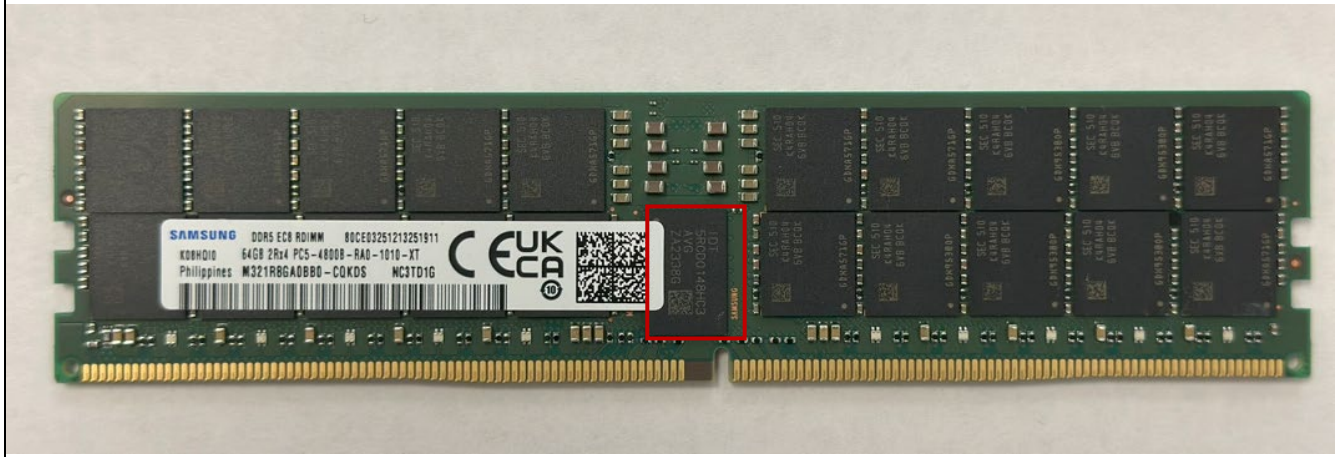
1Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

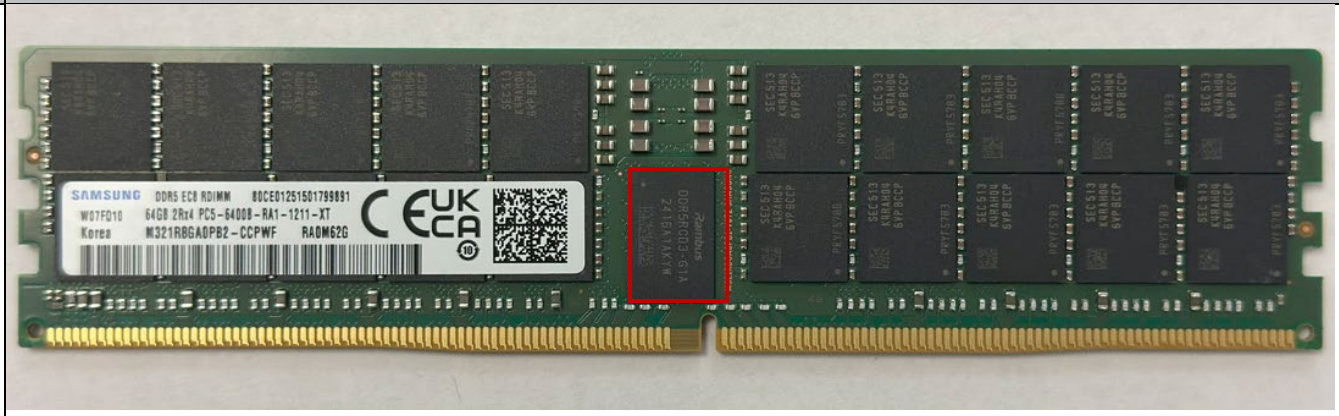
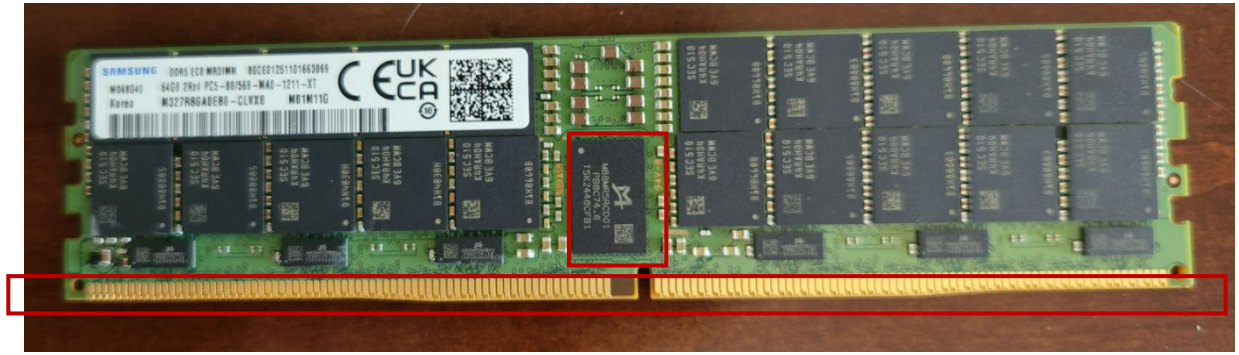
2Rx8					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QCCK	QACS1	QACA	1

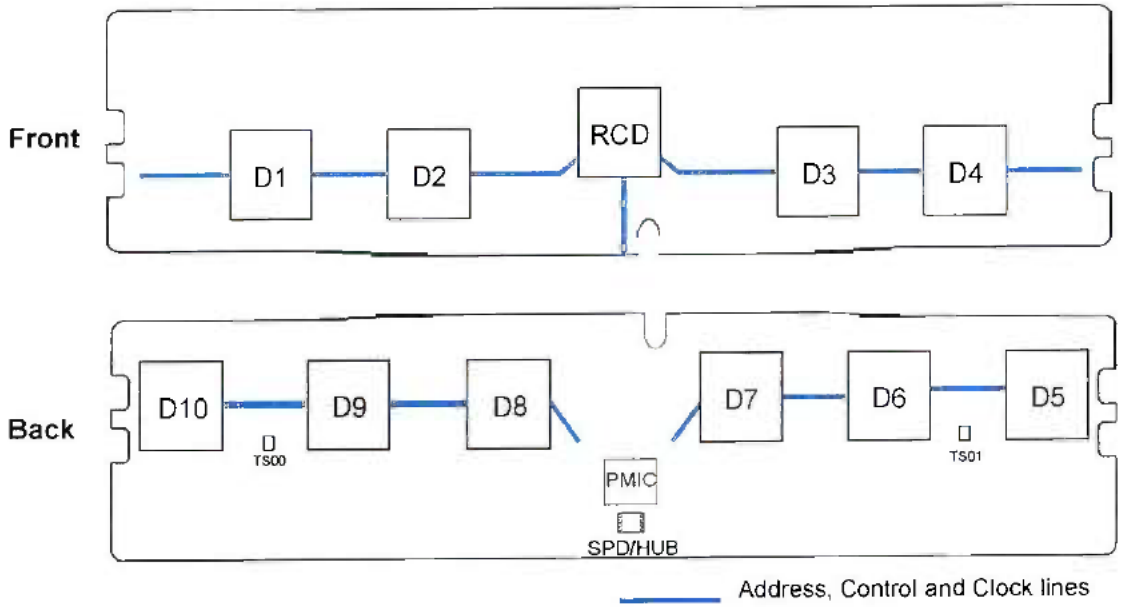
2Rx8 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	
Bottom	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	

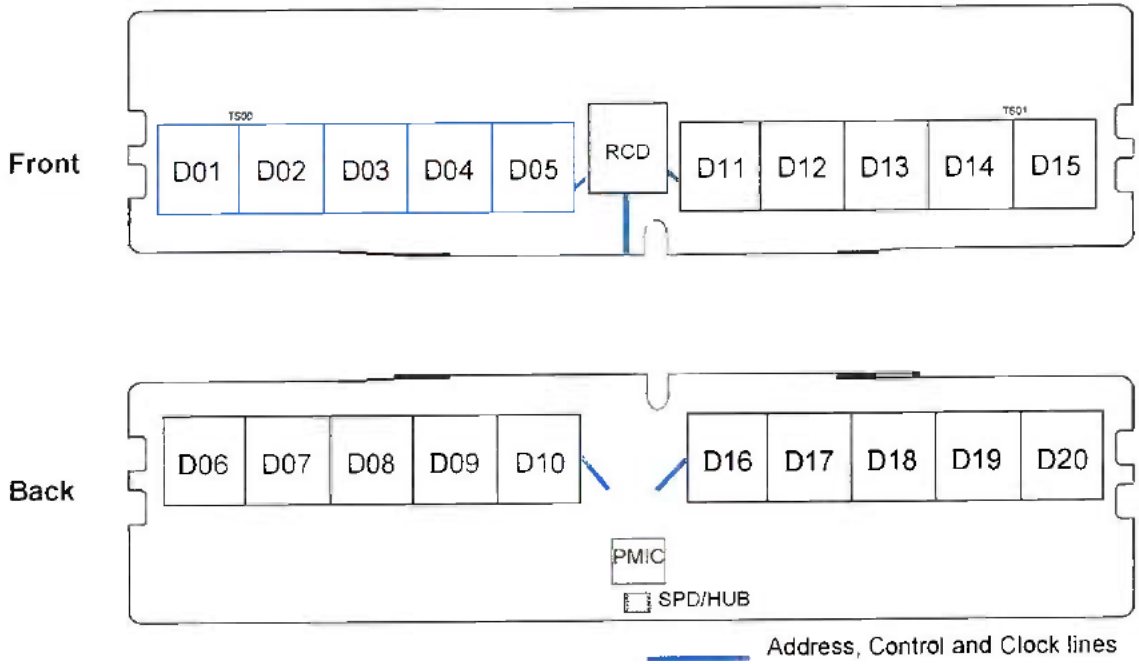
2Rx8 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	
Bottom	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	

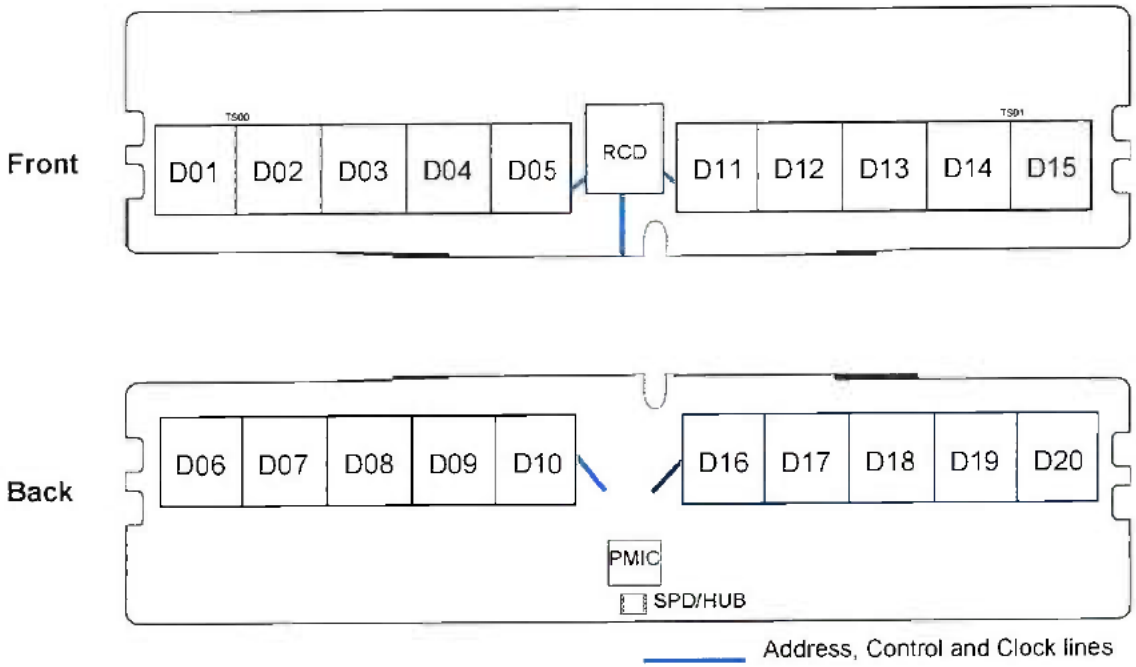
Claim 1	Evidence of Use
	6.9.1 DIMM Connectivity Wiring (cont'd) **1Rx8 (less than 8000 Mbps)** DIMM Side: Row, Clock, CS, CA, Rank Top: Lower, QACK, QACS0, QACA, 0 Bottom: Lower, QACK, QACS0, QACA, 0 **1Rx8 (8000 Mbps and Faster)** DIMM Side: Row, Clock, CS, CA, Rank Top: Lower, QCCK, QACS0, QACA, 0 Bottom: Lower, QCCK, QACS0, QACA, 0 **1Rx8 Sub Channel 0 (Channel A)** Side: DQS0, DQS5, DQS1, DQS6, DQS2, DQS7, DQS3, DQS8, DQS4, DQS9 Nib: Nib 0, Nib 1, Nib 2, Nib 3, Nib 4, Nib 5, Nib 6, Nib 7, Nib 8, Nib 9 Top: [15:8], [31:24] Bottom: [7:0], [23:16], CB[7:0] **1Rx8 Sub Channel 1 (Channel B)** Side: DQS0, DQS5, DQS1, DQS6, DQS2, DQS7, DQS3, DQS8, DQS4, DQS9 Nib: Nib 0, Nib 1, Nib 2, Nib 3, Nib 4, Nib 5, Nib 6, Nib 7, Nib 8, Nib 9 Top: [7:0], [23:16] Bottom: [15:8], [31:24], CB[7:0] **Figure 12 — DIMM Connectivity Wiring** Ex. CC-88 (JEDEC 305B) at 31-32 (showing groups of memory devices on various sides and in various rows on the module configured to receive CA, CS, and data signals via different subsets of CA, CS, and data signal lines).
[**1.c**] circuitry mounted on the PCB and configurable to:	The Samsung Practicing '407 Products each comprise circuitry, such as an RCD, mounted on the PCB. Some examples are shown below, with the RCDs annotated with red boxes:  Ex. ITC-1472 CC-116 (Samsung 4800MHz PC5-38400).

Claim 1	Evidence of Use
	 Ex. ITC-1472 CC-117 (Samsung 5600MHz PC5-44800).  Ex. CC-118 (Samsung 64GB DDR5 PC5-4800 EC8 RDIMM 2Rx4 M321R8GA0BB0-CQK).

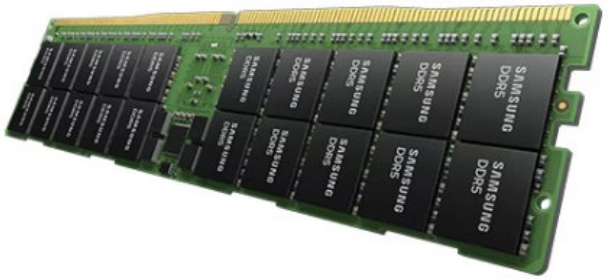
Claim 1	Evidence of Use
	 Ex. CC-119 (Samsung 64GB DDR5 PC5-6400 EC8 RDIMM 2Rx4 M321R8GA0PB2-CCP).  An image of a Samsung MRDIMM M327R8GA0EB0-CLVXB. *See* Ex. CC-111. This is confirmed by a representative datasheet for a Samsung RDIMM:

Claim 1	Evidence of Use
	 Ex. CC-89 at 21 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	 Ex. CC-89 at 25 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	 Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	 Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet)
[**1.c.1**] receive from the memory controller a system clock via the one or more clock signal lines and input control and address (C/A) signals via the C/A signal lines;	The Samsung Practicing '407 Products comprise circuitry mounted on the PCB and configurable to receive from the memory controller a system clock via the one or more clock signal lines and input control and address (C/A) signals via the C/A signal lines. For example, Samsung described its RDIMMs as including "a register [RCD] for enhancing the clock, command and control signals." Ex. CC-95 (Samsung DRAM Modules). This indicates that the register can be configured to receive input clock, control and command signals:

Claim 1	Evidence of Use
	RDIMM **Registered DIMM** Include a register for enhancing the clock, command and control signals Error correction is available by adding 8-bit parity signals Supports x4 / x8 Organization / up to 2 ranks per DIMM and 3DPC configuration Application : Server  The clock signals are received from the system as a system clock via the one or more clock signals, and the control and address (C/A) signals received by the RCD at the host-facing input side are received via the C/A signal lines:

Claim 1	Evidence of Use

[Table 5] PIN Description

Pin Name	Description
CA[6:0]_A CA[6:0]_B	SDRAM Address and Command Bus
CS[1:0]_A CS[1:0]_B	SDRAM Chip Select
PAR_A PAR_B	SDRAM Parity input
CK_t	SDRAM Clocks (true/positive)
CK_c	SDRAM Clocks (complement/negative)
ALERT_n	SDRAM alert for CRC error
RESET_n	Set DRAM to known state
PCAMP	Control and Monitor Port
HSCL	I2C/I3C-Basic Host Sideband Bus Clock
HSDA	I2C/I3C-Basic Host Sideband Bus Data
HSA	I2C/I3C-Basic Host Sideband Bus Address
LBDQ	Loopback data output:

Pin Name	Description
DQ[31:0]_A DQ[31:0]_B	DIMM memory data bus channel A and B
CB[7:0]_A CB[7:0]_B	DIMM ECC check bits(CB) channel A and B
DQS[9:0]_A_t DQS[9:0]_B_t	SDRAM data strobes (positive line of differential pair)
DQS[9:0]_A_c DQS[9:0]_B_c	SDRAM data strobes (negative line of differential pair)
TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
VIN_BULK	DIMM Power Supply from system to PMIC
VIN_MGMT	DIMM Power Supply from system to PMIC
VSS	Power supply return (ground)
RFU	Reserved for future use
LBDQS	Loopback data strobe output

Ex. CC-89 at 9.

[Table 4] PIN Configuration

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VIN_BULK	145	VIN_BULK	50	VSS	194	DQ31_A	96	CB0_B	240	VSS
2	RFU	146	VIN_BULK	51	CB0_A	195	VSS	97	VSS	241	CB2_B
3	VIN_MGMT	147	PWR_GOOD/FAIL_n	52	VSS	196	CB2_A	98	CB1_B	242	VSS
4	SCL	148	SAA	53	CB1_A	197	VSS	99	VSS	243	CB3_B
5	SDA	149	RFU	54	VSS	198	CB3_A	100	DQ0_B	244	VSS
6	VSS	150	RFU	55	DQS4_A_t	199	VSS	101	VSS	245	DQ2_B
7	DQ0_A	151	VSS	56	DQS4_A_c	200	DQS9_A_c,TDQS9_A_c	102	DQ1_B	246	VSS
8	VSS	152	DQ2_A	57	VSS	201	DQS9_A_t,TDQS9_A_t	103	VSS	247	DQ3_B
9	DQ1_A	153	VSS	58	CB4_A	202	VSS	104	DQS0_B_t	248	VSS
10	VSS	154	DQ3_A	59	VSS	203	CB6_A	105	DQS0_B_c	249	DQS5_B_c,TDQS5_B_c
11	DQS0_A_t	155	VSS	60	CB5_A	204	VSS	106	VSS	250	DQS5_B_t,TDQS5_B_t
12	DQS0_A_c	156	DQS5_A_c, TDQS5_A_c	61	VSS	205	CB7_A	107	DQ4_B	251	VSS
13	VSS	157	DQS5_A_t, TDQS5_A_t	62	ALERT_n	206	VSS	108	VSS	252	DQ6_B
14	DQ4_A	158	VSS	63	VSS	207	RESET_n	109	DQ5_B	253	VSS
15	VSS	159	DQ5_A	64	CS0_A_n	208	VSS	110	VSS	254	DQ7_B
16	DQ5_A	160	VSS	65	VSS	209	CS1_A_n	111	DQ8_B	255	VSS
17	VSS	161	DQ7_A	66	CA0_A	210	VSS	112	VSS	256	DQ10_B
18	DQ8_A	162	VSS	67	VSS	211	CA1_A	113	DQ9_B	257	VSS
19	VSS	163	DQ10_A	68	CA2_A	212	VSS	114	VSS	258	DQ11_B
20	DQ9_A	164	VSS	69	VSS	213	CA3_A	115	DQS1_B_t	259	VSS
21	VSS	165	DQ11_A	70	CA4_A	214	VSS	116	DQS1_B_c	260	DQS6_B_c,TDQS6_B_c
22	DQS1_A_t	166	VSS	71	VSS	215	CA5_A	117	VSS	261	DQS6_B_t,TDQS6_B_t
23	DQS1_A_c	167	DQS6_A_c,TDQS6_A_c	72	CA6_A	216	VSS	118	DQ12_B	262	VSS
24	VSS	168	DQS6_A_t,TDQS6_A_t	73	VSS	217	CK_t	119	VSS	263	DQ14_B
25	DQ12_A	169	VSS	74	PAR_A	218	CK_c	120	DQ13_B	264	VSS
26	VSS	170	DQ14_A	75	VSS	219	VSS	121	VSS	265	DQ15_B
27	DQ13_A	171	VSS	KEY				122	DQ16_B	266	VSS
28	VSS	172	DQ15_A					123	VSS	267	DQ18_B
29	DQ16_A	173	VSS					124	DQ17_B	268	VSS
30	VSS	174	DQ18_A	76	CA0_B	220	RFU	125	VSS	269	DQ19_B
31	DQ17_A	175	VSS	77	VSS	221	CA1_B	126	DQS2_B_t	270	VSS
32	VSS	176	DQ19_A	78	CA2_B	222	VSS	127	DQS2_B_c	271	DQS7_B_c,TDQS7_B_c
33	DQS2_A_t	177	VSS	79	VSS	223	CA3_B	128	VSS	272	DQS7_B_t,TDQS7_B_t
34	DQS2_A_c	178	DQS7_A_c,TDQS7_A_c	80	CA4_B	224	VSS	129	DQ20_B	273	VSS
35	VSS	179	DQS7_A_t, TDQS7_A_t	81	VSS	225	CA5_B	130	VSS	274	DQ22_B
36	DQ20_A	180	VSS	82	CA6_B	226	VSS	131	DQ21_B	275	VSS
37	VSS	181	DQ22_A	83	VSS	227	PAR_B	132	VSS	276	DQ23_B
38	DQ21_A	182	VSS	84	CS0_B_n	228	VSS	133	DQ24_B	277	VSS
39	VSS	183	DQ23_A	85	VSS	229	CS1_B_n	134	VSS	278	DQ26_B
40	DQ24_A	184	VSS	86	LBD, RSP_A_n	230	VSS	135	DQ25_B	279	VSS
41	VSS	185	DQ26_A	87	LBS, RSP_B_n	231	RFU	136	VSS	280	DQ27_B
42	DQ25_A	186	VSS	88	VSS	232	RFU	137	DQS3_B_t	281	VSS
43	VSS	187	DQ27_A	89	CB4_B	233	VSS	138	DQS3_B_c	282	DQS8_B_c,TDQS8_B_c
44	DQS3_A_t	188	VSS	90	VSS	234	CB6_B	139	VSS	283	DQS8_B_t,TDQS8_B_t
45	DQS3_A_c	189	DQS8_A_c,TDQS8_A_c	91	CB5_B	235	VSS	140	DQ28_B	284	VSS
46	VSS	190	DQS8_A_t, TDQS8_A_t	92	VSS	236	CB7_B	141	VSS	285	DQ30_B
47	DQ28_A	191	VSS	93	DQS9_B_t, TDQS9_B_t	237	VSS	142	DQ29_B	286	VSS
48	VSS	192	DQ30_A	94	DQS9_B_c,TDQS9_B_c	238	DQS4_B_c	143	VSS	287	DQ31_B
49	DQ29_A	193	VSS	95	VSS	239	DQS4_B_t	144	RFU	288	VSS

Claim 1	Evidence of Use
	Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 6 (illustrating clock signal lines (e.g., “CK_t” and “CK_c”), control/address (C/A) signal lines (e.g., “CA[]_A,” “CA[]_B,” “CS[]_A_n,” and “CS[]_B_n”), and data signal lines (e.g., “DQ[]_A” and “DQ[]_B”)).

Front Side Pin Label	Pin	Pin	Back side Pin Label
VIN_BULK	1	145	VIN_BULK
RFU	2	146	VIN_BULK
VIN_MGMT	3	147	PWR_GOOD/FAIL_n
HSCL	4	148	HSA
HSDA	5	149	RFU
VSS	6	150	RFU
DQ0_A	7	151	VSS
VSS	8	152	DQ2_A
DQ1_A	9	153	VSS
VSS	10	154	DQ3_A
DQS0_A_t	11	155	VSS
DQS0_A_c	12	156	DQS5_A_c, TDQS5_A_c
VSS	13	157	DQS5_A_t, TDQS5_A_t DBI0_A_n
DQ4_A	14	158	VSS
VSS	15	159	DQ6_A
DQ5_A	16	160	VSS
VSS	17	161	DQ7_A
DQ8_A	18	162	VSS
VSS	19	163	DQ10_A
DQ9_A	20	164	VSS
VSS	21	165	DQ11_A
DQS1_A_t	22	166	VSS
DQS1_A_c	23	167	DQS6_A_c, TDQS6_A_c
VSS	24	168	DQS6_A_t, TDQS6_A_t DBI1_A_n
DQ12_A	25	169	VSS
VSS	26	170	DQ14_A
DQ13_A	27	171	VSS
VSS	28	172	DQ15_A
DQ16_A	29	173	VSS
VSS	30	174	DQ18_A
DQ17_A	31	175	VSS
VSS	32	176	DQ19_A
DQS2_A_t	33	177	VSS
DQS2_A_c	34	178	DQS7_A_c, TDQS7_A_c
VSS	35	179	DQS7_A_t, TDQS7_A_t DBI2_n
DQ20_A	36	180	VSS
VSS	37	181	DQ22_A
DQ21_A	38	182	VSS

Front Side Pin Label	Pin	Pin	Back side Pin Label
PAR_A	74	218	CK_c
V33	75	219	V33
	Key		
CA0_B	76	220	RFU
VSS	77	221	CA1_B
CA2_B	78	222	VSS
VSS	79	223	CA3_B
CA4_B	80	224	VSS
VSS	81	225	CA5_B
CA6_B	82	226	VSS
VSS	83	227	PAR_B
CS0_B_n	84	228	VSS
VSS	85	229	CS1_B_n
LBD, RSP_A_n	86	230	VSS
LBS, RSP_B_n	87	231	RFU
VSS	88	232	RFU
CB4_B	89	233	VSS
VSS	90	234	CB6_B
CB5_B	91	235	VSS
VSS	92	236	CB7_B
DQS9_B_t, TDQS9_B_t DBI4_B_n	93	237	VSS
DQS9_B_c, TDQS9_B_c	94	238	DQS4_B_c
VSS	95	239	DQS4_B_t
CB0_B	96	240	VSS
V33	97	241	CB2_B
CB1_B	98	242	VSS
VSS	99	243	CB3_B
DQ0_B	100	244	VSS
VSS	101	245	DQ2_B
DQ1_B	102	246	VSS
VSS	103	247	DQ3_BDQ3_B
DQS0_B_t	104	248	VSS
DQS0_B_c	105	249	DQS5_B_c, TDQS5_B_c
VSS	106	250	DQS5_B_t, TDQS5_B_t DBI0_B_n
DQ4_B	107	251	VSS
VSS	108	252	DQ6_B
DQ5_B	109	253	VSS

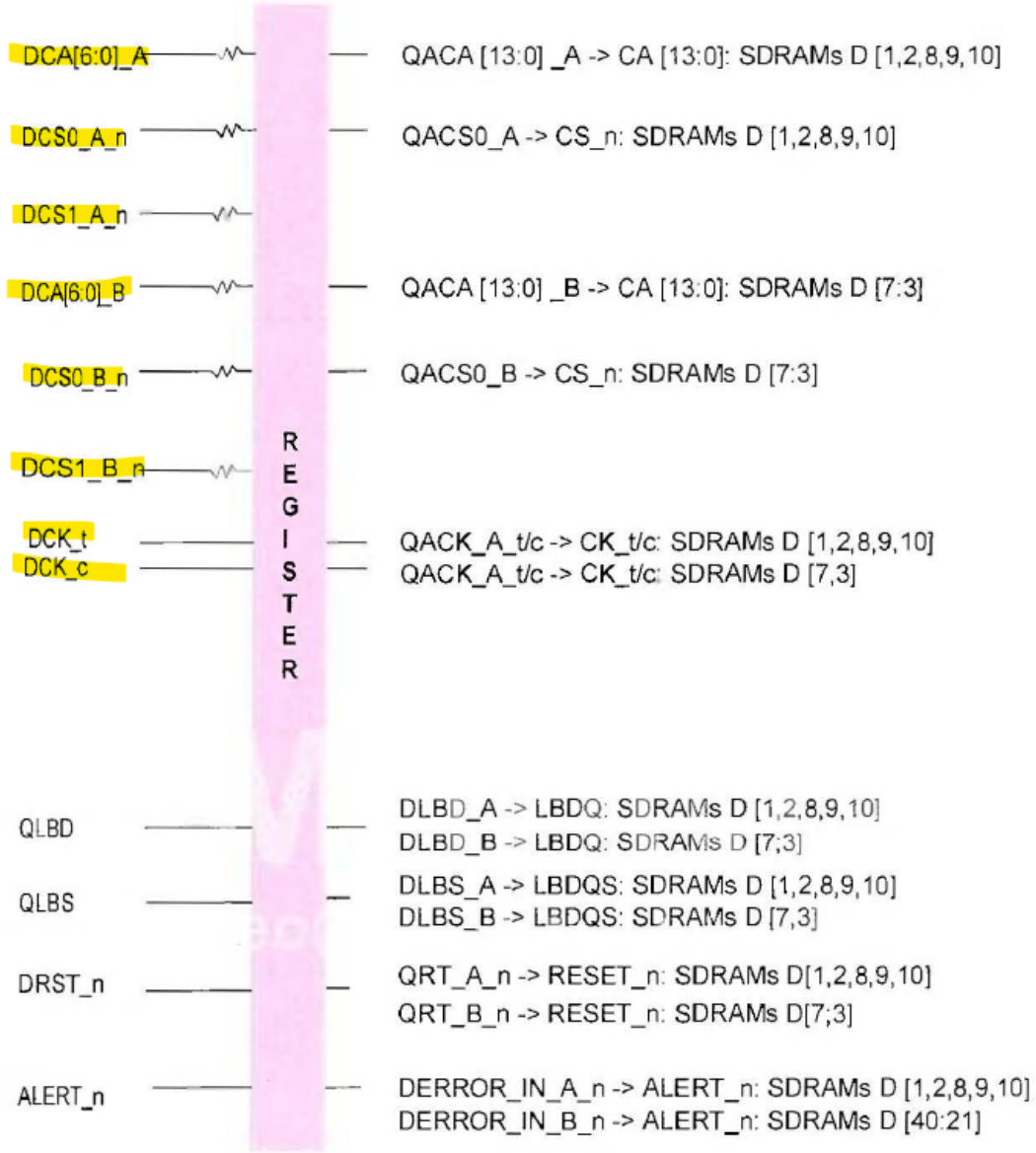
Claim 1	Evidence of Use

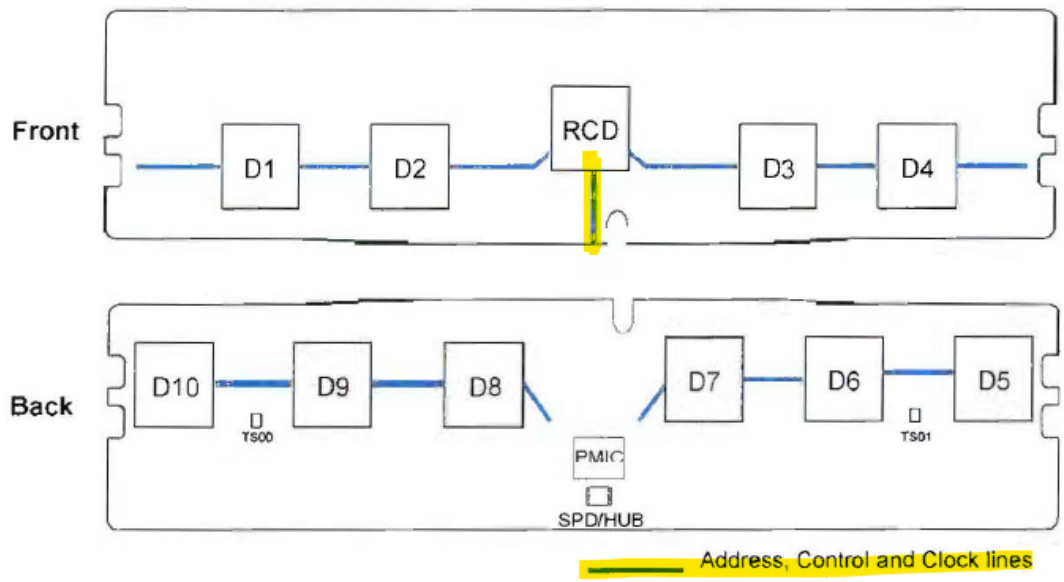
Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	39	183	DQ23_A
DQ24_A	40	184	V33
VSS	41	185	DQ26_A
DQ25_A	42	186	VSS
VSS	43	187	DQ27_A
DQS3_A_t	44	188	VSS
DQS3_A_c	45	189	DQS8_A_c, TDQS8_A_c
VSS	46	190	DQS8_A_t, TDQS8_A_t DBI3_A_n
DQ28_A	47	191	VSS
VSS	48	192	DQ30_A
DQ29_A	49	193	VSS
VSS	50	194	DQ31_A
CB0_A	51	195	VSS
VSS	52	196	CB2_A
CB1_A	53	197	VSS
VSS	54	198	CB3_A
DQS4_A_t	55	199	VSS
DQS4_A_c	56	200	DQS9_A_c, TDQS9_A_c
VSS	57	201	DQS9_A_t, TDQS9_A_t DBI4_A_n
CB4_A	58	202	VSS
VSS	59	203	CB6_A
CB5_A	60	204	VSS
VSS	61	205	CB7_A
ALERT_n	62	206	VSS
VSS	63	207	RESET_n
CS0_A_n	64	208	VSS
VSS	65	209	CS1_A_n
CA0_A	66	210	VSS
VSS	67	211	CA1_A
CA2	68	212	VSS
VSS	69	213	CA3_A
CA4_A	70	214	VSS
VSS	71	215	CA5_A
CA6_A	72	216	VSS
VSS	73	217	CK_t

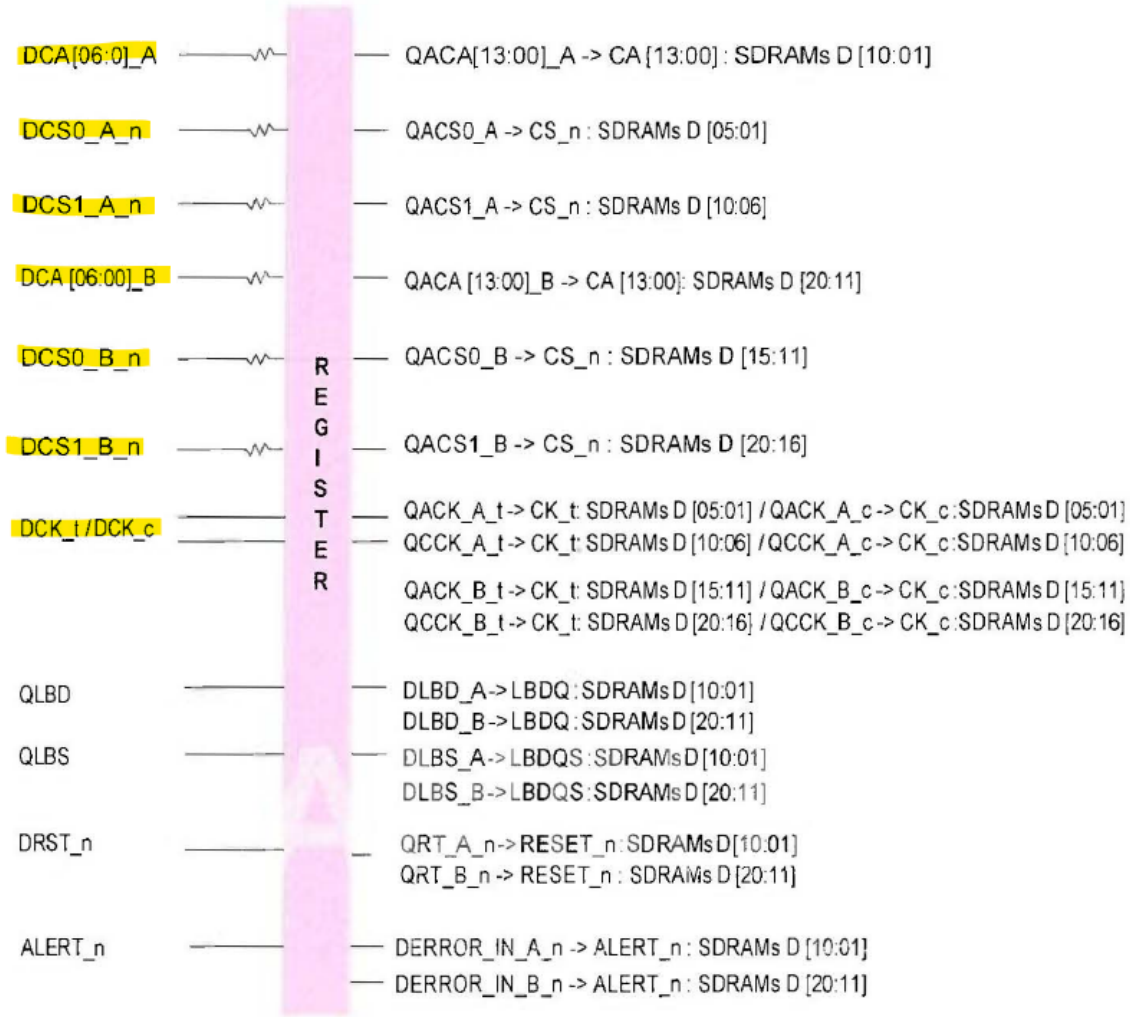
Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	110	254	DQ7_B
DQ8_B	111	255	VSS
VSS	112	256	DQ10_B
DQ9_B	113	257	VSS
VSS	114	258	DQ11_B
DQS1_B_t	115	259	VSS
DQS1_B_c	116	260	DQS6_B_c, TDQS6_B_c
VSS	117	261	DQS6_B_t, TDQS6_B_t DBI1_B_n
DQ12_B	118	262	VSS
VSS	119	263	DQ14_B
DQ13_B	120	264	VSS
VSS	121	265	DQ15_B
DQ16_B	122	266	VSS
VSS	123	267	DQ18_B
DQ17_B	124	268	VSS
VSS	125	269	DQ19_B
DQS2_B_t	126	270	V33
DQS2_B_c	127	271	DQS7_B_c, TDQS7_B_c
VSS	128	272	DQS7_B_t, TDQS7_B_t DBI2_B_n
DQ20_B	129	273	VSS
VSS	130	274	DQ22_B
DQ21_B	131	275	VSS
VSS	132	276	DQ23_B
DQ24_B	133	277	VSS
VSS	134	278	DQ26_B
DQ25_B	135	279	VSS
VSS	136	280	DQ27_B
DQS3_B_t	137	281	VSS
DQS3_B_c	138	282	DQS8_B_c, TDQS8_B_c
VSS	139	283	DQS8_B_t, TDQS8_B_t DBI3_B_n
DQ28_B	140	284	VSS
VSS	141	285	DQ30_B
DQ29_B	142	286	VSS
VSS	143	287	DQ31_B
RFU	144	288	VSS

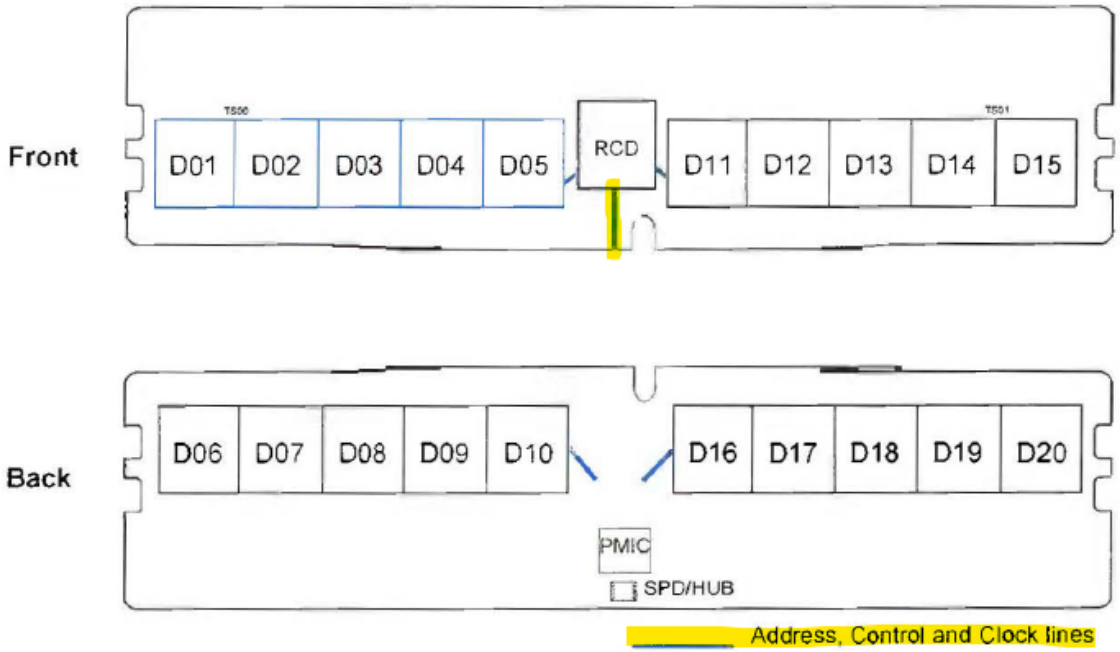
Figure 1. Wiring Assignments

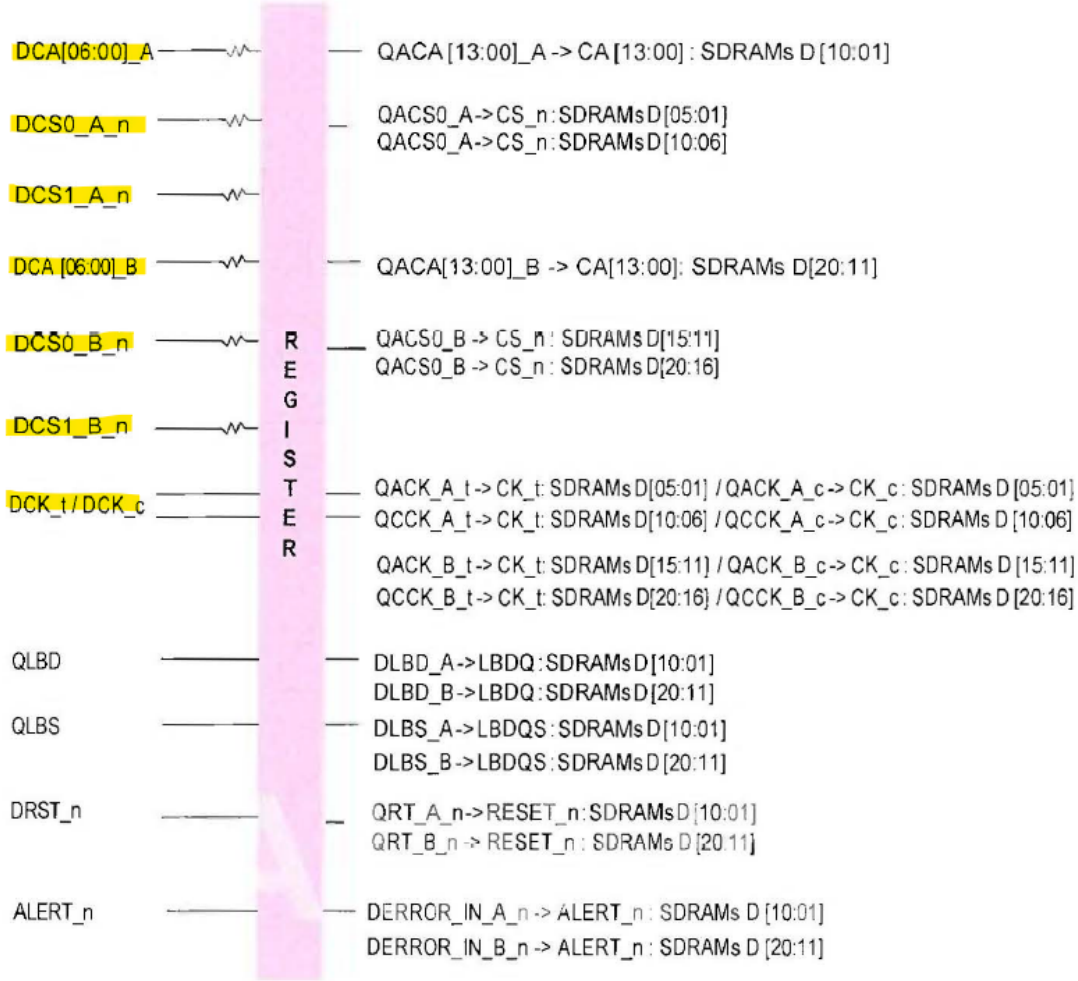
Claim 1	Evidence of Use
	Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 7-8 (illustrating clock signal lines (e.g., “CK_t” and “CK_c”), control/address (C/A) signal lines (e.g., “CA[]_A,” “CA[]_B,” “CS[]_A_n,” and “CS[]_B_n”), and data signal lines (e.g., “DQ[]_A” and “DQ[]_B”)).

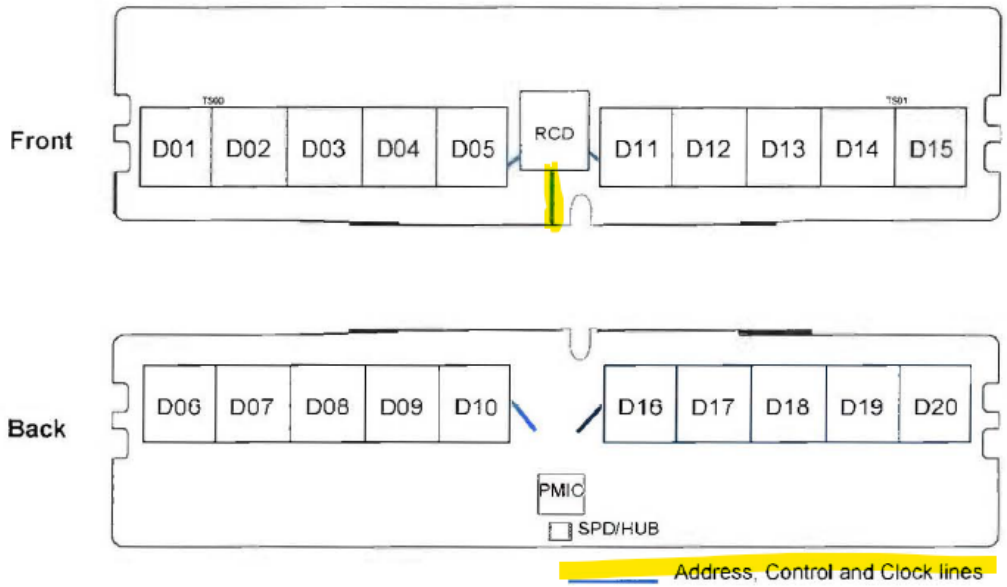

DCA[6:0]_A
DCS0_A_n
DCS1_A_n
DCA[6:0]_B
DCS0_B_n
DCS1_B_n
DCK_t
DCK_c
REGISTER
QACA [13:0] _A -> CA [13:0]: SDRAMs D [1,2,8,9,10]
QACS0_A -> CS_n: SDRAMs D [1,2,8,9,10]
QACA [13:0] _B -> CA [13:0]: SDRAMs D [7:3]
QACS0_B -> CS_n: SDRAMs D [7:3]
QACK_A_t/c -> CK_t/c: SDRAMs D [1,2,8,9,10]
QACK_A_t/c -> CK_t/c: SDRAMs D [7,3]
QLBD
QLBS
DRST_n
ALERT_n
DLBD_A -> LBDQ: SDRAMs D [1,2,8,9,10]
DLBD_B -> LBDQ: SDRAMs D [7;3]
DLBS_A -> LBDQS: SDRAMs D [1,2,8,9,10]
DLBS_B -> LBDQS: SDRAMs D [7,3]
QRT_A_n -> RESET_n: SDRAMs D[1,2,8,9,10]
QRT_B_n -> RESET_n: SDRAMs D[7;3]
DERROR_IN_A_n -> ALERT_n: SDRAMs D [1,2,8,9,10]
DERROR_IN_B_n -> ALERT_n: SDRAMs D [40:21]

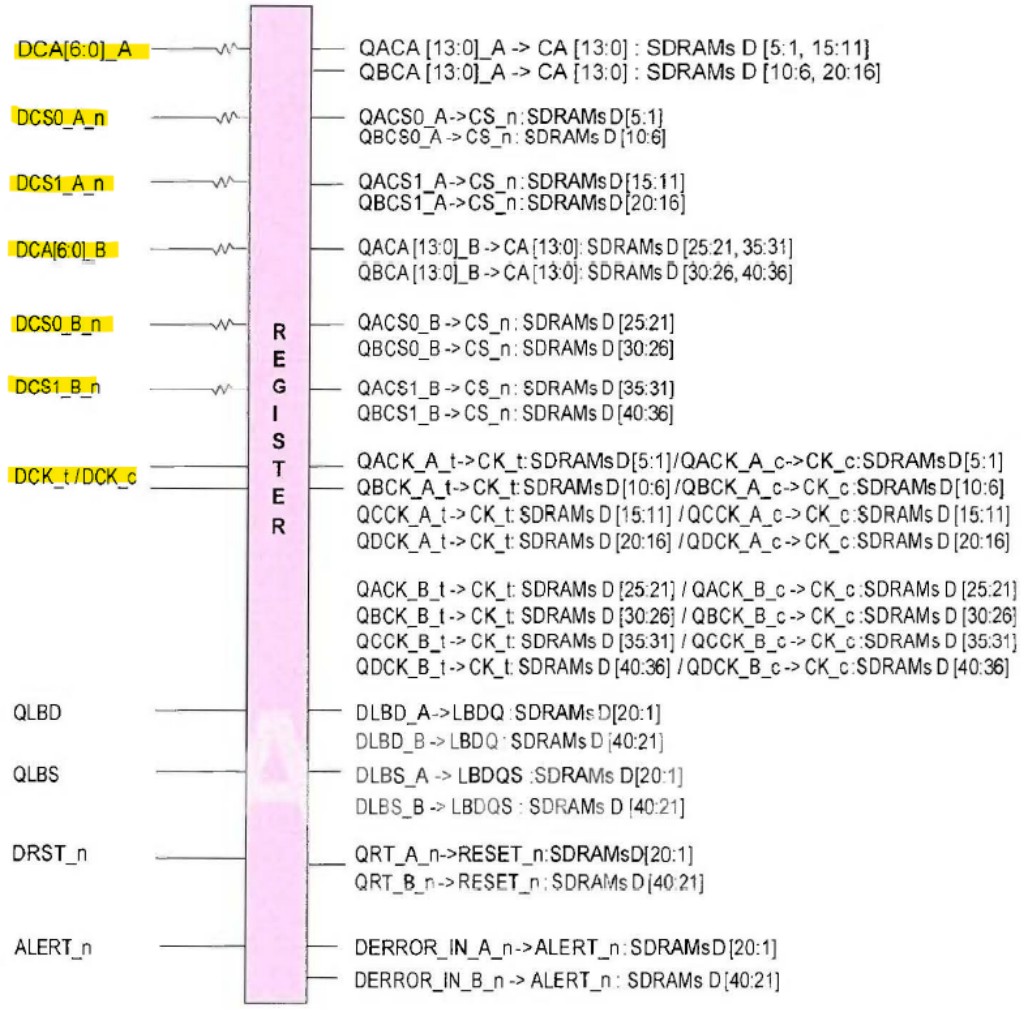
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 21.

Claim 1	Evidence of Use
	

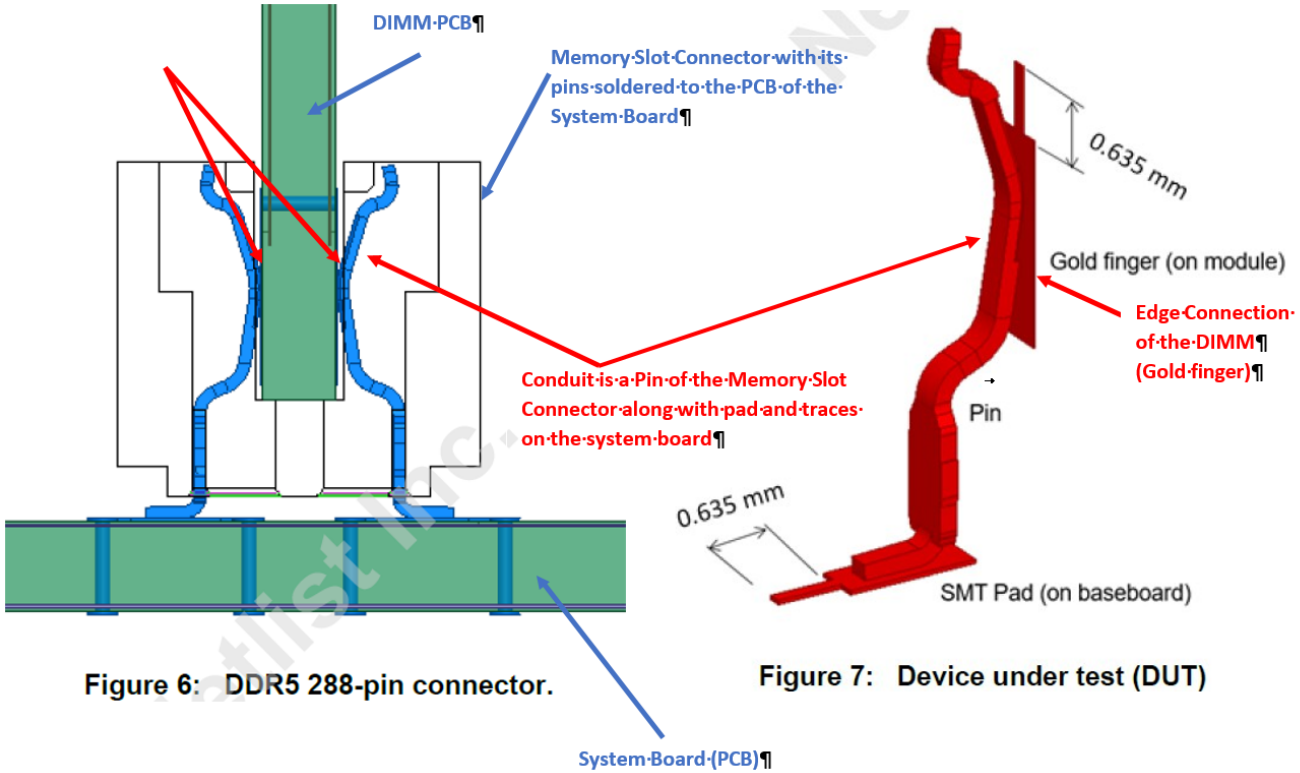
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 25.

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 29.

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 33. As explained *supra*, the Samsung Practicing ’407 Products are JEDEC compliant. The DCA, DCS and DCK signals are therefore received via the corresponding C/A, C/S and CK signals lines in the system bus because the DCA, DCS and DCK pins of an RDIMM each mate with a corresponding connector in the memory slot to form electrical connection to the corresponding slot pin and signal traces, as illustrated below:

Claim 1	Evidence of Use
	 Figure 6: DDR5 288-pin connector. Figure 7: Device under test (DUT) Ex. CC-73 (JEDEC PS-005B) at 13, Figs. 6–7 (annotated) (illustrating an edge connection on a DIMM being electrically connected with a corresponding pin in the memory slot and the corresponding signal trace/line on the system board). The JEDEC DDR5 RDIMM standard further demonstrates the RCD circuitry is configurable to receive from the memory controller a system clock via the one or more clock signal lines (*e.g.,* “CK_t” and “CK_c” / “DCK_t” and “DCK_c”) and input control and address (C/A) signals via the C/A signal lines (*e.g.,* “CA[]_A” and “CA[]_B”/ “DCA[]_A” and “DCA[]_B” / “CS[]_A_n” and “CS[]_B_n” / “DCS[]_A_n” and “DCS[]_B_n”)). *See, e.g.,*

Claim 1	Evidence of Use
	Table 3 — Pin Definitions Ex. CC-88 (JEDEC 305B) at 3 (illustrating circuitry inputs for receiving clock signal lines (*e.g.,* "CK_t" and "CK_c") and control/address (C/A) signal lines (*e.g.,* "CA[]_A," "CA[]_B," "CS[]_A_n," and "CS[]_B_n") from the memory controller). **Table 4 — Input/Output Functional Description** Ex. CC-88 (JEDEC 305B) at 4 (illustrating circuitry inputs for receiving clock signal lines (*e.g.,* "CK_t" and "CK_c") and control/address (C/A) signal lines (*e.g.,* "CA[]_A" and "CA[]_B") from the memory controller).

Pin Name	Description	Pin Name	Description
CA[6:0]_A CA[6:0]_B	Command and Address (CA) Bus	DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A and B
CS[1:0]_A_n CS[1:0]_B_n	Control (Chip Select) (CS_n)	CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A and B
PAR_A PAR_B	Parity input	DQS[9:0]_A_t DQS[9:0]_B_t	Data Strobes (positive line of differential pair)
CK_t	Clock (true/positive)	DQS[9:0]_A_c DQS[9:0]_B_c	Data Strobes (negative line of differential pair)
CK_c	Clock (complement/negative)	TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.

Symbol	Type	I/O Levels	Function
CK_t, CK_c,	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All CA and CS_n input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[6:0]_A CA[6:0]_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during Mode Register Set commands.

Claim 1	Evidence of Use

DQ[31:0]_A DQ[31:0]_B	Input/ Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	Input/ Output	VDD	ECC Checkbits Input/ Output: Bi-directional data bus - for 8-bit ECC (EC8) all 8 bits are used - for 4-bit ECC (EC4) [3:0] bits are used; [7:4] bits are floating

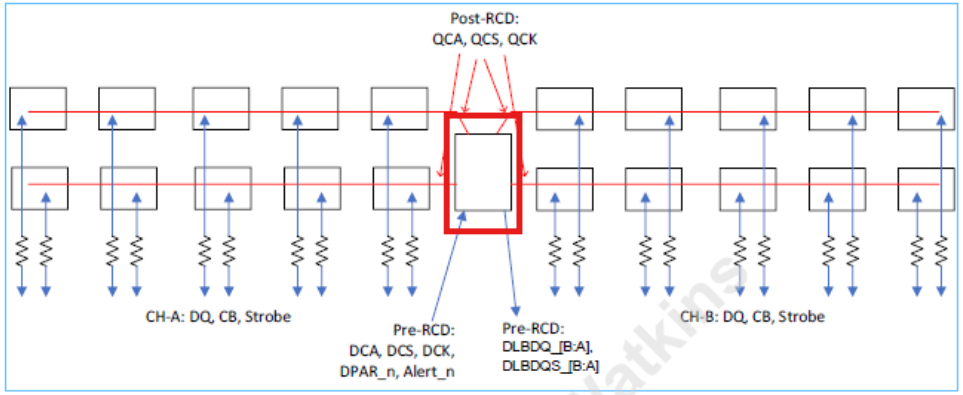
Ex. CC-88 (JEDEC 305B) at 4.

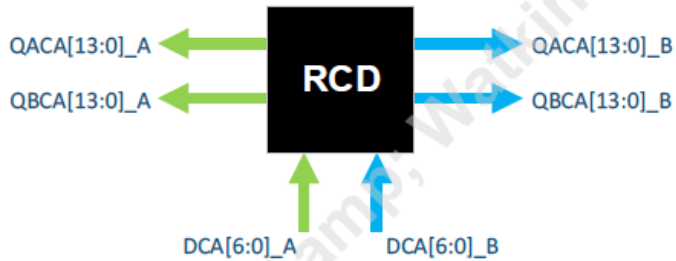
Table 4 — Input/Output Functional Description (cont'd)

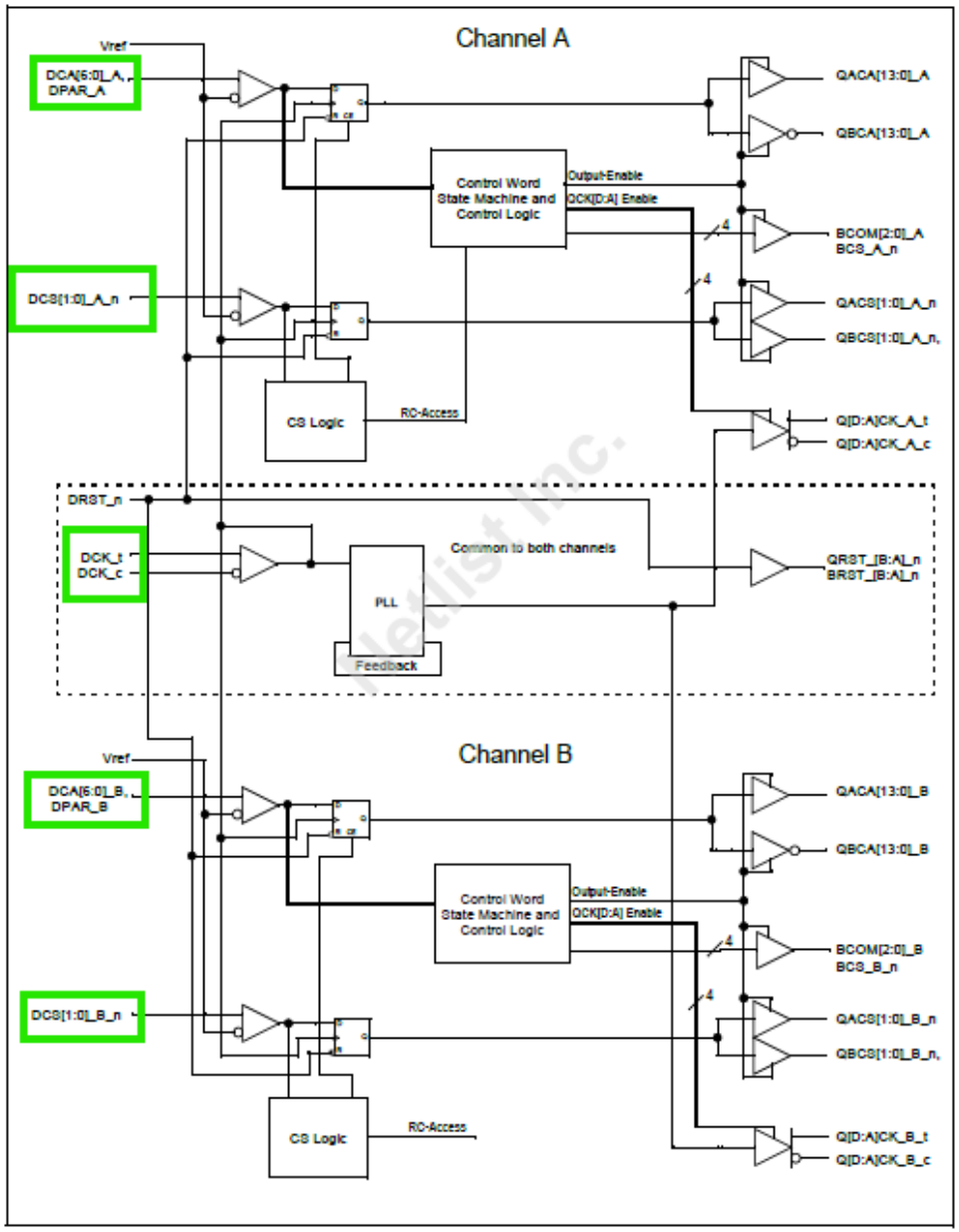
Symbol	Type	I/O Levels	Function
DQS[9:0]_A_t DQS[9:0]_B_t DQS[9:0]_A_c DQS[9:0]_B_c	Input/ Output	VDD	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The Data Strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential Data Strobe only and does not support single-ended.
TDQS[9:5]_A_t TDQS[9:5]_B_t	Input	VDD	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs.
TDQS[9:5]_A_c TDQS[9:5]_B_c	Input	VDD	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs.

Ex. CC-88 (JEDEC 305B) at 5.

Claim 1	Evidence of Use
	6.1 Signal Groups This standard categorizes DDR5 SDRAM timing-critical signals into specific groups. Figure 2 — (Example) RDIMM 2Rx4 Topology summarizes the high-speed signal groups for RDIMM. Signal groups, except Data and Strobe, implement a fly-by topology. Actual signal names in Annex may vary from individual reference design. The signal groups are: Pre-RCD - Pre-RCD CA and CS group includes: DCA[6:0]_[B:A], DCS[1:0]_[B:A]_n, DPAR_[B:A] - Pre-RCD Clock group includes: DCK_t and DCK_c - Pre-RCD Other group includes: ALERT_n, DRST_n - Pre-RCD Loopback group includes: DLBDQ_[B:A], DLBDQS_[B:A] Post-RCD to SDRAM - Post-RCD CA group includes Q[B:A]CA[13:0]_[B:A] - Post-RCD CS group includes Q[B:A]CS[1:0]_[B:A]_n - Post-RCD Clock group includes Q[D:A]CK_[B:A]_t, Q[D:A]CK_[B:A]_c - Post-RCD Other group includes QRST_[B:A]_n, DERROR_[B:A]_n - Post-RCD Other group includes QLBDQ_[B:A], QLBDQS_[B:A] DQ and DQS - edge connector pin to SDRAM with series resistor SideBand - Host to Hub group: HSDA, HSCL, HSA - Hub local bus group: LSDA, LSCL (star topology from Hub) Ex. CC-88 (JEDEC 305B) at 12 (illustrating circuitry inputs for receiving clock signal lines (*e.g.,* “DCK_t” and “DCK_c”) and control/address (C/A) signal lines (*e.g.,* “DCA[]_A,” “DCA[]_B,” “DCS[]_A_n,” and “DCS[]_B_n”) from the memory controller).

Claim 1	Evidence of Use
	6.1 Signal Groups (cont'd)  **Figure 2 — (Example) RDIMM 2Rx4 Topology** Ex. CC-88 (JEDEC 305B) at 13 (illustrating RCD, in red, receiving "Pre-RCD" control and address signals ("DCA" and "DCS") and clock signals ("DCK") from the memory controller). Furthermore, according to the JEDEC RCD specification, the RCD receives on its input side DCA, DCS and DCK signals.

Claim 1	Evidence of Use
	3.4.1 Double Data Rate DCA The DDR5 RCD will support DDR (Double Data Rate) on the host-interface DCA signals. The host-interface CA bus is 7 bits, plus parity. The DRAM-interface CA bus remains SDR (Single Data Rate) and is 14 bits and without parity. The RCD will expand the incoming host-interface 7-bit DCA bus to 14 bits on the DRAM interface. Table 8 shows the mapping of the incoming DCA bits to the output QCA. The Chip Selects remain SDR on both the host-interface and DRAM interface. The two channel DDR5RCD has six CA ports, two DCA input ports and four QCA output ports as shown in Figure 6. **Table 8 — DDR CA Mapping DCA to QCA** UI: 0 — DCA0 QCA0, DCA1 QCA1, DCA2 QCA2, DCA3 QCA3, DCA4 QCA4, DCA5 QCA5, DCA6 QCA6 UI: 1 — DCA0 QCA7, DCA1 QCA8, DCA2 QCA9, DCA3 QCA10, DCA4 QCA11, DCA5 QCA12, DCA6 QCA13  **Figure 6 — RCD DCA and QCA Ports** Ex. CC-32 (JEDEC 82-512) at 15 (illustrating circuitry inputs for receiving control/address (C/A) signal lines (*e.g.,* "DCA[]_A" and "DCA[]_B") from the memory controller).


Channel A
Vref
DCA[6:0]_A,
DPAR_A
QACA[13:0]_A
QBCA[13:0]_A
Control Word
State Machine and
Control Logic
Output-Enable
QCK[D:A] Enable
BCOM[2:0]_A
BCS_A_n
DCS[1:0]_A_n
QACS[1:0]_A_n
QBCS[1:0]_A_n,
CS Logic
RC-Access
Q[D:A]CK_A_t
Q[D:A]CK_A_c
DRST_n
DCK_t
DCK_c
Common to both channels
PLL
Feedback
QRST_[B:A]_n
BRST_[B:A]_n
Channel B
Vref
DCA[6:0]_B,
DPAR_B
QACA[13:0]_B
QBCA[13:0]_B
Control Word
State Machine and
Control Logic
Output-Enable
QCK[D:A] Enable
BCOM[2:0]_B
BCS_B_n
DCS[1:0]_B_n
QACS[1:0]_B_n
QBCS[1:0]_B_n,
CS Logic
RC-Access
Q[D:A]CK_B_t
Q[D:A]CK_B_c

Claim 1	Evidence of Use
	Ex. CC-32 (JEDEC 82-512) at 7 (illustrating circuitry inputs for receiving clock signal lines (*e.g.,* "DCK_t" and "DCK_c") and control/address (C/A) signal lines (*e.g.,* "DCA[]_A," "DCA[]_B," "DCS[]_A_n," and "DCS[]_B_n") from the memory controller).

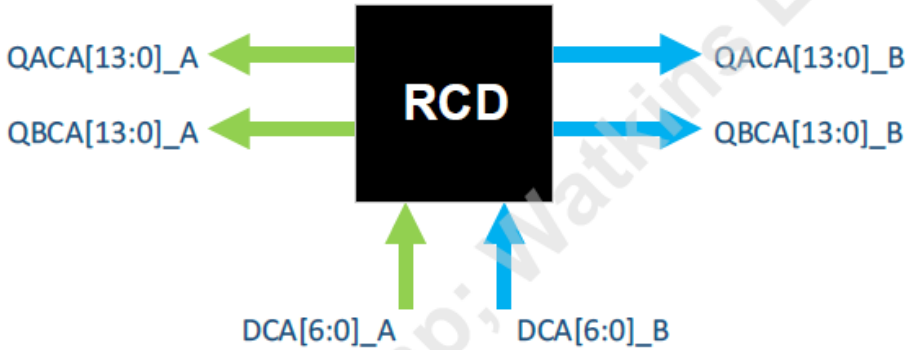
Signal Group	Signal Name	Type	Description
Input Control bus	DCS[1:0]_[B:A]_n	POD V_{REF} based	Chip Select inputs to the RCD. Two inputs per DRAM channel.
Input Address and Command bus	DCA[6:0]_[B:A]	POD V_{REF} based	Command/Address bus inputs to the RCD. Separate sets per channel.
Parity input	DPAR_[B:A]	POD V_{REF} based	Command Address input parity is received on the DPAR pin and should maintain even parity across the CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
Clock inputs	DCK_t/DCK_c	POD differential	Differential system clock input pair to the PLL. The clock is common to both RCD channels, CH_A and CH_B.

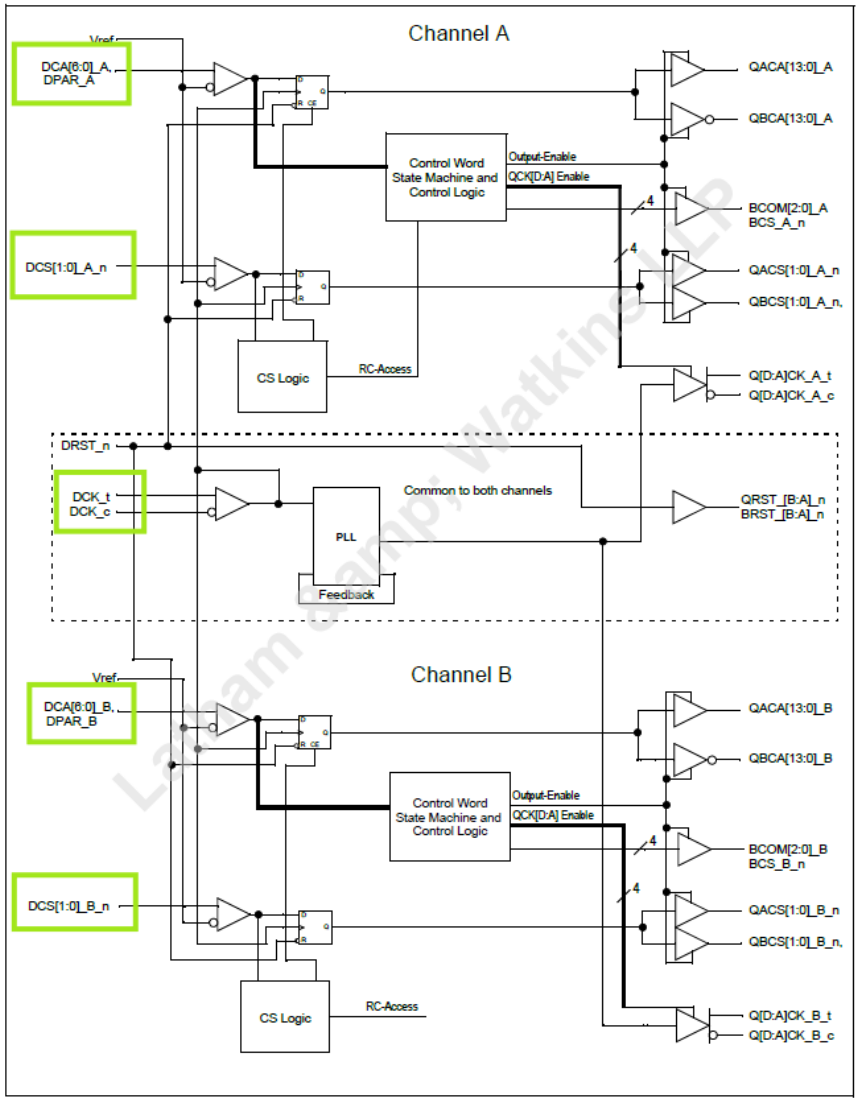
Ex. CC-32 (JEDEC 82-512) at 4 (illustrating circuitry inputs for receiving clock signal lines (*e.g.,* "DCK_t" and "DCK_c") and control/address (C/A) signal lines (*e.g.,* "DCA[]_A," "DCA[]_B," "DCS[]_A_n," and "DCS[]_B_n") from the memory controller).

3.1 Description

The DDR5RCD02 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

Ex. CC-32 (JEDEC 82-512) at 6.

Claim 1	Evidence of Use
	3.4.1 Double Data Rate DCA The DDR5 RCD will support DDR (Double Data Rate) on the host-interface DCA signals. The host-interface CA bus is 7 bits, plus parity. The DRAM-interface CA bus remains SDR (Single Data Rate) and is 14 bits and without parity. The RCD will expand the incoming host-interface 7-bit DCA bus to 14 bits on the DRAM interface. Table 8 shows the mapping of the incoming DCA bits to the output QCA. The Chip Selects remain SDR on both the host-interface and DRAM interface. The two channel DDR5RCD has six CA ports, two DCA input ports and four QCA output ports as shown in Figure 6. **Table 8 — DDR CA Mapping DCA to QCA** UI: 0 — DCA0 QCA0, DCA1 QCA1, DCA2 QCA2, DCA3 QCA3, DCA4 QCA4, DCA5 QCA5, DCA6 QCA6 UI: 1 — DCA0 QCA7, DCA1 QCA8, DCA2 QCA9, DCA3 QCA10, DCA4 QCA11, DCA5 QCA12, DCA6 QCA13  **Figure 6 — RCD DCA and QCA Ports** Ex. CC-30 (JEDEC 82-513) at 15.

Claim 1	Evidence of Use
	 Ex. CC-30 (JEDEC 82-513) at 7.

Latham Sampy Watkins LLP

<table>
<tr><th>Claim 1</th><th>Evidence of Use</th></tr>
<tr><td></td><td>

2.2 Terminal Functions

Table 2 — Terminal Functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCS[1:0]_[B:A]_n	POD V_{REF} based	Chip Select inputs to the RCD. Two inputs per DRAM channel.
Input Address and Command bus	DCA[6:0]_[B:A]	POD V_{REF} based	Command/Address bus inputs to the RCD. Separate sets per channel.
Parity input	DPAR_[B:A]	POD V_{REF} based	Command Address input parity is received on the DPAR pin and should maintain even parity across the CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
Clock inputs	DCK_t/DCK_c	POD differential	Differential system clock input pair to the PLL. The clock is common to both RCD channels, CH_A and CH_B.

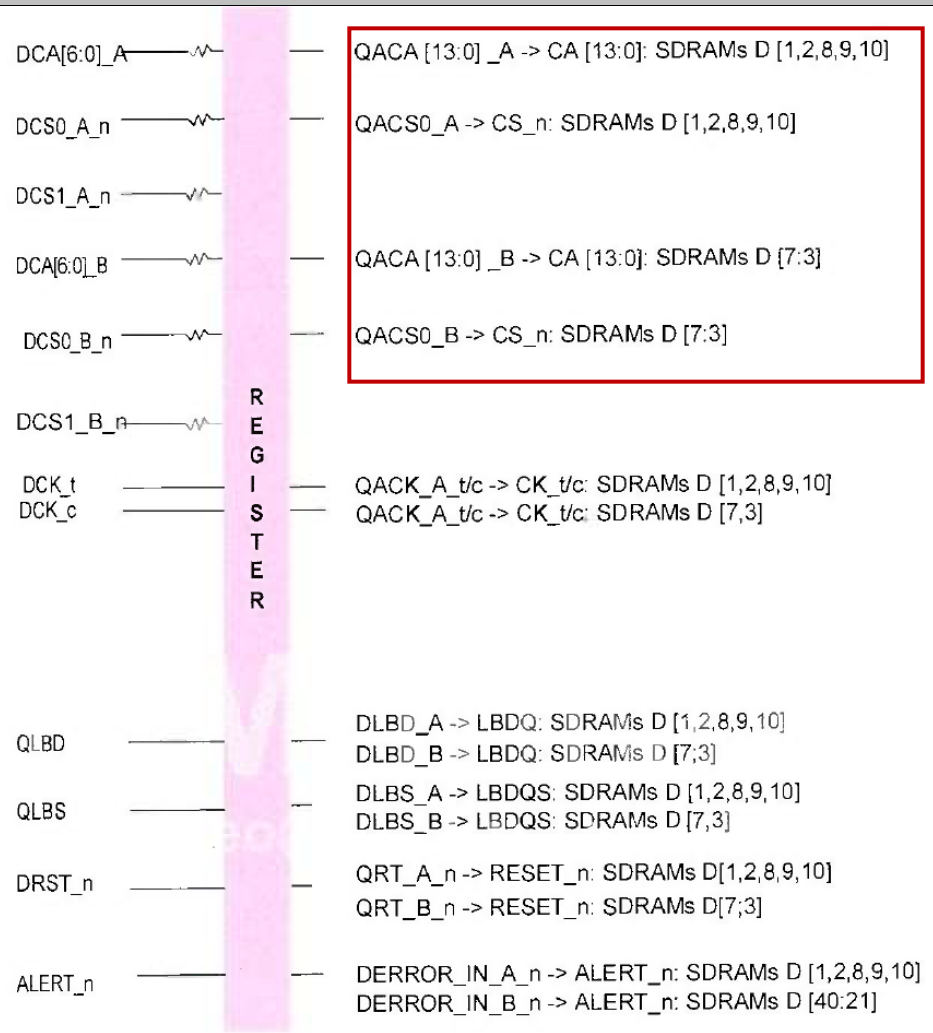
Ex. CC-30 (JEDEC 82-513) at 4.

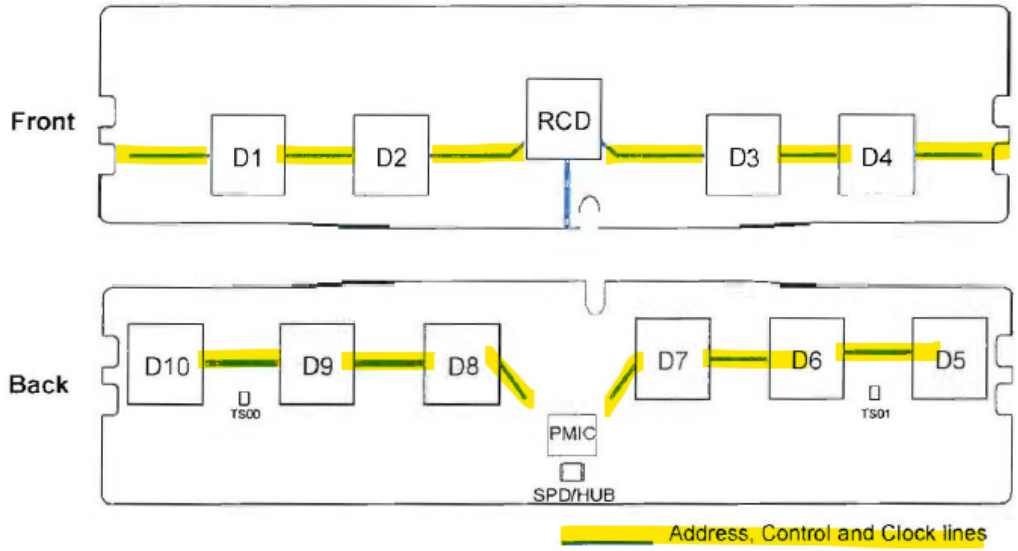
3.1 Description

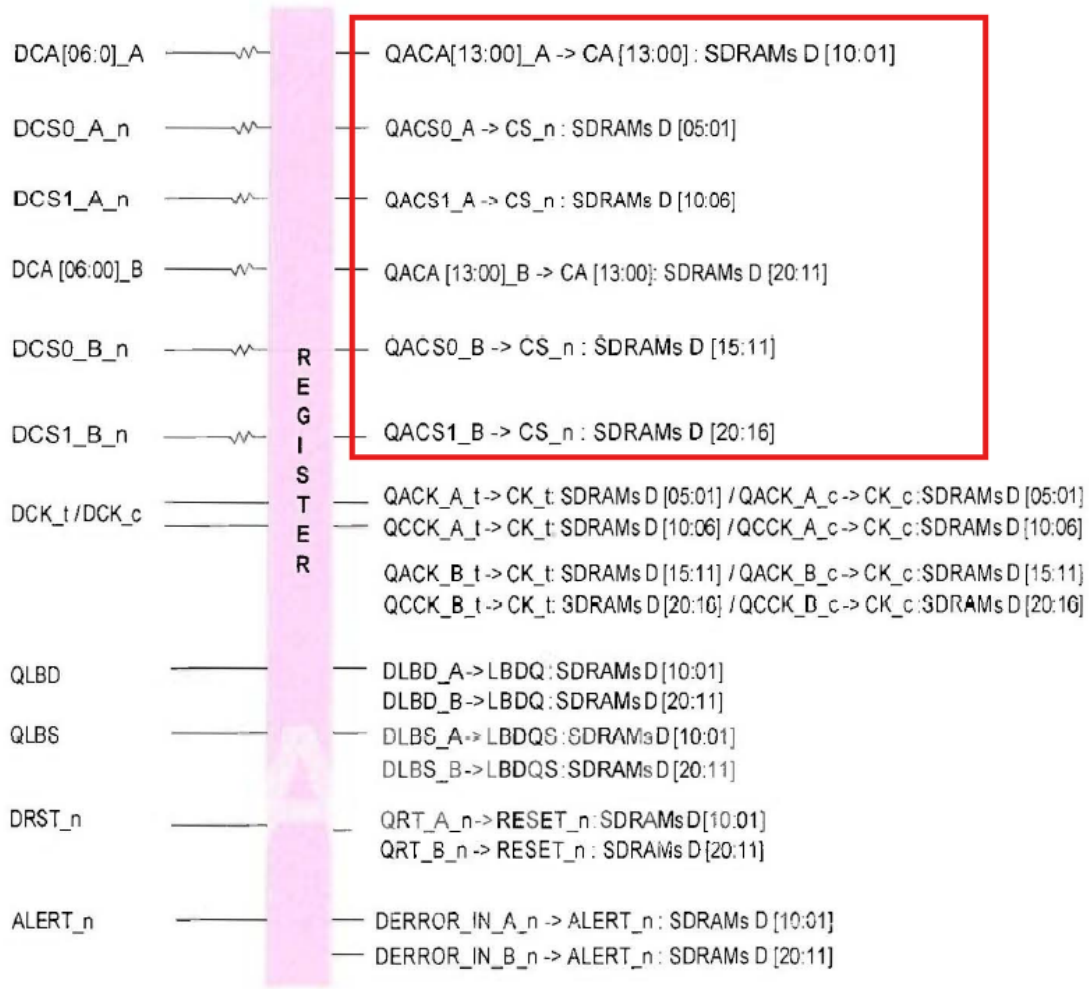
The DDR5RCD03 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

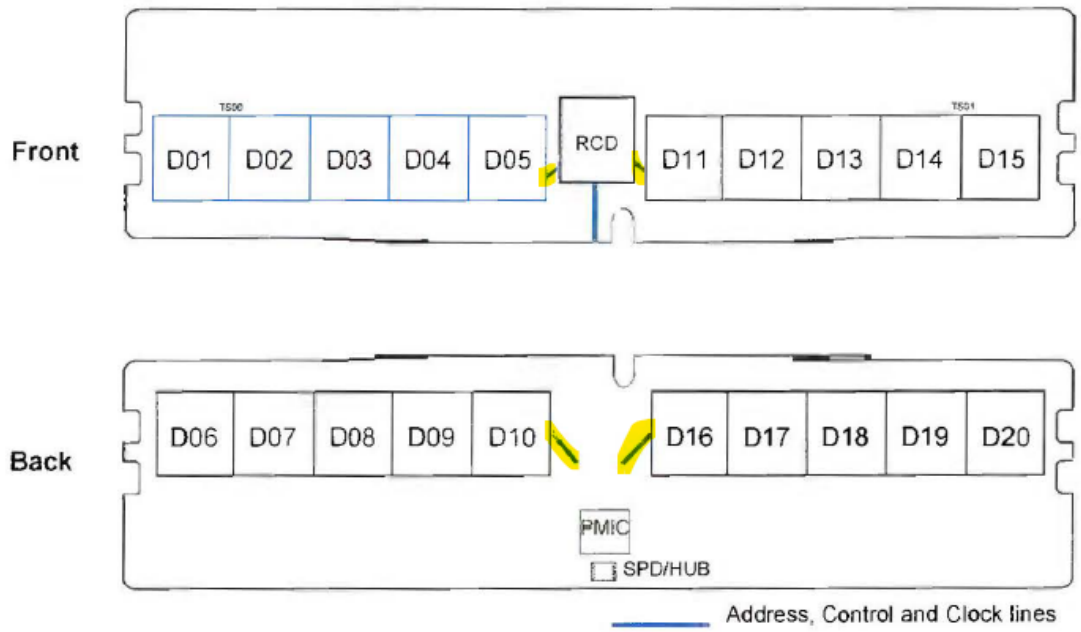
Ex. CC-30 (JEDEC 82-513) at 6.

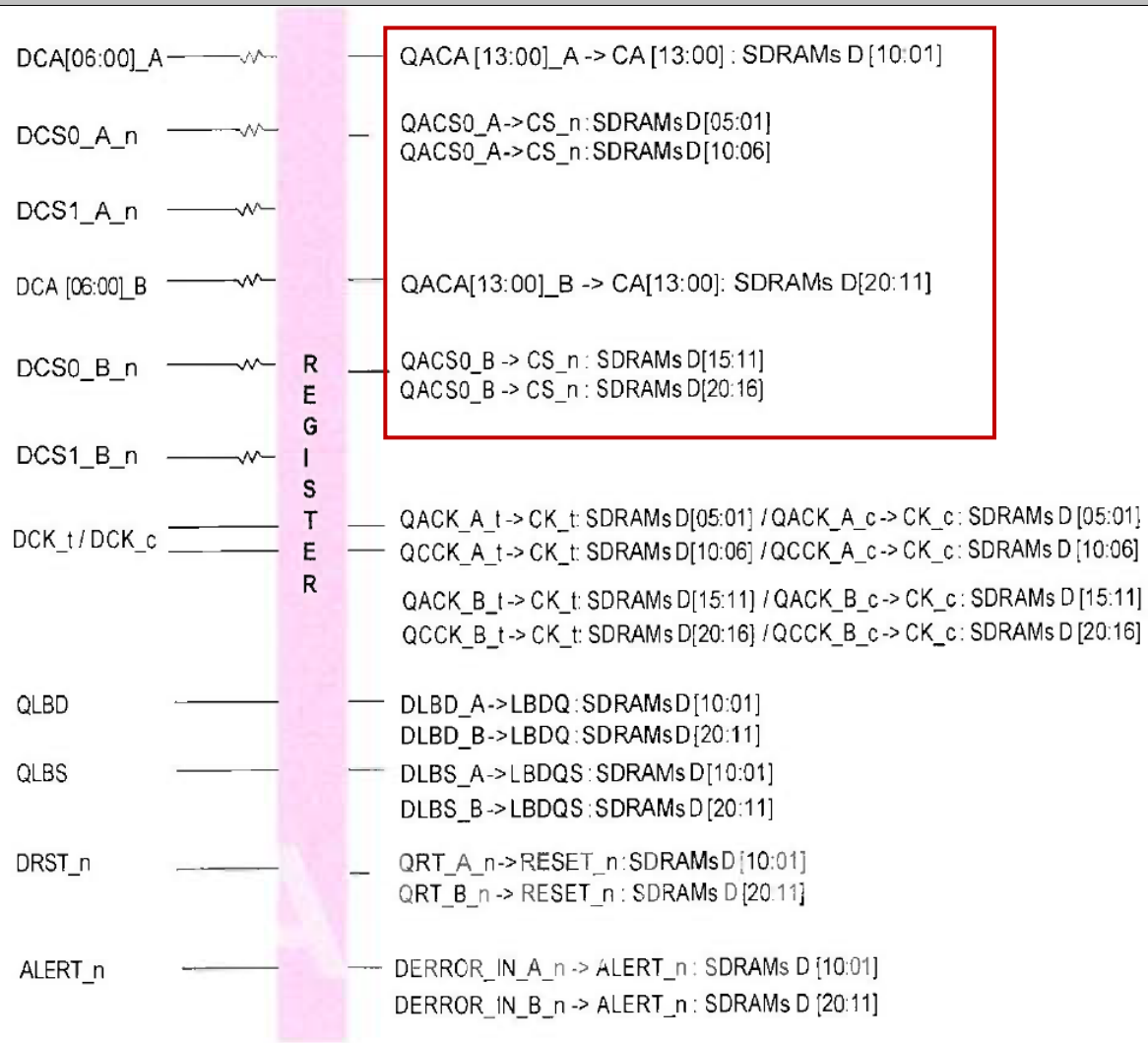
</td></tr>
<tr><td>[1.c.2] generate module C/A signals in response to the input C/A signals;</td><td>The Samsung Practicing ’407 Products each comprise circuitry mounted on the PCB and configurable to generate module C/A signals in response to the input C/A signals, as illustrated below:</td></tr>
</table>

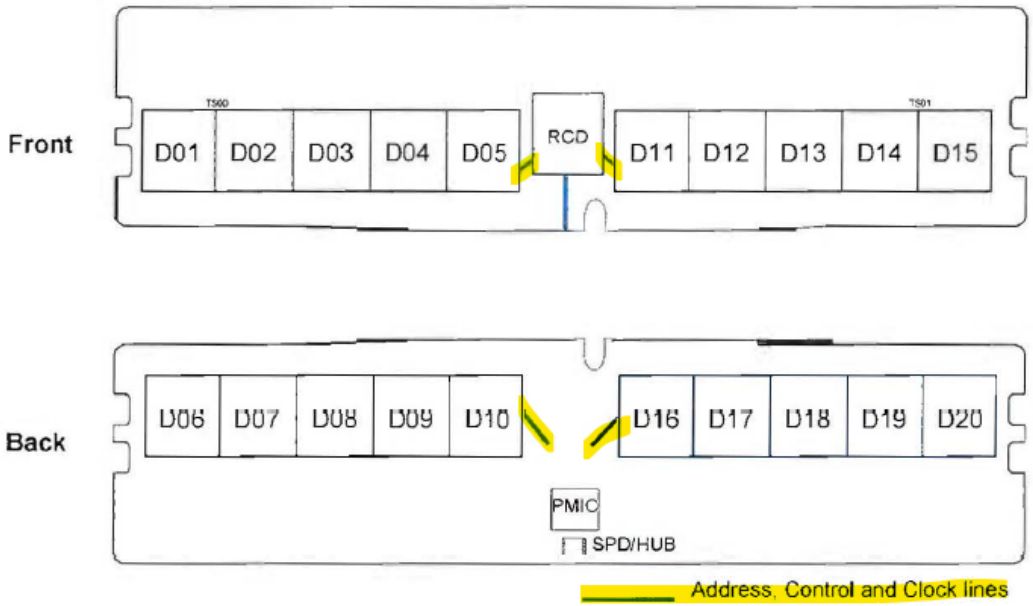
Claim 1	Evidence of Use
	

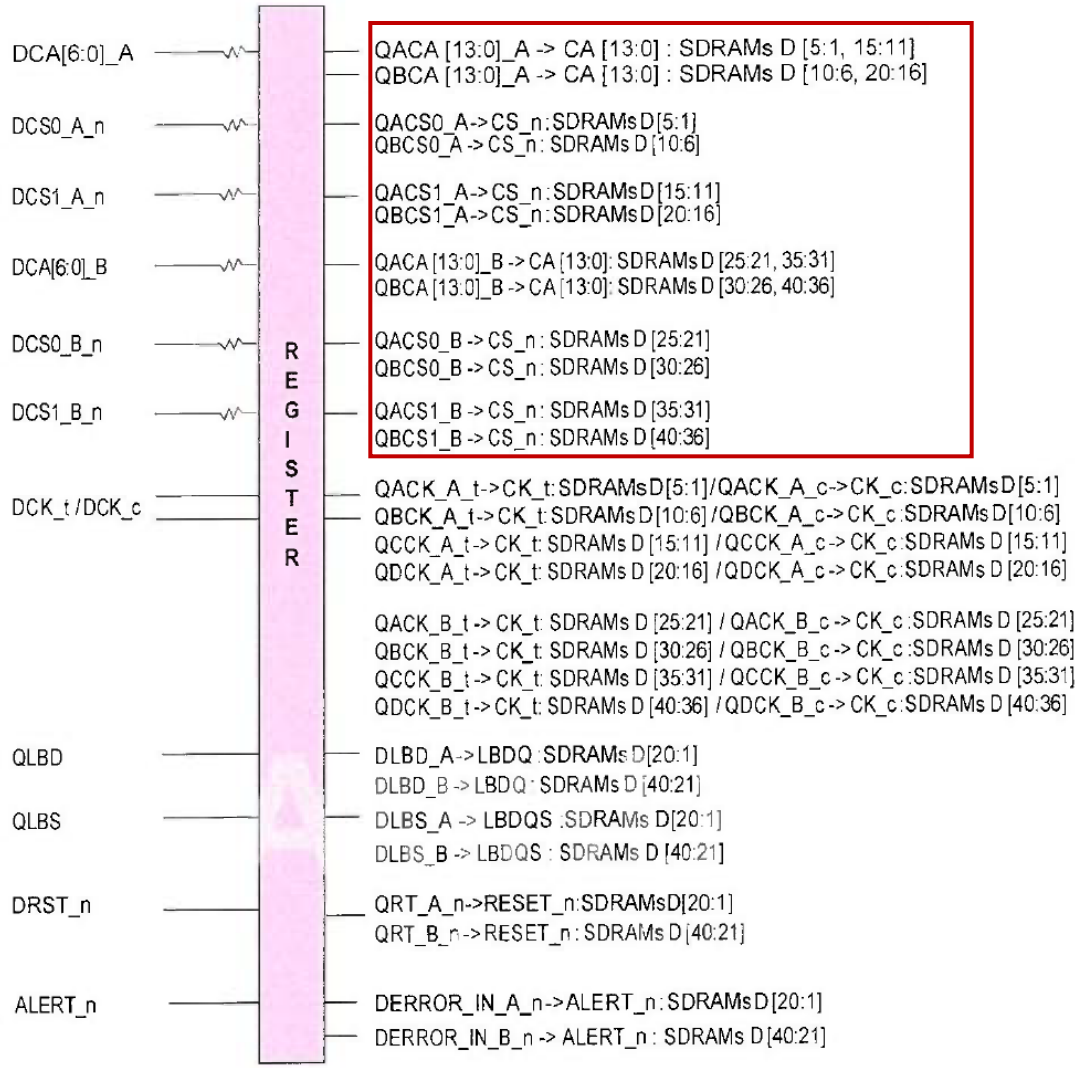
Claim 1	Evidence of Use
	 Ex. CC-89 at 21 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	

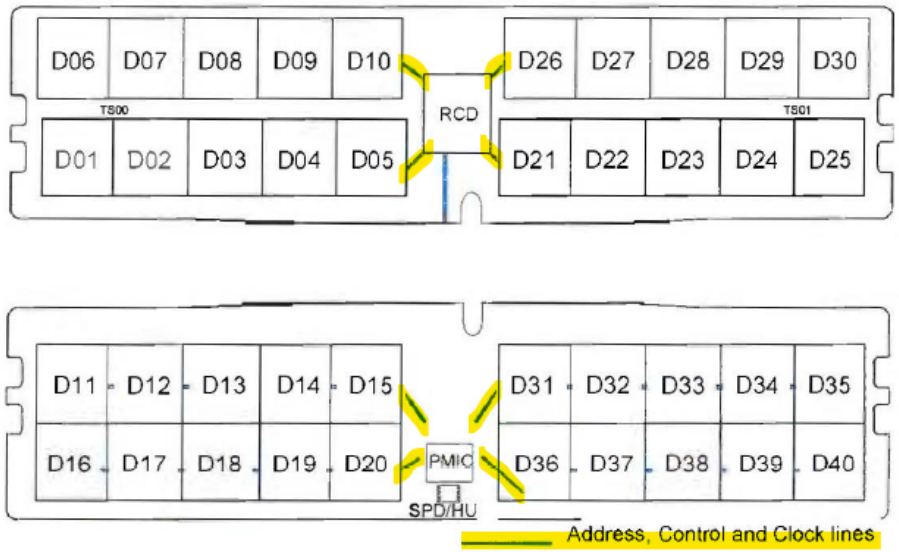
Claim 1	Evidence of Use
	 Ex. CC-89 at 25 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use



Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet)

As explained supra, the Samsung Practicing '407 Products are JEDEC compliant. According to the JEDEC RCD specifications, RCD outputs module C/A signals (such as QACA, QBCA, QACS and QBCS signals) in response to the input C/A signals (DCA and DCS) received from the host.

3.1 Description

The DDR5RCD02 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels.

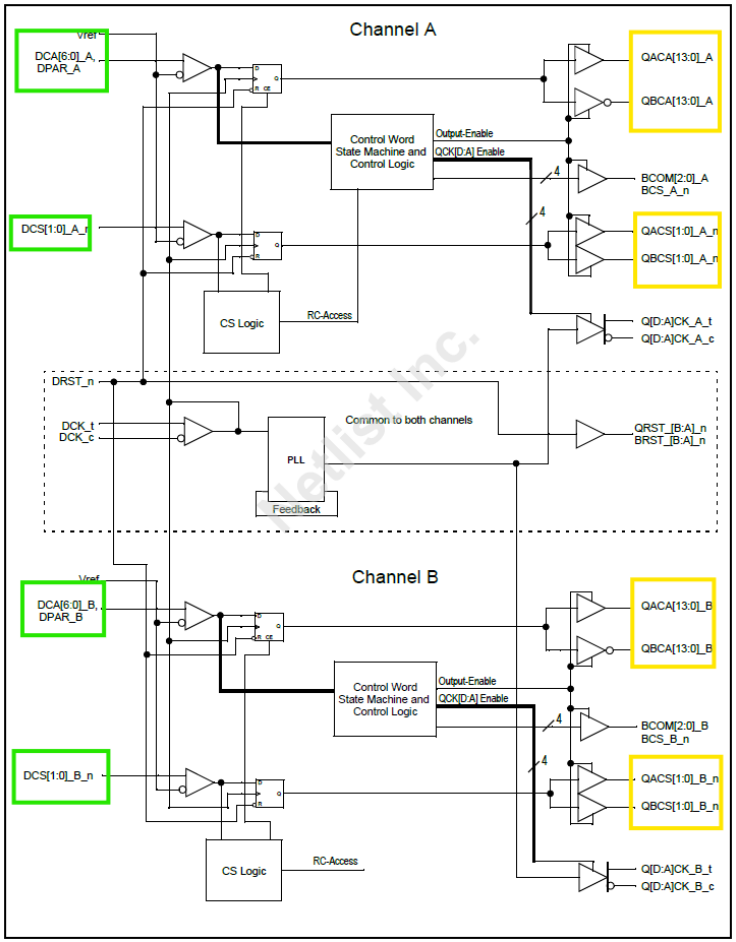
Claim 1	Evidence of Use
	Ex. CC-32 (JEDEC 82-512) at 6.

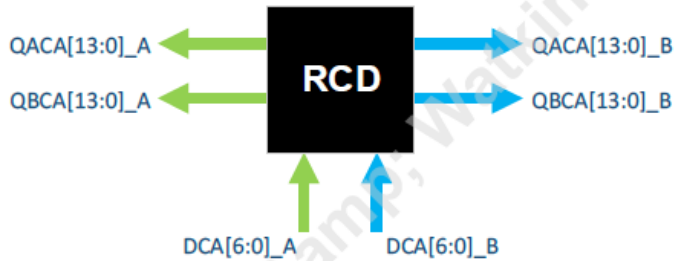
2.2 Terminal Functions

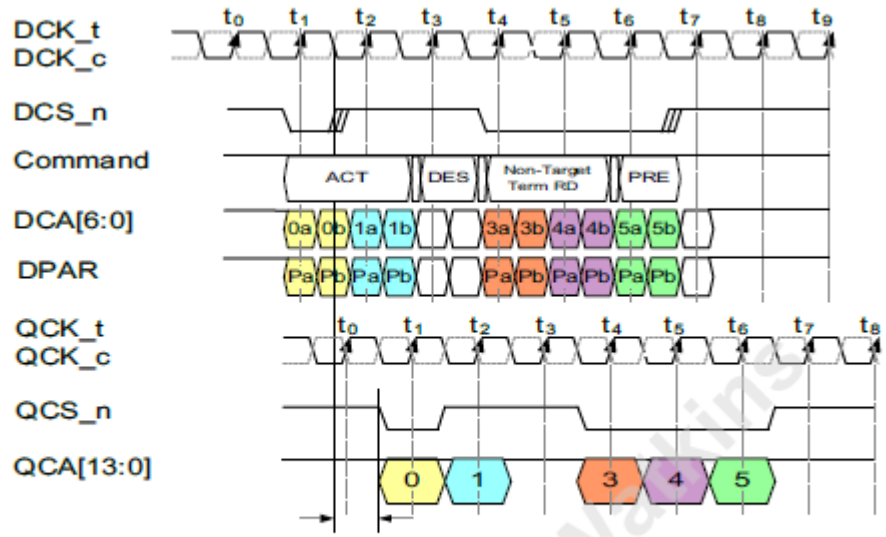
Table 2 — Terminal Functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCS[1:0]_[B:A]_n	POD V_{REF} based	Chip Select inputs to the RCD. Two inputs per DRAM channel.
Input Address and Command bus	DCA[6:0]_[B:A]	POD V_{REF} based	Command/Address bus inputs to the RCD. Separate sets per channel.
Parity input	DPAR_[B:A]	POD V_{REF} based	Command Address input parity is received on the DPAR pin and should maintain even parity across the CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
Clock inputs	DCK_t/DCK_c	POD differential	Differential system clock input pair to the PLL. The clock is common to both RCD channels, CH_A and CH_B.
Loopback	DLBD_[B:A] DLBS_[B:A]	POD V_{REF} based	Loopback Inputs to RCD DLBD - loopback Data DLBS - loopback Strobe
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Error input	DERROR_IN_[B:A]_n	Low voltage swing POD input	DRAM CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. There is a separate signal per channel.
Data buffer control and communication outputs	BCS_[B:A]_n	POD	Data buffer chip selects. Indicate a valid command on the BCOM bus, and used to signal non-target termination. Separate per DRAM channel.
	BCOM[2:0]_[B:A]	POD	Data buffer command. The start of each command is signaled by an active chip select. Separate per DRAM channel.
	BRST_[B:A]_n	CMOS	Re-driven or CMD based reset. This is an asynchronous output. It is the responsibility of the RCD BRST to reset the DDR5 Data Buffer on all DIMM topologies.
	BCK_[B:A]_t BCK_[B:A]_c	POD differential	Differential clock output pair to the data buffer. Separate per DRAM channel.
Output Control bus	Q[B:A]CS[1:0]_[B:A]_n	POD	Chip Select signals to the DRAMs. 2 copies of each signal.
Output Address and Command bus	Q[B:A]CA[13:0]_[B:A]	POD	Command/Address bus outputs to the DRAMs, valid after the specified clock count and immediately following a rising edge of the clock. Two copies of each signal. When Output Inversion is enabled in RW00[5], Copy B output signals get inverted during all commands other than Deselect. Both copies drive High during idle cycles (i.e., Deselect).
Clock outputs	Q[B:A]CK_[B:A]_t	POD differential	Clock outputs to the DRAMs. Four copies per channel

	Ex. CC-32 (JEDEC 82-512) at 4.

Claim 1	Evidence of Use
	 Ex. CC-32 (JEDEC 82-512) at 7 (showing the RCD circuitry generates module C/A signals shown in yellow in response to the input C/A signals shown in green).

Claim 1	Evidence of Use
	3.4.1 Double Data Rate DCA The DDR5 RCD will support DDR (Double Data Rate) on the host-interface DCA signals. The host-interface CA bus is 7 bits, plus parity. The DRAM-interface CA bus remains SDR (Single Data Rate) and is 14 bits and without parity. The RCD will expand the incoming host-interface 7-bit DCA bus to 14 bits on the DRAM interface. Table 8 shows the mapping of the incoming DCA bits to the output QCA. The Chip Selects remain SDR on both the host-interface and DRAM interface. The two channel DDR5RCD has six CA ports, two DCA input ports and four QCA output ports as shown in Figure 6. **Table 8 — DDR CA Mapping DCA to QCA** UI: DCA0, DCA1, DCA2, DCA3, DCA4, DCA5, DCA6 0: QCA0, QCA1, QCA2, QCA3, QCA4, QCA5, QCA6 1: QCA7, QCA8, QCA9, QCA10, QCA11, QCA12, QCA13  **Figure 6 — RCD DCA and QCA Ports** Ex. CC-32 (JEDEC 82-512) at 15. **3.3.3 QCA Bus Operation** Under normal operation, the RCD passes commands through from the D inputs to the Q outputs when a command is present on the bus, and drives HIGH on the QCA outputs when no command is being sent. The RCD passes the DCA bus through when either DCS input is active but there are exceptions to this: • If the register detects a parity error and parity checking is enabled, the DCA bus is still passed through to DRAM and QCS is blocked. • During the 2nd UI of a 2 UI command, the DCA bus must be passed through. There will only be a DCS signal active for the 2nd UI if a non-target termination is being signaled to a rank. • When DRAM interface Block MR Mode is enabled RW01[1] = 0. • When CA Pass-through mode is enabled RW00[2] = 1.

Claim 1	Evidence of Use
	Ex. CC-32 (JEDEC 82-512) at 9.  NOTE Timing Diagram for 0 nCK command latency adder. **Figure 9 — DDR CA Multi-Command Timing Diagram Example** Ex. CC-32 (JEDEC 82-512) at 17 (timing diagram showing the generation of module C/A signals (QCA[13:0]) in response to the input C/A signals (DCA[6:0]).

Claim 1	Evidence of Use
	3.1 Description The DDR5RCD03 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs. It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels. Ex. CC-30 (JEDEC 82-513) at 6.

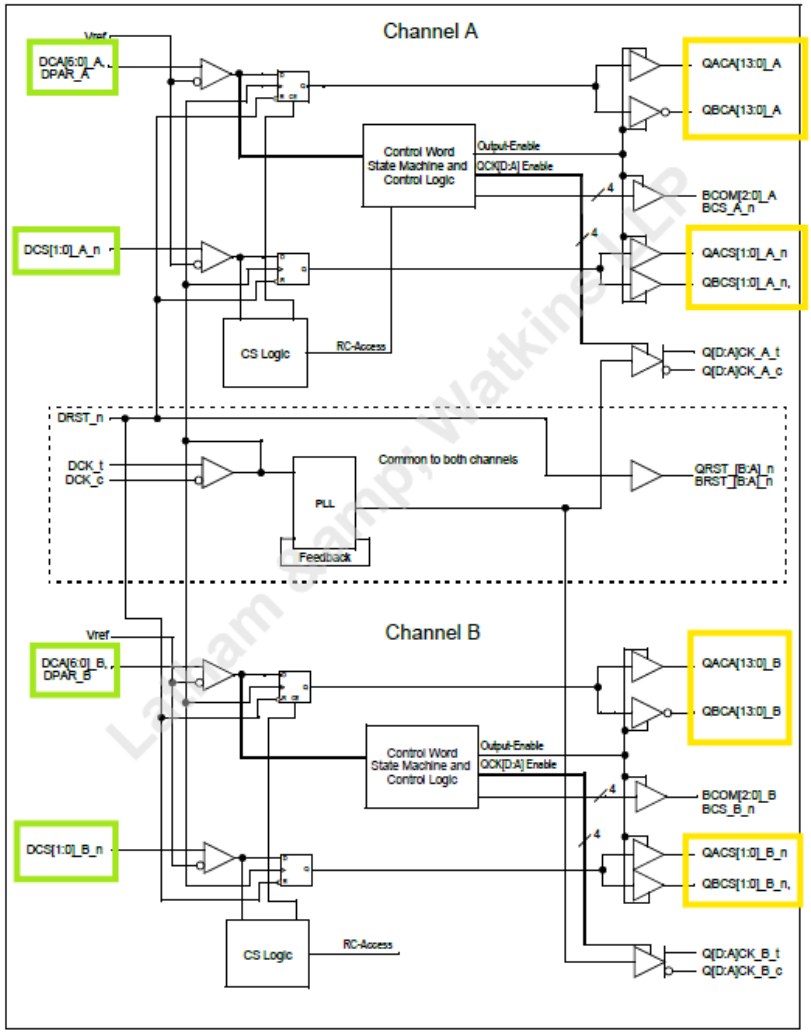
Claim 1	Evidence of Use

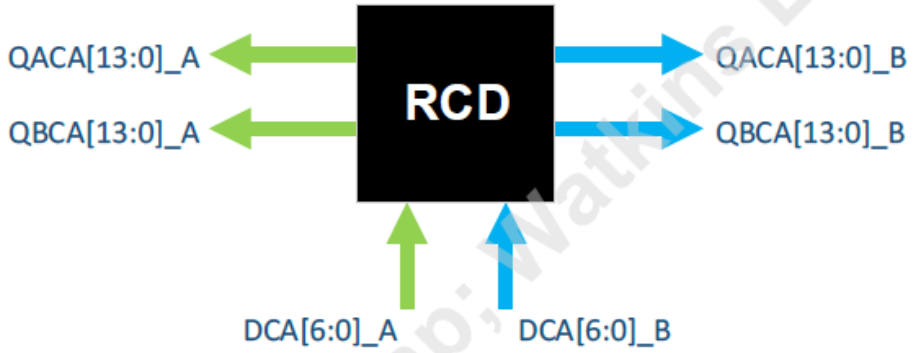
2.2 Terminal Functions

Table 2 — Terminal Functions

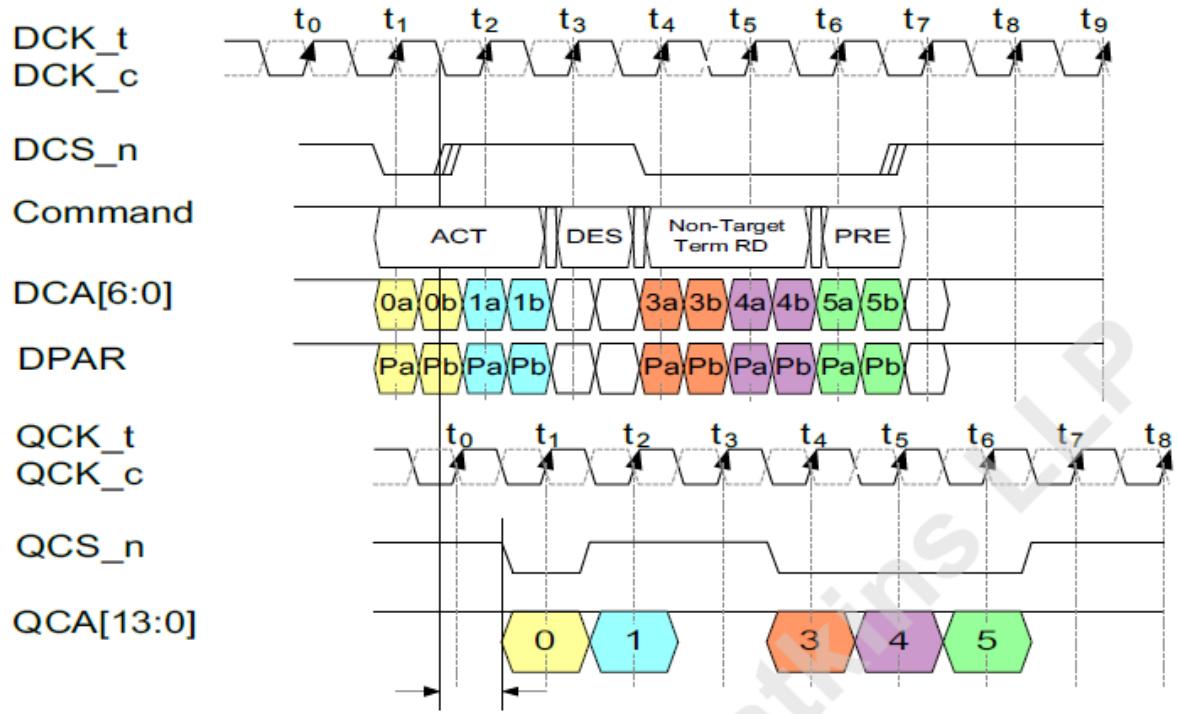
Signal Group	Signal Name	Type	Description
Input Control bus	DCS[1:0]_[B:A]_n	POD V_{REF} based	Chip Select inputs to the RCD. Two inputs per DRAM channel.
Input Address and Command bus	DCA[6:0]_[B:A]	POD V_{REF} based	Command/Address bus inputs to the RCD. Separate sets per channel.
Parity input	DPAR_[B:A]	POD V_{REF} based	Command/Address input parity is received on the DPAR pin and should maintain even parity across the CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
Clock inputs	DCK_t/DCK_c	POD differential	Differential system clock input pair to the PLL. The clock is common to both RCD channels, CH_A and CH_B.
Loopback	DLBD_[B:A] DLBS_[B:A]	POD V_{REF} based	Loopback Inputs to RCD DLBD - loopback Data DLBS - loopback Strobe
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Error input	DERROR_IN_[B:A]_n	Low voltage swing POD input	DRAM CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. There is a separate signal per channel.
Data buffer control and communication outputs	BCS_[B:A]_n	POD	Data buffer chip selects. Indicate a valid command on the BCOM bus, and used to signal non-target termination. Separate per DRAM channel.
	BCOM[2:0]_[B:A]	POD	Data buffer command. The start of each command is signaled by an active chip select. Separate per DRAM channel.
	BRST_[B:A]_n	CMOS	Re-driven or CMD based reset. This is an asynchronous output. It is the responsibility of the RCD BRST to reset the DDR5 Data Buffer on all DIMM topologies.
	BCK_[B:A]_t BCK_[B:A]_c	POD differential	Differential clock output pair to the data buffer. Separate per DRAM channel.
Output Control bus	Q[B:A]CS[1:0]_[B:A]_n	POD	Chip Select signals to the DRAMs. 2 copies of each signal.
Output Address and Command bus	Q[B:A]CA[13:0]_[B:A]	POD	Command/Address bus outputs to the DRAMs, valid after the specified clock count and immediately following a rising edge of the clock. Two copies of each signal. When Output Inversion is enabled in RW00[5], Copy B output signals get inverted during all commands other than Deselect. Both copies drive High during idle cycles (i.e., Deselect).

Ex. CC-30 (JEDEC 82-513) at 4.

Claim 1	Evidence of Use
	 Ex. CC-30 (JEDEC 82-513) at 7 (showing the RCD circuitry generates module C/A signals shown in yellow in response to the input C/A signals shown in green).

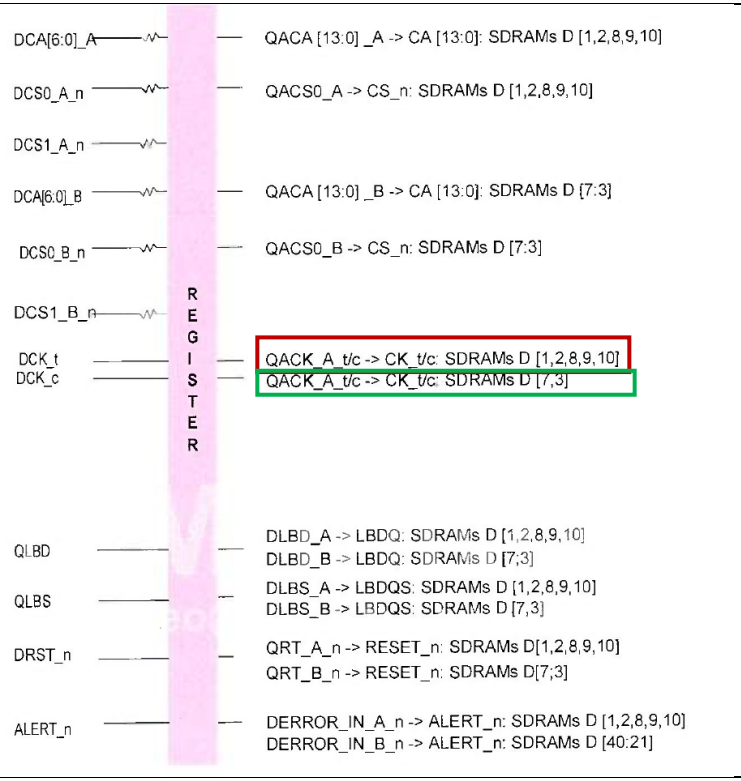
Claim 1	Evidence of Use
	3.4.1 Double Data Rate DCA The DDR5 RCD will support DDR (Double Data Rate) on the host-interface DCA signals. The host-interface CA bus is 7 bits, plus parity. The DRAM-interface CA bus remains SDR (Single Data Rate) and is 14 bits and without parity. The RCD will expand the incoming host-interface 7-bit DCA bus to 14 bits on the DRAM interface. Table 8 shows the mapping of the incoming DCA bits to the output QCA. The Chip Selects remain SDR on both the host-interface and DRAM interface. The two channel DDR5RCD has six CA ports, two DCA input ports and four QCA output ports as shown in Figure 6. **Table 8 — DDR CA Mapping DCA to QCA** UI: 0 — DCA0 QCA0, DCA1 QCA1, DCA2 QCA2, DCA3 QCA3, DCA4 QCA4, DCA5 QCA5, DCA6 QCA6 UI: 1 — DCA0 QCA7, DCA1 QCA8, DCA2 QCA9, DCA3 QCA10, DCA4 QCA11, DCA5 QCA12, DCA6 QCA13  **Figure 6 — RCD DCA and QCA Ports** Ex. CC-30 (JEDEC 82-513) at 15.

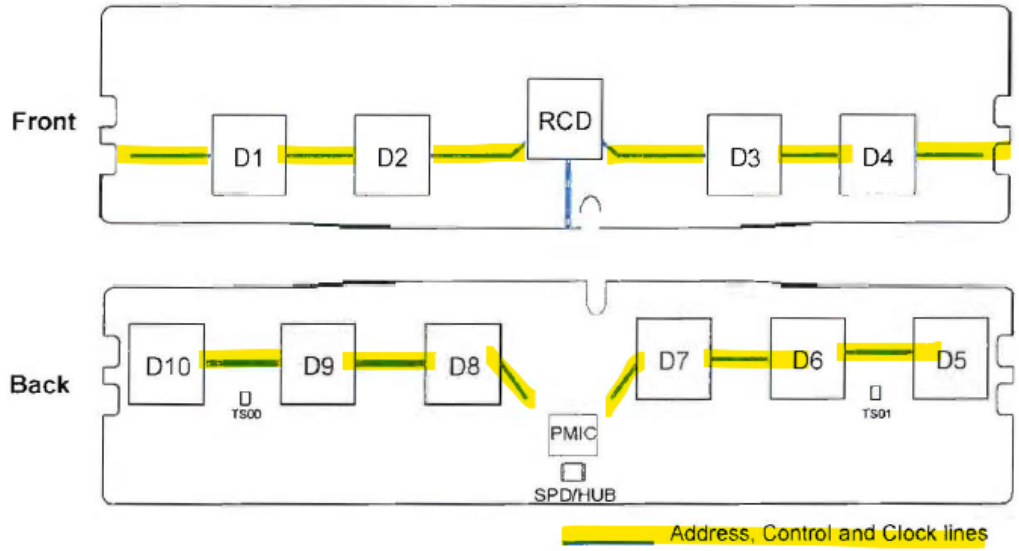
Claim 1	Evidence of Use
	3.3.3 QCA Bus Operation Under normal operation, the RCD passes commands through from the D inputs to the Q outputs when a command is present on the bus, and drives HIGH on the QCA outputs when no command is being sent. The RCD passes the DCA bus through when either DCS input is active but there are exceptions to this: • If the register detects a parity error and parity checking is enabled, the DCA bus is still passed through to DRAM and QCS is blocked. • During the 2nd UI of a 2 UI command, the DCA bus must be passed through. There will only be a DCS signal active for the 2nd UI if a non-target termination is being signaled to a rank. • When DRAM interface Block MR Mode is enabled RW01[1] = 0. • When CA Pass-through mode is enabled RW00[2] = 1. Ex. CC-30 (JEDEC 82-513) at 9.

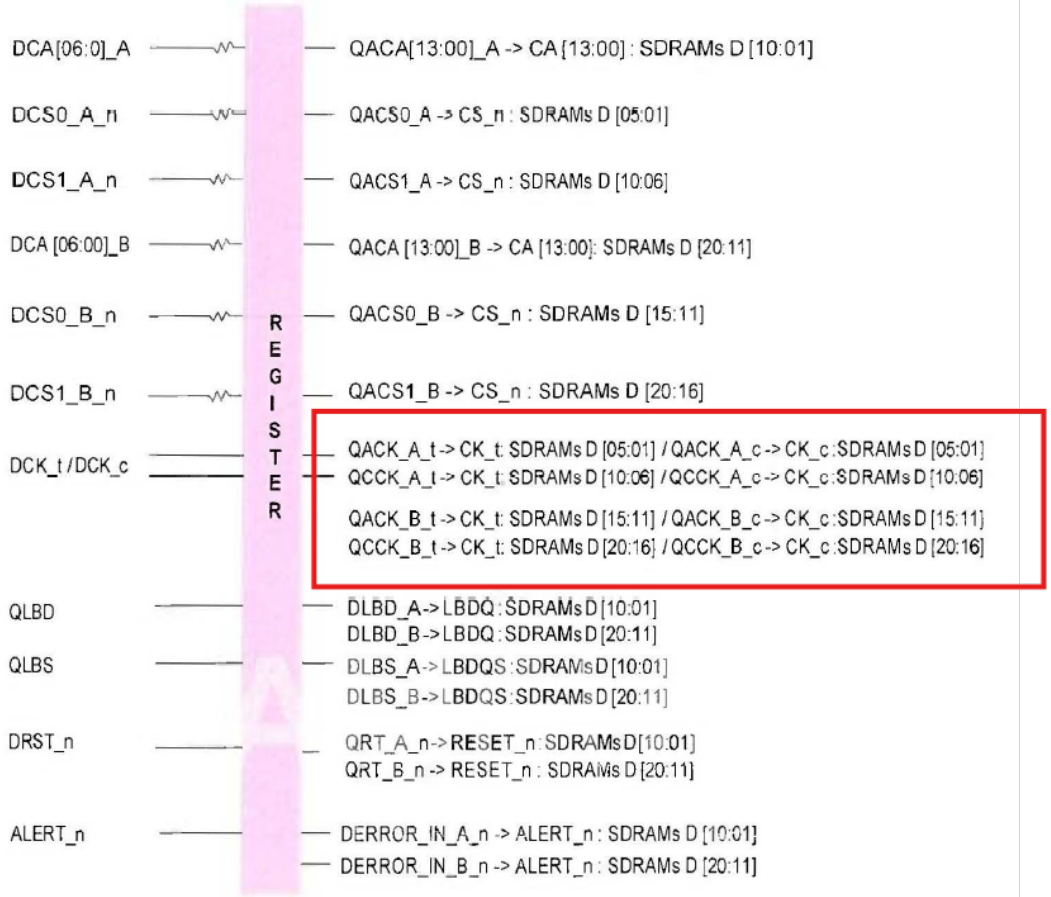
Claim 1	Evidence of Use
	3.4.1 Double Data Rate DCA (cont'd)  NOTE Timing Diagram for 0 nCK command latency adder. **Figure 9 — DDR CA Multi-Command Timing Diagram Example** Ex. CC-30 (JEDEC 82-513) at 17.

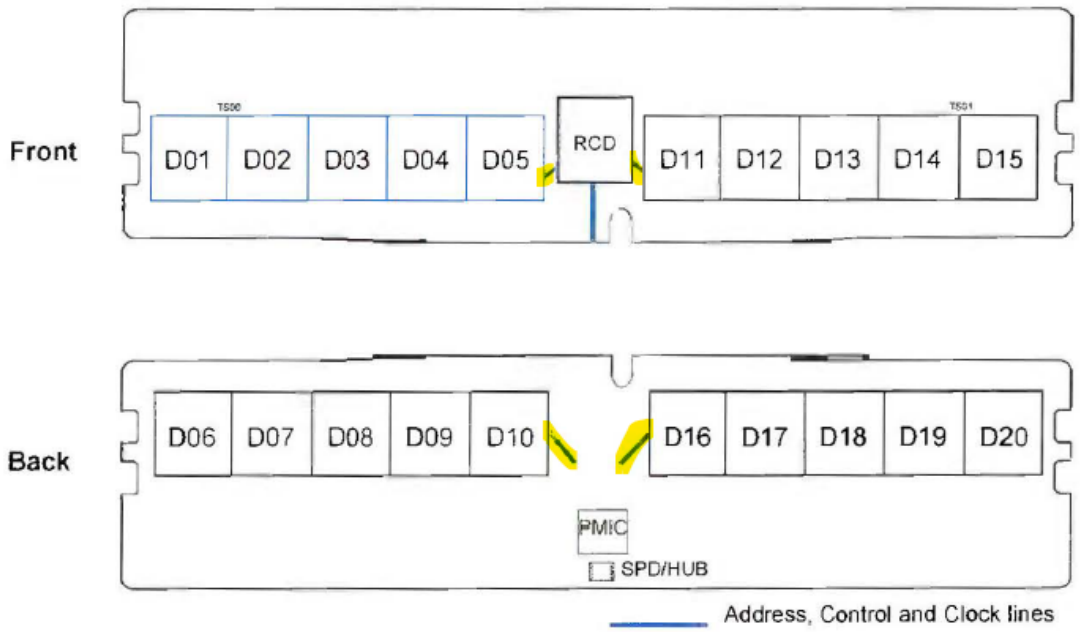
Claim 1	Evidence of Use
	The JEDEC DDR5 RDIMM standard further demonstrates that the Samsung Practicing '407 Products generate module C/A signals (*e.g.,* "QACA[]_A," "QBCA[]_A," "QACA[]_B," and "QBCA[]_B") in response to the input C/A signals (*e.g.,* "DCA[]_A" and "DCA[]_B"). *See, e.g.,* **6.1 Signal Groups** This standard categorizes DDR5 SDRAM timing-critical signals into specific groups. Figure 2 — (Example) RDIMM 2Rx4 Topology summarizes the high-speed signal groups for RDIMM. Signal groups, except Data and Strobe, implement a fly-by topology. Actual signal names in Annex may vary from individual reference design. The signal groups are: Pre-RCD - Pre-RCD CA and CS group includes: DCA[6:0]_[B:A], DCS[1:0]_[B:A]_n, DPAR_[B:A] - Pre-RCD Clock group includes: DCK_t and DCK_c - Pre-RCD Other group includes: ALERT_n, DRST_n - Pre-RCD Loopback group includes: DLBDQ_[B:A], DLBDQS_[B:A] Post-RCD to SDRAM - Post-RCD CA group includes Q[B:A]CA[13:0]_[B:A] - Post-RCD CS group includes Q[B:A]CS[1:0]_[B:A]_n - Post-RCD Clock group includes Q[D:A]CK_[B:A]_t, Q[D:A]CK_[B:A]_c - Post-RCD Other group includes QRST_[B:A]_n, DERROR_[B:A]_n - Post-RCD Other group includes QLBDQ_[B:A], QLBDQS_[B:A] DQ and DQS - edge connector pin to SDRAM with series resistor SideBand - Host to Hub group: HSDA, HSCL, HSA - Hub local bus group: LSDA, LSCL (star topology from Hub) Ex. CC-88 (JEDEC 305B) at 12 (that RCD receives from the memory controller Pre-RCD command and address signals and generate Post-RCD command and address signals).

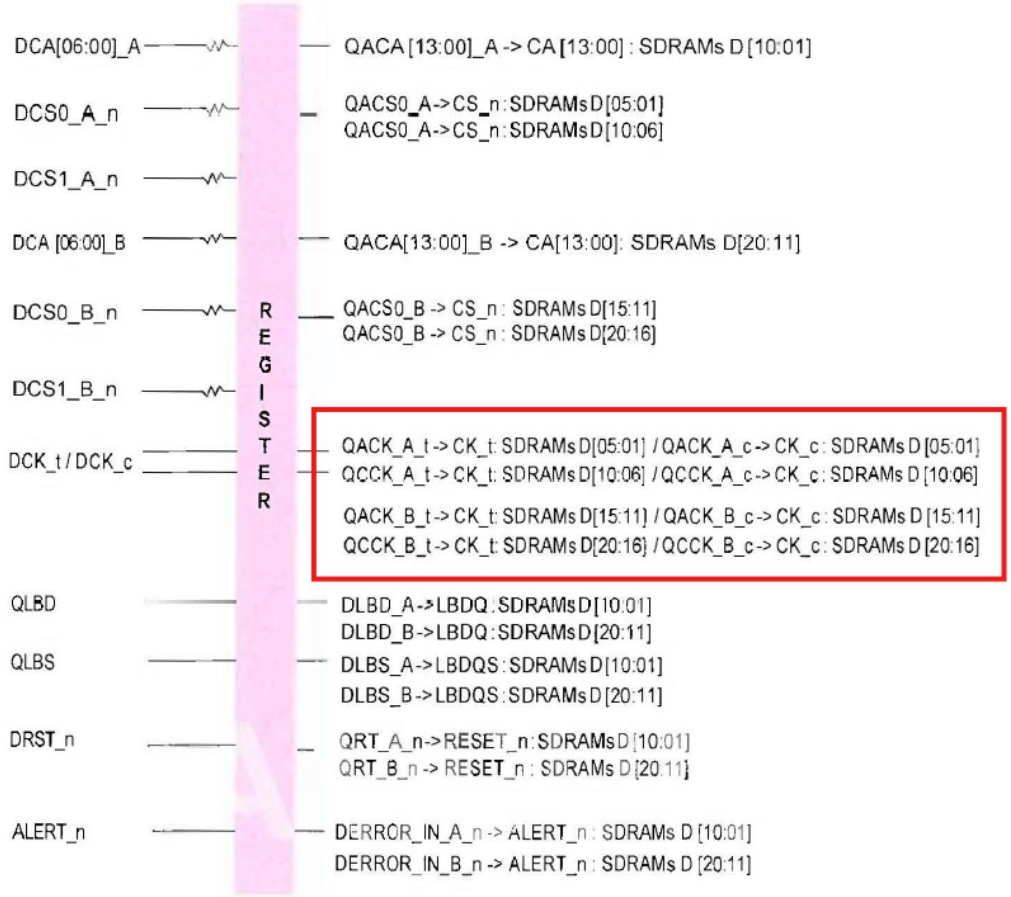
Claim 1	Evidence of Use
[**1.c.3**] generate a plurality of local clocks corresponding, respectively, to the plurality of groups of the memory devices,	The Samsung Practicing ’407 Products comprise circuitry mounted on the PCB and configurable to generate a plurality of local clocks corresponding, respectively, to the plurality of groups of the memory devices. For example, the RCD circuitry is configurable to generate local clock outputs corresponding to the groups of memory devices associated with Channels A and B in different ranks and different locations on the PCB. *See, e.g.,*

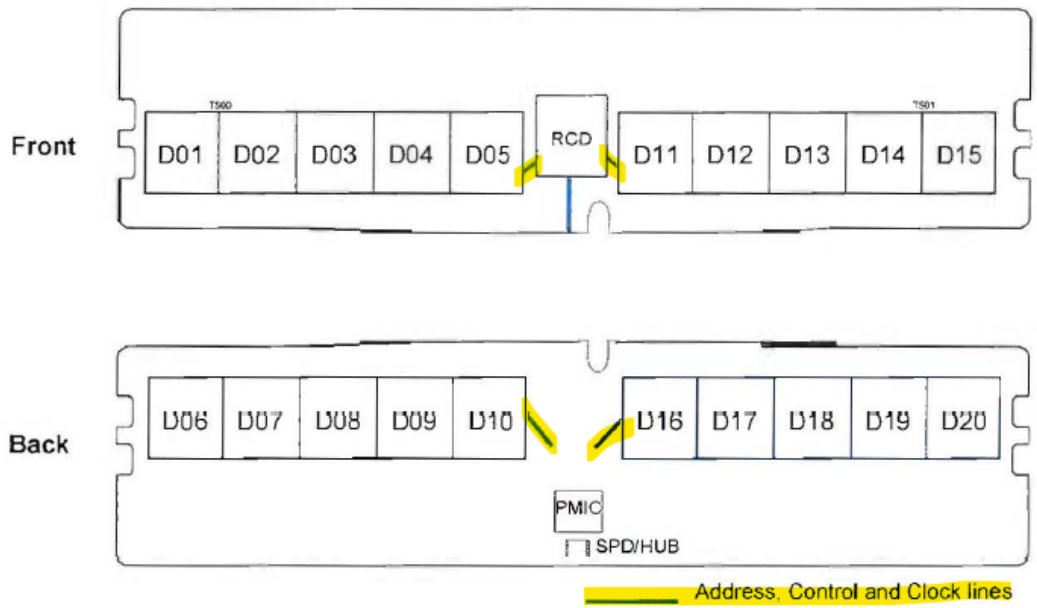

DCA[6:0]_A
QACA [13:0] _A -> CA [13:0]: SDRAMs D [1,2,8,9,10]
DCS0_A_n
QACS0_A -> CS_n: SDRAMs D [1,2,8,9,10]
DCS1_A_n
DCA[6:0]_B
QACA [13:0] _B -> CA [13:0]: SDRAMs D [7:3]
DCS0_B_n
QACS0_B -> CS_n: SDRAMs D [7:3]
DCS1_B_n
REGISTER
DCK_t
DCK_c
QACK_A_t/c -> CK_t/c: SDRAMs D [1,2,8,9,10]
QACK_A_t/c -> CK_t/c: SDRAMs D [7,3]
QLBD
DLBD_A -> LBDQ: SDRAMs D [1,2,8,9,10]
DLBD_B -> LBDQ: SDRAMs D [7;3]
QLBS
DLBS_A -> LBDQS: SDRAMs D [1,2,8,9,10]
DLBS_B -> LBDQS: SDRAMs D [7,3]
DRST_n
QRT_A_n -> RESET_n: SDRAMs D[1,2,8,9,10]
QRT_B_n -> RESET_n: SDRAMs D[7;3]
ALERT_n
DERROR_IN_A_n -> ALERT_n: SDRAMs D [1,2,8,9,10]
DERROR_IN_B_n -> ALERT_n: SDRAMs D [40:21]

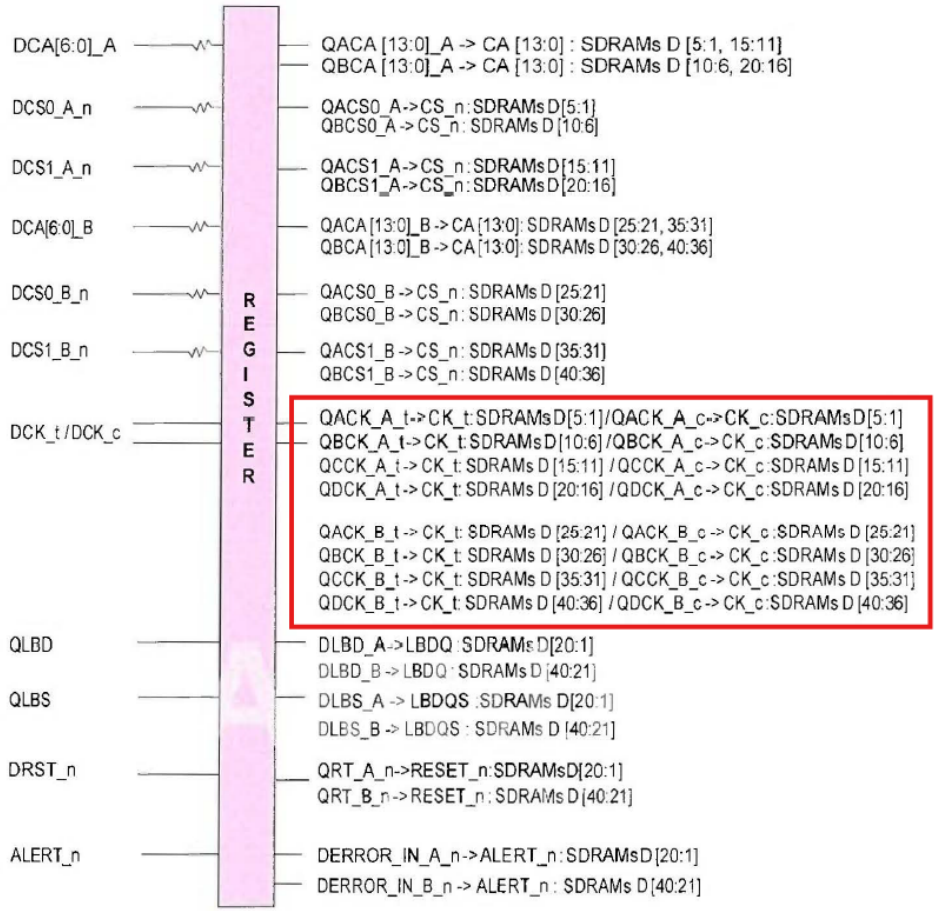
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 21 (RCD generates two sets of local clocks from DCK_t/c corresponding to groups of memory devices: QACK_A_t/c and QACK_B_t/c).

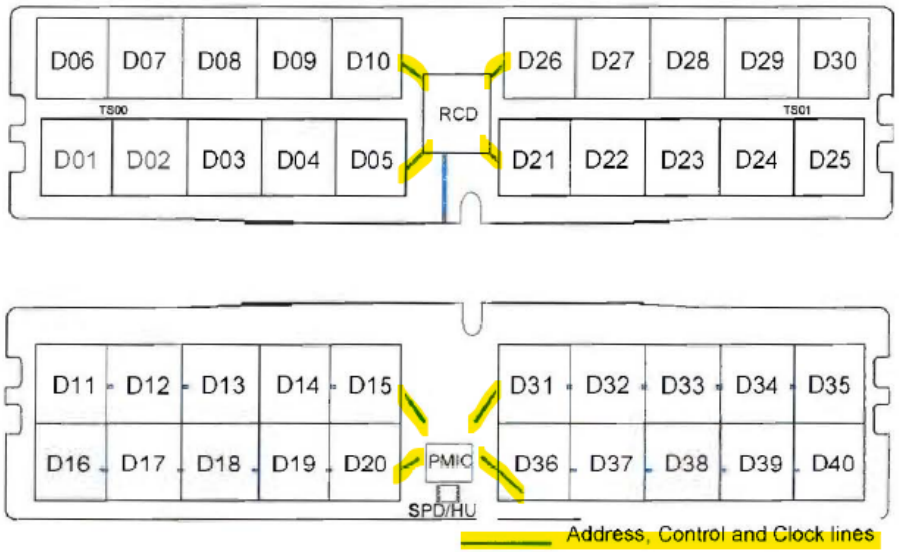
Claim 1	Evidence of Use
	

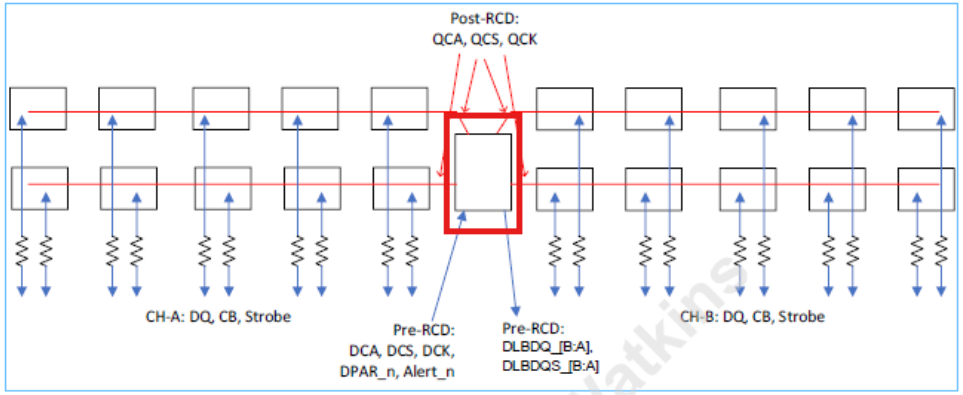
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 25 (RCD generates four sets of local clocks from DCK_t/c corresponding to groups of memory devices: QACK_A_t/c, QCCK_A_t/c, QACK_B_t/c, and QCCK_B_t/c).

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 29 (RCD generates four sets of local clocks from DCK_t/c corresponding to groups of memory devices: QACK_A_t/c, QCCK_A_t/c, QACK_B_t/c, QCCK_B_t/c).

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 29 (RCD generates eights sets of local clocks from DCK_t/c corresponding to groups of memory devices: QACK_A_t/c, QBCK_A_t/c, QCCK_A_t/c, QDCK_A_t/c, QACK_B_t/c, QBCK_B_t/c, QCCK_B_t/c, and QDCK_B_t/c). As explained *supra*, the Samsung Practicing ’407 Products are JEDEC compliant. The JEDEC DDR5 RDIMM standard further demonstrates each Samsung Practicing ’407 Products’ RCD generates multiple local clock signals corresponding, respectively, to the plurality of groups of the memory devices. For example, the RCD generates multiple QCK clock signals.

Claim 1	Evidence of Use
	6.1 Signal Groups (cont'd)  **Figure 2 — (Example) RDIMM 2Rx4 Topology** Ex. CC-88 (JEDEC 305B) at 13 (illustrating RCD, in red, receiving "Pre-RCD" clock ("DCK") and generating "Post-RCD" control and address signals ("QCK")).

Claim 1	Evidence of Use

6.9.1 DIMM Connectivity Wiring

2Rx4					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Top	Upper	QBCK	QBCS0	QBCA	0
Bottom	Lower	QCCK	QACS1	QACA	1
Bottom	Upper	QDCK	QBCS1	QBCA	1

2Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Top		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]
Bottom	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]

2Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Top	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]
Bottom		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

1Rx4					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QCCK	QBCS0	QACA	0

1Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]

1Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

2Rx8					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QCCK	QACS1	QACA	1

2Rx8 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	
Bottom	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	

2Rx8 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	
Bottom	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	

Claim 1	Evidence of Use

6.9.1 DIMM Connectivity Wiring (cont'd)

1Rx8 (less than 8000 Mbps)					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QACK	QACS0	QACA	0
1Rx8 (8000 Mbps and Faster)					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QCCK	QACS0	QACA	0
Bottom	Lower	QCCK	QACS0	QACA	0

1Rx8 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top			[15:8]				[31:24]			
Bottom	[7:0]				[23:16]				CB[7:0]	

1Rx8 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]				[23:16]					
Bottom			[15:8]				[31:24]		CB[7:0]	

Figure 12 — DIMM Connectivity Wiring

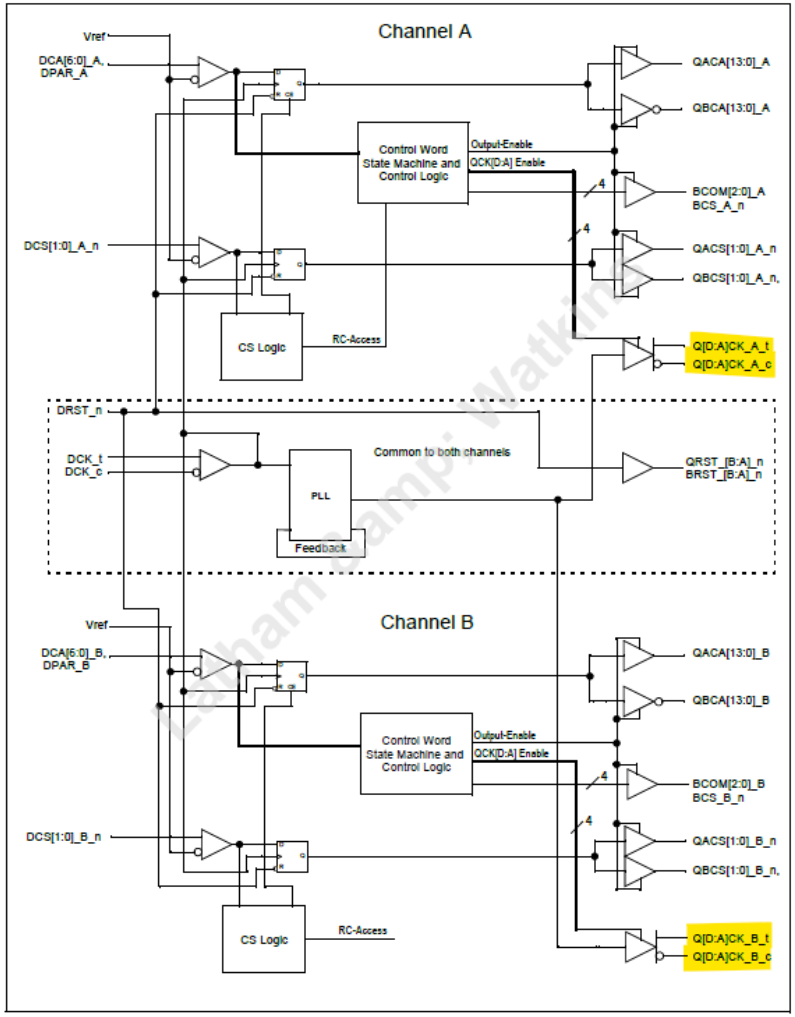
Ex. CC-88 (JEDEC 305B) at 31-32 (showing groups of memory devices on various sides and in various rows on the module configured to receive corresponding local clocks, e.g., QACK, QBCK, QCCK, QDCK, generated by the RCD).

Furthermore, the RCD in the Samsung Practicing '407 Products comply with JEDEC DDR5 RCD specification. The JEDEC DDR5 RCD specification explains the RCD generates a plurality of local clocks corresponding, respectively, to the plurality of groups of the memory devices. *See, e.g.,*

			cycles (i.e., Deselect).
Clock outputs	Q[D:A]CK_[B:A]_t Q[D:A]CK_[B:A]_c	POD differential	Clock outputs to the DRAMs. Four copies per channel.
Loopback	QLBD	POD	Loopback outputs to Host

Ex. CC-32 (JEDEC 82-512) at 4 (showing the RCD includes clock outputs for the memory devices).

Claim 1	Evidence of Use
	3.1 Description The DDR5RCD02 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs. It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels. Ex. CC-32 (JEDEC 82-512) at 6.

Claim 1	Evidence of Use
	3.2 Logic Diagram Positive Logic  Ex. CC-32 (JEDEC 82-512) at 7.

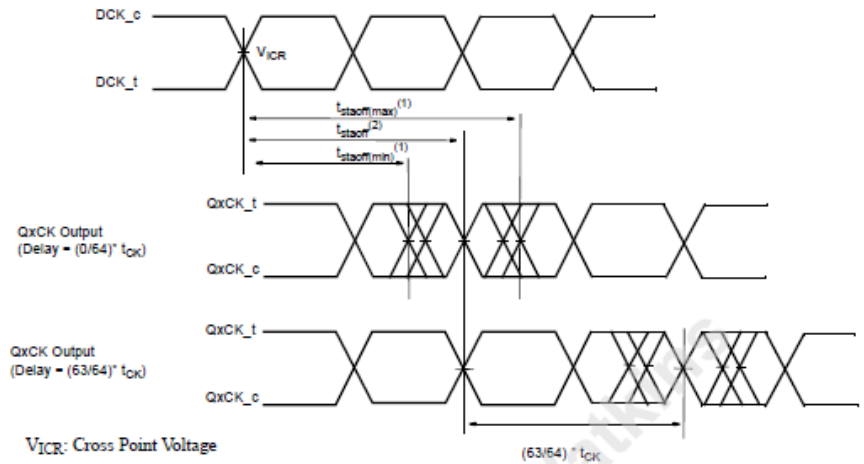
Claim 1	Evidence of Use
[**1.c.3.i**] the plurality of local clocks having respective phase relationships with the system clock,	In the Samsung Practicing ’407 Products, the plurality of local clocks have respective phase relationships with the system clock. As explained *supra*, the Samsung Practicing ’407 Products are JEDEC compliant. The JEDEC DDR5 RCD definition demonstrates the RCD of the Samsung Practicing ’407 Products supports “output delay control,” where the local clocks have respective phase relationships with the system clock. *See, e.g.,* **3.3.8 Per-group Output Delay Control** The RCD supports output delay control for output signal groups defined and located in RW12 to RW1E. The output delay settings are incremental CK fractions of 1/64 tCK. Each signal group can be enabled or disable independently through RCD Control Words. The Host must wait t_{ODU} after the Output Delay Control Word has been written to a signal group before the output becomes stable. The output delay feature controlled by RW12 to RW1E is not supported when the RCD is configured in Test Frequency mode (Band 2, RW05[7] = 1) or in PLL bypass mode (RW05[3:0] = 1111). Ex. CC-32 (JEDEC 82-512) at 12.

Claim 1	Evidence of Use
	Table 23 — Control Words Duplicated for Frequency Context Support

Register Address	Description
RW0A	QCK Signals Driver Characteristics Control Word
RW0C	QxCA and QxCS_n Signals Driver Characteristics Control Word
RW0D	Data Buffer Interface Driver Characteristics Control Word
RW10	IBT Control Word
RW11[3:0]	Command Latency Adder Configuration Control Word
RW12	QACK Output Delay Control Word
RW13	QBCK Output Delay Control Word
RW14	QCCK Output Delay Control Word
RW15	QDCK Output Delay Control Word
RW17 .. RW1A	QxCS_n Output Delay Control Word
RW1B, RW1C	QxCA Output Delay Control Word
RW1D	BCS_n and BCOM[2:0] Output Delay Control Word
RW1E	BCK Output Delay Control Word
RW31[7:4, 0]	DFE Configuration Control Word
RW40 .. RW47	Internal VrefCA Control Word
RW48, RW49	Internal VrefCS Control Word
RW50[0], RW51, RW52[3:0], RW53[3:0], RW54	CTLE Control Words
PG[00, 01]	DFE Gain and Tap 1, Tap 2, Tap 3, Tap 4 Coefficients per Input Receiver
PG[5]RW[7B:60]	Per-bit QCA Output Delay Control Words

Ex. CC-32 (JEDEC 82-512) at 68 (showing local clocks QACK, QBCK, QCCK, and QDCK that have respective phase relationships with the system clock).

For example, local clocks (QxCK) shown below have respective phase relationships with respect to the system clock (DCK).

Claim 1	Evidence of Use
	14.7 Output Clock Driver Characteristics (cont'd)  **Figure 112 — Definition for tstaoff and tdynoff in SDR Mode** Ex. CC-32 (JEDEC 82-512) at 242.

Claim 1	Evidence of Use

8.13.2 RW12 - QACK Output Delay Control Word

Table 118 — RW12: QACK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QACK_t/ QACK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64)* t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QACK_t/QACK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

NOTE 1 These control bits do not have any effect unless RW12[7] = 1.
NOTE 2 RW12[7:0] will be sticky, cleared by power cycle not Reset.
NOTE 3 When feature is enabled the delay settings in RW12[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

Ex. CC-32 (JEDEC 82-512) at 146; *see also id.* at 147-148 (showing tables 119, 120, and 121).

3.3.8 Per-group Output Delay Control

The RCD supports output delay control for output signal groups defined and located in RW12 to RW1E. The output delay settings are incremental CK fractions of 1/64 tCK. Each signal group can be enabled or disable independently through RCD Control Words. The Host must wait t_{ODU} after the Output Delay Control Word has been written to a signal group before the output becomes stable.

3.3.8 Per-group Output Delay Control (cont'd)

The output delay feature controlled by RW12 to RW1E is not supported when the RCD is configured in Test Frequency mode (Band 2, RW05[7] = 1) or in PLL bypass mode (RW05[3:0] = 1111).

Ex. CC-30 (JEDEC 82-513) at 11-12.

Claim 1	Evidence of Use
	Table 23 — Control Words Duplicated for Frequency Context Support **Register Address** / **Description** RW0A — QCK Signals Driver Characteristics Control Word RW0C — QxCA and QxCS_n Signals Driver Characteristics Control Word RW0D — Data Buffer Interface Driver Characteristics Control Word RW10 — IBT Control Word RW11[3:0] — Command Latency Adder Configuration Control Word RW12 — QACK Output Delay Control Word RW13 — QBCK Output Delay Control Word RW14 — QCCK Output Delay Control Word RW15 — QDCK Output Delay Control Word RW17 .. RW1A — QxCS_n Output Delay Control Word RW1B, RW1C — QxCA Output Delay Control Word RW1D — BCS_n and BCOM[2:0] Output Delay Control Word RW1E — BCK Output Delay Control Word RW31[7:4, 0] — DFE Configuration Control Word RW33[7:6] — DFE Tap 5 and Tap 6 Configuration Control Word RW40 .. RW47 — Internal VrefCA Control Word RW48, RW49 — Internal VrefCS Control Word RW50[0], RW51, RW52[3:0], RW53[3:0], RW54 — CTLE Control Words PG[00, 01] — DFE Gain and Tap 1, Tap 2, Tap 3, Tap 4, Tap 5, Tap 6 Coefficients per Input Receiver PG[5]RW[7B:60] — Per-bit QCA Output Delay Control Words Ex. CC-30 (JEDEC 82-513) at 70 (showing local clocks QACK, QBCK, QCCK, and QDCK that have respective phase relationships with the system clock).

Claim 1	Evidence of Use

8.13.2 RW12 - QACK Output Delay Control Word

Table 119 — RW12: QACK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QACK_t/ QACK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64)* t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QACK_t/QACK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

NOTE 1 These control bits do not have any effect unless RW12[7] = 1.
NOTE 2 RW12[7:0] will be sticky, cleared by power cycle not Reset.
NOTE 3 When feature is enabled the delay settings in RW12[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.3 RW13 - QBCK Output Delay Control Word

Table 120 — RW13: QBCK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QBCK_t/ QBCK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QBCK_t/QBCK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

NOTE 1 These control bits do not have any effect unless RW13[7] = 1.
NOTE 2 RW13[7:0] will be sticky, cleared by power cycle not Reset.
NOTE 3 When feature is enabled the delay settings in RW13[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.4 RW14 - QCCK Output Delay Control Word

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Table 121 — RW14: QCCK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QCCK_t/ QCCK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QCCK_t/QCCK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

NOTE 1 These control bits do not have any effect unless RW14[7] = 1.
NOTE 2 RW14[7:0] will be sticky, cleared by power cycle not Reset.
NOTE 3 When feature is enabled the delay settings in RW14[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

Claim 1	Evidence of Use

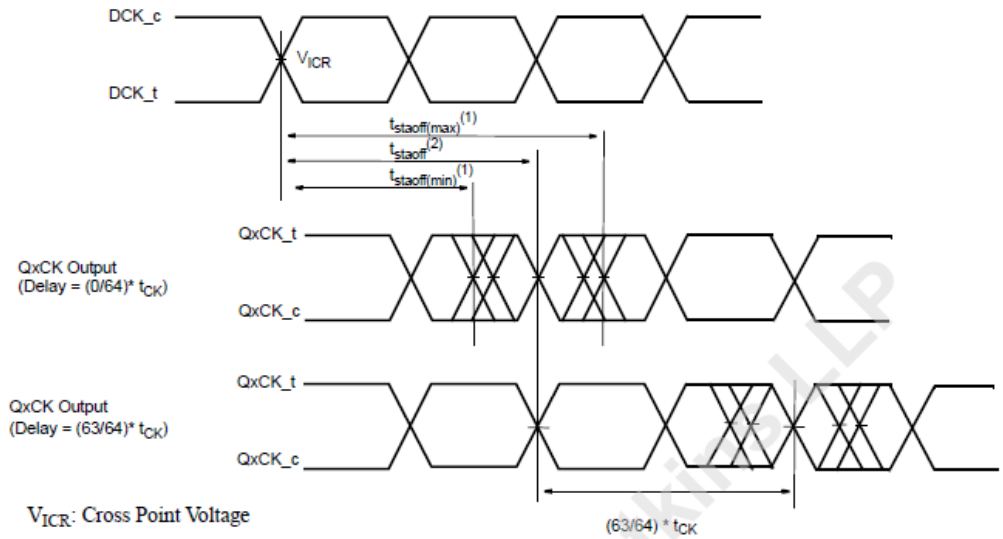
8.13.5 RW15 - QDCK Output Delay Control Word

Table 122 — RW15: QDCK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QDCK_t/ QDCK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QDCK_t/QDCK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

NOTE 1 These control bits do not have any effect unless RW15[7] = 1.
NOTE 2 RW15[7:0] will be sticky, cleared by power cycle not Reset.
NOTE 3 When feature is enabled the delay settings in RW15[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

Ex. CC-30 (JEDEC 82-513) at 150-152 (showing that local clocks QACK, QBCK, QCCK, and QDCK have respective phase relationships with the system clock).

Claim 1	Evidence of Use
	14.7 Output Clock Driver Characteristics (cont'd)  1. $t_{staoff(max/min)}$ = propagation delay specification limits for clock signal (rising DCK input clock edge to rising QxCK output clock edge for corresponding data cycles) over process, voltage and temperature. 2. t_{staoff} = measured propagation delay for clock signal (rising DCK input clock edge to rising QxCK output clock edge for corresponding data cycles). 3. t_{dynoff} = maximum propagation delay variation over voltage and temperature within t_{staoff} window. This includes all sources of jitter and drift (e.g. thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc.) except reference clock noise. **Figure 112 — Definition for tstaoff and tdynoff in SDR Mode** Ex. CC-30 (JEDEC 82-513) at 253.
[**1.c.3.ii**] the respective phase relationships being	In the Samsung Practicing '407 Products, the respective phase relationships are programmable independently of each other.

Claim 1	Evidence of Use
programmable independently of each other; and	As explained *supra*, the Samsung Practicing ’407 Products are JEDEC compliant. The JEDEC DDR5 RCD definition demonstrates the RCD of the Samsung Practicing ’407 Products supports “output delay control,” where the local clocks have respective phase relationships with the system clock. The delay control of the local clocks (QxCK) with respect to the system clock (DCK) can be independently programmed. *See, e.g.,* **3.3.8 Per-group Output Delay Control** The RCD supports output delay control for output signal groups defined and located in RW12 to RW1E. The output delay settings are incremental CK fractions of 1/64 tCK. Each signal group can be enabled or disable independently through RCD Control Words. The Host must wait t_{ODU} after the Output Delay Control Word has been written to a signal group before the output becomes stable. The output delay feature controlled by RW12 to RW1E is not supported when the RCD is configured in Test Frequency mode (Band 2, RW05[7] = 1) or in PLL bypass mode (RW05[3:0] = 1111). Ex. CC-32 (JEDEC 82-512) at 12 (showing “output delay” for output signal groups).

Claim 1	Evidence of Use
	Table 23 — Control Words Duplicated for Frequency Context Support Ex. CC-32 (JEDEC 82-512) at 68 (showing delays in QACK, QBCK, QCCK, and QDCK can be set independently).

Register Address	Description
RW0A	QCK Signals Driver Characteristics Control Word
RW0C	QxCA and QxCS_n Signals Driver Characteristics Control Word
RW0D	Data Buffer Interface Driver Characteristics Control Word
RW10	IBT Control Word
RW11[3:0]	Command Latency Adder Configuration Control Word
RW12	QACK Output Delay Control Word
RW13	QBCK Output Delay Control Word
RW14	QCCK Output Delay Control Word
RW15	QDCK Output Delay Control Word
RW17 .. RW1A	QxCS_n Output Delay Control Word
RW1B, RW1C	QxCA Output Delay Control Word
RW1D	BCS_n and BCOM[2:0] Output Delay Control Word
RW1E	BCK Output Delay Control Word
RW31[7:4, 0]	DFE Configuration Control Word
RW40 .. RW47	Internal VrefCA Control Word
RW48, RW49	Internal VrefCS Control Word
RW50[0], RW51, RW52[3:0], RW53[3:0], RW54	CTLE Control Words
PG[00, 01]	DFE Gain and Tap 1, Tap 2, Tap 3, Tap 4 Coefficients per Input Receiver
PG[5]RW[7B:60]	Per-bit QCA Output Delay Control Words

Claim 1	Evidence of Use
	8.13.2 RW12 - QACK Output Delay Control Word **Table 118 — RW12: QACK Output Delay Control Word** Setting: OP7 OP6 OP5 OP4 OP3 OP2 OP1 OP0 x x 0 0 0 0 0 0 — Output Delay Control for QACK_t/QACK_c Output Signals[1,2] — Delay Outputs by +(0/64) * t_{CK} (Same as Default) x x 0 0 0 0 0 1 — Delay Outputs by +(1/64) * t_{CK} x x 0 0 0 0 1 0 — Delay Outputs by +(2/64)* t_{CK} x x ... — ... x x 1 1 1 1 0 1 — Delay Outputs by +(61/64) * t_{CK} x x 1 1 1 1 1 0 — Delay Outputs by +(62/64) * t_{CK} x x 1 1 1 1 1 1 — Delay Outputs by +(63/64) * t_{CK} x 0 x x x x x x — Reserved — Reserved x 1 x x x x x x — Reserved 0 x x x x x x x — Output Delay Feature Enable for QACK_t/QACK_c[2] — (Default) Feature Disabled 1 x x x x x x x — Feature Enabled[3] NOTE 1 These control bits do not have any effect unless RW12[7] = 1. NOTE 2 RW12[7:0] will be sticky, cleared by power cycle not Reset. NOTE 3 When feature is enabled the delay settings in RW12[5:0] require a time of t_{ODU} for the delay to become stable on the outputs. Ex. CC-32 (JEDEC 82-512) at 146; *see also id.* at 147-148 (showing how to program the delays independently, in tables 119, 120, and 121).

Claim 1	Evidence of Use

Table 232 — Output Clock Driver Characteristics at Application Mode (Frequency Band 1) (cont'd)

Symbol	Parameter	Conditions	DDR5-3200		DDR5-3600		DDR5-4000/ 4400/4800		DDR5-5200/ 5600		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
tSTAB_DBDATA	LRDIMM stabilization time for commands requiring use of data path	DCK_t/DCK_c stable	-	4.14	-	4.14	-	4.14	-	4.14	µs	4,5
t_{CKsk}	Fractional Clock Output Skew		-	20	-	20	-	20	-	20	ps	6
t_{staoff}	Clock delay through the register between the input clock and output clock		Min:(t_{PDM}(min) + 1/2 tCK); Max: (t_{PDM}(max) + 1/2 tCK)								ps	7,8
t_{dynoff}	Maximum re-driven dynamic clock offset		-	40	-	35	-	35	-	35	ps	9,10

NOTE 1 At Down-bin Data Rate (1980 MT/s ≤ f ≤ 2100 MT/s), the max value of tSTAB01 is 10µs.

NOTE 2 This parameter applies to control word writes to RW05/RW06 and Bit OP0 in RW00. Since application of RW05/RW06 is postponed in the frequency change sequence defined in Section 5.4.2, a t_{STAB01} waiting time is always sufficient after exit from Self Refresh with Clock Stop (i.e., t_{STAB02} is not required). See timing diagrams in Figure 35 on page 48 and Figure 36 on page 49.

NOTE 3 Measured from start of DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface but does not require the use of data path (e.g., SRX, NOP, etc.).

NOTE 4 Applies only to Self Refresh Exit without frequency change.

NOTE 5 Measured from start of DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface and requires the use of data path (e.g., WR, RD).

NOTE 6 This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 113). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to left side clock pairs between QACK_A_t/QACK_A_c and QCCK_A_t/QCCK_A_c, as well as right side of the clock pairs between QACK_B_t/QACK_B_c and QCCK_B_t/QCCK_B_c. Similarly, to left side clock pairs between QBCK_A_t/QBCK_A_c and QDCK_A_t/QDCK_A_c, as well as right side of the clock pairs between QBCK_B_t/QBCK_B_c and QDCK_B_t/QDCK_B_c. This is not a tested parameter and has to be considered as a design goal only.

NOTE 7 RW05/RW06 must be set to correct speed and the device must run at one of the speed nodes defined in Table 199 on page 191. See Figure 111 and Figure 112.

NOTE 8 This measures the delay from the rising differential input clock which samples incoming DCA to the rising differential output clock that will be used to sample the same QCA data. The parameter describes the maximum and minimum QxCK clock t_{PD}.

NOTE 9 V_{DD} measurement DC bandwidth is limited to 20 MHz.

NOTE 10 See Figure 111 and Figure 112.

Ex. CC-32 (JEDEC 82-512) at 240 (describing "output clock skew" that "is specified for the clock pairs on each side of the register independently").

Claim 1	Evidence of Use

14.7 Output Clock Driver Characteristics (cont'd)

Table 233 — Output Clock Driver Characteristics at Test Mode (Frequency Band 2)

Symbol	Parameter	Conditions	Test Frequency (140 to 990 MHz)		Unit	Note
			Min	Max		
tSTAB01	RCD Stabilization time from start of DCK toggle to PLL lock	DCK_t/DCK_c stable	-	50	µs	
tSTAB02	RCD Stabilization time from control word write to PLL lock	DCK_t/DCK_c stable	-	50	µs	1
t_{CKsk}	Fractional Clock Output Skew		-	100	ps	2
t_{staoff}	Clock delay through the register between the input clock and output clock		Min:(t_{PDM}(min) + 1/2 tCK); Max: (t_{PDM}(max) + 1/2 tCK)		ps	3,4
t_{dynoff}	Maximum re-driven dynamic clock offset		-	500	ps	5,6

NOTE 1 This parameter applies to control word writes to RW05 and Bit OP0 in RW00.

NOTE 2 This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 113). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to left side clock pairs between QACK_A_t/QACK_A_c and QCCK_A_t/QCCK_A_c, as well as right side of the clock pairs between QACK_B_t/QACK_B_c and QCCK_B_t/QCCK_B_c. Similarly, to left side clock pairs between QBCK_A_t/QBCK_A_c and QDCK_A_t/QDCK_A_c, as well as right side of the clock pairs between QBCK_B_t/QBCK_B_c and QDCK_B_t/QDCK_B_c. This is not a tested parameter and has to be considered as a design goal only.

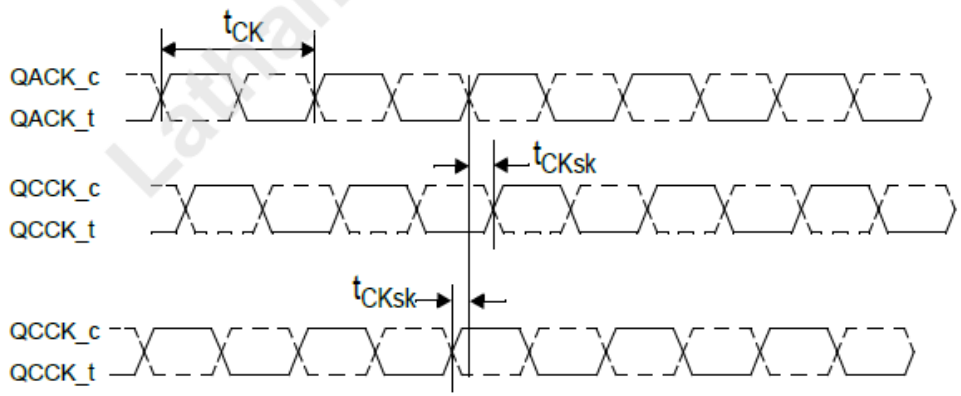
NOTE 3 RW05 must not be set to enable PLL bypass mode and the device must run within the Test Frequency range defined in Table 199 on page 191. See Figure 111 and Figure 112.

NOTE 4 This measures the delay from the rising differential input clock which samples incoming DCA to the rising differential output clock that will be used to sample the same QCA data. The parameter describes the maximum and minimum QxCK clock t_{PD}.

NOTE 5 V_{DD} measurement DC bandwidth is limited to 20 MHz.

NOTE 6 See Figure 111 and Figure 112.

Ex. CC-32 (JEDEC 82-512) at 241 (describing "output clock skew" that "is specified for the clock pairs on each side of the register independently").

Claim 1	Evidence of Use
	 **Figure 113 — Clock Output (QxCK) Skew** Ex. CC-32 (JEDEC 82-512) at 242. **3.3.8 Per-group Output Delay Control** The RCD supports output delay control for output signal groups defined and located in RW12 to RW1E. The output delay settings are incremental CK fractions of 1/64 tCK. Each signal group can be enabled or disable independently through RCD Control Words. The Host must wait t_{ODU} after the Output Delay Control Word has been written to a signal group before the output becomes stable. **3.3.8 Per-group Output Delay Control (cont'd)** The output delay feature controlled by RW12 to RW1E is not supported when the RCD is configured in Test Frequency mode (Band 2, RW05[7] = 1) or in PLL bypass mode (RW05[3:0] = 1111). Ex. CC-30 (JEDEC 82-513) at 11-12.

Claim 1	Evidence of Use
	Table 23 — Control Words Duplicated for Frequency Context Support

Register Address	Description
RW0A	QCK Signals Driver Characteristics Control Word
RW0C	QxCA and QxCS_n Signals Driver Characteristics Control Word
RW0D	Data Buffer Interface Driver Characteristics Control Word
RW10	IBT Control Word
RW11[3:0]	Command Latency Adder Configuration Control Word
RW12	QACK Output Delay Control Word
RW13	QBCK Output Delay Control Word
RW14	QCCK Output Delay Control Word
RW15	QDCK Output Delay Control Word
RW17 .. RW1A	QxCS_n Output Delay Control Word
RW1B, RW1C	QxCA Output Delay Control Word
RW1D	BCS_n and BCOM[2:0] Output Delay Control Word
RW1E	BCK Output Delay Control Word
RW31[7:4, 0]	DFE Configuration Control Word
RW33[7:6]	DFE Tap 5 and Tap 6 Configuration Control Word
RW40 .. RW47	Internal VrefCA Control Word
RW48, RW49	Internal VrefCS Control Word
RW50[0], RW51, RW52[3:0], RW53[3:0], RW54	CTLE Control Words
PG[00, 01]	DFE Gain and Tap 1, Tap 2, Tap 3, Tap 4, Tap 5, Tap 6 Coefficients per Input Receiver
PG[5]RW[7B:60]	Per-bit QCA Output Delay Control Words

Ex. CC-30 (JEDEC 82-513) at 70 (showing local clocks QACK, QBCK, QCCK, and QDCK that have respective phase relationships with the system clock).

Claim 1	Evidence of Use

8.13.2 RW12 - QACK Output Delay Control Word

Table 119 — RW12: QACK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QACK_t/ QACK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64)* t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QACK_t/QACK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

NOTE 1 These control bits do not have any effect unless RW12[7] = 1.
NOTE 2 RW12[7:0] will be sticky, cleared by power cycle not Reset.
NOTE 3 When feature is enabled the delay settings in RW12[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.3 RW13 - QBCK Output Delay Control Word

Table 120 — RW13: QBCK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QBCK_t/ QBCK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QBCK_t/QBCK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

NOTE 1 These control bits do not have any effect unless RW13[7] = 1.
NOTE 2 RW13[7:0] will be sticky, cleared by power cycle not Reset.
NOTE 3 When feature is enabled the delay settings in RW13[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.4 RW14 - QCCK Output Delay Control Word

Netlist Inc.

Table 121 — RW14: QCCK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QCCK_t/ QCCK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QCCK_t/QCCK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

NOTE 1 These control bits do not have any effect unless RW14[7] = 1.
NOTE 2 RW14[7:0] will be sticky, cleared by power cycle not Reset.
NOTE 3 When feature is enabled the delay settings in RW14[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

Claim 1	Evidence of Use

8.13.5 RW15 - QDCK Output Delay Control Word

Table 122 — RW15: QDCK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QDCK_t/ QDCK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QDCK_t/QDCK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

NOTE 1 These control bits do not have any effect unless RW15[7] = 1.
NOTE 2 RW15[7:0] will be sticky, cleared by power cycle not Reset.
NOTE 3 When feature is enabled the delay settings in RW15[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

Ex. CC-30 (JEDEC 82-513) at 150-152 (showing that local clocks QACK, QBCK, QCCK, and QDCK have respective phase relationships with the system clock).

14.7 Output Clock Driver Characteristics

Table 237 — Output Clock Driver Characteristics at Application Mode (Frequency Band 1)

Symbol	Parameter	Conditions	DDR5-3200		DDR5-3600		DDR5-4000~6400		Unit
			Min	Max	Min	Max	Min	Max	
t_{STAB01}[1]	RCD Stabilization time from start of DCK toggle to PLL lock	DCK_t/ DCK_c stable	-	3.5	-	3.5	-	3.5	µs
t_{STAB02}	RCD Stabilization time from control word write to PLL lock[2]	DCK_t/ DCK_c stable	-	25.0	-	25.0	-	25.0	µs
t_{STAB_DB}	Data Buffer Stabilization time	BCK_t/ BCK_c stable	See DDR5DB03 Specification						µs
t_{STAB_DBCMD}	LRDIMM stabilization time for commands **not** requiring use of data path[3,4]	DCK_t/ DCK_c stable	-	3.5	-	3.5	-	3.5	µs
t_{STAB_DBDATA}	LRDIMM stabilization time for commands requiring use of data path[5,4]	DCK_t/ DCK_c stable	-	4.14	-	4.14	-	4.14	µs
t_{CKsk}	Fractional Clock Output Skew[6]		-	20	-	20	-	20	ps
t_{staoff}[7]	Clock delay through the register between the input clock and output clock[8]		Min:(t_{PDM}(min) + 1/2 tCK); Max: (t_{PDM}(max) + 1/ 2 tCK)						ps
t_{dynoff}[9]	Maximum re-driven dynamic clock offset[10]		-	40	-	35	-	35	ps

NOTE 1 At Down-bin Data Rate (1980 MT/s ≤ f ≤ 2100 MT/s), the max value of tSTAB01 is 10 µs.

NOTE 2 This parameter applies to control word writes to RW05/RW06 and Bit OP0 in RW00. Since application of RW05/RW06 is postponed in the frequency change sequence defined in Section 5.4.2, a t_{STAB01} waiting time is always sufficient after exit from Self Refresh with Clock Stop (i.e., t_{STAB02} is not required). See timing diagrams in Figure 35 and Figure 36.

NOTE 3 Measured from start of DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface but does not require the use of data path (e.g., SRX, NOP, etc.).

NOTE 4 Applies only to Self Refresh Exit without frequency change.

NOTE 5 Measured from start of DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface and requires the use of data path (e.g., WR, RD).

NOTE 6 This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 113). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to left side clock pairs between QACK_A_t/ QACK_A_c and QCCK_A_t/QCCK_A_c, as well as right side of the clock pairs between QACK_B_t/QACK_B_c, and QCCK_B_t/ QCCK_B_c. Similarly, to left side clock pairs between QBCK_A_t/QBCK_A_c and QDCK_A_t/QDCK_A_c, as well as right side of the clock pairs between QBCK_B_t/QBCK_B_c and QDCK_B_t/QDCK_B_c. This is not a tested parameter and has to be considered as a design goal only.

NOTE 7 RW05/RW06 must be set to correct speed and the device must run at one of the speed nodes defined in Table 204. See Figure 111 and Figure 112.

NOTE 8 This measures the delay from the rising differential input clock which samples incoming DCA to the rising differential output clock that will be used to sample the same QCA data. The parameter describes the maximum and minimum QxCK clock t_{PD}.

NOTE 9 V_{DD} measurement DC bandwidth is limited to 20 MHz.

NOTE 10 See Figure 111 and Figure 112.

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Claim 1	Evidence of Use
	Ex. CC-32 (JEDEC 82-513) at 250 (describing "output clock skew" that "is specified for the clock pairs on each side of the register independently").

14.7 Output Clock Driver Characteristics (cont'd)

Table 238 — Output Clock Driver Characteristics at Test Mode (Frequency Band 2)

Symbol	Parameter	Conditions	Test Frequency (140 to 990 MHz)		Unit
			Min	Max	
t_{STAB01}	RCD Stabilization time from start of DCK toggle to PLL lock	DCK_t/DCK_c stable	-	50	µs
t_{STAB02}	RCD Stabilization time from control word write to PLL lock[1]	DCK_t/DCK_c stable	-	50	µs
t_{CKsk}	Fractional Clock Output Skew[2]		-	100	ps
t_{staoff}[3]	Clock delay through the register between the input clock and output clock[4]		Min:(t_{PDM}(min) + 1/2 tCK); Max: (t_{PDM}(max) + 1/2 tCK)		ps
t_{dynoff}[5]	Maximum re-driven dynamic clock offset[6]		-	500	ps

NOTE 1 This parameter applies to control word writes to RW05 and Bit OP0 in RW00.

NOTE 2 This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 113). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to left side clock pairs between QACK_A_t/QACK_A_c and QCCK_A_t/QCCK_A_c, as well as right side of the clock pairs between QACK_B_t/QACK_B_c, and QCCK_B_t/QCCK_B_c. Similarly, to left side clock pairs between QBCK_A_t/QBCK_A_c and QDCK_A_t/QDCK_A_c, as well as right side of the clock pairs between QBCK_B_t/QBCK_B_c, and QDCK_B_t/QDCK_B_c. This is not a tested parameter and has to be considered as a design goal only.

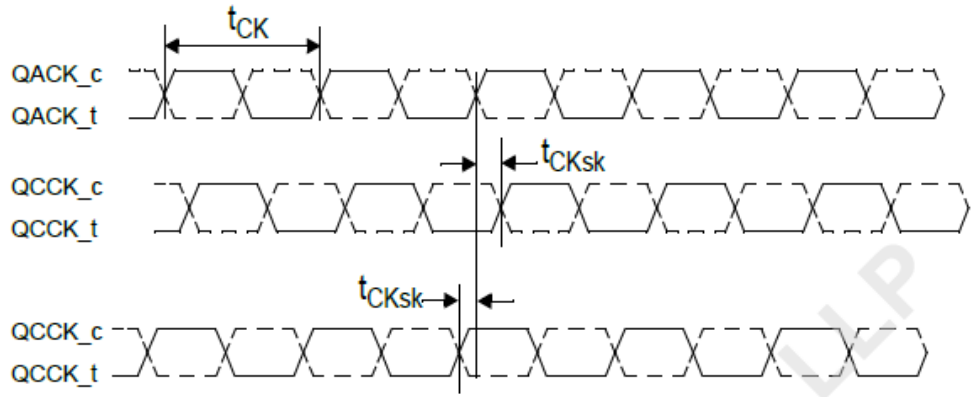
NOTE 3 RW05 must not be set to enable PLL bypass mode and the device must run within the Test Frequency range defined in Table 204. See Figure 111 and Figure 112.

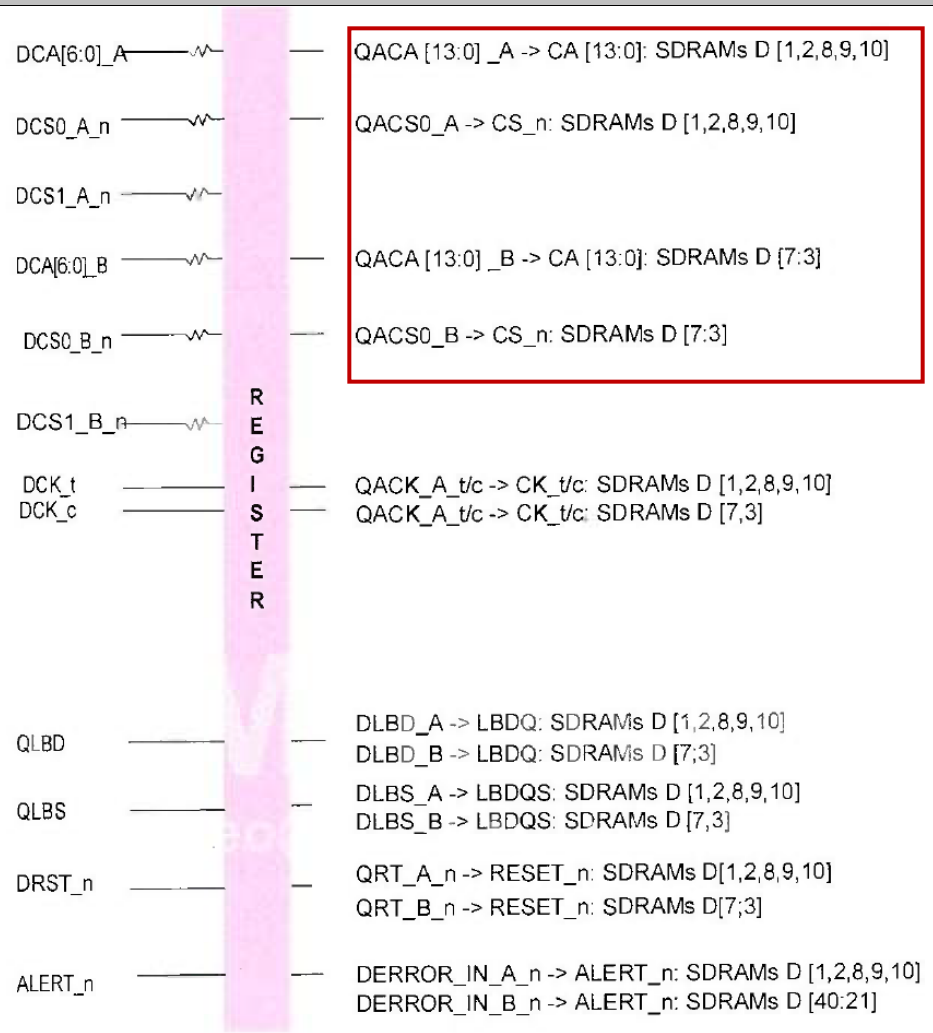
NOTE 4 This measures the delay from the rising differential input clock which samples incoming DCA to the rising differential output clock that will be used to sample the same QCA data. The parameter describes the maximum and minimum QxCK clock t_{PD}.

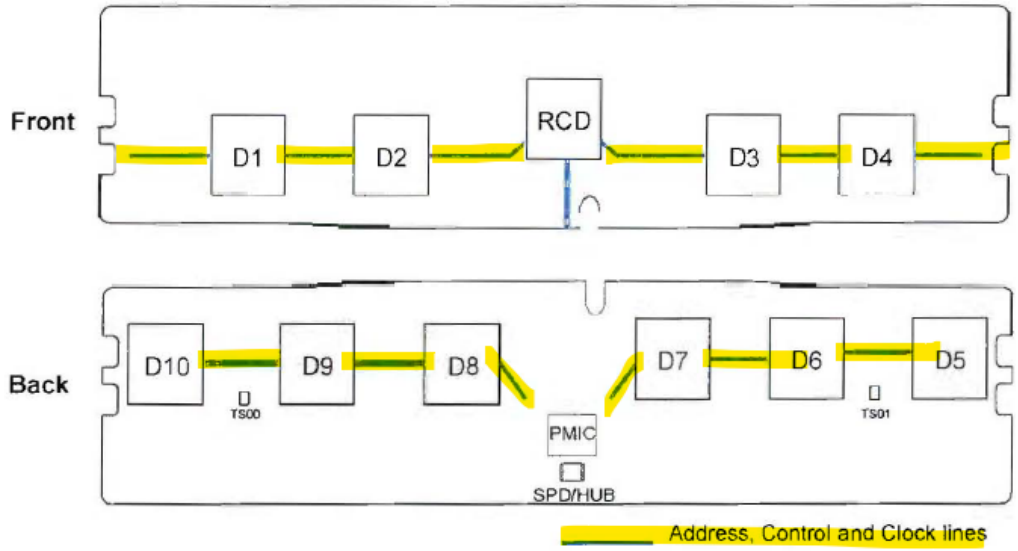
NOTE 5 V_{DD} measurement DC bandwidth is limited to 20 MHz.

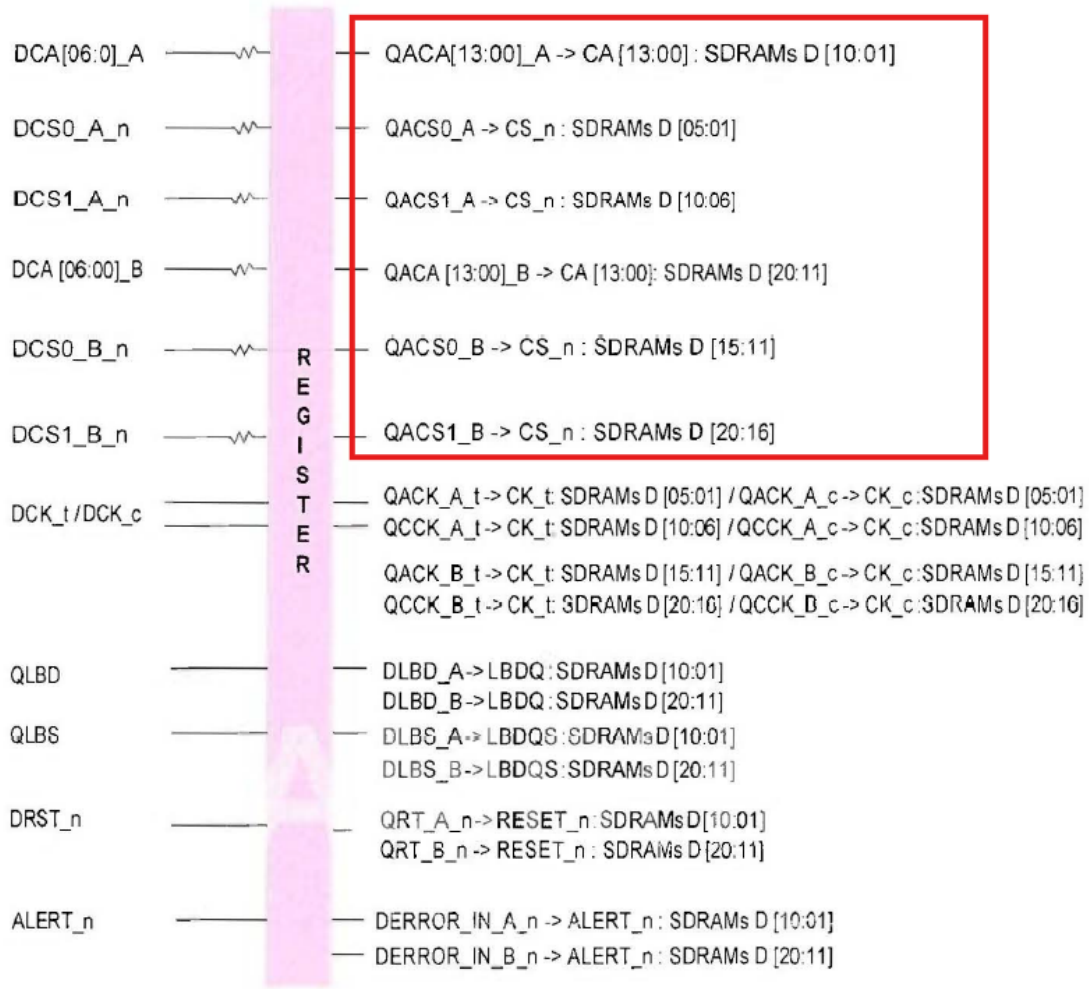
NOTE 6 See Figure 111 and Figure 112.

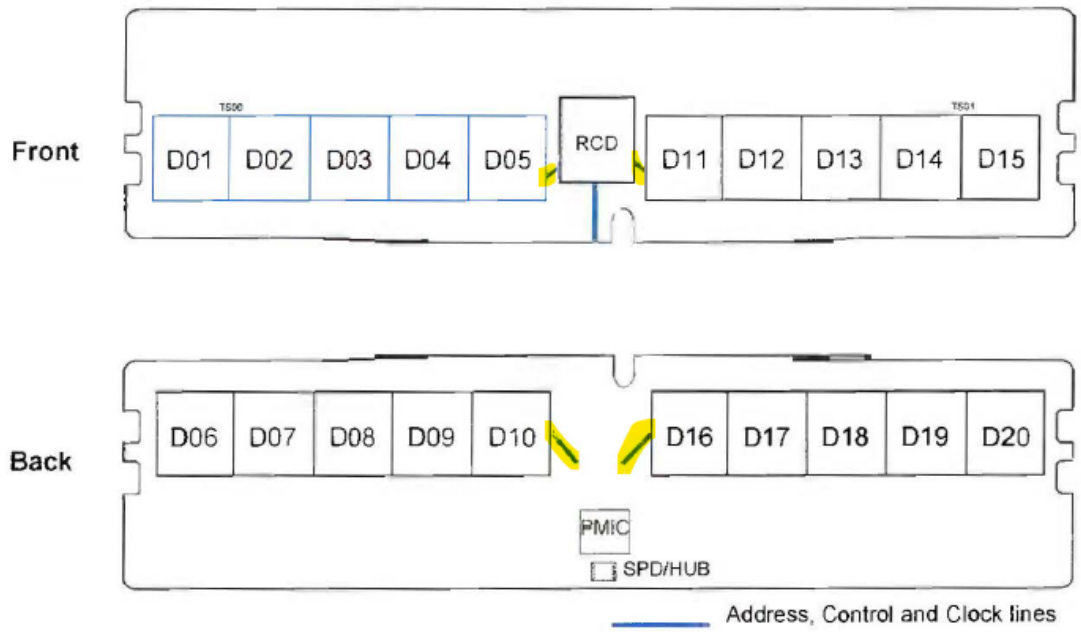
	Ex. CC-32 (JEDEC 82-513) at 251 (describing "output clock skew" that "is specified for the clock pairs on each side of the register independently").

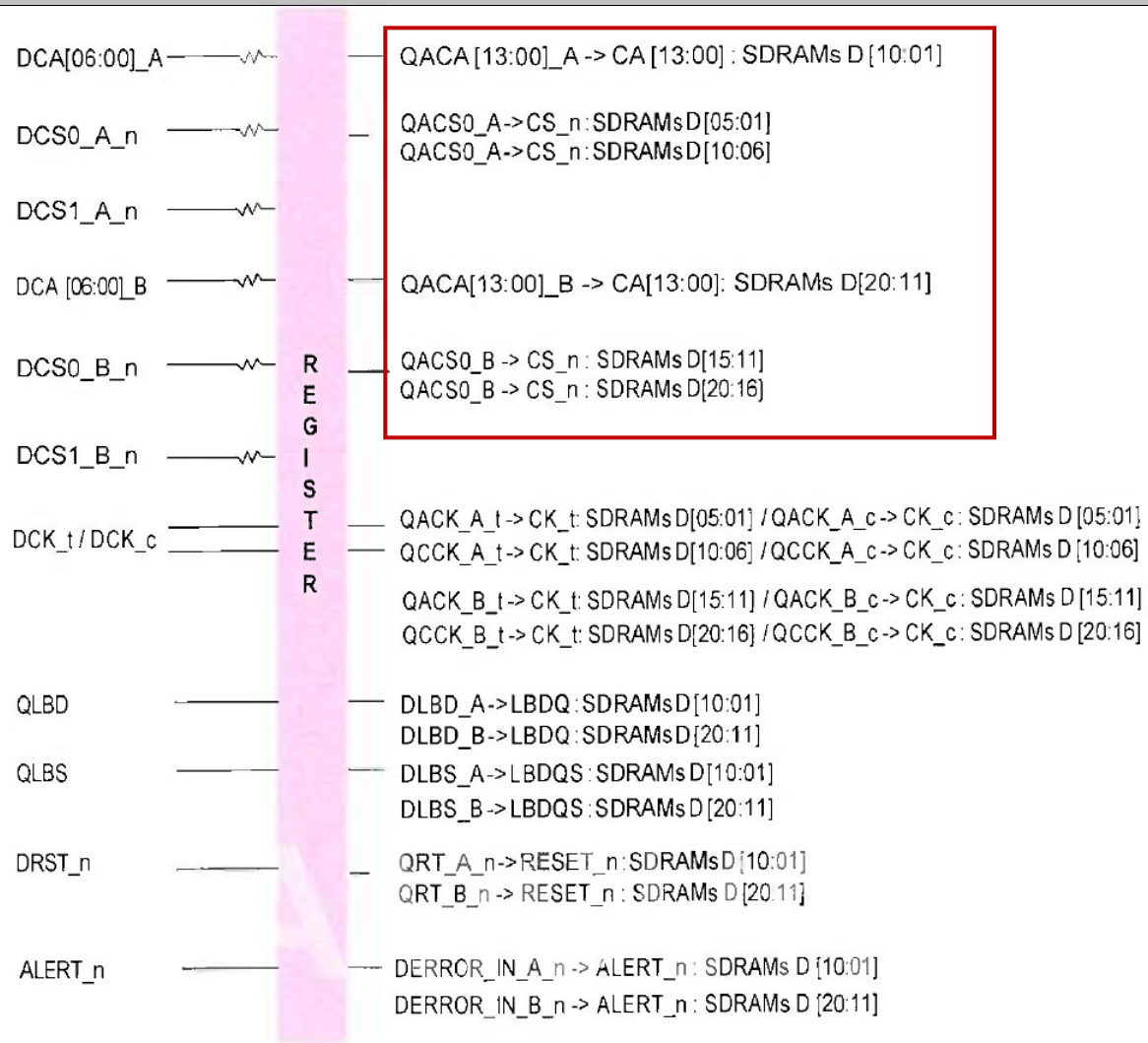
Claim 1	Evidence of Use
	14.7 Output Clock Driver Characteristics (cont'd)  **Figure 113 — Clock Output (QxCK) Skew** Ex. CC-32 (JEDEC 82-513) at 254.
[**1.c.4**] output the module C/A signals to the memory devices; and	*See* evidence cited for element [1.c.2]. The Samsung Practicing '407 Products comprise circuitry mounted on the PCB and configurable to output the module C/A signals to the memory devices. For example, the module C/A signals (such as QACA, QBCA, QACS and QBCS signals) are output to the SDRAM memory devices. *See, e.g.,*

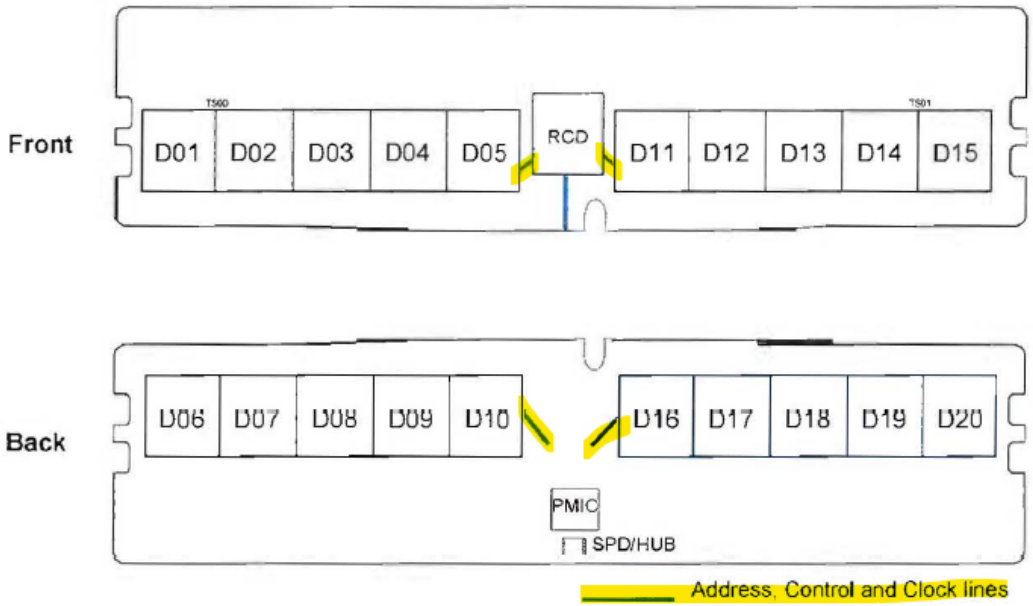
Claim 1	Evidence of Use
	

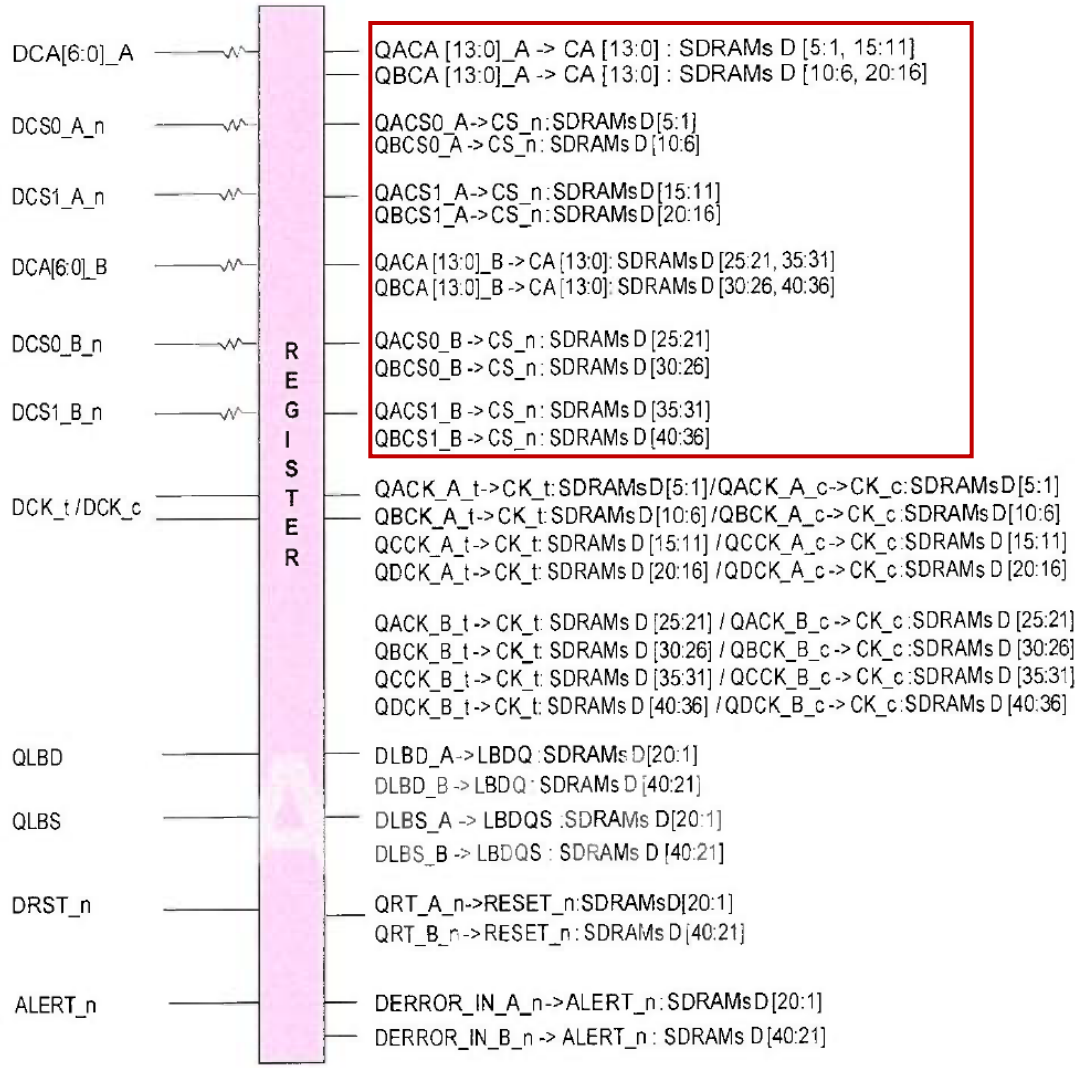
Claim 1	Evidence of Use
	 Ex. CC-89 at 21 (Samsung DDR5 RDIMM Datasheet)

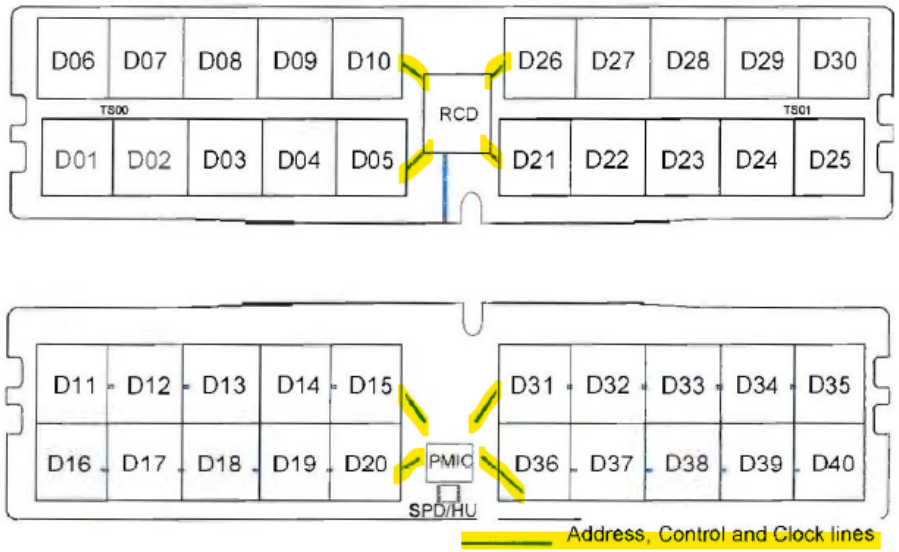
Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 at 25 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet)

Claim 1	Evidence of Use
	

Claim 1	Evidence of Use
	 Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet) As explained supra, the Samsung Practicing '407 Products are JEDEC compliant. According to the JEDEC RCD specifications, RCD outputs module C/A signals (such as QACA, QBCA, QACS and QBCS signals) in response to the input C/A signals (DCA and DCS) received from the host. **3.1 Description** The DDR5RCD02 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs. It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels.

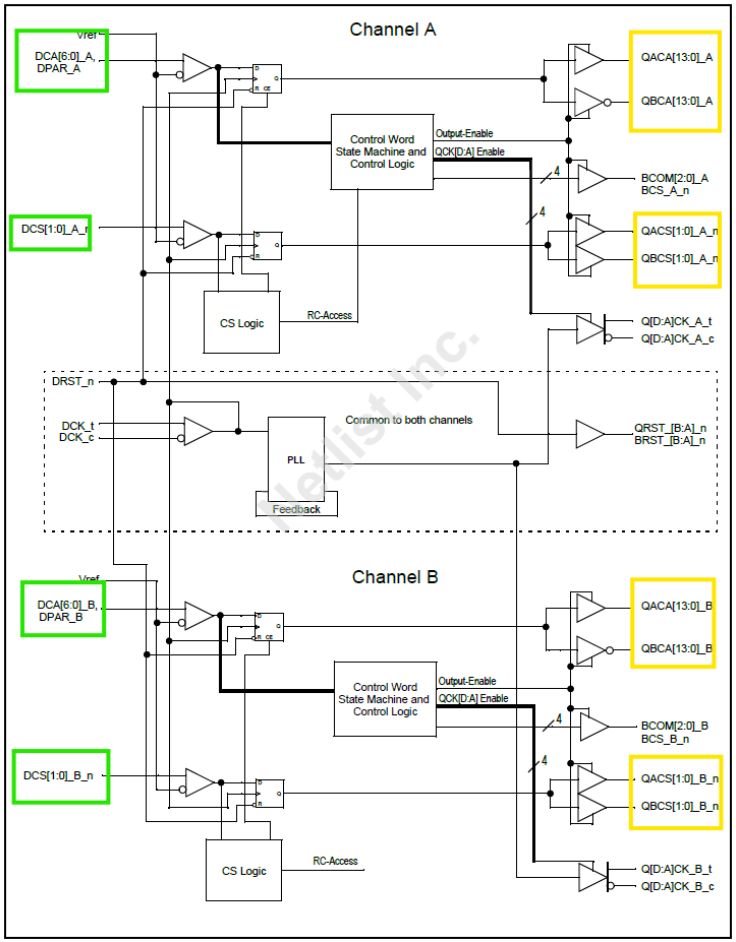
Claim 1	Evidence of Use
	Ex. CC-32 (JEDEC 82-512) at 6.

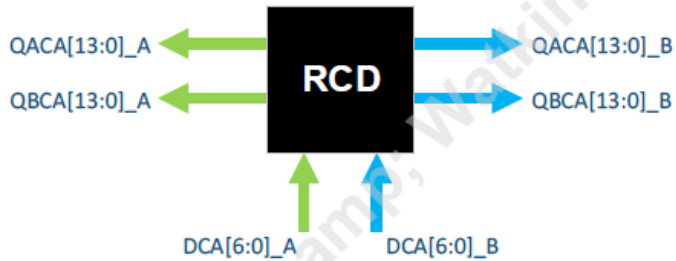
2.2 Terminal Functions

Table 2 — Terminal Functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCS[1:0]_[B:A]_n	POD V_{REF} based	Chip Select inputs to the RCD. Two inputs per DRAM channel.
Input Address and Command bus	DCA[6:0]_[B:A]	POD V_{REF} based	Command/Address bus inputs to the RCD. Separate sets per channel.
Parity input	DPAR_[B:A]	POD V_{REF} based	Command Address input parity is received on the DPAR pin and should maintain even parity across the CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
Clock inputs	DCK_t/DCK_c	POD differential	Differential system clock input pair to the PLL. The clock is common to both RCD channels, CH_A and CH_B.
Loopback	DLBD_[B:A] DLBS_[B:A]	POD V_{REF} based	Loopback Inputs to RCD DLBD - loopback Data DLBS - loopback Strobe
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Error input	DERROR_IN_[B:A]_n	Low voltage swing POD input	DRAM CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. There is a separate signal per channel.
Data buffer control and communication outputs	BCS_[B:A]_n	POD	Data buffer chip selects. Indicate a valid command on the BCOM bus, and used to signal non-target termination. Separate per DRAM channel.
	BCOM[2:0]_[B:A]	POD	Data buffer command. The start of each command is signaled by an active chip select. Separate per DRAM channel.
	BRST_[B:A]_n	CMOS	Re-driven or CMD based reset. This is an asynchronous output. It is the responsibility of the RCD BRST to reset the DDR5 Data Buffer on all DIMM topologies.
	BCK_[B:A]_t BCK_[B:A]_c	POD differential	Differential clock output pair to the data buffer. Separate per DRAM channel.
Output Control bus	Q[B:A]CS[1:0]_[B:A]_n	POD	Chip Select signals to the DRAMs. 2 copies of each signal.
Output Address and Command bus	Q[B:A]CA[13:0]_[B:A]	POD	Command/Address bus outputs to the DRAMs, valid after the specified clock count and immediately following a rising edge of the clock. Two copies of each signal. When Output Inversion is enabled in RW00[5], Copy B output signals get inverted during all commands other than Deselect. Both copies drive High during idle cycles (i.e., Deselect).
Clock outputs	Q[B:A]CK_[B:A]_t	POD differential	Clock outputs to the DRAMs. Four copies per channel

	Ex. CC-32 (JEDEC 82-512) at 4.

Claim 1	Evidence of Use
	 Ex. CC-32 (JEDEC 82-512) at 7 (showing the RCD circuitry outputs module C/A signals shown in yellow to memory devices).

Claim 1	Evidence of Use
	3.4.1 Double Data Rate DCA The DDR5 RCD will support DDR (Double Data Rate) on the host-interface DCA signals. The host-interface CA bus is 7 bits, plus parity. The DRAM-interface CA bus remains SDR (Single Data Rate) and is 14 bits and without parity. The RCD will expand the incoming host-interface 7-bit DCA bus to 14 bits on the DRAM interface. Table 8 shows the mapping of the incoming DCA bits to the output QCA. The Chip Selects remain SDR on both the host-interface and DRAM interface. The two channel DDR5RCD has six CA ports, two DCA input ports and four QCA output ports as shown in Figure 6. **Table 8 — DDR CA Mapping DCA to QCA** UI: DCA0, DCA1, DCA2, DCA3, DCA4, DCA5, DCA6 0: QCA0, QCA1, QCA2, QCA3, QCA4, QCA5, QCA6 1: QCA7, QCA8, QCA9, QCA10, QCA11, QCA12, QCA13  **Figure 6 — RCD DCA and QCA Ports** Ex. CC-32 (JEDEC 82-512) at 15. **3.3.3 QCA Bus Operation** Under normal operation, the RCD passes commands through from the D inputs to the Q outputs when a command is present on the bus, and drives HIGH on the QCA outputs when no command is being sent. The RCD passes the DCA bus through when either DCS input is active but there are exceptions to this: • If the register detects a parity error and parity checking is enabled, the DCA bus is still passed through to DRAM and QCS is blocked. • During the 2nd UI of a 2 UI command, the DCA bus must be passed through. There will only be a DCS signal active for the 2nd UI if a non-target termination is being signaled to a rank. • When DRAM interface Block MR Mode is enabled RW01[1] = 0. • When CA Pass-through mode is enabled RW00[2] = 1.

Claim 1	Evidence of Use
	Ex. CC-32 (JEDEC 82-512) at 9. **3.1 Description** The DDR5RCD03 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs. It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels. Ex. CC-30 (JEDEC 82-513) at 6.

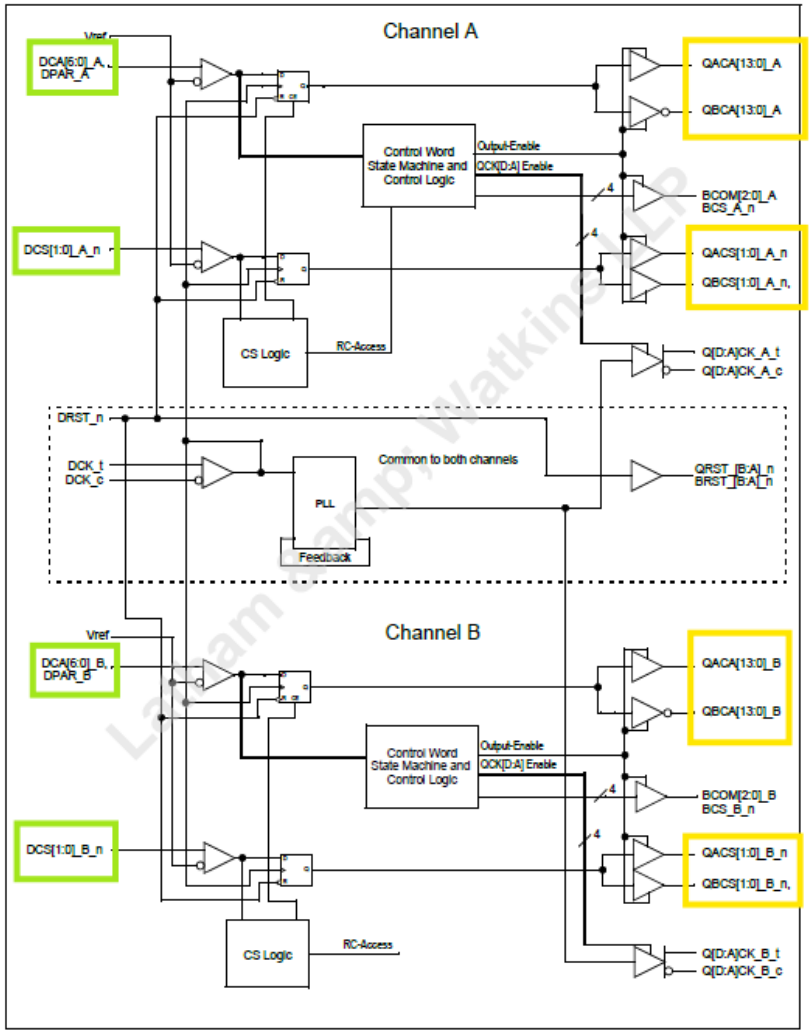
Claim 1	Evidence of Use

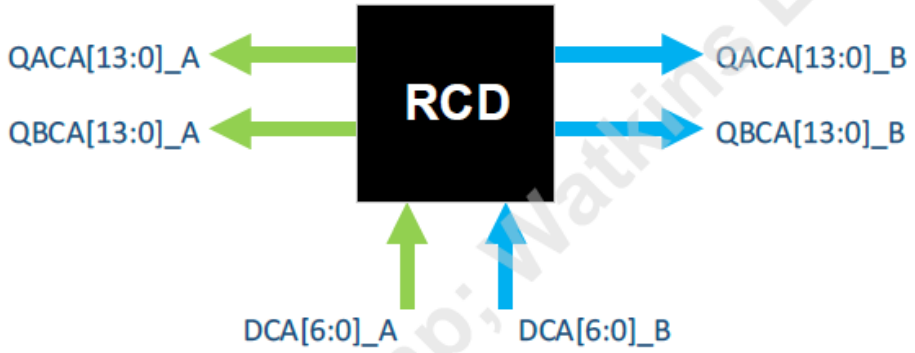
2.2 Terminal Functions

Table 2 — Terminal Functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCS[1:0]_[B:A]_n	POD V_{REF} based	Chip Select inputs to the RCD. Two inputs per DRAM channel.
Input Address and Command bus	DCA[6:0]_[B:A]	POD V_{REF} based	Command/Address bus inputs to the RCD. Separate sets per channel.
Parity input	DPAR_[B:A]	POD V_{REF} based	Command/Address input parity is received on the DPAR pin and should maintain even parity across the CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
Clock inputs	DCK_t/DCK_c	POD differential	Differential system clock input pair to the PLL. The clock is common to both RCD channels, CH_A and CH_B.
Loopback	DLBD_[B:A] DLBS_[B:A]	POD V_{REF} based	Loopback Inputs to RCD DLBD - loopback Data DLBS - loopback Strobe
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Error input	DERROR_IN_[B:A]_n	Low voltage swing POD input	DRAM CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. There is a separate signal per channel.
Data buffer control and communication outputs	BCS_[B:A]_n	POD	Data buffer chip selects. Indicate a valid command on the BCOM bus, and used to signal non-target termination. Separate per DRAM channel.
	BCOM[2:0]_[B:A]	POD	Data buffer command. The start of each command is signaled by an active chip select. Separate per DRAM channel.
	BRST_[B:A]_n	CMOS	Re-driven or CMD based reset. This is an asynchronous output. It is the responsibility of the RCD BRST to reset the DDR5 Data Buffer on all DIMM topologies.
	BCK_[B:A]_t BCK_[B:A]_c	POD differential	Differential clock output pair to the data buffer. Separate per DRAM channel.
Output Control bus	Q[B:A]CS[1:0]_[B:A]_n	POD	Chip Select signals to the DRAMs. 2 copies of each signal.
Output Address and Command bus	Q[B:A]CA[13:0]_[B:A]	POD	Command/Address bus outputs to the DRAMs, valid after the specified clock count and immediately following a rising edge of the clock. Two copies of each signal. When Output Inversion is enabled in RW00[5], Copy B output signals get inverted during all commands other than Deselect. Both copies drive High during idle cycles (i.e., Deselect).

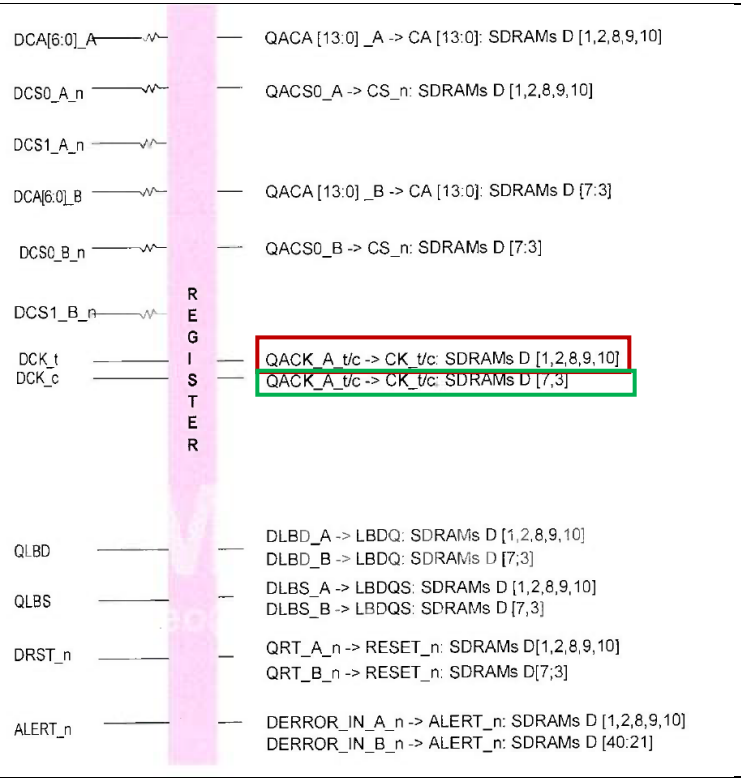
Ex. CC-30 (JEDEC 82-513) at 4.

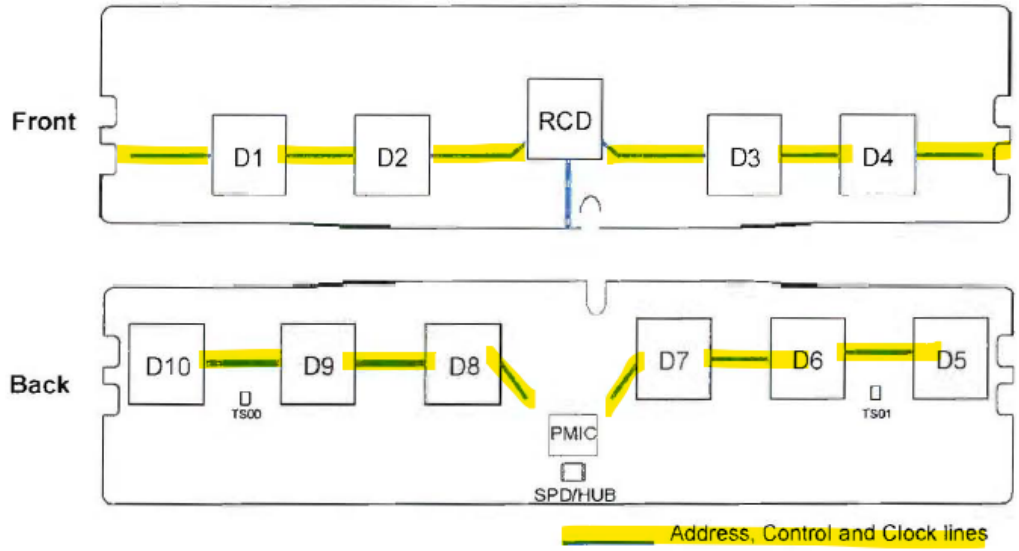
Claim 1	Evidence of Use
	 Ex. CC-30 (JEDEC 82-513) at 7 (showing the RCD circuitry generates module C/A signals shown in yellow in response to the input C/A signals shown in green).

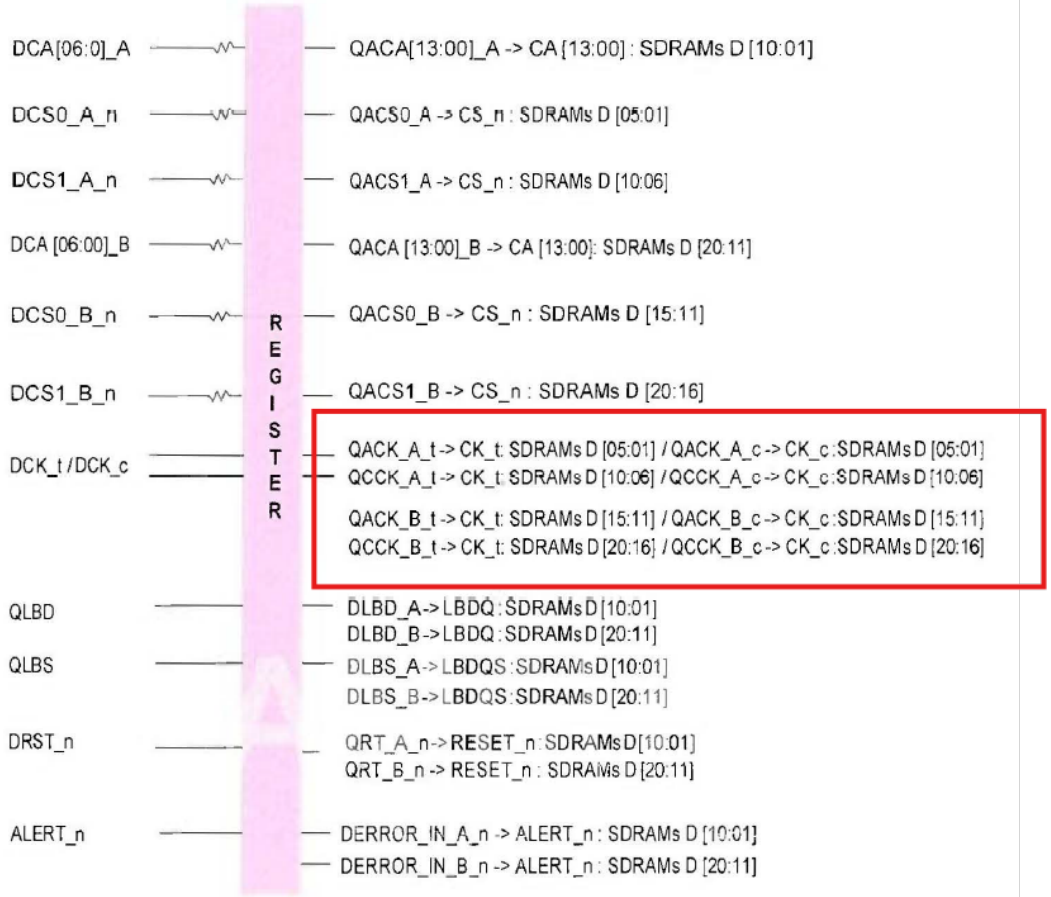
Claim 1	Evidence of Use
	3.4.1 Double Data Rate DCA The DDR5 RCD will support DDR (Double Data Rate) on the host-interface DCA signals. The host-interface CA bus is 7 bits, plus parity. The DRAM-interface CA bus remains SDR (Single Data Rate) and is 14 bits and without parity. The RCD will expand the incoming host-interface 7-bit DCA bus to 14 bits on the DRAM interface. Table 8 shows the mapping of the incoming DCA bits to the output QCA. The Chip Selects remain SDR on both the host-interface and DRAM interface. The two channel DDR5RCD has six CA ports, two DCA input ports and four QCA output ports as shown in Figure 6. **Table 8 — DDR CA Mapping DCA to QCA** UI: 0 — DCA0 QCA0, DCA1 QCA1, DCA2 QCA2, DCA3 QCA3, DCA4 QCA4, DCA5 QCA5, DCA6 QCA6 UI: 1 — DCA0 QCA7, DCA1 QCA8, DCA2 QCA9, DCA3 QCA10, DCA4 QCA11, DCA5 QCA12, DCA6 QCA13  **Figure 6 — RCD DCA and QCA Ports** Ex. CC-30 (JEDEC 82-513) at 15.

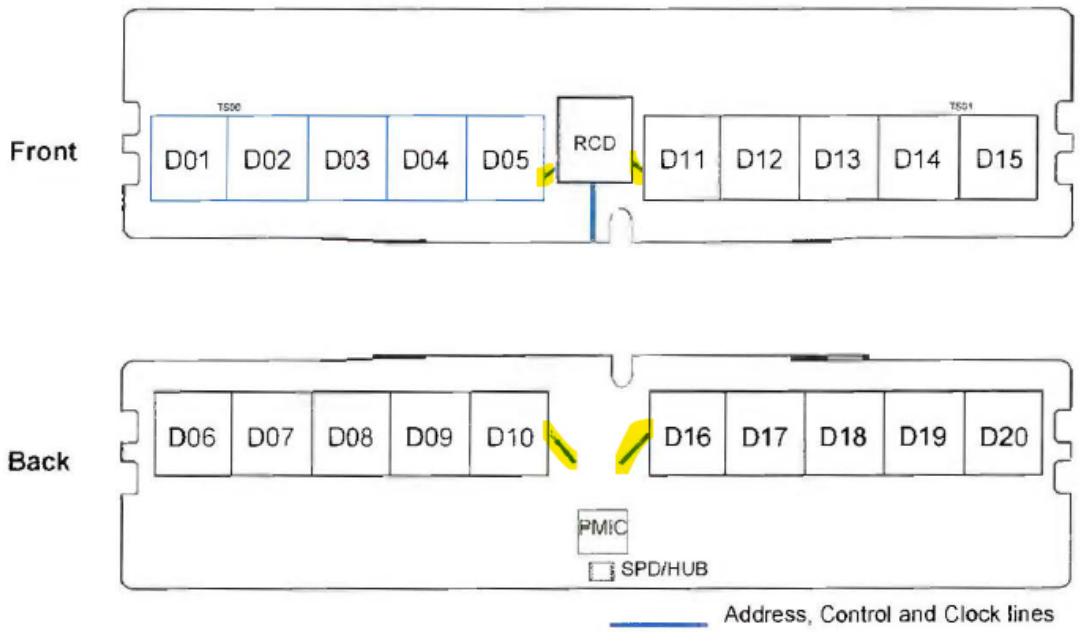
Claim 1	Evidence of Use
	3.3.3 QCA Bus Operation Under normal operation, the RCD passes commands through from the D inputs to the Q outputs when a command is present on the bus, and drives HIGH on the QCA outputs when no command is being sent. The RCD passes the DCA bus through when either DCS input is active but there are exceptions to this: • If the register detects a parity error and parity checking is enabled, the DCA bus is still passed through to DRAM and QCS is blocked. • During the 2nd UI of a 2 UI command, the DCA bus must be passed through. There will only be a DCS signal active for the 2nd UI if a non-target termination is being signaled to a rank. • When DRAM interface Block MR Mode is enabled RW01[1] = 0. • When CA Pass-through mode is enabled RW00[2] = 1. Ex. CC-30 (JEDEC 82-513) at 9. The JEDEC DDR5 RDIMM standard further demonstrates that the Samsung Practicing ’407 Products output module C/A signals (*e.g.,* “QACA[]_A,” “QBCA[]_A,” “QACA[]_B,” and “QBCA[]_B”) to memory devices. *See, e.g.,*

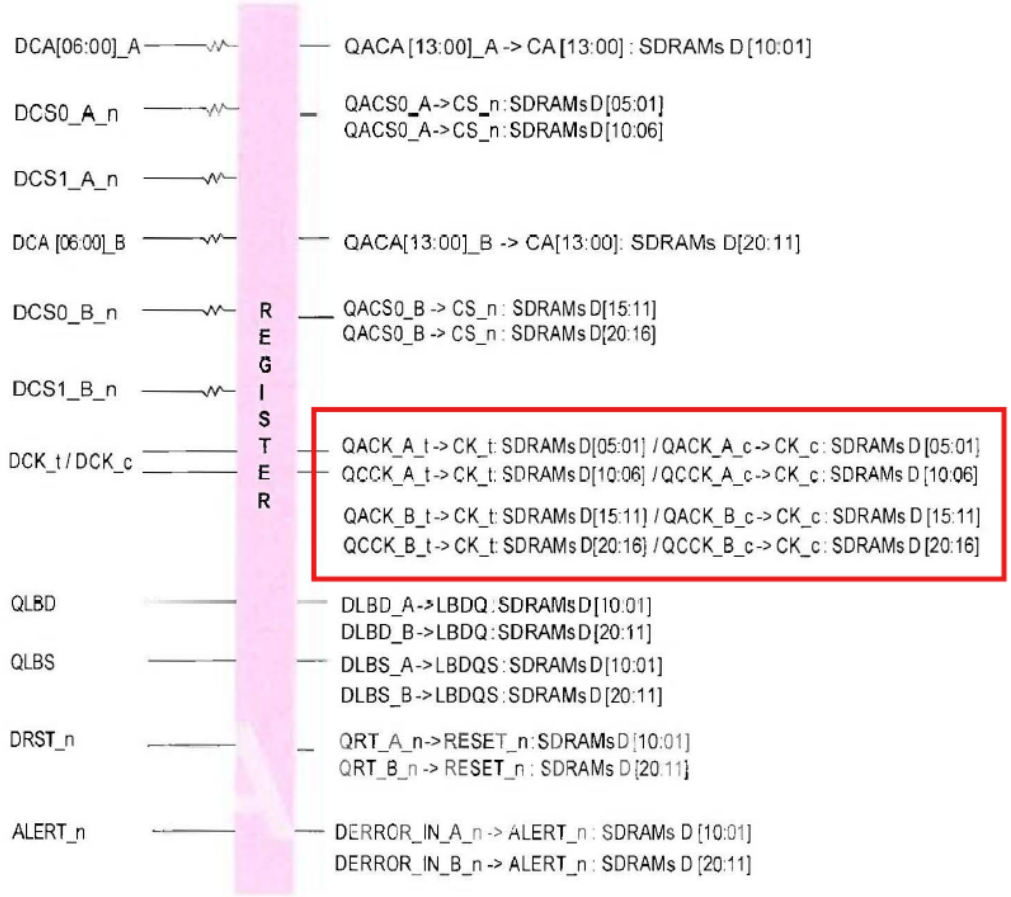
Claim 1	Evidence of Use
	6.1 Signal Groups This standard categorizes DDR5 SDRAM timing-critical signals into specific groups. Figure 2 — (Example) RDIMM 2Rx4 Topology summarizes the high-speed signal groups for RDIMM. Signal groups, except Data and Strobe, implement a fly-by topology. Actual signal names in Annex may vary from individual reference design. The signal groups are: Pre-RCD - Pre-RCD CA and CS group includes: DCA[6:0]_[B:A], DCS[1:0]_[B:A]_n, DPAR_[B:A] - Pre-RCD Clock group includes: DCK_t and DCK_c - Pre-RCD Other group includes: ALERT_n, DRST_n - Pre-RCD Loopback group includes: DLBDQ_[B:A], DLBDQS_[B:A] Post-RCD to SDRAM - Post-RCD CA group includes Q[B:A]CA[13:0]_[B:A] - Post-RCD CS group includes Q[B:A]CS[1:0]_[B:A]_n - Post-RCD Clock group includes Q[D:A]CK_[B:A]_t, Q[D:A]CK_[B:A]_c - Post-RCD Other group includes QRST_[B:A]_n, DERROR_[B:A]_n - Post-RCD Other group includes QLBDQ_[B:A], QLBDQS_[B:A] DQ and DQS - edge connector pin to SDRAM with series resistor SideBand - Host to Hub group: HSDA, HSCL, HSA - Hub local bus group: LSDA, LSCL (star topology from Hub) Ex. CC-88 (JEDEC 305B) at 12 (that RCD outputs Post-RCD command and address signals to memory devices).
[**1.c.5**] output the plurality of local clocks to the memory devices,	*See* evidence cited for element [1.c.3]. The Samsung Practicing '407 Products comprise circuitry mounted on the PCB and configurable to output the plurality of local clocks to the memory devices. For example: The DDR5 RCD circuitry in the Samsung Practicing '407 Products is configurable to output the plurality of local clocks (e.g., "QACK_A_t," "QBCK_A_t," "QCCK_A_t," "QDCK_A_t," "QACK_B_t," "QBCK_B_t," "QCCK_B_t," "QDCK_B_t," "QACK_A_c," "QBCK_A_c," "QCCK_A_c," "QDCK_A_c," "QACK_B_c," "QBCK_B_c," "QCCK_B_c," and "QDCK_B_c") to SDRAM and DRAM memory devices as shown below. *See, e.g.,*

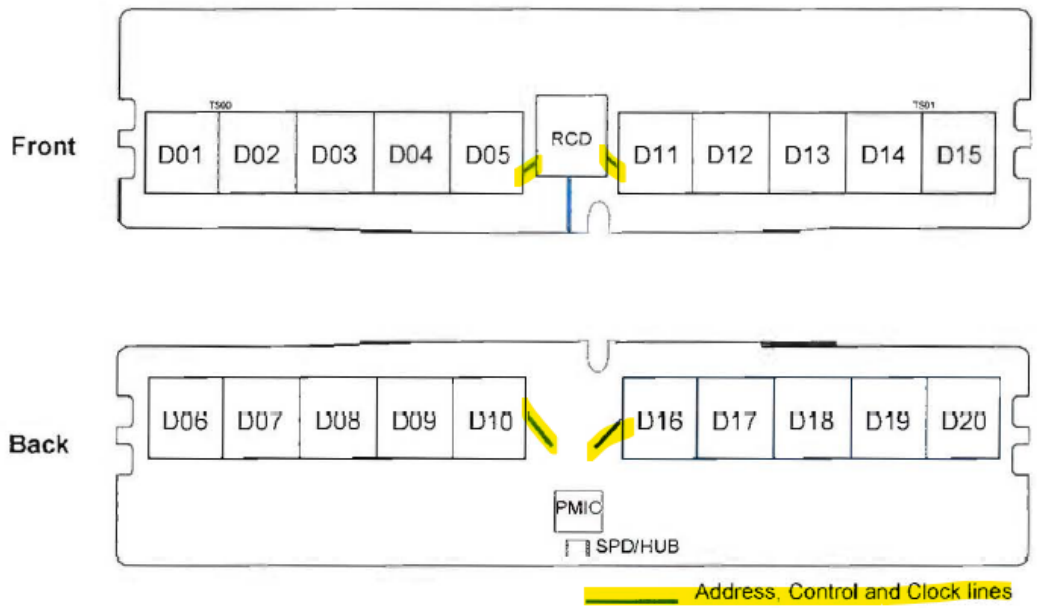

DCA[6:0]_A
QACA [13:0] _A -> CA [13:0]: SDRAMs D [1,2,8,9,10]
DCS0_A_n
QACS0_A -> CS_n: SDRAMs D [1,2,8,9,10]
DCS1_A_n
DCA[6:0]_B
QACA [13:0] _B -> CA [13:0]: SDRAMs D [7:3]
DCS0_B_n
QACS0_B -> CS_n: SDRAMs D [7:3]
DCS1_B_n
REGISTER
DCK_t
DCK_c
QACK_A_t/c -> CK_t/c: SDRAMs D [1,2,8,9,10]
QACK_A_t/c -> CK_t/c: SDRAMs D [7,3]
QLBD
DLBD_A -> LBDQ: SDRAMs D [1,2,8,9,10]
DLBD_B -> LBDQ: SDRAMs D [7;3]
QLBS
DLBS_A -> LBDQS: SDRAMs D [1,2,8,9,10]
DLBS_B -> LBDQS: SDRAMs D [7,3]
DRST_n
QRT_A_n -> RESET_n: SDRAMs D[1,2,8,9,10]
QRT_B_n -> RESET_n: SDRAMs D[7;3]
ALERT_n
DERROR_IN_A_n -> ALERT_n: SDRAMs D [1,2,8,9,10]
DERROR_IN_B_n -> ALERT_n: SDRAMs D [40:21]

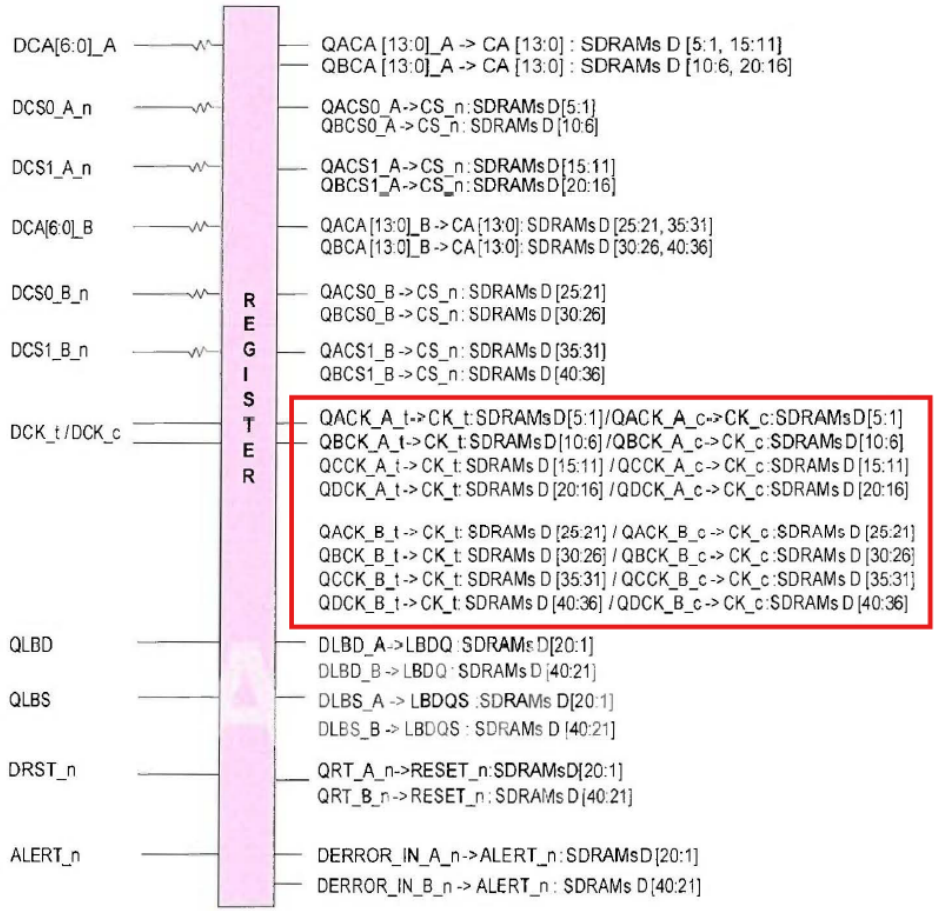
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 21 (RCD generates two sets of local clocks from DCK_t/c corresponding to groups of memory devices: QACK_A_t/c and QACK_B_t/c).

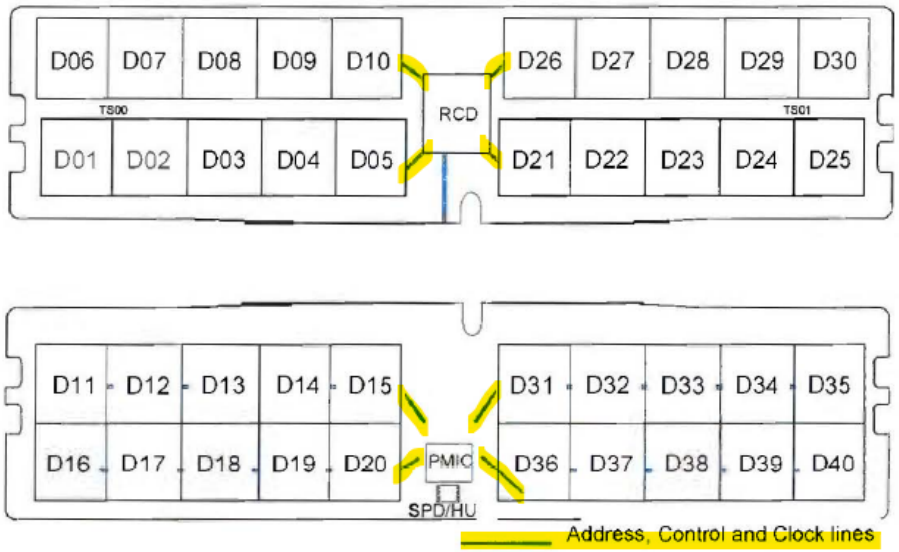
Claim 1	Evidence of Use
	

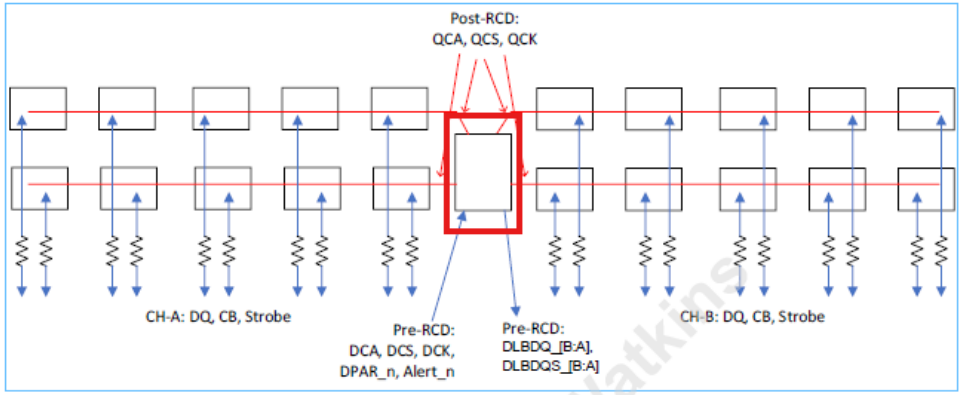
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 25 (RCD generates four sets of local clocks from DCK_t/c corresponding to groups of memory devices: QACK_A_t/c, QCCK_A_t/c, QACK_B_t/c, and QCCK_B_t/c).

Claim 1	Evidence of Use
	

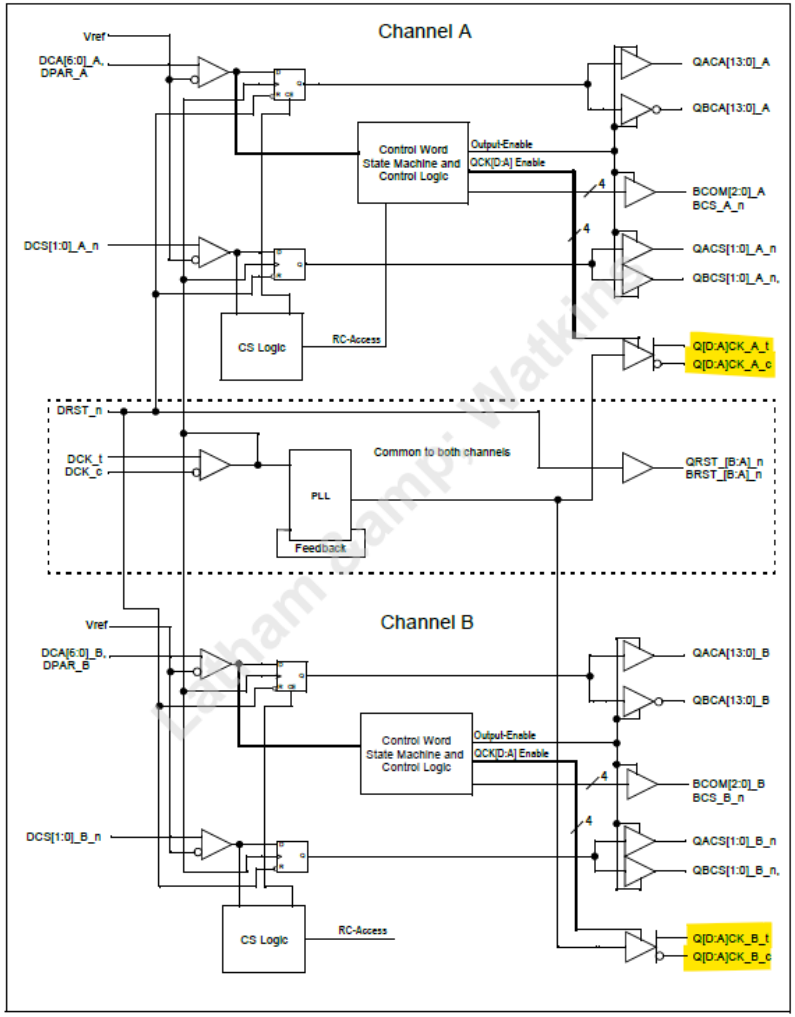
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 29 (RCD generates four sets of local clocks from DCK_t/c corresponding to groups of memory devices: QACK_A_t/c, QCCK_A_t/c, QACK_B_t/c, QCCK_B_t/c).

Claim 1	Evidence of Use
	

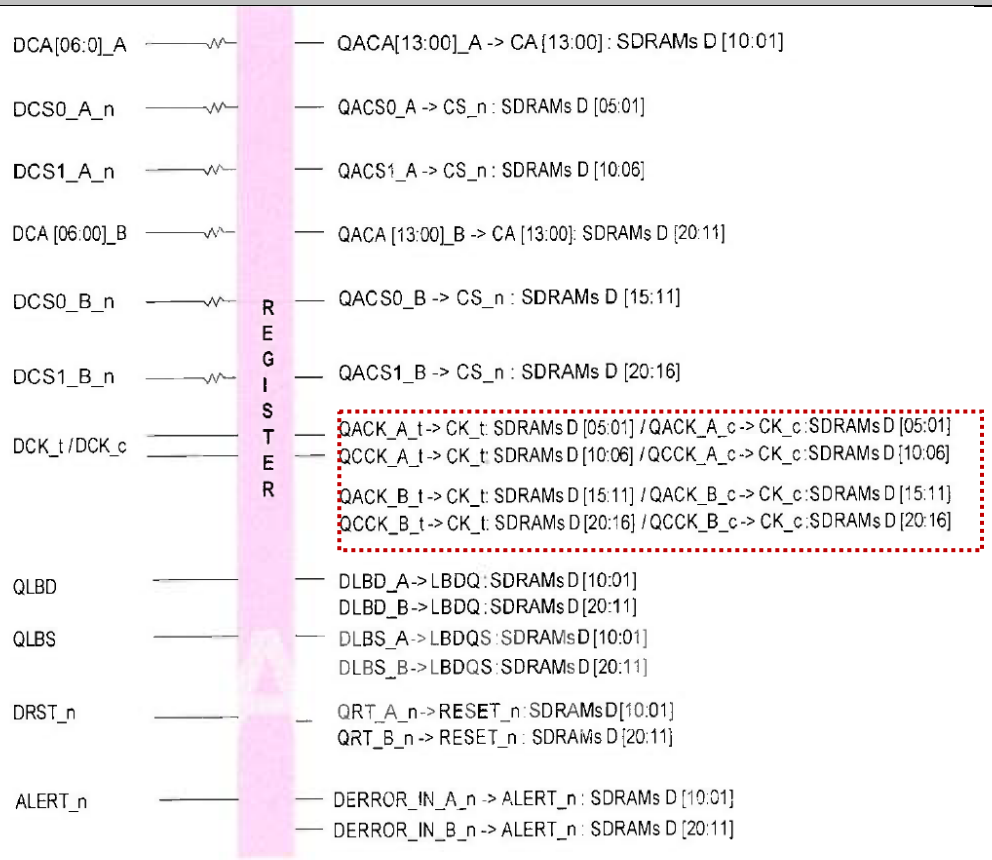
Claim 1	Evidence of Use
	 Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 29 (RCD generates eights sets of local clocks from DCK_t/c corresponding to groups of memory devices: QACK_A_t/c, QBCK_A_t/c, QCCK_A_t/c, QDCK_A_t/c, QACK_B_t/c, QBCK_B_t/c, QCCK_B_t/c, and QDCK_B_t/c). As explained *supra*, the Samsung Practicing ’407 Products are JEDEC compliant. The JEDEC DDR5 RDIMM standard further demonstrates each Samsung Practicing ’407 Products’ RCD outputs a plurality of local clocks to the memory devices.

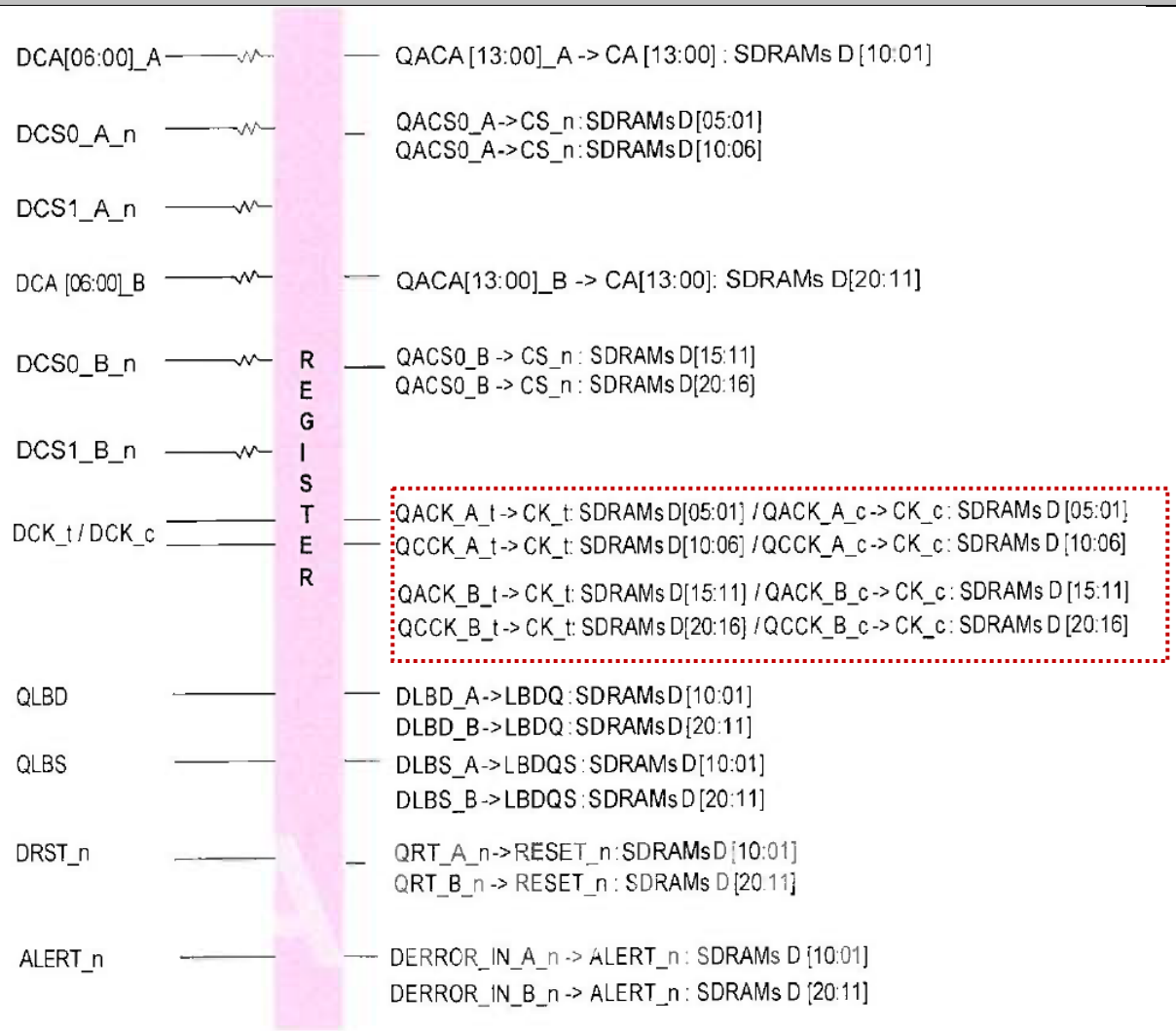
Claim 1	Evidence of Use
	6.1 Signal Groups (cont'd)  **Figure 2 — (Example) RDIMM 2Rx4 Topology** Ex. CC-88 (JEDEC 305B) at 13 (illustrating RCD, in red, receiving "Pre-RCD" clock ("DCK") and generating "Post-RCD" control and address signals ("QCK")). Furthermore, the RCD in the Samsung Practicing '407 Products comply with JEDEC DDR5 RCD specification. The JEDEC DDR5 RCD specification explains the RCD outputs the plurality of local clocks to the memory devices. *See, e.g.,* cycles (i.e., Deselect). Clock outputs | Q[D:A]CK_[B:A]_t Q[D:A]CK_[B:A]_c | POD differential | Clock outputs to the DRAMs. Four copies per channel. Loopback | QLBD | POD | Loopback outputs to Host Ex. CC-32 (JEDEC 82-512) at 4 (showing the RCD includes clock outputs for the memory devices).

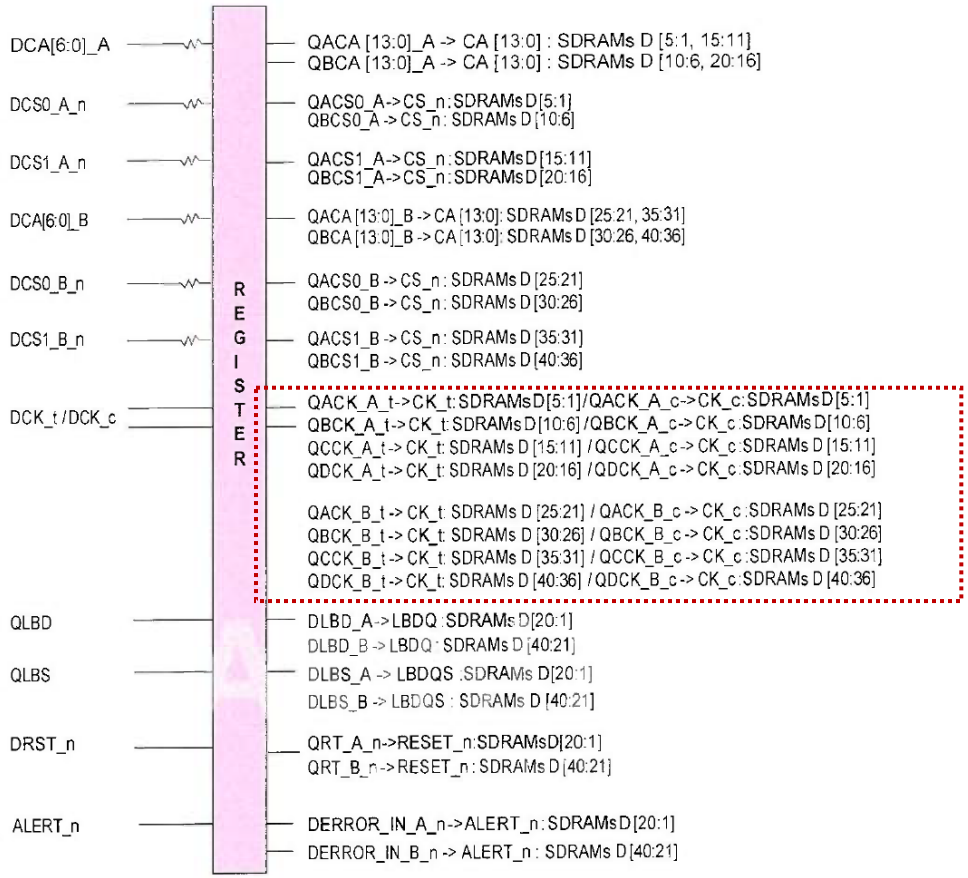
Claim 1	Evidence of Use
	3.1 Description The DDR5RCD02 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs. It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels. Ex. CC-32 (JEDEC 82-512) at 6.

Claim 1	Evidence of Use
	3.2 Logic Diagram Positive Logic  Ex. CC-32 (JEDEC 82-512) at 7.

Claim 1	Evidence of Use
[**1.c.5.i**] wherein a respective local clock having a respective programmable phase relationship with the system clock is output to a corresponding group of the memory devices and not to any other group of the memory devices,	In the Samsung Practicing '407 Products, a respective local clock has a respective programmable phase relationship with the system clock is output to a corresponding group of the memory devices and not to any other group of the memory devices. For example: The local clocks generated by the RCD with a programmable phase relationship with the system clock (*see* limitations 1.c.3, 1.c.3.i, and 1.c.3.ii above) are output to a corresponding group of the memory devices and not to any other group of the memory devices. *See, e.g.,*

Claim 1	Evidence of Use
	 Ex. CC-89 at 25 (Samsung DDR5 RDIMM Datasheet) (illustrating, e.g., that (1) local clock signals "QACK_A_t" and "QACK_A_c" are output from the RCD to the "CK_t" and "CK_c" inputs of memory devices "SDRAMs D [05:01]" but no other memory devices and (2) local clock signals "QACK_B_t" and "QACK_B_c" are output from the RCD to the "CK_t" and "CK_c" inputs of memory devices "SDRAMs D [15:11]" but no other memory devices).

Claim 1	Evidence of Use
	 Ex. CC-89 at 29 (Samsung DDR5 RDIMM Datasheet) (illustrating, e.g., that (1) local clock signals "QACK_A_t" and "QACK_A_c" are output from the RCD to the "CK_t" and "CK_c" inputs of memory devices

Claim 1	Evidence of Use
	"SDRAMs D [05:01]" but no other memory devices and (2) local clock signals "QACK_B_t" and "QACK_B_c" are output from the RCD to the "CK_t" and "CK_c" inputs of memory devices "SDRAMs D [15:11]" but no other memory devices).  Ex. CC-89 at 33 (Samsung DDR5 RDIMM Datasheet) (illustrating, e.g., that (1) local clock signals "QACK_A_t" and "QACK_A_c" are output from the RCD to the "CK_t" and "CK_c" inputs of memory devices "SDRAMs D [5:1]" but no other memory devices and (2) local clock signals "QACK_B_t" and "QACK_B_c"

Claim 1	Evidence of Use
	are output from the RCD to the "CK_t" and "CK_c" inputs of memory devices "SDRAMs D [25:21]" but no other memory devices). As explained *supra*, the Samsung Practicing '407 Products are JEDEC compliant. The JEDEC DDR5 RDIMM standard further demonstrates the local clocks generated by the Samsung Practicing '407 Products' RCD with a programmable phase relationship with the system clock (*see* limitations 1.c.3, 1.c.3.i, and 1.c.3.ii above) are output to a corresponding group of the memory devices and not to any other group of the memory devices.

Claim 1	Evidence of Use

6.9.1 DIMM Connectivity Wiring

2Rx4					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Top	Upper	QBCK	QBCS0	QBCA	0
Bottom	Lower	QCCK	QACS1	QACA	1
Bottom	Upper	QDCK	QBCS1	QBCA	1

2Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Top		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]
Bottom	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]

2Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Top	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]
Bottom		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

1Rx4					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QCCK	QBCS0	QACA	0

1Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]

1Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

2Rx8					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QCCK	QACS1	QACA	1

2Rx8 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	
Bottom	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	

2Rx8 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	
Bottom	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	

Claim 1	Evidence of Use
	6.9.1 DIMM Connectivity Wiring (cont'd) **1Rx8 (less than 8000 Mbps)** DIMM Side: Row, Clock, CS, CA, Rank Top: Lower, QACK, QACS0, QACA, 0 Bottom: Lower, QACK, QACS0, QACA, 0 **1Rx8 (8000 Mbps and Faster)** DIMM Side: Row, Clock, CS, CA, Rank Top: Lower, QCCK, QACS0, QACA, 0 Bottom: Lower, QCCK, QACS0, QACA, 0 **1Rx8 Sub Channel 0 (Channel A)** Side: DQS0, DQS5, DQS1, DQS6, DQS2, DQS7, DQS3, DQS8, DQS4, DQS9 Nib: Nib 0, Nib 1, Nib 2, Nib 3, Nib 4, Nib 5, Nib 6, Nib 7, Nib 8, Nib 9 Top: [15:8], [31:24] Bottom: [7:0], [23:16], CB[7:0] **1Rx8 Sub Channel 1 (Channel B)** Side: DQS0, DQS5, DQS1, DQS6, DQS2, DQS7, DQS3, DQS8, DQS4, DQS9 Nib: Nib 0, Nib 1, Nib 2, Nib 3, Nib 4, Nib 5, Nib 6, Nib 7, Nib 8, Nib 9 Top: [7:0], [23:16] Bottom: [15:8], [31:24], CB[7:0] **Figure 12 — DIMM Connectivity Wiring** Ex. CC-88 (JEDEC 305B) at 31-32 (showing local clocks, e.g., QACK, QBCK, QCCK, QDCK, being output to certain groups of memory devices but not others).
[**1.c.5.ii**] wherein the corresponding group of the memory devices is configurable to perform memory read or write operations by communicating data signals with the memory controller via a corresponding subset of data signal lines in accordance with the respective local clock.	In the Samsung Practicing '407 Products, the corresponding group of the memory devices is configurable to perform memory read or write operations by communicating data signals with the memory controller via a corresponding subset of data signal lines in accordance with the respective local clock. For example, a group of memory devices in the Samsung Practicing '407 Products associated with Channel A perform memory read and write operations by communicating data signals with the memory controller via a subset of data signal lines (e.g., "DQ[]_A"), and a group of memory devices in the Samsung Practicing '407 Products associated with Channel B perform memory read and write operations by communicating data signals with the memory controller via a subset of data signal lines (e.g., "DQ[]_B"). *See, e.g.*:

Claim 1	Evidence of Use

[Table 5] PIN Description

Pin Name	Description
CA[6:0]_A CA[6:0]_B	SDRAM Address and Command Bus
CS[1:0]_A CS[1:0]_B	SDRAM Chip Select
PAR_A PAR_B	SDRAM Parity input
CK_t	SDRAM Clocks (true/positive)
CK_c	SDRAM Clocks (complement/negative)
ALERT_n	SDRAM alert for CRC error
RESET_n	Set DRAM to known state
PCAMP	Control and Monitor Port
HSCL	I2C/I3C-Basic Host Sideband Bus Clock
HSDA	I2C/I3C-Basic Host Sideband Bus Data
HSA	I2C/I3C-Basic Host Sideband Bus Address
LBDQ	Loopback data output:

Pin Name	Description
DQ[31:0]_A DQ[31:0]_B	DIMM memory data bus channel A and B
CB[7:0]_A CB[7:0]_B	DIMM ECC check bits(CB) channel A and B
DQS[9:0]_A_t DQS[9:0]_B_t	SDRAM data strobes (positive line of differential pair)
DQS[9:0]_A_c DQS[9:0]_B_c	SDRAM data strobes (negative line of differential pair)
TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
VIN_BULK	DIMM Power Supply from system to PMIC
VIN_MGMT	DIMM Power Supply from system to PMIC
VSS	Power supply return (ground)
RFU	Reserved for future use
LBDQS	Loopback data strobe output

Ex. CC-89 at 9.

[Table 4] PIN Configuration

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VIN_BULK	145	VIN_BULK	50	VSS	194	DQ31_A	96	CB0_B	240	VSS
2	RFU	146	VIN_BULK	51	CB0_A	195	VSS	97	VSS	241	CB2_B
3	VIN_MGMT	147	PWR_GOOD/FAIL_n	52	VSS	196	CB2_A	98	CB1_B	242	VSS
4	SCL	148	SAA	53	CB1_A	197	VSS	99	VSS	243	CB3_B
5	SDA	149	RFU	54	VSS	198	CB3_A	100	DQ0_B	244	VSS
6	VSS	150	RFU	55	DQS4_A_t	199	VSS	101	VSS	245	DQ2_B
7	DQ0_A	151	VSS	56	DQS4_A_c	200	DQS9_A_c,TDQS9_A_c	102	DQ1_B	246	VSS
8	VSS	152	DQ2_A	57	VSS	201	DQS9_A_t,TDQS9_A_t	103	VSS	247	DQ3_B
9	DQ1_A	153	VSS	58	CB4_A	202	VSS	104	DQS0_B_t	248	VSS
10	VSS	154	DQ3_A	59	VSS	203	CB6_A	105	DQS0_B_c	249	DQS5_B_c,TDQS5_B_c
11	DQS0_A_t	155	VSS	60	CB5_A	204	VSS	106	VSS	250	DQS5_B_t,TDQS5_B_t
12	DQS0_A_c	156	DQS5_A_c, TDQS5_A_c	61	VSS	205	CB7_A	107	DQ4_B	251	VSS
13	VSS	157	DQS5_A_t, TDQS5_A_t	62	ALERT_n	206	VSS	108	VSS	252	DQ6_B
14	DQ4_A	158	VSS	63	VSS	207	RESET_n	109	DQ5_B	253	VSS
15	VSS	159	DQ5_A	64	CS0_A_n	208	VSS	110	VSS	254	DQ7_B
16	DQ5_A	160	VSS	65	VSS	209	CS1_A_n	111	DQ6_B	255	VSS
17	VSS	161	DQ7_A	66	CA0_A	210	VSS	112	VSS	256	DQ10_B
18	DQ8_A	162	VSS	67	VSS	211	CA1_A	113	DQ9_B	257	VSS
19	VSS	163	DQ10_A	68	CA2_A	212	VSS	114	VSS	258	DQ11_B
20	DQ9_A	164	VSS	69	VSS	213	CA3_A	115	DQS1_B_t	259	VSS
21	VSS	165	DQ11_A	70	CA4_A	214	VSS	116	DQS1_B_c	260	DQS6_B_c,TDQS6_B_c
22	DQS1_A_t	166	VSS	71	VSS	215	CA5_A	117	VSS	261	DQS6_B_t,TDQS6_B_t
23	DQS1_A_c	167	DQS6_A_c,TDQS6_A_c	72	CA6_A	216	VSS	118	DQ12_B	262	VSS
24	VSS	168	DQS6_A_t,TDQS6_A_t	73	VSS	217	CK_t	119	VSS	263	DQ14_B
25	DQ12_A	169	VSS	74	PAR_A	218	CK_c	120	DQ13_B	264	VSS
26	VSS	170	DQ14_A	75	VSS	219	VSS	121	VSS	265	DQ15_B
27	DQ13_A	171	VSS	KEY				122	DQ16_B	266	VSS
28	VSS	172	DQ15_A					123	VSS	267	DQ18_B
29	DQ16_A	173	VSS					124	DQ17_B	268	VSS
30	VSS	174	DQ18_A	76	CA0_B	220	RFU	125	VSS	269	DQ19_B
31	DQ17_A	175	VSS	77	VSS	221	CA1_B	126	DQS2_B_t	270	VSS
32	VSS	176	DQ19_A	78	CA2_B	222	VSS	127	DQS2_B_c	271	DQS7_B_c,TDQS7_B_c
33	DQS2_A_t	177	VSS	79	VSS	223	CA3_B	128	VSS	272	DQS7_B_t,TDQS7_B_t
34	DQS2_A_c	178	DQS7_A_c,TDQS7_A_c	80	CA4_B	224	VSS	129	DQ20_B	273	VSS
35	VSS	179	DQS7_A_t, TDQS7_A_t	81	VSS	225	CA5_B	130	VSS	274	DQ22_B
36	DQ20_A	180	VSS	82	CA6_B	226	VSS	131	DQ21_B	275	VSS
37	VSS	181	DQ22_A	83	VSS	227	PAR_B	132	VSS	276	DQ23_B
38	DQ21_A	182	VSS	84	CS0_B_n	228	VSS	133	DQ24_B	277	VSS
39	VSS	183	DQ23_A	85	VSS	229	CS1_B_n	134	VSS	278	DQ26_B
40	DQ24_A	184	VSS	86	LBD, RSP_A_n	230	VSS	135	DQ25_B	279	VSS
41	VSS	185	DQ26_A	87	LBS, RSP_B_n	231	RFU	136	VSS	280	DQ27_B
42	DQ25_A	186	VSS	88	VSS	232	RFU	137	DQS3_B_t	281	VSS
43	VSS	187	DQ27_A	89	CB4_B	233	VSS	138	DQS3_B_c	282	DQS8_B_c,TDQS8_B_c
44	DQS3_A_t	188	VSS	90	VSS	234	CB6_B	139	VSS	283	DQS8_B_t,TDQS8_B_t
45	DQS3_A_c	189	DQS8_A_c,TDQS8_A_c	91	CB5_B	235	VSS	140	DQ28_B	284	VSS
46	VSS	190	DQS8_A_t, TDQS8_A_t	92	VSS	236	CB7_B	141	VSS	285	DQ30_B
47	DQ28_A	191	VSS	93	DQS9_B_t, TDQS9_B_t	237	VSS	142	DQ29_B	286	VSS
48	VSS	192	DQ30_A	94	DQS9_B_c,TDQS9_B_c	238	DQS4_B_c	143	VSS	287	DQ31_B
49	DQ29_A	193	VSS	95	VSS	239	DQS4_B_t	144	RFU	288	VSS

Claim 1	Evidence of Use
	Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 6.

Front Side Pin Label	Pin	Pin	Back side Pin Label
VIN_BULK	1	145	VIN_BULK
RFU	2	146	VIN_BULK
VIN_MGMT	3	147	PWR_GOOD/FAIL_n
HSCL	4	148	HSA
HSDA	5	149	RFU
VSS	6	150	RFU
DQ0_A	7	151	VSS
VSS	8	152	DQ2_A
DQ1_A	9	153	VSS
VSS	10	154	DQ3_A
DQS0_A_t	11	155	VSS
DQS0_A_c	12	156	DQS5_A_c, TDQS5_A_c
VSS	13	157	DQS5_A_t, TDQS5_A_t DBI0_A_n
DQ4_A	14	158	VSS
VSS	15	159	DQ6_A
DQ5_A	16	160	VSS
VSS	17	161	DQ7_A
DQ8_A	18	162	VSS
VSS	19	163	DQ10_A
DQ9_A	20	164	VSS
VSS	21	165	DQ11_A
DQS1_A_t	22	166	VSS
DQS1_A_c	23	167	DQS6_A_c, TDQS6_A_c
VSS	24	168	DQS6_A_t, TDQS6_A_t DBI1_A_n
DQ12_A	25	169	VSS
VSS	26	170	DQ14_A
DQ13_A	27	171	VSS
VSS	28	172	DQ15_A
DQ16_A	29	173	VSS
VSS	30	174	DQ18_A
DQ17_A	31	175	VSS
VSS	32	176	DQ19_A
DQS2_A_t	33	177	VSS
DQS2_A_c	34	178	DQS7_A_c, TDQS7_A_c
VSS	35	179	DQS7_A_t, TDQS7_A_t DBI2_n
DQ20_A	36	180	VSS
VSS	37	181	DQ22_A
DQ21_A	38	182	VSS

Front Side Pin Label	Pin	Pin	Back side Pin Label
PAR_A	74	218	CK_c
V33	75	219	V33
	Key		
CA0_B	76	220	RFU
VSS	77	221	CA1_B
CA2_B	78	222	VSS
VSS	79	223	CA3_B
CA4_B	80	224	VSS
VSS	81	225	CA5_B
CA6_B	82	226	VSS
VSS	83	227	PAR_B
CS0_B_n	84	228	VSS
VSS	85	229	CS1_B_n
LBD, RSP_A_n	86	230	VSS
LBS, RSP_B_n	87	231	RFU
VSS	88	232	RFU
CB4_B	89	233	VSS
VSS	90	234	CB6_B
CB5_B	91	235	VSS
VSS	92	236	CB7_B
DQS9_B_t, TDQS9_B_t DBI4_B_n	93	237	VSS
DQS9_B_c, TDQS9_B_c	94	238	DQS4_B_c
VSS	95	239	DQS4_B_t
CB0_B	96	240	VSS
V33	97	241	CB2_B
CB1_B	98	242	VSS
VSS	99	243	CB3_B
DQ0_B	100	244	VSS
VSS	101	245	DQ2_B
DQ1_B	102	246	VSS
VSS	103	247	DQ3_BDQ3_B
DQS0_B_t	104	248	VSS
DQS0_B_c	105	249	DQS5_B_c, TDQS5_B_c
VSS	106	250	DQS5_B_t, TDQS5_B_t DBI0_B_n
DQ4_B	107	251	VSS
VSS	108	252	DQ6_B
DQ5_B	109	253	VSS

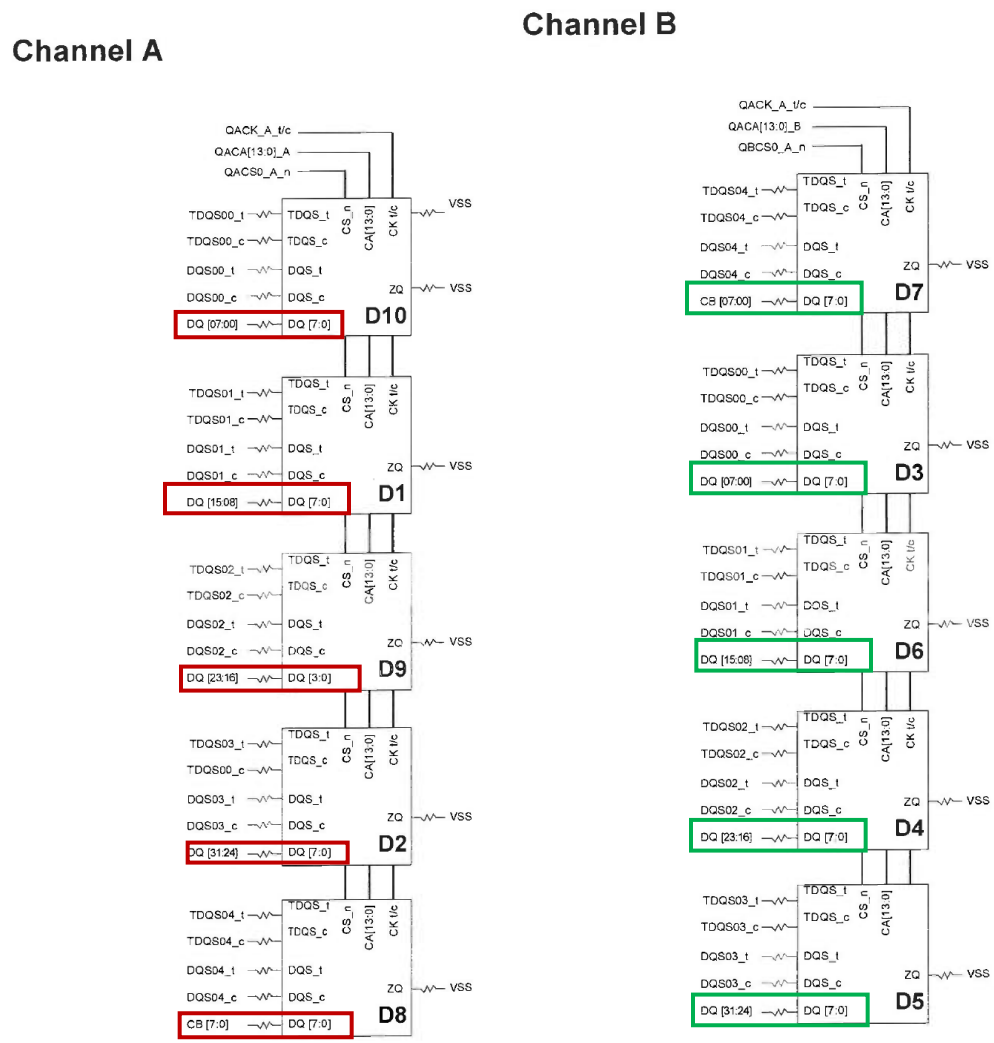
Claim 1	Evidence of Use

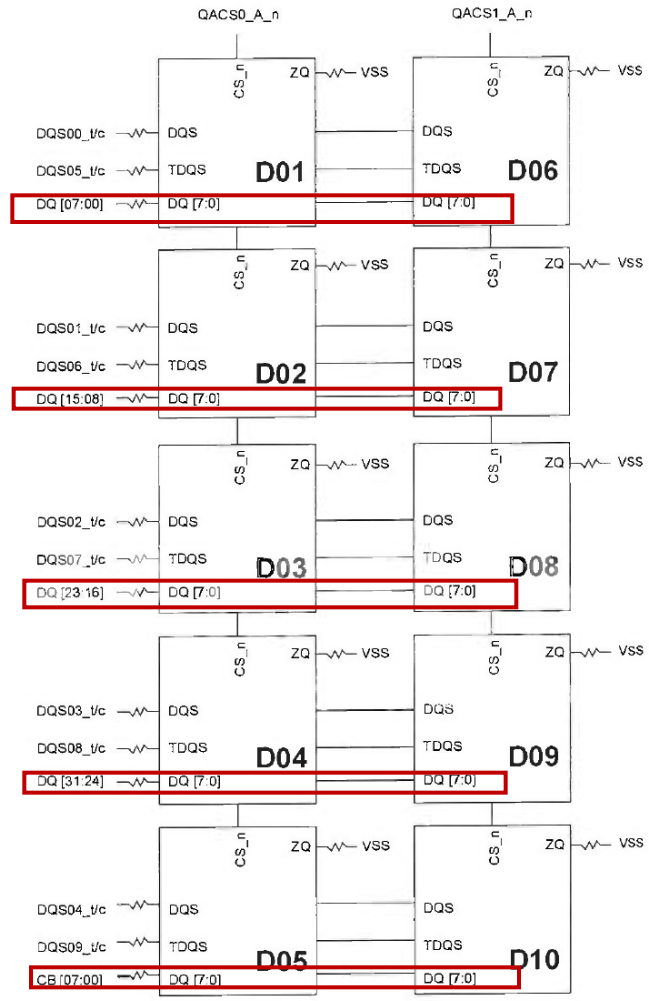
Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	39	183	DQ23_A
DQ24_A	40	184	V33
VSS	41	185	DQ26_A
DQ25_A	42	186	VSS
VSS	43	187	DQ27_A
DQS3_A_t	44	188	VSS
DQS3_A_c	45	189	DQS8_A_c, TDQS8_A_c
VSS	46	190	DQS8_A_t, TDQS8_A_t DBI3_A_n
DQ28_A	47	191	VSS
VSS	48	192	DQ30_A
DQ29_A	49	193	VSS
VSS	50	194	DQ31_A
CB0_A	51	195	VSS
VSS	52	196	CB2_A
CB1_A	53	197	VSS
VSS	54	198	CB3_A
DQS4_A_t	55	199	VSS
DQS4_A_c	56	200	DQS9_A_c, TDQS9_A_c
VSS	57	201	DQS9_A_t, TDQS9_A_t DBI4_A_n
CB4_A	58	202	VSS
VSS	59	203	CB6_A
CB5_A	60	204	VSS
VSS	61	205	CB7_A
ALERT_n	62	206	VSS
VSS	63	207	RESET_n
CS0_A_n	64	208	VSS
VSS	65	209	CS1_A_n
CA0_A	66	210	VSS
VSS	67	211	CA1_A
CA2	68	212	VSS
VSS	69	213	CA3_A
CA4_A	70	214	VSS
VSS	71	215	CA5_A
CA6_A	72	216	VSS
VSS	73	217	CK_t

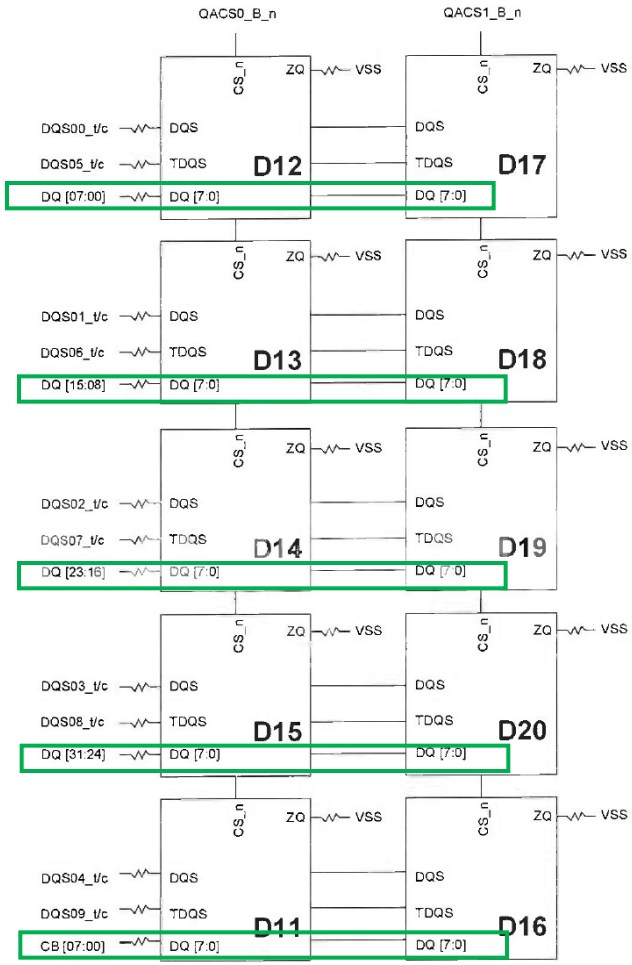
Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	110	254	DQ7_B
DQ8_B	111	255	VSS
VSS	112	256	DQ10_B
DQ9_B	113	257	VSS
VSS	114	258	DQ11_B
DQS1_B_t	115	259	VSS
DQS1_B_c	116	260	DQS6_B_c, TDQS6_B_c
VSS	117	261	DQS6_B_t, TDQS6_B_t DBI1_B_n
DQ12_B	118	262	VSS
VSS	119	263	DQ14_B
DQ13_B	120	264	VSS
VSS	121	265	DQ15_B
DQ16_B	122	266	VSS
VSS	123	267	DQ18_B
DQ17_B	124	268	VSS
VSS	125	269	DQ19_B
DQS2_B_t	126	270	V33
DQS2_B_c	127	271	DQS7_B_c, TDQS7_B_c
VSS	128	272	DQS7_B_t, TDQS7_B_t DBI2_B_n
DQ20_B	129	273	VSS
VSS	130	274	DQ22_B
DQ21_B	131	275	VSS
VSS	132	276	DQ23_B
DQ24_B	133	277	VSS
VSS	134	278	DQ26_B
DQ25_B	135	279	VSS
VSS	136	280	DQ27_B
DQS3_B_t	137	281	VSS
DQS3_B_c	138	282	DQS8_B_c, TDQS8_B_c
VSS	139	283	DQS8_B_t, TDQS8_B_t DBI3_B_n
DQ28_B	140	284	VSS
VSS	141	285	DQ30_B
DQ29_B	142	286	VSS
VSS	143	287	DQ31_B
RFU	144	288	VSS

Figure 1. Wiring Assignments

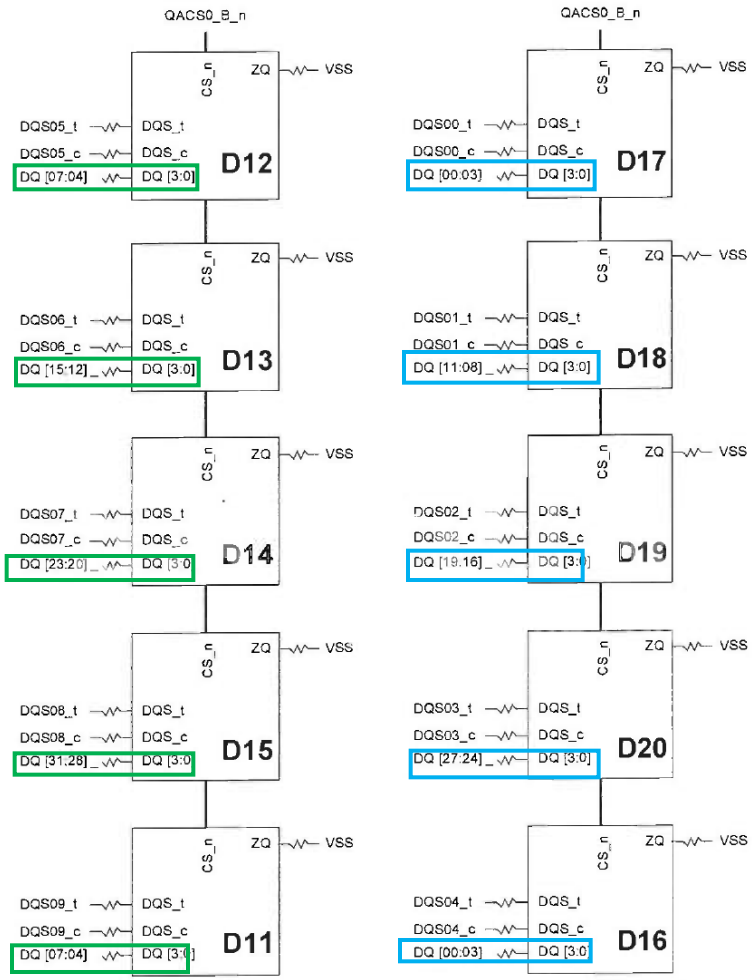
Claim 1	Evidence of Use
	Ex. CC-89 (Samsung DDR5 RDIMM Datasheet) at 7-8.

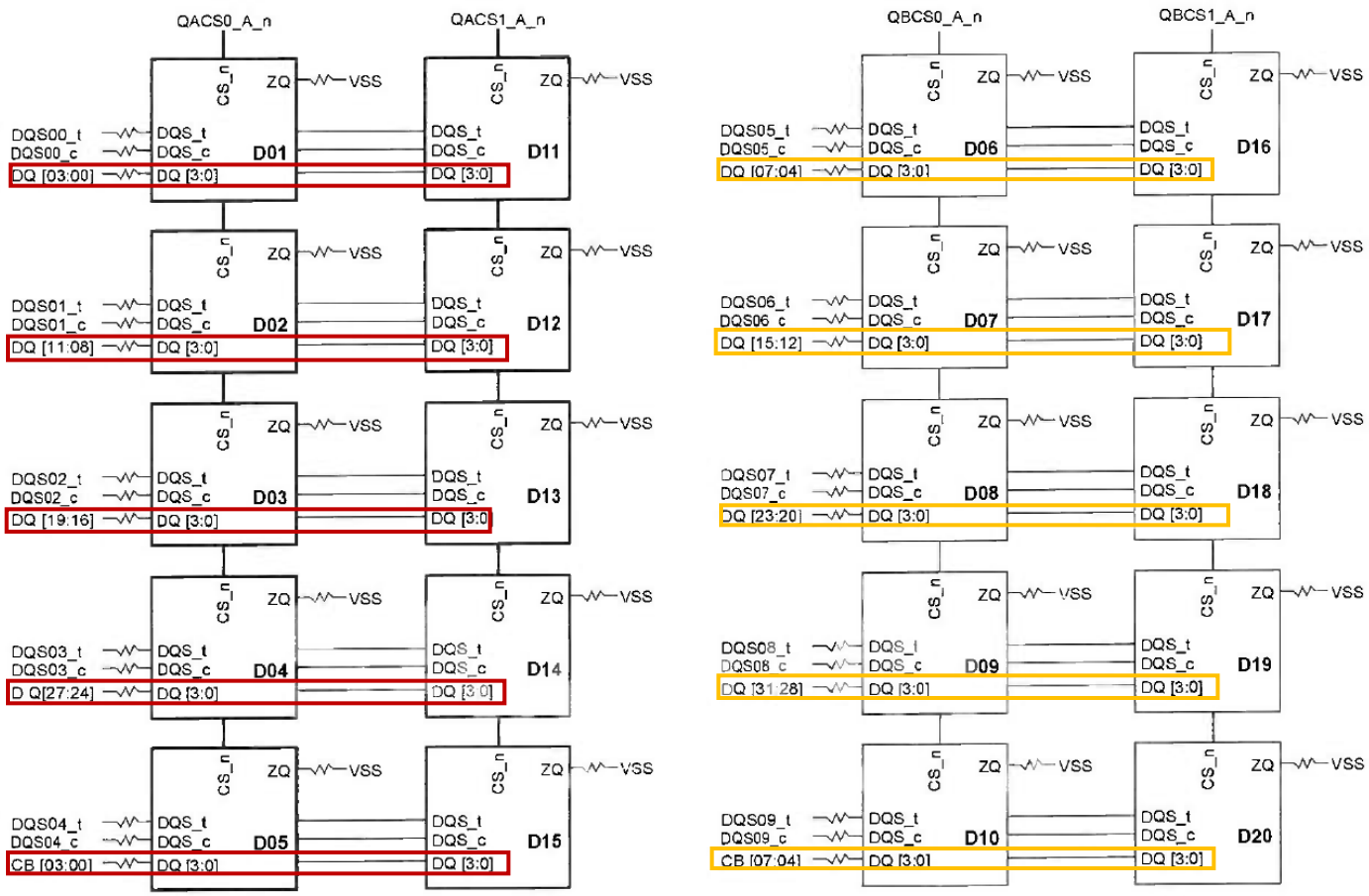


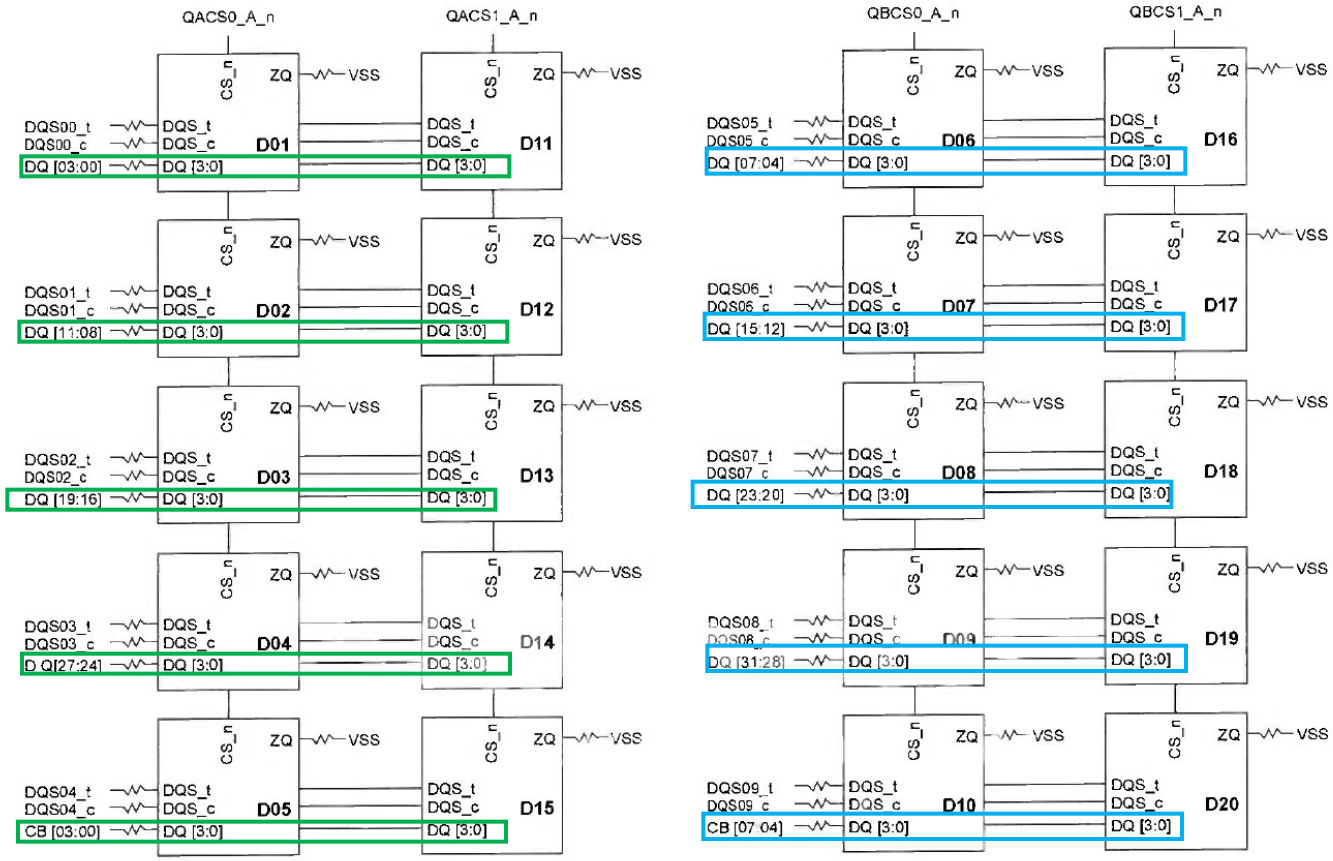
Claim 1	Evidence of Use
	Channel A  Ex. CC-89 at 26

Claim 1	Evidence of Use
	Channel B  Ex. CC-89 at 27

Claim 1	Evidence of Use
	Channel A Ex. CC-89 at 30

Claim 1	Evidence of Use
	Channel B  Ex. CC-89 at 31

Claim 1	Evidence of Use
	Channel A  Ex. CC-89 at 34

Claim 1	Evidence of Use
	Channel B  Ex. CC-89 at 35 As explained *supra*, the Samsung Practicing ’407 Products are JEDEC compliant. The JEDEC DDR5 RDIMM standard further demonstrates groups of memory devices perform memory read and write operations by

Claim 1	Evidence of Use
	communicating data signals with the memory controller via corresponding subsets of data signal lines (e.g., DQS[]).

6.9.1 DIMM Connectivity Wiring

2Rx4					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Top	Upper	QBCK	QBCS0	QBCA	0
Bottom	Lower	QCCK	QACS1	QACA	1
Bottom	Upper	QDCK	QBCS1	QBCA	1

2Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Top		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]
Bottom	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]

2Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Top	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]
Bottom		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

1Rx4					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QCCK	QBCS0	QACA	0

1Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]

1Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

2Rx8					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QCCK	QACS1	QACA	1

2Rx8 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	
Bottom	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	

2Rx8 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	
Bottom	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	

Claim 1	Evidence of Use

6.9.1 DIMM Connectivity Wiring (cont'd)

1Rx8 (less than 8000 Mbps)					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QACK	QACS0	QACA	0
1Rx8 (8000 Mbps and Faster)					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QCCK	QACS0	QACA	0
Bottom	Lower	QCCK	QACS0	QACA	0

1Rx8 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top			[15:8]				[31:24]			
Bottom	[7:0]				[23:16]				CB[7:0]	

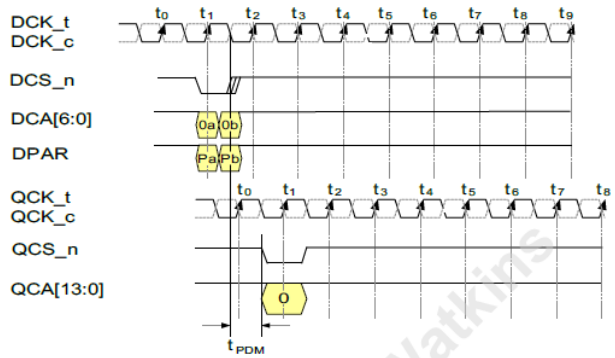
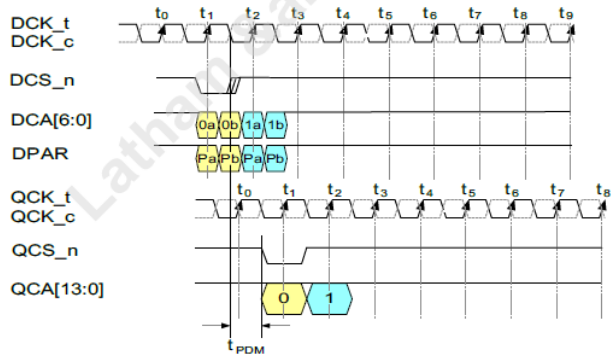
1Rx8 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]				[23:16]					
Bottom			[15:8]				[31:24]		CB[7:0]	

Figure 12 — DIMM Connectivity Wiring

Ex. CC-88 (JEDEC 305B) at 31-32 (showing memory devices receiving data from the memory controller via subsets of data signal lines, e.g., [3:0], [11:8], [15:12]).

Furthermore, the memory devices in the Samsung Practicing '407 Products are configurable to perform memory read or write operations by communicating data signals in accordance with their respective local clock signals (e.g., "QACK_A_t," "QBCK_A_t," "QCCK_A_t," "QDCK_A_t," "QACK_B_t," "QBCK_B_t," "QCCK_B_t," "QDCK_B_t," "QACK_A_c," "QBCK_A_c," "QCCK_A_c," "QDCK_A_c," "QACK_B_c," "QBCK_B_c," "QCCK_B_c," and "QDCK_B_c") as those signals are delivered to the "CK_t" and "CK_c" inputs of their respective memory devices.

As explained *supra*, the Samsung Practicing '407 Products are JEDEC compliant. The JEDEC DDR5 RCD definition further demonstrates the chip select signal (QCS) and command and address signal (QCA) received by each DDR memory device is synchronized with the local clock (QCK):

Claim 1	Evidence of Use
	3.4.1 Double Data Rate DCA (cont'd)  NOTE Timing Diagram for 0 nCK command latency adder. **Figure 7 — One UI DRAM Command Timing Diagram**  NOTE Timing Diagram for 0 nCK command latency adder. **Figure 8 — Two UI DRAM Command Timing Diagram** Ex. CC-32 (JEDEC 82-512) at 16. See also Ex. CC-30 (JEDEC 82-513) at 16.

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Claim 1	Evidence of Use
	The JEDEC DDR5 RCD definition explains the Samsung Practicing '407 Products are configurable to perform READ and WRITE operations synchronized with the local clock QCK. *See, e.g.,*:

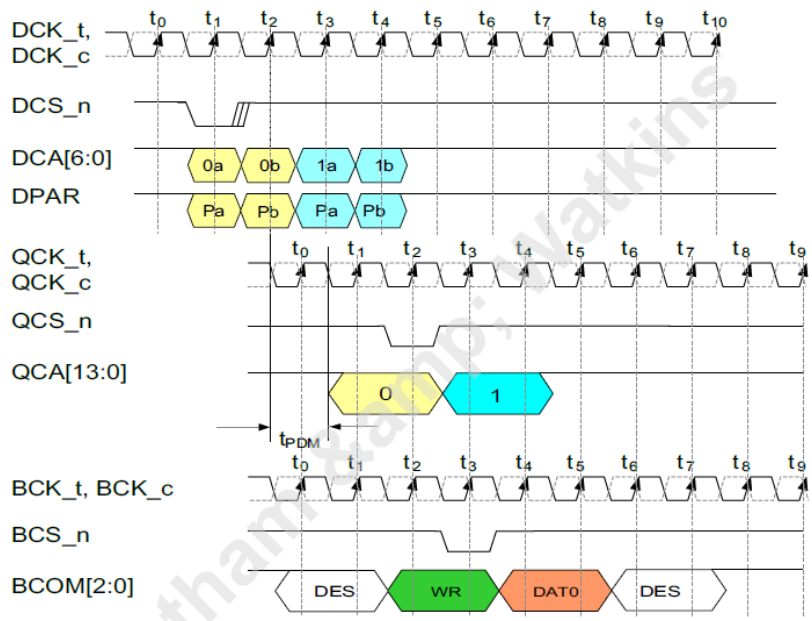

Figure 11 — SDR1 Mode Example of DRAM WR Command with RW00[1] = 0

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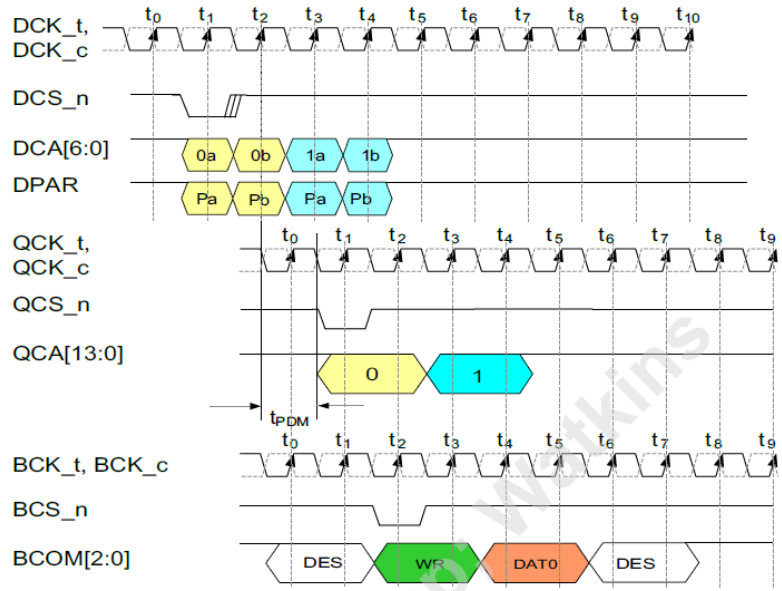
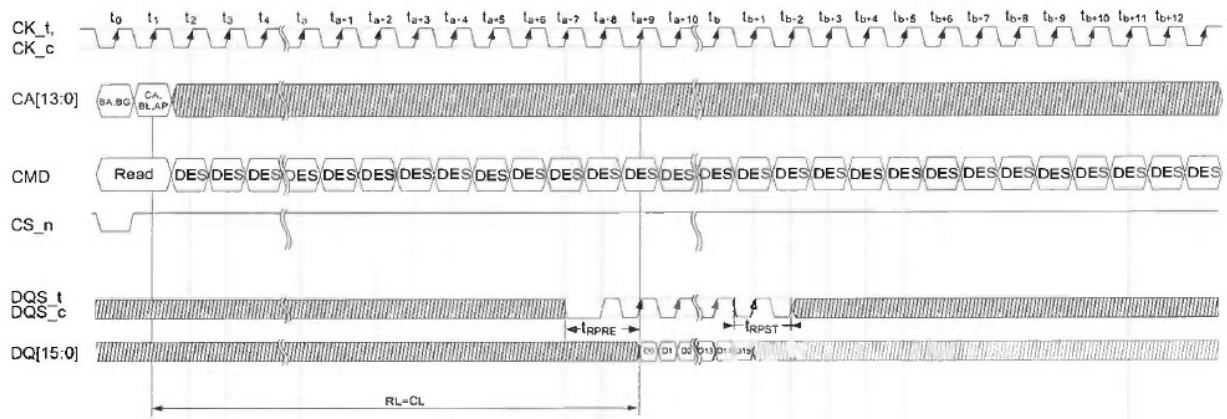
Claim 1	Evidence of Use
	 **Figure 12 — SDR2 Mode Example of DRAM WR Command with RW00[1] = 1** Ex. CC-32 (JEDEC 82-512) at 18-19. See also Ex. CC-30 (JEDEC 82-513) at 18-19. Further, the timing diagrams for read and write operations show that DQ signals appear after a set latency in terms of clock cycles after the module C/A signals are received. As another example, DQ is output/received in relation to DQS, and DQS is aligned with clock signals in predetermined manner. So the DQ output/input is in accordance with local clock signals.

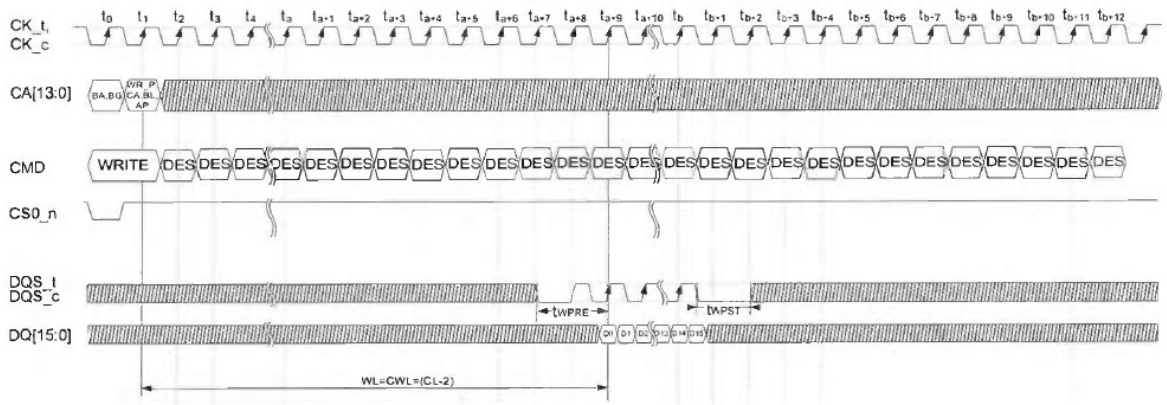
Claim 1	Evidence of Use
	4.7 Read Operation The Read Operation causes the DRAM to retrieve and output data stored in its array. The Read Operation is initiated by the Read Command during which the beginning column address and bank/group address for the data to be retrieved from the array is provided. The data is driven by the DRAM on its DQ pins RL (CL) cycles after the Read Command along with the proper waveform on the DQS inputs. Read Latency (RL or CL) is defined from the Read command to data and is not affected by the Read DQS offset timing (MR40 OP[2:0]). **4.7.1 READ Burst Operation** During a READ or WRITE command, DDR5 shall support BC8, BL16, BL32 (optional) and BL32 OTF (optional) during the READ or WRITE. MR0[1:0] is used to select burst operation mode.  NOTES: 1. BL=16, Preamble = 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble 2. DES commands are shown for ease of illustration; other commands may be valid at these times. 3. In this example, Read DQS Offset Timing is set to 0 Clocks. **Figure 35 — READ Burst Operation (BL16)** Ex. CC-05 (JESD79-5) at 135.

Claim 1	Evidence of Use

4.8.2 Write Burst Operation

The following write timing diagrams are to help understand the meaning of each write parameter; the diagrams are just examples. The details of each parameter are defined separately.

In these write timing diagrams, for clarity of illustration, CK and DQS are shown aligned. As well, DQS and DQ are shown center-aligned. Offset between CK and DQS, and between DQS and DQ may be appropriate.



NOTES:
1. BL=16, 2tCK Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The DQ signal is shown as "Don't Care" before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 49 — WRITE Burst Operation (BL16)

Ex. CC-05 (JESD79-5) at 147.