Quantitative evaluation of energy distribution of interface trap density at MoS_2 MOS interfaces by the Terman method

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***Abstract*—**We have evaluated interfacial properties of exfoliated MoS_2 MOS interfaces with HfO_2, Al_2O_3, and SiO_2 by C-V measurements of thick-body MoS_2 MOS capacitors. The Terman method have revealed that most of the MoS_2 MOS interfaces exhibit a D_{it} peak of approximately 1×10^{13} $cm^{-2}eV^{-1}$ at an energy level of around 0.35-0.4 eV from the midgap regardless of the gate dielectrics, which is attributable to the sulfur vacancies of MoS_2. We have also revealed that some MoS_2 MOS interfaces have a nearly constant D_{it} of around 1×10^{12} $cm^{-2}eV^{-1}$ when there seems to be no sulfur vacancies. The analysis of the subthreshold swings in the MoS_2 MOSFETs and TCAD simulation support the same energy distribution of D_{it}. Thus, we have successfully grasped the energy distribution of D_{it} at the native MoS_2 MOS interfaces which is not strongly dependent on the gate dielectrics.

I. Introduction

After the emergence of graphene by exfoliation [1], 2D materials have attracted considerable attention due to their unique materials properties. Among 2D materials, atomically-thin MoS_2 exhibits semiconductor properties with a sizable bandgap, high mobility, and low permittivity, suitable for deeply-scaled MOSFETs beyond Si [2] as shown in Fig. 1. Moreover, there seems to be no dangling bonds on the surfaces of MoS_2, which may allow us to obtain superior MOS interfaces. However, the MoS_2 MOS interfacial properties have not been well understood yet. There are some reports tying to reveal the interface properties of MoS_2 by measuring a capacitance and conductance in a FET or capacitor with a thin MoS_2 layer as shown in Fig. 2(a). However, the large series resistance caused by the thin MoS_2 channel results in the large frequency dispersion in the measured capacitance, making it difficult to extract the interface trap density (D_{it}) in a straightforward manner [3]. Moreover, the thin MoS_2 compared with the maximum depletion-layer width results in no capacitance change according to the depletion-layer width change in C-V measurements, which prevents us from determining the energy distribution of D_{it} [4]. Therefore, it is indispensable to evaluate the MoS_2 MOS interfacial properties by using the well-established method.

In this paper, we have examined properties of MoS_2 MOS interface by C-V measurements of thick-body MoS_2 MOS capacitors with HfO_2, Al_2O_3, and SiO_2 as a gate dielectric shown in Fig. 2(b). Since the MoS_2 thickness is large enough for achieving full depletion, the Terman method is applicable to extract the energy distribution of D_{it}. In conjunction with the subthreshold swing analyses in the MoS_2 MOSFETs, we have successfully grasped the universal D_{it} distribution model of the native MoS_2 MOS interface regardless of the gate dielectrics.

II. Fabrication of MoS_2 MOS Capacitor

To extract the D_{it} distribution by the Terman method, the MoS_2 thickness must be greater than its maximum depletion-layer width. As shown in Fig. 3, when the doping concentration is more than 1×10^{15} cm^{-3}, the MoS_2 thickness of more than 1 μm is sufficient for achieving the maximum depletion-layer width in C-V measurements. Fig. 4 is the fabrication procedure of MoS_2 MOS capacitors. First, a thick MoS_2 layer is exfoliated from a MoS_2 bulk crystal. Then, a part of the top MoS_2 layer is exfoliated and transferred on an n^+-Si substrate by using a tweezer. Prior to the transfer, a gate dielectric of HfO_2, Al_2O_3, and SiO_2 is formed on each Si substrate. After the transfer, metal electrodes for back contact to the MoS_2 are deposited on the sample through a shadow mask. Then, the MoS_2 layer is isolated by dry etching with SF_6 and Ar. We use the metal electrode as a mask for dry etching. Finally, an Al electrode is deposited on the back side of the Si substrate to apply a gate voltage. Fig. 5 is a plan-view photo and surface profile of the fabricated MoS_2 MOS capacitor. We confirm that the thickness of the capacitor exceeds 1 μm. Fig. 6 shows the Raman spectrum of the exfoliated MoS_2 layer. First, we examine the metal contact to the back of the MoS_2 layer. We deposit Al, W, Ti, Ni, Pt, and Au electrodes on the MoS_2 directly transferred on an n^+-Si substrate. The I-V measurements in Fig. 7 shows that the Au electrode provides us the best Ohmic contact to MoS_2 among the tested metals. In the following experiments, we use the Au electrodes in all the samples.

III. D_{IT} Evaluation by the Terman Method

First, we perform C-V measurements for the MoS_2 MOS capacitors with 10-nm-thick HfO_2, Al_2O_3, or 20-nm-thick SiO_2 gate dielectric. Fig. 8 show C-V curves of the HfO_2/MoS_2 MOS capacitor. We observe the clear capacitance change according to an increase in the depletion-layer width by applying a gate voltage owing to the sufficiently thick MoS_2 layer. We also find no frequency dispersion from 1 kHz to 1 MHz. One of the most distinct features in the C-V curves is a hump observed at a bias

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voltage of around -0.3 V, which can be attributed to the interface trap response. We observe similar C-V curves with a hump in the Al_2O_3/MoS_2 and SiO_2/MoS_2 MOS capacitors as shown in Figs. 9 and 10. It is worth noting that the capacitance change in the SiO_2/MoS_2 capacitor looks small due to the relatively thick SiO_2 and its low permittivity as compared with Al_2O_3 and HfO_2.

We apply the Terman method for the C-V curves in Figs. 8-10 to obtain the D_{it} and its energy level. Fig. 11 is the extracted energy distribution of D_{it} at the HfO_2/MoS_2 MOS interface. In the Terman method, the accurate impurity concentration N_D of the MoS_2 layer is required especially to determine the D_{it} close to the midgap. However, there is uncertainty in the extraction of N_D from the capacitance minimum value because of the existence of slow traps in the valence band side discussed later. Therefore, we extract the D_{it} spectrum by assuming N_D of 3.0×10^{16}, 3.5×10^{16}, and 4.0×10^{16} cm^{-3}. The Terman method reveals the significant D_{it} peak at an energy level of around 0.35 – 0.4 eV regardless of the assumed N_D values, corresponding to the hump in the C-V curve in Fig. 8. The peak value reaches around 1×10^{13} $cm^{-2}eV^{-1}$. We find similar D_{it} peaks at the Al_2O_3/MoS_2 and SiO_2/MoS_2 interfaces as shown in Figs. 12 and 13. Thus, we can conclude that the discovered D_{it} peak reflects the nature of MoS_2 which does not depend on the type of a gate dielectric. Recently, H. Qiu et al. reported that the sulfur vacancies at a MoS_2 interface induce localized states at an energy level of approximately 0.35 eV above the midgap [5]. Since the energy level of this localized state is close to the energy level of the D_{it} peak in Fig. 11-13, the observed D_{it} peak might originate from the sulfur vacancies in MoS_2. As shown in Figs. 11-13, we have uncertainty in the D_{it} at an energy level below 0.25 eV. However, the D_{it} at this energy range is likely to be around 1×10^{12} $cm^{-2}eV^{-1}$, which can be estimated from the subthreshold swing in the MoS_2 MOSFETs as discussed later.

We find some of the MoS_2 MOS capacitors exhibit no hump in the C-V curves as shown in Fig. 14. It is found in Fig. 15 that there is no D_{it} peak related to the sulfur vacancies. This result suggests that the pristine MoS_2 interface, which is not exposed to high-temperature processes, has a nearly constant D_{it} of around 1×10^{12} $cm^{-2}eV^{-1}$ in the conduction band side. We also examine the impact of slow traps on the hysteresis in the C-V curves. When the HfO_2/MoS_2 capacitor shown in Fig. 14 is measured in the range from -1V to 1V, there is no hysteresis in the C-V curves. However, we observe the significant V_{fb} shift when the C-V curves measured from -2V to 1V as shown in Fig. 16, resulting in the large hysteresis. This V_{fb} shift indicates the existence of slow traps in the valence band side.

IV. Analysis of S.S. in MoS_2 MOSFETs

To verify the energy distribution of D_{it}, we analyze subthreshold swing (S.S.) in MoS_2 MOSFETs. Fig. 17 shows a schematic and plan-view photo of the fabricated MoS_2 MOSFETs with a back-gate configuration. First, we deposit 10-nm-thick HfO_2 or Al_2O_3 on an n^+-Si substrate by ALD. Then, an exfoliated MoS_2 layer is transferred on the substrate. The thickness of the MoS_2 layer is around 7 – 8 nm. Finally, EB-evaporated Au S/D electrodes are formed by lift-off. The I_d-V_d characteristics of the MoS_2 MOSFET with the Al_2O_3 gate dielectric is shown in Fig. 18. Owing to the thin gate dielectric, we achieve the excellent transfer characteristic. The effective mobility is approximately 16 cm^2/Vs. Fig. 19 is the S.S. of the Al_2O_3/MoS_2 MOSFET measured with V_d of 0.05 V. We find a nearly flat S.S. at V_g from -0.7 V to -0.5 V with a minimum S.S. of approximately 70 mV/dec. From the measured S.S., the energy distribution of D_{it} is extracted as shown in Fig. 20. To determine the energy level of D_{it}, we perform TCAD simulation. The simulated I_d-V_d curve in Fig. 18 is in agreement with the experiment by assuming a constant D_{it} of 1×10^{12} $cm^{-2}eV^{-1}$. As shown in Fig. 20, we find D_{it} of around 1×10^{12} $cm^{-2}eV^{-1}$ at an energy level from 0.15 eV to 0.3 eV, corresponding to the D_{it} distribution which we have discussed in the Terman method analyses. Fig. 21 shows the I_d-V_d of the HfO_2/MoS_2 MOSFET, in which we observe a kink in the subthreshold slope at V_d of 0.05 V. To estimate the D_{it} distribution, TCAD simulation is performed again. When we assume a constant D_{it} of 2×10^{12} $cm^{-2}eV^{-1}$ and a Gaussian distribution of D_{it} with a peak D_{it} of 8×10^{12} $cm^{-2}eV^{-1}$ and a standard deviation of 0.05 eV as shown in Fig. 22, which is similar to the D_{it} distribution obtained from the Terman method, we obtain the excellent fitting to the experimental result as shown in Fig. 21. Thus, the D_{it} distribution model extracted from the S.S. analyses in Fig. 22 strongly supports the energy distribution of D_{it} obtained from the C-V measurements.

V. Conclusion

We have discussed the energy distributions of D_{it} at the MoS_2 MOS interfaces with HfO_2, Al_2O_3, and SiO_2 by applying the Terman method to the thick-body MoS_2 MOS capacitors. We have found the distinct D_{it} peak of 1×10^{13} $cm^{-2}eV^{-1}$ regardless of the gate dielectric, which is attributable to the defect traps induced by the sulfur vacancies in MoS_2. We have also revealed that the native MoS_2 interface exhibits a nearly constant D_{it} of around 1×10^{12} $cm^{-2}eV^{-1}$ when there seems to be no sulfur vacancies. In conjunction with the S.S. analyses of the MoS_2 MOSFETs, we have successfully clarified the energy distribution of D_{it} at MoS_2 MOS interfaces.

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Fig. 1: Schematic of monolayer MoS_2 which has fundamental advantages for deeply-scaled MOSFETs such as atomically thin body, high mobility, low permittivity, and no dangling bonds on its surface. However, MoS_2 MOS interface properties have been not well understood yet.

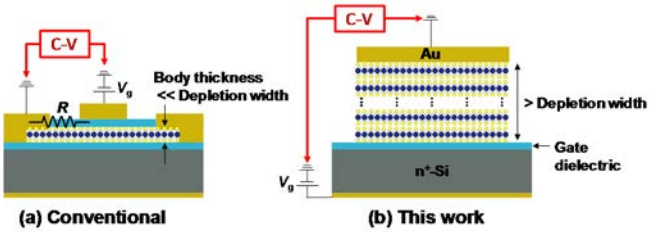

Fig. 2: (a) Conventional device structure for evaluation of MOS interface properties by C-V measurement and (b) MoS_2 MOS capacitors with a thick body proposed in this work.

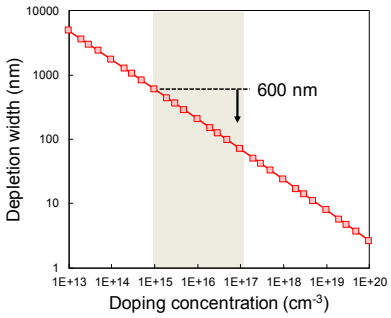

Fig. 3: Maximum depletion-layer width in MoS_2 MOS capacitor.

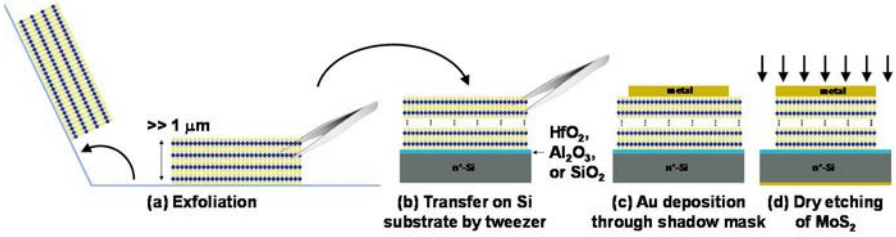

Fig. 4: Fabrication procedure of MoS_2 MOS capacitor: (a) exfoliation of thick MoS_2 film from a bulk crystal by scotch tape, (b) transfer a part of the top MoS_2 layer on an n^+-Si substrate with a gate dielectric such as HfO_2, Al_2O_3, and SiO_2 by tweezer, (c) Au electrode deposition through a shadow mask to make an electrode for back contact to MoS_2 film, and (d) dry etching of MoS_2 film to isolate each capacitor through Au electrode as a hard mask.

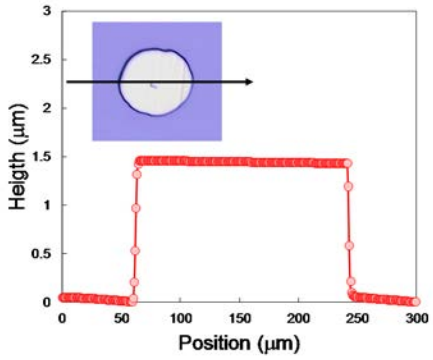

Fig. 5: Plan-view and surface profile of the fabricated MoS_2 MOS capacitor.

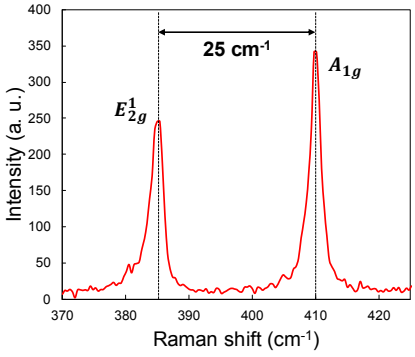

Fig. 6: Raman spectrum of MoS_2 sample exfoliated and transferred on the Si substrate.

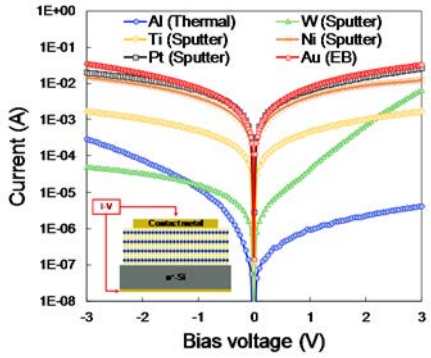

Fig. 7: I-V characteristics of Metal/MoS_2/n^+-Si samples.

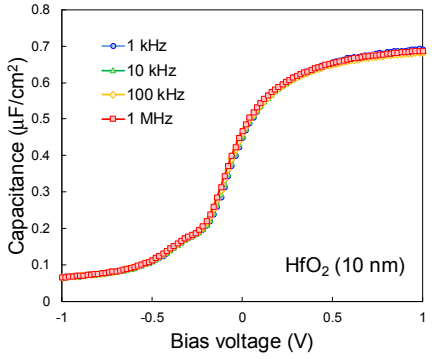

Fig. 8: C-V curves of MoS_2 MOS capacitor with 10-nm-thick HfO_2 gate dielectric.

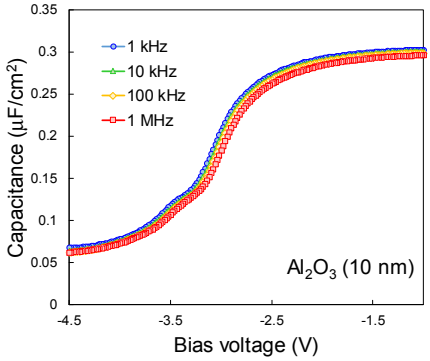

Fig. 9: C-V curves of MoS_2 MOS capacitor with 10-nm-thick Al_2O_3 gate dielectric.

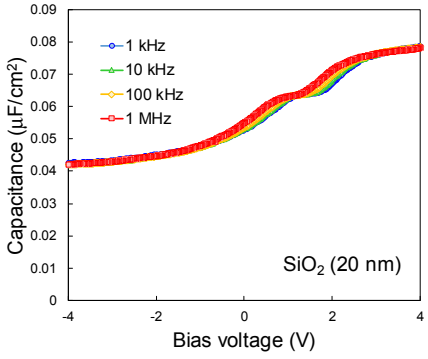

Fig. 10: C-V curves of MoS_2 MOS capacitor with 20-nm-thick SiO_2 gate dielectric.

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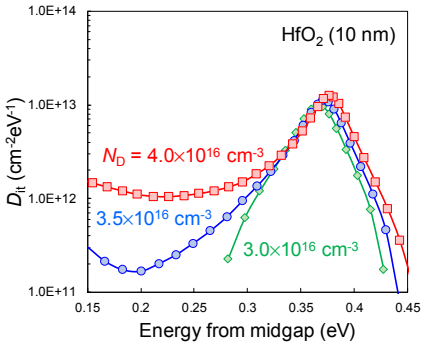

Fig. 11: D_{it} distributions at the HfO_2/MoS_2 interface extracted by the Terman method.

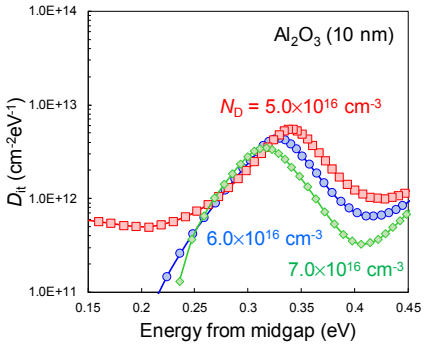

Fig. 12: D_{it} distributions at the Al_2O_3/MoS_2 interface extracted by the Terman method.

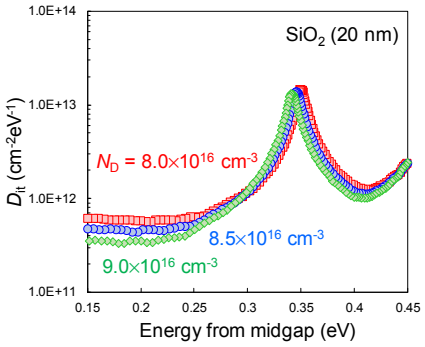

Fig. 13: D_{it} distributions at the SiO_2/MoS_2 interface extracted by the Terman method.

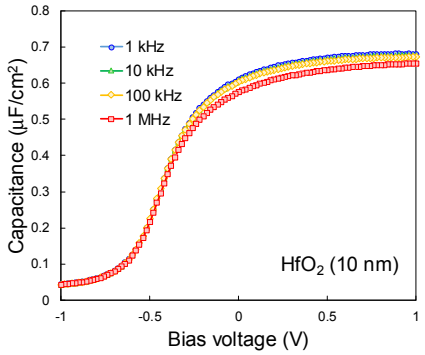

Fig. 14: C-V curves of HfO_2/MoS_2 MOS capacitor with no hump.

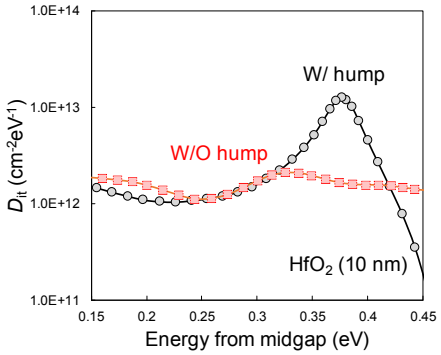

Fig. 15: Comparison of D_{it} distributions at HfO_2/MoS_2 interfaces in Fig. 8 and Fig. 14.

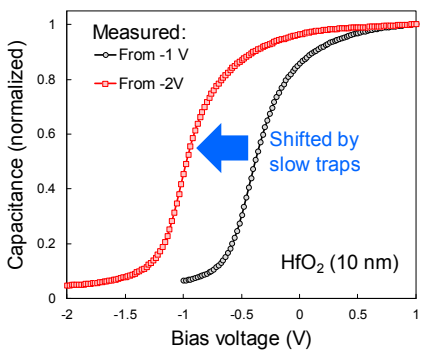

Fig. 16: V_{fb} shift in C-V curve of HfO_2/MoS_2 MOS capacitor caused by slow traps.

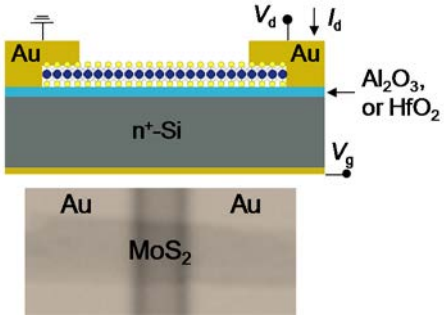

Fig. 17: Schematic and Plan-view photo of MoS_2 MOSFET with a back gate.

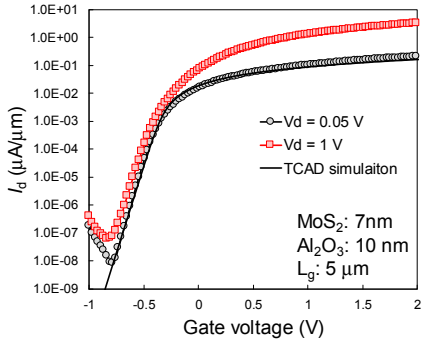

Fig. 18: I_d-V_g of Al_2O_3/MoS_2 MOSFET.

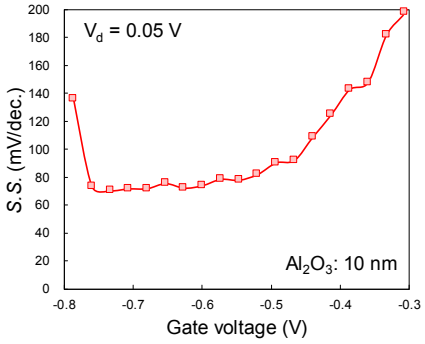

Fig. 19: S.S. of Al_2O_3/MoS_2 MOSFET.

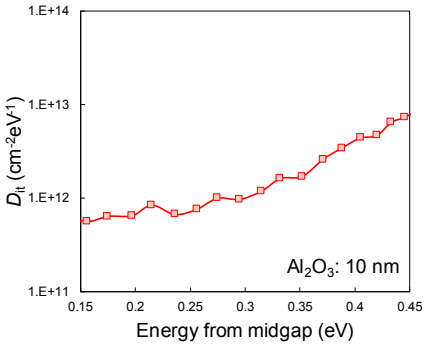

Fig. 20: D_{it} distribution Al_2O_3/MoS_2 interface extracted from S.S.

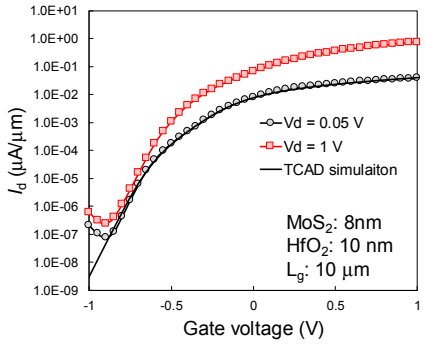

Fig. 21: I_d-V_g of HfO_2/MoS_2 MOSFET and TCAD simulation with the assumed D_{it} model.

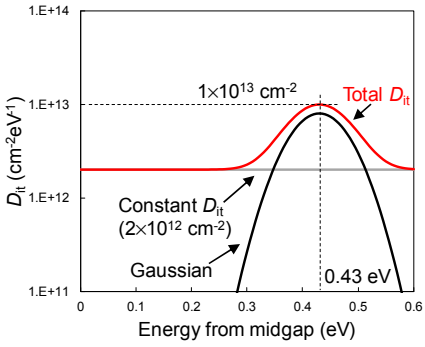

Fig. 22: D_{it} distribution model of MoS_2 MOS interface obtained from TCAD simulation.