

## BASIC ELECTRONICS LABORATORY

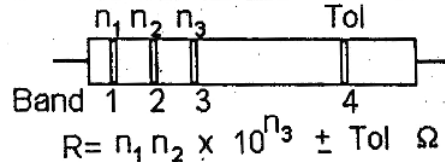
### EXPERIMENT NO: 1

#### MEASUREMENT OF RESISTANCE, CLASSIFICATION OF CAPACITORS DIODE TESTING

**A Note On Reading Resistor Values:** The colour bands on resistors are used to indicate the nominal values of their resistance and the permitted tolerance on that value. The first three bands (closest together) give the value of the resistor in ohms ( $\Omega$ ). The band at the end of the resistor indicates the first significant digit ( $n_1$ ) and the next band indicates the second digit ( $n_2$ ). The third band indicates the number of zeros following these two digits ( $n_3$ ). The bands are colour coded as follows:

Colour	Black	Brown	Red	Orange	Yellow	Green	Blue	Violet	Grey	White
Digit	0	1	2	3	4	5	6	7	8	9

A red fourth band means the resistor's value will be within 2% of the stated value, gold 5%, and silver 10%. Absence of the fourth band indicates a  $\pm 20\%$  tolerance.



**A Note On Reading Capacitor Values:** *Big capacitors* are polarized. The terminal - (+) must be at least as negative (positive) as the other terminal. These have values marked in  $\mu\text{F}$ .

**Smaller Capacitors:** Tantalum: These are often coloured cylinders. Mylar: These are yellow cylinders made of long coils of metal foils separated by thin dielectrics. Fat rectangular shaped capacitors are often made of Metallized Polyester film. Ceramic: These are often disc shaped.

While reading small capacitor values one must remember that in electronics these are in the range pF-  $\mu\text{F}$  (a few pF to a few  $\mu\text{F}$ ). Some examples of the markings and the corresponding values are given below.

Markings	A100	10KH	475K	475M	.01M	.1MFD	473J
Read as	100pF $\pm 20\%$	10 KpF $\pm 20\%$	$47 \times 10^5 \text{ pF}$ $\pm 10\%$	$47 \times 10^5 \text{ pF}$ $\pm 20\%$	.01 $\mu\text{F}$ $\pm 20\%$	0.1 $\mu\text{F}$ $\pm 20\%$	0.047 $\mu\text{F}$ $\pm 5\%$
Markings	4R7 $\mu$	560M	101K	4k7	22n	0.1	Colour band
Read as	4.7 $\mu\text{F}$ $\pm 20\%$	560pF $\pm 20\%$	$10 \times 10^1 \text{ pF}$ $\pm 10\%$	$4.7 \times 10^3 \text{ pF}$ $\pm 20\%$	22nF $\pm 20\%$	0.1 $\mu\text{F}$ $\pm 20\%$	Value read from top to bottom.

**I. Experiment:** (i) Identify the resistors in the board. (ii) Read their values. (iii) Use a multimeter in the 'Resistance' mode to measure these values. In case of non autoranging multimeters use the range that gives the maximum accuracy of the readings.

**CAUTION:** No voltage other than that due to the multimeter should be present across the resistors while measuring resistance.

(iv) Identify the capacitors in the board. (v) Read their values. You may also measure the capacitance with your multimeter if it has the capacitance measuring mode.

(vi) Identify the inductor in the board.

**A Note On Ground (sometimes called Earth):** Symbol: (sometimes ). This term indicates a 'common reference' point in the circuit. It does not necessarily mean that it actually goes to earth.

P.T.O.

**ADDITIONAL NOTE ON READING CAPACITOR VALUES:**

Large capacitors have the value printed plainly on them, such as 10 $\mu$ F (Ten Micro Farads) but smaller disk types along with plastic film types often have just 2 or three numbers on them?

First, most will have three numbers, but sometimes there are just two numbers. These are read as Pico-Farads. An example: 47 printed on a small disk can be assumed to be 47 Pico-Farads (or 47 puff as some like to say)

Now, what about the three numbers? It is somewhat similar to the resistor code. The first two are the 1st and 2nd significant digits and the third is a multiplier code. Most of the time the last digit tells you how many zeros to write after the first two digits, but the standard has a couple of curves that you probably will never see. But just to be complete here it is in a table.

Third digit	Multiplier (this times the first two digits gives you the value in Pico-Farads)
0	1
1	10
2	100
3	1,000
4	10,000
5	100,000
6 not used	
7 not used	
8	.01
9	.1

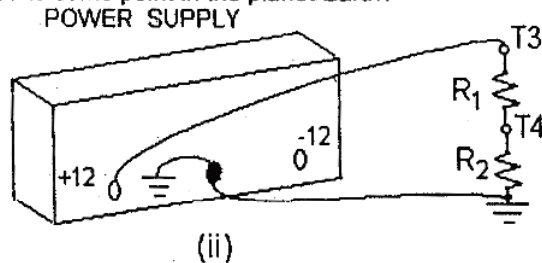
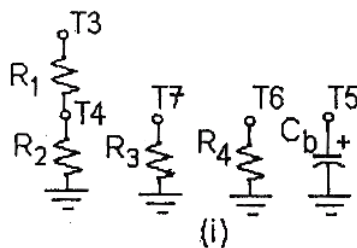
Now for an example: A capacitor marked 104 is 10 with 4 more zeros or 100,000pF which is otherwise referred to as a .1  $\mu$ F capacitor.

Most kit builders don't need to go further, but I know you want to learn more. Anyway, Just to confuse you some more there is sometimes a tolerance code given by a single letter. I don't know why there were picked in the order they are, except that it kind of follows the middle row of keys on a typewriter.

So a 103J is a 10,000 pF with +/-5% tolerance

Letter symbol	Tolerance of capacitor
D	+/- 0.5 pF
F	+/- 1%
G	+/- 2%
H	+/- 3%
J	+/- 5%
K	+/- 10%
M	+/- 20%
P	+100% , -0%
Z	+80%, -20%

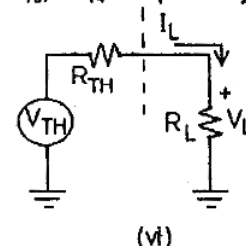
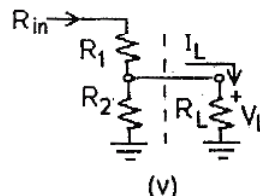
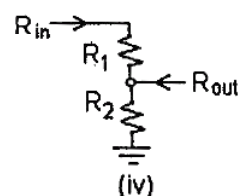
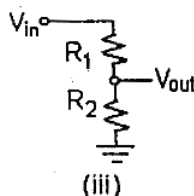
**II. Experiment:** (I) In the board identify the circuit shown in Fig.(i). *Question:* What is the resistance between terminals T3 and T7? Measure this resistance and thereby verify that the bottom ends of R2 and R3 are electrically joined. Will the resistance between T3 and T7 differ if the ground points are instead actually connected to some point in the planet Earth?



(II) Make the voltage divider connection, Fig.(ii). Using the multimeter's appropriate voltage range (**CAUTION:** in case of non auto-ranging multimeter, begin from the highest range and then switch to the range which gives maximum accuracy) measure the applied voltage  $V_{T3}$  at T3 (i.e. the voltage between T3 and ground). Verify that the voltage  $V_{T4}$  at T4 is given by

$$V_{out} = V_{in} \times R_2 / (R_1 + R_2), \quad \text{where } V_{in} = V_{T3} \text{ and } V_{out} = V_{T4}.$$

Thus Fig.(ii) corresponds to Fig.(iii) with  $V_{in}$ ,  $V_{out}$  replaced by  $V_{T3}$ ,  $V_{T4}$  respectively.



**Thevenin Model Of The Voltage Divider:** *Problem:* What are  $R_{in}$ ,  $R_{out}$  in Fig.(iv)? The voltage divider can be viewed in different ways, Figs.(iii)-(vi). Figure(v) and Fig.(vi) are general ways of viewing Fig.(iii). Figure(iii) is a special case of Fig.(v) or Fig.(vi) with  $R_L = \infty$ , i.e. no load case.

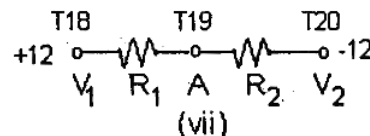
$R_{in}$  in Fig.(iv) and Fig.(v) is the resistance seen looking into the input terminal. Thus in Fig.(iii) and Fig.(iii)  $R_{in} = (R_1 + R_2)$ , whilst in Fig.(v)  $R_{in} = R_1 + (R_2 \parallel R_L)$ .

$R_{out}$  is the resistance seen by the load  $R_L$ . Assuming the voltage source is an ideal voltage source (source resistance =  $0 \Omega$ ),  $R_{out} = R_1 \times R_2 / (R_1 + R_2) = R_1 \parallel R_2$ .

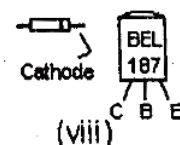
The Thevenin model of the voltage divider is a voltage source  $V_{TH}$  ( $=V_{out}$ ) in series with a source resistance  $R_{TH}$  ( $=R_{out}$ ), Fig.(vi).

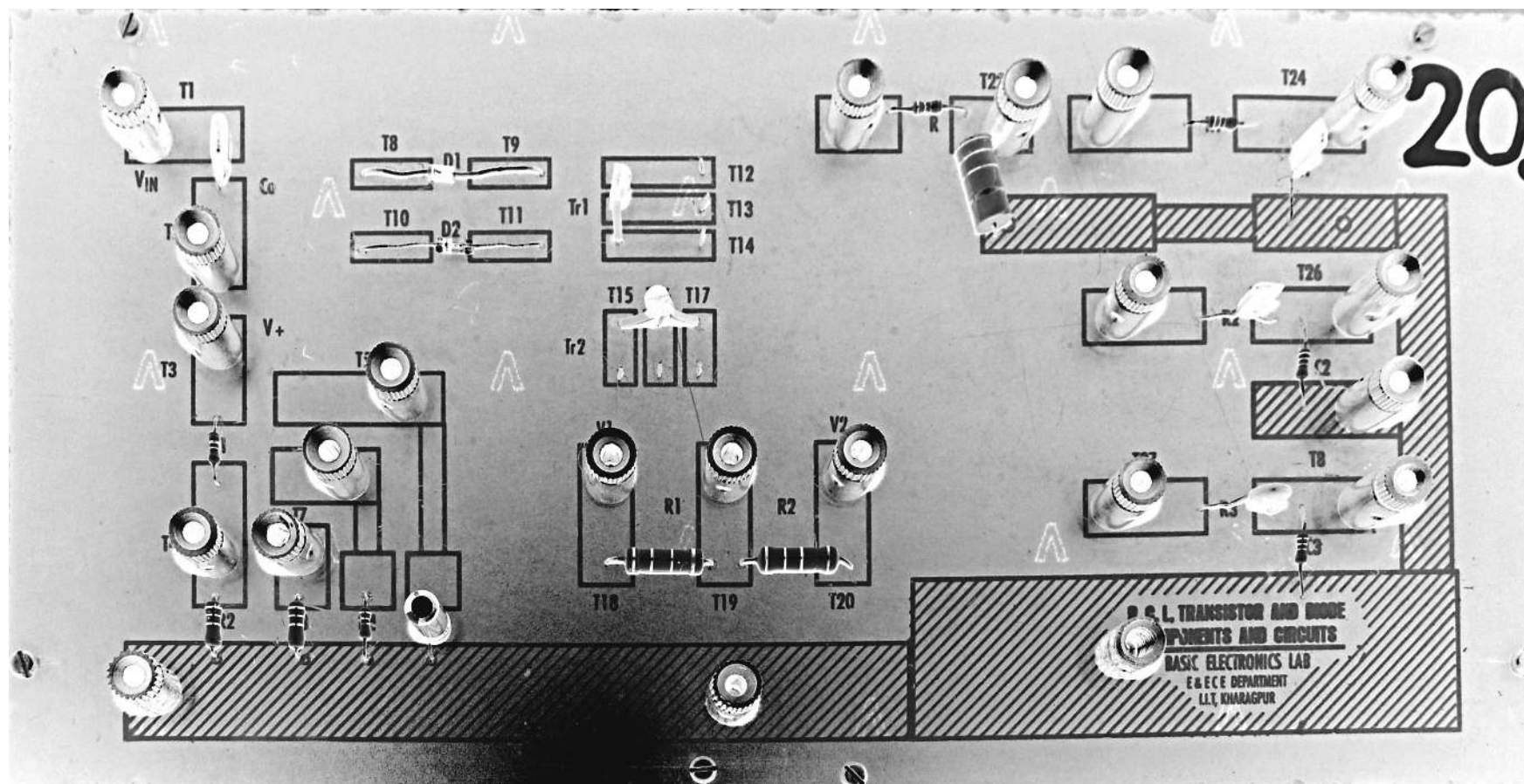
**III. Experiment:** (I) Calculate the voltage  $V_L$  and the current  $I_L$  in Fig.(v) using Ohm's law and in Fig.(vi) when (a)  $R_L = R_3$  (by connecting T7 to T4, Fig.(i)), (b)  $R_L = R_4$  (by connecting only T6 to T4), (c)  $R_L = R_3 \parallel R_4$  (by connecting T6 & T7 to T4). Compare your calculations with direct measurements of  $V_L$ . (II) Repeat (a) to (b) above, with capacitor  $C_b$  parallel to  $R_L$ , i.e. by connecting in addition T5 to T4.

(III) Make the connections shown in Fig.(vii) by applying +12V between T18 & ground and -12V between T20 & ground.  $V_A$  at T19 and compare with that given by  $V_A = (V_1 \times R_2 + V_2 \times R_1) / (R_1 + R_2)$ .



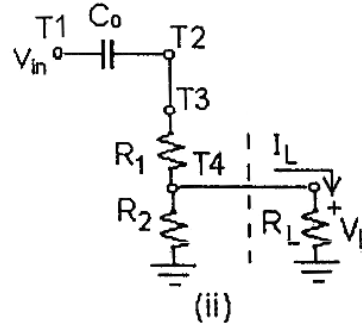
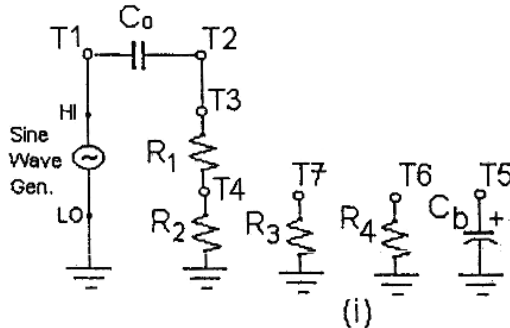
**IV. Active Devices:** (I) Locate the diodes  $D_1$ ,  $D_2$  and the transistors TR1, TR2 in the board. Identify their terminals. (II) Using the multimeter in the 'Diode-check' position determine the quality and thereby the semiconductor material type for each of these devices. (III) Verify that for transistors the forward bias diode drops  $IV_{BE} > IV_{BC}$ . Thus distinguish between the C and E terminals. (IV) Measure  $h_{FE}$  of the transistor if this measurement facility is available with your multimeter.





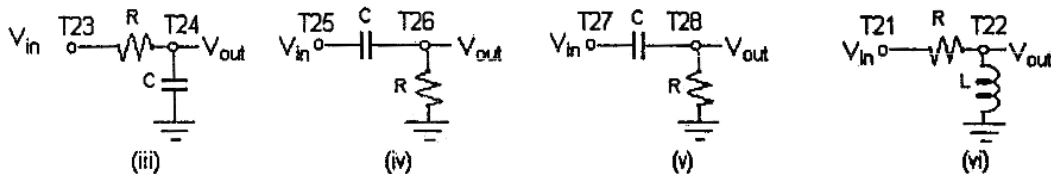
- Discrete components (R, C, diodes, transistors) on left-hand-side of the measurement-board are meant for Experiment 01
- R-C, C-R, R-L circuits on the right-hand-side are meant for Experiment 02

**BASIC ELECTRONICS LABORATORY**  
**EXPERIMENT NO: 2**  
**FAMILIARISATION WITH SIGNAL GENERATOR, OSCILLOSCOPE**  
**AND STUDIES ON RC, CR, and RL CIRCUITS**



**I. EXPERIMENT:**  
**VOLTAGE DIVIDER:**

- (i) Connect the voltage divider circuit shown in Fig.(i) and Fig.(ii).
- (ii) Set the signal generator to produce a 6 V p-p, 20 KHz sine wave. Apply this signal to CH1 (Y1) of your scope and measure/trace its amplitude and frequency; see Note I below.
- (iii) Display and measure  $V_L$ , Fig.(ii), in CH2 (Y2) for the cases where (a)  $R_L = \infty$ , i.e. no load case, (b)  $R_L = R_3$  (by connecting T7 to T4, Fig.(i)), (c)  $R_L = R_4$  (by connecting only T6 to T4), (d)  $R_L = R_3 \parallel R_4$  (by connecting T6 & T7 to T4),
- (iv) Compare these with  $V_L$  calculated using Thevenin model (Remark, note that for 20 KHz:  $X_{C0} = 1/\omega C_0 \ll R_1$ ).
- (v) Repeat steps(iii) & (iv) with capacitor  $C_b$  parallel to  $R_L$  (i.e. join in addition T5 to T4).



**II. EXPERIMENT:**  
**FREQUENCY RESPONSE:**

**(a) R-C Network:**

- (i) Record R & C values in Fig.(iii).
- (ii) Apply a sine wave signal  $V_{in}$  of about 1.2V p-p. Display and measure this signal in the Scope's CH1 (Y1).
- (iii) Display and measure  $V_{out}$  in CH2 (Y2).
- (iv) Maintain constant input amplitude, vary frequency in convenient steps over the range of your signal generator (at least from 10 Hz to 500KHz). Use step size such that less (more) readings are taken when  $V_{out}$  varies slowly (fast).
- (v) Plot  $V_{out}/V_{in}$  vs. frequency. See Note II below. Determine filter type.
- (vi) Record the 3 dB cutoff frequency  $f_c$ .
- (vii) Compare with the theoretical  $f_c = 1/2\pi RC$ .

**(b) C-R Network:**

- (i) Record the R & C values in Fig.(iv).
- (ii) Repeat steps a(ii) to a(vii).

P.T.O.

(iii) Record the R & C values in Fig.(v).

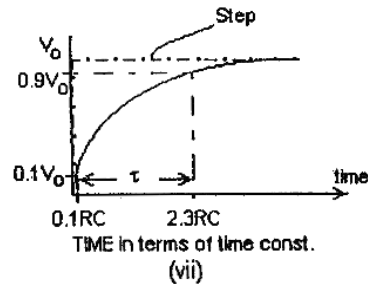
(iv) Repeat steps a(ii) to a(vii).

(c) **R-L Network:**

(i) Record the value of R in Fig.(vi). Here  $L \approx 2.2\text{mH}$ .

(ii) Repeat steps a(ii) to a(vi).

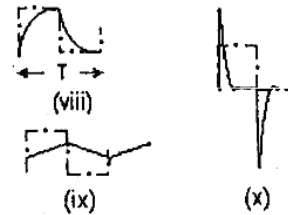
(iii) Compare with the theoretical  $f_c = R/2\pi L$ .



### III. EXPERIMENT:

#### PULSE RESPONSE:

- (i) Set the signal generator to produce a 1.2 V p-p pulse (or square) waveform. Apply this signal to CH1 (Y1) of your scope and measure/trace its amplitude and pulse repetition frequency (PRF = 1/T).
- (ii) Obtain/trace the indicated displays with the help of the typical oscilloscope settings shown in the table below. Your settings may differ due to component variations from board to board.



Circuit	V <sub>out</sub> displayed in CH2	PRF	Time/div	Volts/div for Output Display	Case
R-C, Fig.(iii)	Fig.(viii)	150 Hz	1ms	0.2 V	$T \gg RC$
R-C, Fig.(iii)	Fig.(ix)	1.5 KHz	0.2 ms	0.1 V	$T \ll RC$ , integrator
C-R, Fig.(v)	Fig.(x)	1.5 KHz	0.1 ms	0.2 V	$T \gg RC$ , differentiator
R-L, Fig.(vi)	Fig.(x)	15 KHz	50 $\mu\text{s}$	0.2 V	$T \gg L/R$ , differentiator

- (iii) For Fig.(viii) type response measure the rise time using Fig.(vii). Compare this with the theoretical:  $\tau = 2.2 RC = 0.35/f_c$ , where  $f_c$  is the 3 dB cutoff frequency or Low Pass Filter bandwidth.
- (iv) Obtain a variety of results using other values of PRFs.
- (v) Obtain comparable results for the circuit of Fig.(iv).

#### NOTE:

##### I. Typical Oscilloscope Settings:

Be certain that all scope controls are in their "Calibrated" position and that you know the horizontal and vertical sensitivity (scale factors) of the display.

Signal Input to:	CH1 (Y1)	CH2 (Y2)	Both the channels CH1 & CH2
Select Trigger Source From:	CH1 (Y1)	CH2 (Y2)	Channel having the larger amplitude signal

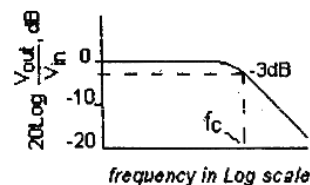
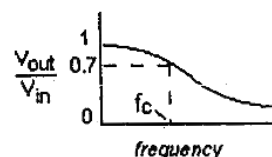
Adjust Vertical and Horizontal shift controls to centre the display.

Adjust Trigger Level control to stabilize the display.

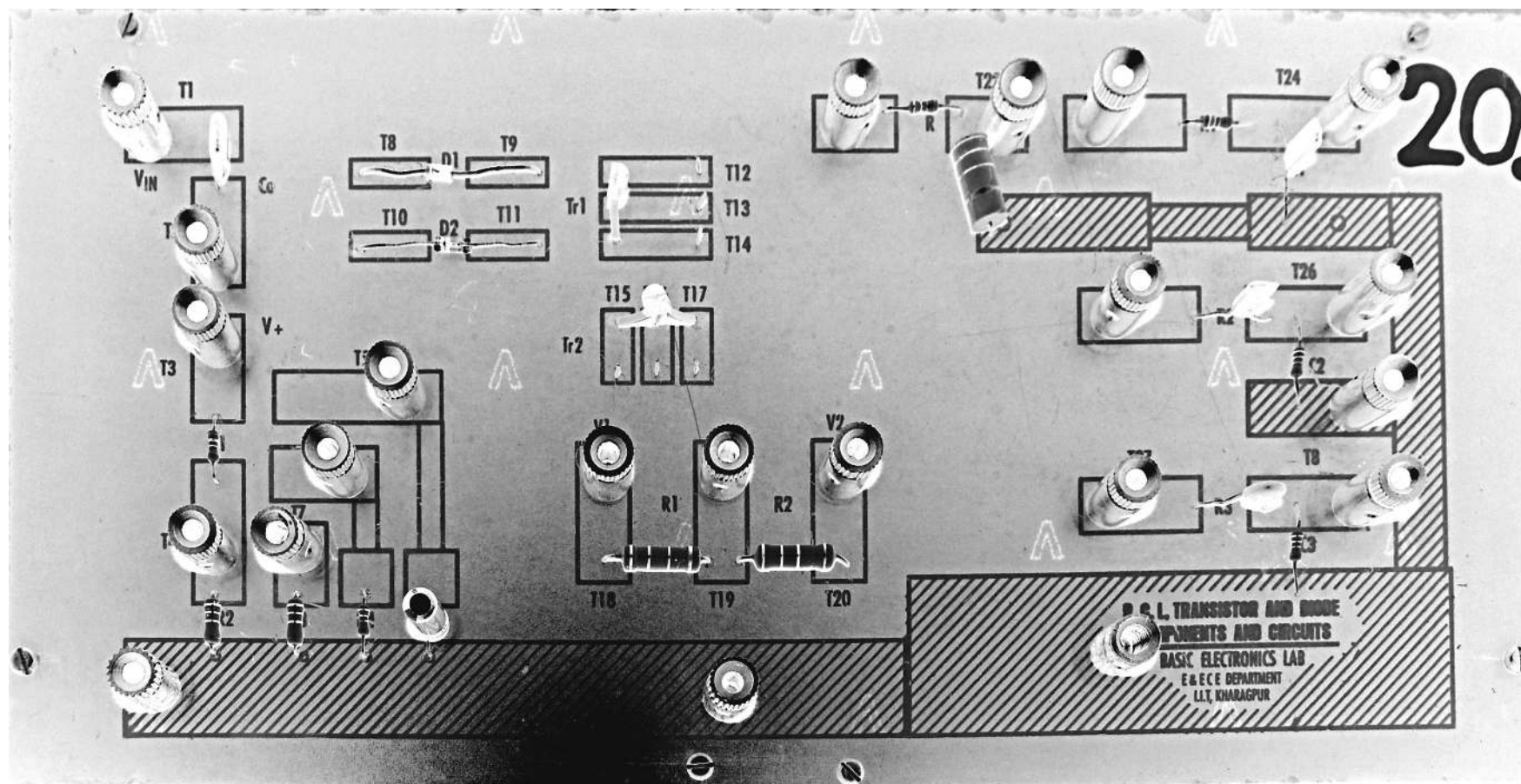
Signal Freq	1Hz	10Hz	100Hz	1KHz	10KHz	100KHz
Time/div	0.1ms	20ms	5ms- 1ms	1ms-0.1ms	0.1ms-10 $\mu\text{s}$	10 $\mu\text{s}$ - 1 $\mu\text{s}$

Signal Amp	20 V p-p	4V p-p	0.4V p-p	40mV p-p	10mV p-p
Volts/div	10V - 5V	2V - 0.5V	0.2V - 0.05V	20mV- 5mV	5mV- 2mV

- II. **Log-Log Plots:** Signal amplitudes seem to vary slowly with frequency in the scope whereas in the texts show sharp changes. This is an effect of the compression of the axes on the usual (Text's) graph. The scopes signal varies linearly; the text's version is log-log.

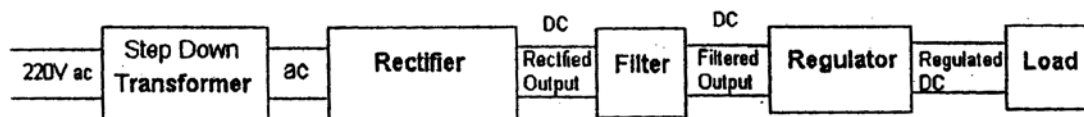




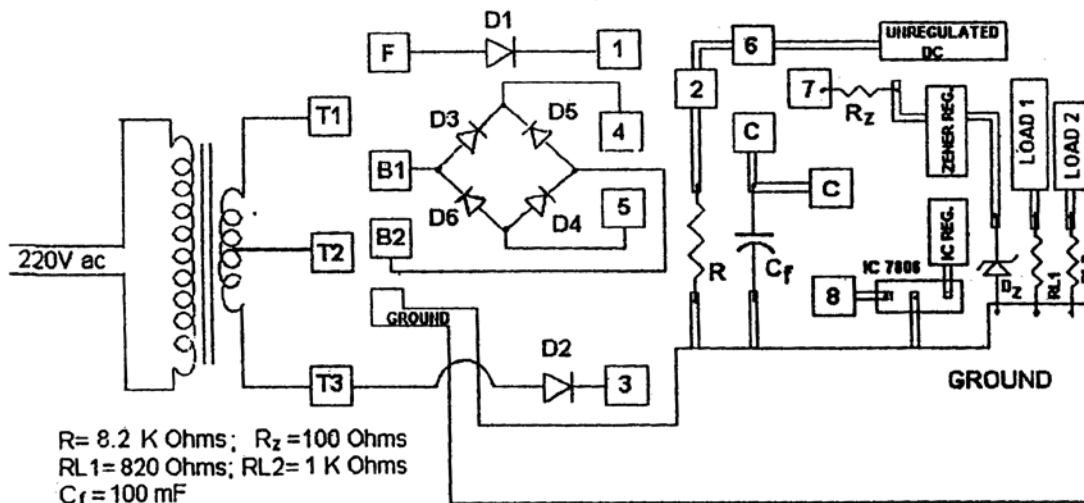


- Discrete components (R, C, diodes, transistors) on left-hand-side of the measurement-board are meant for Experiment 01
- R-C, C-R, R-L circuits on the right-hand-side are meant for Experiment 02

## STUDIES ON RECTIFIERS AND POWER SUPPLY



**Fig.1** POWER SUPPLY BLOCK DIAGRAM



**Fig.2** Circuit Board Layout.

### EXPERIMENT :

1. Trace the circuit in the board. Locate in the board the various components shown in Fig.2. Identify in the given board the various blocks of Fig.1.
2. Observe (and record) the transformer secondary voltages between the terminals 'T1' & 'T2', 'T2' & 'T3', and between 'T1' and 'T3' using Oscilloscope.
3. Realize the half wave rectifier using the steps given in Note I (i) below.
4. Observe the rectified waveform across 'Unregulated DC' & 'Ground' using Oscilloscope.
5. Determine  $V_m$  and calculate  $V_r(\text{rms})$  the rms value of the ac component (see Fig.3).
6. Switch the oscilloscope vertical input between ac and dc positions, observe the shift in the display and thereby obtain the dc component  $V_{dc}$ . A higher Volts/div may be needed to keep the shift within the screen. Measure  $V_{dc}$  using multimeter and compare.
7. Calculate the ripple factor =  $V_r(\text{rms})/V_{dc}$ .
8. Filter the rectified waveform using the steps given in Note II below.
9. Use the Oscilloscope to observe the ripple in the filtered output waveform. Using triangular waveform approximation obtain  $V_r(\text{rms})$  the rms value of the ac component. Repeat steps 6 and 7 to get the ripple factor with capacitor filter.
10. Realize the full wave rectifier of Note I(ii) below. Repeat steps 4 to 9.
11. Realize the full wave Bridge rectifier of Note I(iii) below. Repeat steps 4 to 9.
12. **Voltage Regulation:**
  - (a) Make the half wave rectifier connections using Note I(i).
  - (b) Note that now the 'Unregulated DC' terminal is the 'Output' terminal. Obtain  $V_{NL}$  and  $V_{FL}$  using the steps given in Note III(i)-(iv).
  - (c) Calculate the voltage regulation  $V.R. = (V_{NL} - V_{FL})/V_{FL}$ .
  - (d) Realize the full wave rectifier using Note I(ii). Repeat steps 12(b) & 12(c).

P.T.O.



(e) Realize the Bridge rectifier using Note I(iii). Repeat steps 12(b) & 12(c).

(f) **Zener Diode Regulation:**

- (i) Obtain the full wave rectified and filtered voltage using Note I(ii) & II or I(iii) & II.
- (ii) Apply this voltage to the Zener Regulator by making the connections between terminals 'C' & '7'.
- (iii) The terminal 'Zener Regltd' is now the 'Output' terminal. Follow Note III(i)-(iv) to obtain  $V_{NL}$  and  $V_{FL}$ . Repeat step 12(c).

(g) **IC 7806 Regulation:**

- (i) Repeat steps 12(f)(i).
- (ii) Apply this voltage to the IC 7806 Regulator by connecting the terminals 'C' & '8'.
- (iii) The terminal 'IC Regltd' is now the 'Output' terminal. Follow Note III(i)-(iv) to obtain  $V_{NL}$  and  $V_{FL}$ . Repeat step 12(c).

**NOTE:**

I. **Rectifier Realizations:** Rectified output is obtained at the 'Unregulated DC' terminal, on making the following connections

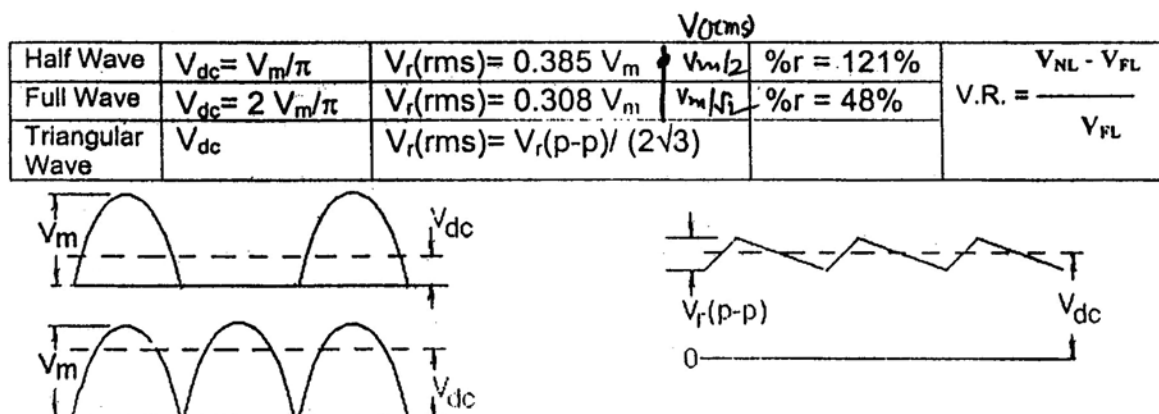
- (i) **Half Wave:** Remove all connections. Join 'T1' & 'F', 'T2' & 'Ground', '1' & '2'.
- (ii) **Full Wave with center-tapped transformer:** Remove all connections. Join 'T1' & 'F', 'T2' & 'Ground', '3' & '1', '1' & '2'
- (iii) **Full Wave Bridge Rectifier:** Remove all connections. Join 'T1' & 'B1', 'T2' & 'B2', '5' & 'Ground', '4' & '2'.

II. **Filtering the Rectified Signal:** Connect the terminals '6' & 'C'. The filtered output is then available at the terminal 'Unregulated DC'.

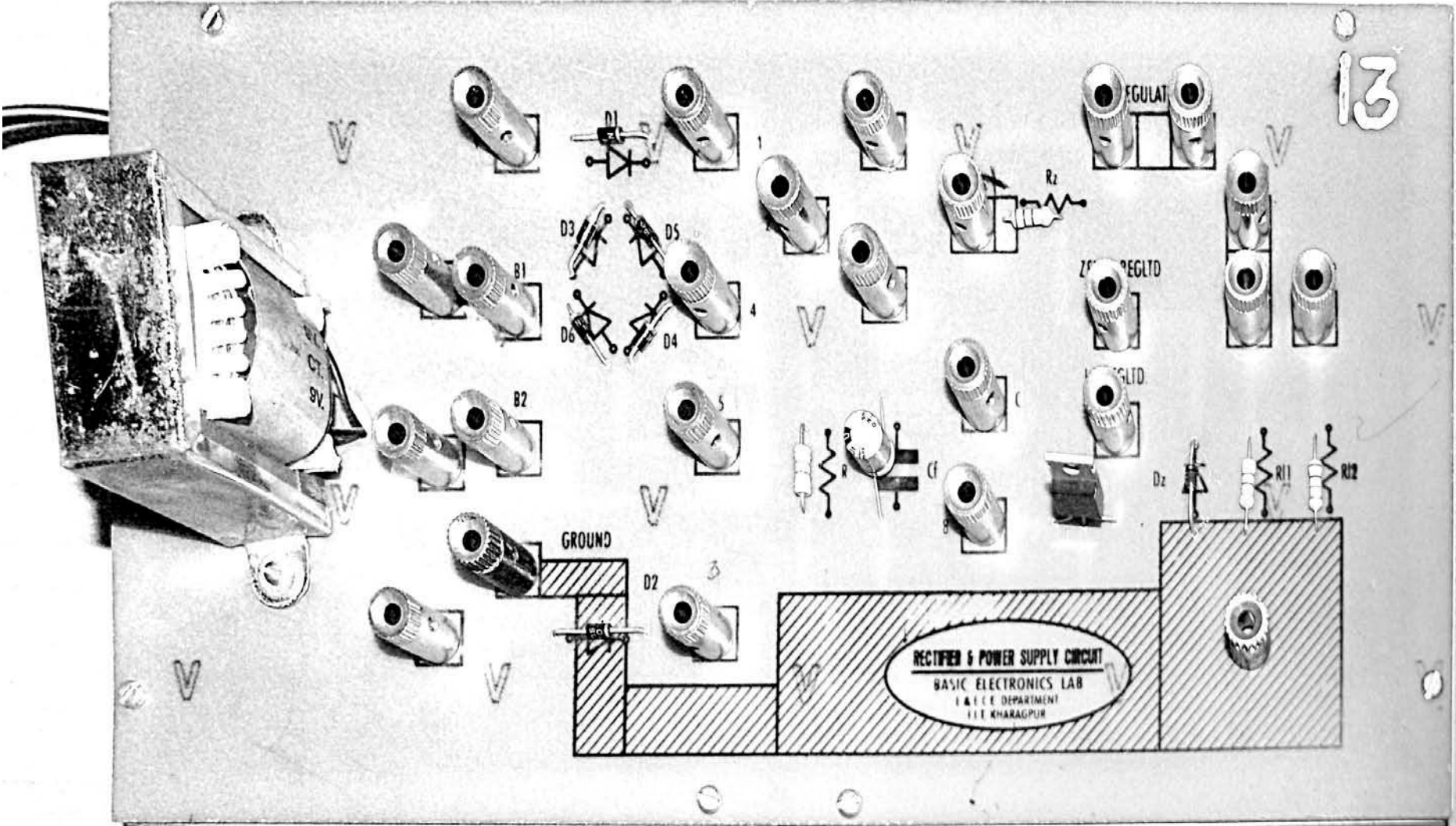
III. **Output voltage across various Loads** is obtained as follows:

- (i) Measure voltage  $V_{NL}$  at the 'Output' terminal when no load is connected.
- (ii) Connect load  $R_{L1}$  by joining the terminals 'Load 1' and 'Output'. Measure the voltage at the 'Output' terminal.
- (iii) Disconnect  $R_{L1}$ . Connect load  $R_{L2}$  by joining the terminals 'Load 2' and the 'Output'. Measure the voltage at the 'Output' terminal.
- (iv) Apply full load by connecting together 'Load 1', 'Load 2', and 'Output'. Measure the full load voltage  $V_{FL}$  at the 'Output' terminal.

IV. **The ac readings** of the multimeter (or the ac millivoltmeter) is correct only for sinusoidal ac waveforms. The readings of these instruments will be in error when the input is half wave, or full wave or triangular wave.



**Fig.3**



STUDIES ON SMALL SIGNAL CE AMPLIFIER

Trace the circuit of the CE-amplifier given in Part-1 of the board (see bottom side). Note down the component values and match them against Fig.1.

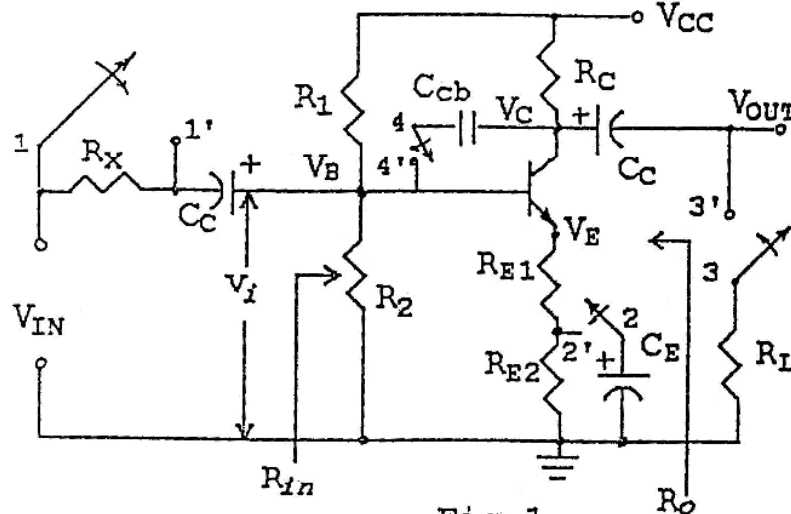


Fig. 1

$R_1 = 47K$   
 $R_2 = 4.7K$   
 $R_C = 6.8K$   
 $R_{E1} = 0.33K$   
 $R_{E2} = 0.33K$   
 $R_X = 1K$   
 $R_L = 1K$   
 $C_C = 10mF$   
 $C_E = 100mF$   
 $C_{Cb} = 33pF$

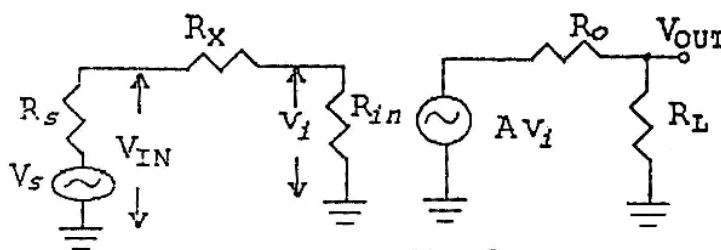


Fig. 2

Measurement of DC conditions:

Supply +12 Volts  $V_{CC}$  to the amplifier circuit from the dc power supply. Remember to connect the power supply ground to the circuit ground! Measure  $V_B$ ,  $V_C$ , and  $V_E$ . Remember these voltages are measured with respect to the circuit ground. Knowing these and the resistance values calculate  $V_{BE}$ ,  $V_{CE}$ ,  $I_C$  and  $I_E$ . Determine whether the amplifier is biased in the active region and whether the Q-point is suitably located.

Measurement of Signal Handling Capacity:

- (i) Short the resistor  $R_X$  (by connecting a jumper wire across it; i.e. by joining the points 1 – 1' in Fig.1. Bypass  $R_{E2}$  by joining points 2 – 2' (thereby connecting  $C_E$  across  $R_{E2}$ ). Apply a mid-band frequency (say 4 KHz) sinusoidal voltage of about 100 mV p-p amplitude at  $V_{IN}$  and observe the output waveform on the CRO. Measure the gain. Increase the input voltage in steps and measure

the corresponding output voltages. Note the maximum input voltage  $V_{SM}$  for which the gain remains constant (or beyond which the  $V_{OUT}$  vs  $V_{IN}$  curve deviates from a straight line). This is the signal handling capacity. A quick (but crude) way of determining  $V_{SM}$  is to note the maximum input voltage for which the CRO displayed output voltage remains undistorted. Note when using CRO, it is convenient to measure the peak to peak voltage.

- (ii) Now connect the load  $R_L$  by joining points 3 – 3'. Measure  $V_{SM}$ . Compare this result with that of (i).

#### Measurement of Frequency Response:

- (i) Keep  $R_X$  shorted, load  $R_L$  and capacitor  $C_E$  connected. Choose a convenient sinusoidal  $V_{IN}$  (amplitude well below  $V_{SM}$ ). Vary the frequency over the range of your signal generator (say 100 Hz – 1000 KHz) in convenient steps. Record the corresponding  $V_{OUT}$  at each step. It is convenient to choose a constant amplitude  $V_{IN}$ . This may be ensured by noting the peak-to-peak amplitude in the CRO at each frequency step. Increase the number of steps in regions where change in  $V_{OUT}$  is large. Plot the frequency response of the amplifier (i.e. plot  $20\log(V_{OUT}/V_{IN})$  vs frequency). From the plot determine the lower and upper cutoff frequencies. These are the frequencies at which the ratio  $20\log(V_{OUT}/V_{IN})$  falls 3-dB below its maximum value.
- (ii) Now disconnect load  $R_L$  by removing the connection between the points 3-3'. Obtain the frequency response as in (i) above.
- (iii) Effect of  $C_E$ : Keep 1 – 1', 3 – 3' connected. Remove the connection between 2 – 2'. Measure the frequency response. Compare with (i) above. Finally, consider the case when point 2' is instead connected to the emitter (i.e.  $R_{E1}$  &  $R_{E2}$  are fully bypassed) and measure the frequency response. Compare this response with those above.
- (iv) Miller effect due to  $C_{cb}$ : Disconnect 1 – 1'. Connect 2 – 2' and 3 – 3'. Now measure the frequency response when  
 (a) terminals 4 – 4' are connected,  
 (b) terminals 4 – 4' are disconnected.  
 Compare the results of (a) and (b) above.

#### Measurement of Input Resistance in the Mid-Frequency Range:

Connect 1 – 1', 2 – 2' and disconnect 3 – 3', 4 – 4'. For a  $V_{IN}$  having amplitude well below the signal capacity  $V_{SM}$  and frequency well within the midfrequency range, measure the output voltage  $V_{OUT}|_O$ . [From Fig.2:  $V_{OUT}|_O = A \cdot V_S \cdot R_{IN} / (R_{IN} + R_S)$ ]. Now disconnect 1 – 1' and measure the output voltage  $V_{OUT}|_{R_X}$ . [From Fig.2:  $V_{OUT}|_{R_X} = A \cdot V_S \cdot R_{IN} / (R_{IN} + R_S + R_X)$ ].

$$\text{Then the input resistance is given by: } R_{IN} = \frac{R_X \cdot V_{out}|_{R_X}}{V_{out}|_O - V_{out}|_{R_X}} - R_S$$

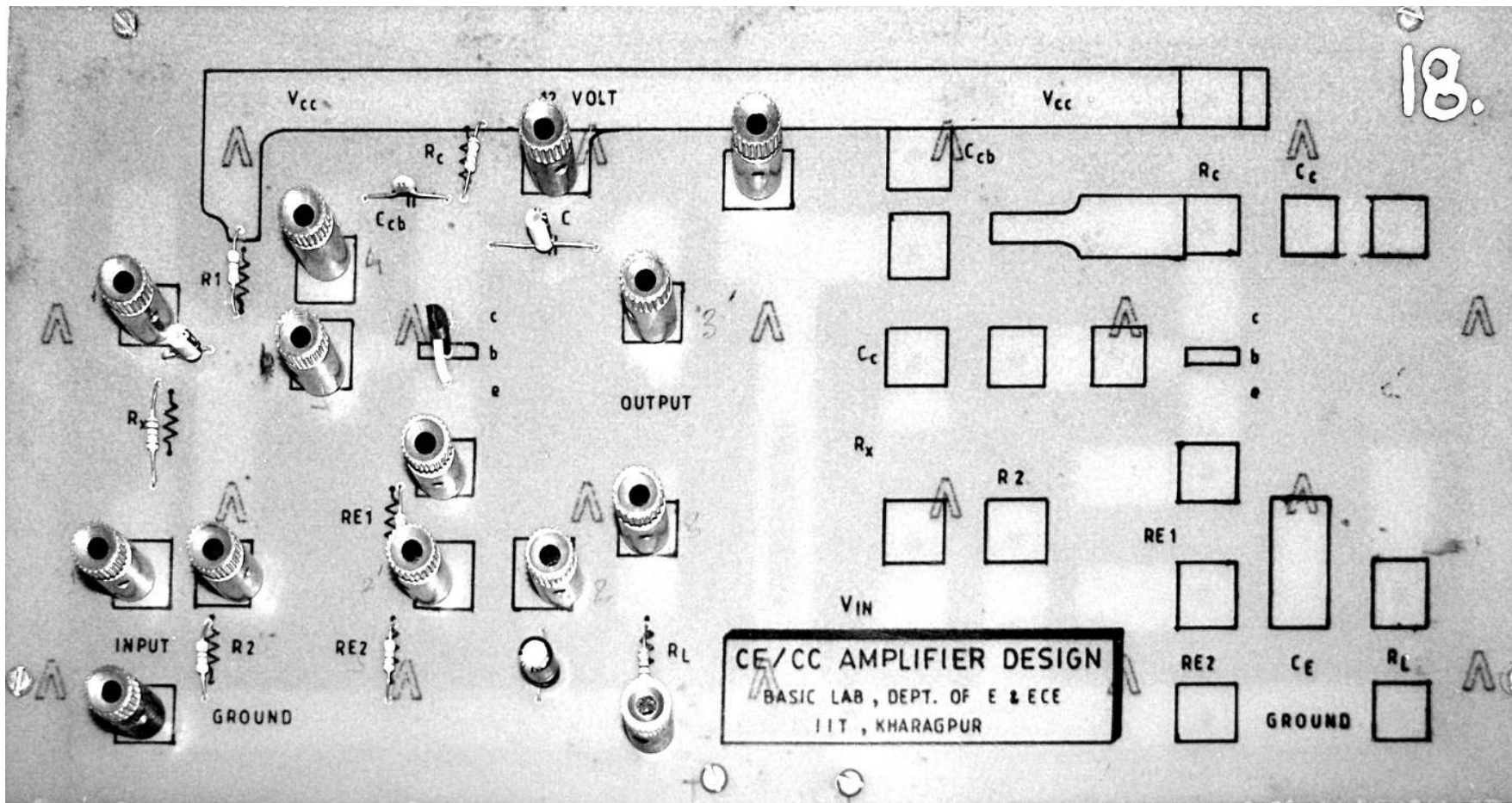
#### Measurement of Output Resistance in the Mid-Frequency Range.

Connect 1 – 1', 2 – 2', 3 – 3' and disconnect 4 – 4'. Then for a  $V_{IN}$  well below the signal handling capacity  $V_{SM}$  and frequency well within the midfrequency range let the measured output voltage be  $V_{OUT}|_{R_L}$ . [From Fig.2:  $V_{OUT}|_{R_L} = A \cdot V_{IN} \cdot R_L / (R_O + R_S)$ ].

Now disconnect 3 – 3'. Then the measured output voltage is  $V_{OUT}|_{\infty}$ . [From Fig.2:  $V_{OUT}|_{\infty} = A \cdot V_{IN}$ ]. Then the output resistance is given by

$$R_{OUT} = R_L \cdot \frac{V_{OUT}|_{\infty} - V_{OUT}|_{R_L}}{V_{OUT}|_{R_L}}$$





## STUDIES ON ANALOG CIRCUITS USING OP-AMP

### PROCEDURE:

I. Trace the circuit in the board. Locate the components of Fig.1a. Figure 1b shows the op-amp IC 741 pin configuration. The board is powered by a bipolar supply (+12 and -12 V versus ground). Near the top of the board is a voltage divider. If terminal V4 is grounded then we have the approximate no load voltages  $V_1=+6.5V$ ,  $V_2=+3.3V$  and  $V_3=2.2V$ . If instead -12V is applied to terminal V4 then we have approximately:  $V_1=+1.0V$ ,  $V_2=-5.4V$  and  $V_3=-7.7V$ .

#### II. DC Gain

a. Realise the op-amp in the inverting configuration shown in Fig.2. Use  $R_i=10K\Omega$  and  $R_f=10K\Omega$ . Apply the bipolar supply to power the board and thereby the amplifier. **Note:** We have stopped indicating op-amp power supply connections. Remember that these connections must be made. Apply an input of 1V dc (use the voltage divider to obtain this voltage). Measure the actual values of  $V_{in}$  as this will be  $< 1V$  due to input resistance  $R_i$  of the circuit. Compare your results with  $V_{out} = -(R_f/R_i)V_{in}$ . Repeat this procedure for  $R_f=27K\Omega$ ,  $47K\Omega$  and  $100K\Omega$ .

b. **Virtual ground.** With  $R_i=10K\Omega$  and  $R_f=100K\Omega$ , measure the voltage at the inverting input pin2 of the op-amp. Can you say that the pin2 is at virtual ground compared to  $V_{in}$ ?

c. **Input Resistance:** Measure the voltage across  $R_i$  (which we will call  $V_i$ ) and use this to calculate  $I_i$ . Now measure  $V_{in}$ . Calculate the input impedance  $R_{in}=V_{in}/I_i$ . Your answer, of course, will be very close to  $R_i$ .

With  $V_{in}=1V$ ,  $R_i=1K\Omega$  and  $R_f=10K\Omega$ , calculate and then measure  $V_{out}$ . Repeat for  $R_f=27K\Omega$ ,  $47K\Omega$  and  $100K\Omega$ . At what point does the amplifier cease to be linear? At what output voltages does the op-amp saturate? Repeat this procedure for  $V_{in}$  with other dc values. How are the saturation voltage levels related to the power supply voltages?

#### III. Non Inverting Amplifier:

a. Realise the noninverting amplifier shown in Fig.3. Use  $R_i=10K\Omega$ ,  $R_f=10K\Omega$ . Apply a 1V<sub>pp</sub>, 10KHz input. Measure the gain and compare this with your calculations. Do this for  $R_f=27K\Omega$ ,  $47K\Omega$  and  $100K\Omega$  as well. Make a table comparing experimental value for the gain and the computed values. Can you tell from what you see on the oscilloscope whether or not the output is inverted? Calculate the reactance of the capacitor at 10KHz. Is it necessary to include this in your gain calculations?

b. **Frequency Response:** Measure the gain  $A_f$  of the circuit in Fig.3 from 1 to 100KHz in convenient steps (say 10KHz), for  $R_f=27K\Omega$ ,  $47K\Omega$  and  $100K\Omega$ , keeping  $R_i=10K\Omega$ . You should notice that the high gain circuit begins to roll off sooner than the lower gain circuit. Determine the bandwidth and then the gainxbandwidth product in each case. The gain with feedback resistor  $R_f$  is given by  $A_f = A_0 / (1 + \beta A_0)$  where  $\beta = R_i / (R_i + R_f)$ . Use your data to calculate  $A_0$ .

#### IV. Voltage follower:

Realise the circuit of Fig.4. Apply  $V_{in}=1V$  dc. Is the inverting pin2 at virtual ground? Explain. Verify that  $V_{out}=V_{in}$ . Also find the maximum (+ve) and minimum (-ve) voltages where this stops being true.

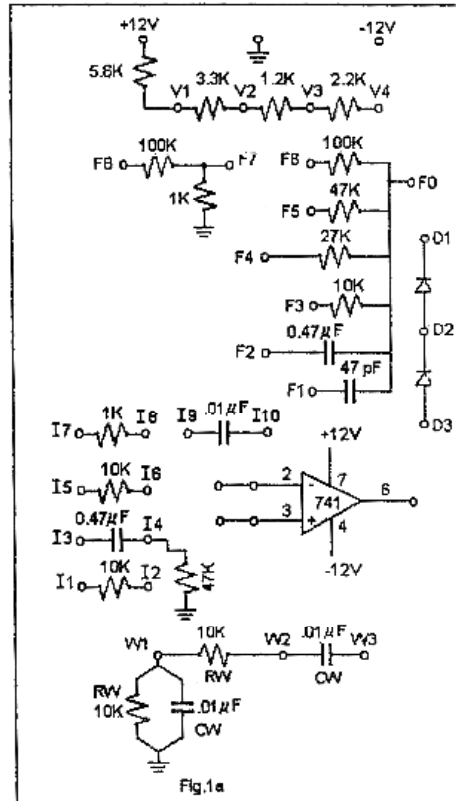


Fig.1a

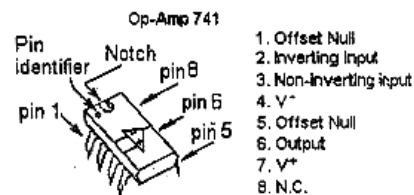


Fig.1b

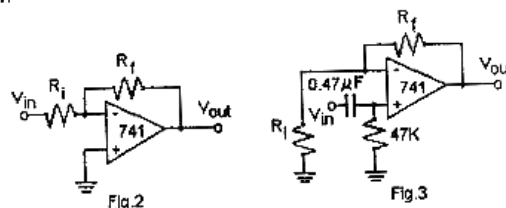


Fig.2

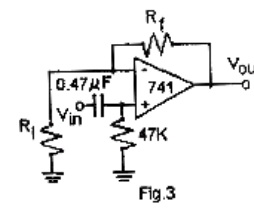


Fig.3

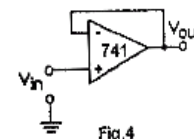


Fig.4



**V. Adder:**

a. Build the adder circuit of Fig.5. Apply dc voltages of  $V_1=2V$  and  $V_2=3V$  to the inputs. Measure and record the actual  $V_1$ ,  $V_2$  and  $V_{out}$ . Compare with theory.

b. **Summing Amplifier** The same circuit can be used to add DC offset to a signal. Apply a  $1V_{p-p}$ , 1KHz signal to  $V_1=V_{in}$ . Apply DC voltages ranging from 6.5V to -7.5V to  $V_2=V_{offset}$ . Display  $V_{out}$  in the scope and observe the DC offset (by switching the ac/dc switch of the scope input).

**VI. Superposition:** a. We have till now considered circuits that accept signals at only one of the two input terminals of the op amp (the inverting or the noninverting inputs). In this experiment we shall work with an op-amp circuit (Fig.6a) that provides simultaneous inputs at the inverting and noninverting terminals. The relation between  $V_{out}$  and the inputs can be obtained using Horowitz and Hill's Golden Rules. However, use can also be made of the superposition theorem: which in this case implies that if  $V_{out1}$  ( $V_{out2}$ ) is the response due to input  $V_1$  ( $V_2$ ) acting alone, i.e. with the other input  $V_2$  ( $V_1$ ) being zeroed (grounded in this case). Then response due to both inputs  $V_1$  and  $V_2$  acting simultaneously is  $V_{out} = V_{out1} + V_{out2}$ .

**Procedure:** Choose  $R_f=10K\Omega$ . Apply  $V_1=3V$  and  $V_2=2V$  dc. Measure  $V_1$ ,  $V_2$ , and  $V_{out}$  and compare with theory. Repeat this procedure for  $R_f=47K\Omega$  and  $100K\Omega$ .

b. **Differential Amplifier:** Realise the circuit of Fig.6b.

Here:  $V_{out} = V_2 \times [R_3/(R_2+R_3)] \times (1+R_f/R_1) - V_1 \times (R_f/R_1)$   
 Choose  $R_1=10K\Omega$ ,  $R_2=10K\Omega$ ,  $R_3=47K\Omega$  and  $R_f=27K\Omega$ . Apply  $V_1=2V$  and  $V_2=3V$  dc. Measure and record the actual values of  $V_1$ ,  $V_2$  and  $V_{out}$ . Compare measured  $V_{out}$  with theory. Repeat this procedure for  $R_f=47K\Omega$ . Note for  $R_2=R_1$  and  $R_3=R_f$  the result is considerably simplified:  
 $V_{out} = (R_f/R_1) \times (V_2 - V_1)$ . The output is directly proportional to the difference of the inputs.

**VII. Integrator**

Realise the circuit of Fig.7. Apply a 5KHz sine-wave of  $1V_{p-p}$ . Observe  $V_{out}$  and  $V_{in}$  together in the scope and observe the phase difference. Also measure the gain and compare with theory. Next apply a  $1V_{p-p}$ , 5KHz square wave input. Observe and record  $V_{out}$  and  $V_{in}$  together in the scope. Record and trace the display. Repeat the above for frequencies ranging from 1KHz to 10KHz. Compare your results with theory [ $V_{out} = -(1/RC) \int V_{in} dt + \text{const}$ ].

**VIII. Differentiator**

Realise the circuit of Fig.8. Apply a  $0.2V_{p-p}$ , 1KHz square wave to the input. Look at the input and output together in the oscilloscope. Record/Trace your results. Repeat the above with frequencies ranging from 1KHz to 10KHz. Compare your results with theory [ $V_{out} = -RC \times (dV_{in}/dt)$ ]. Repeat the above for a sine wave and then for a triangular wave.

**IX. Active Rectifier**

Realise the circuit of Fig.9a. Apply a sine wave ( $V_{p-p}=0.1V$ , 1KHz). Look at the output and input simultaneously in an oscilloscope. Record the display. Next construct the Improved rectifier of Fig.9b and repeat the above. Compare these results.

**X. Wien Bridge Oscillator:**

Realise the circuit shown in Fig.10. Choose  $R_f=10K\Omega$  and  $R_i=10K\Omega$ . If oscillations occur, measure the frequency of the output waveform. Compare with the theoretical  $f=(1/2\pi RC)$ , where  $R=10K$  and  $C=0.01\mu F$ . Repeat this procedure for  $R_f=27K\Omega$ ,  $27K\Omega$ ,  $100K\Omega$  and  $100K\Omega$ . Use your data to obtain the ratio  $R_f/R_i$  for which oscillations occur. Also determine the ratio for which the output is a good sine-wave.

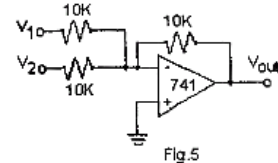


Fig.5

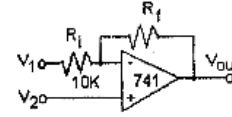


Fig.6a

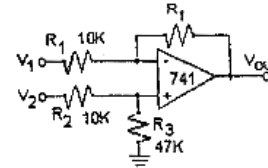


Fig.6b

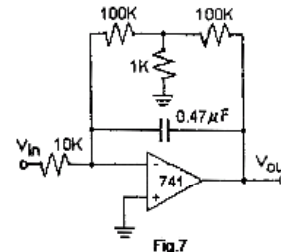


Fig.7

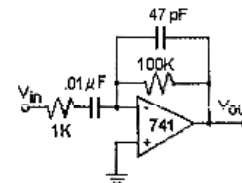


Fig.8

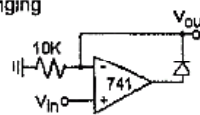


Fig.9a

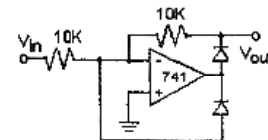


Fig.9b

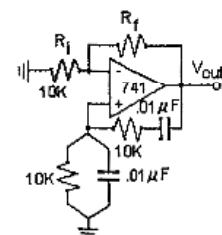
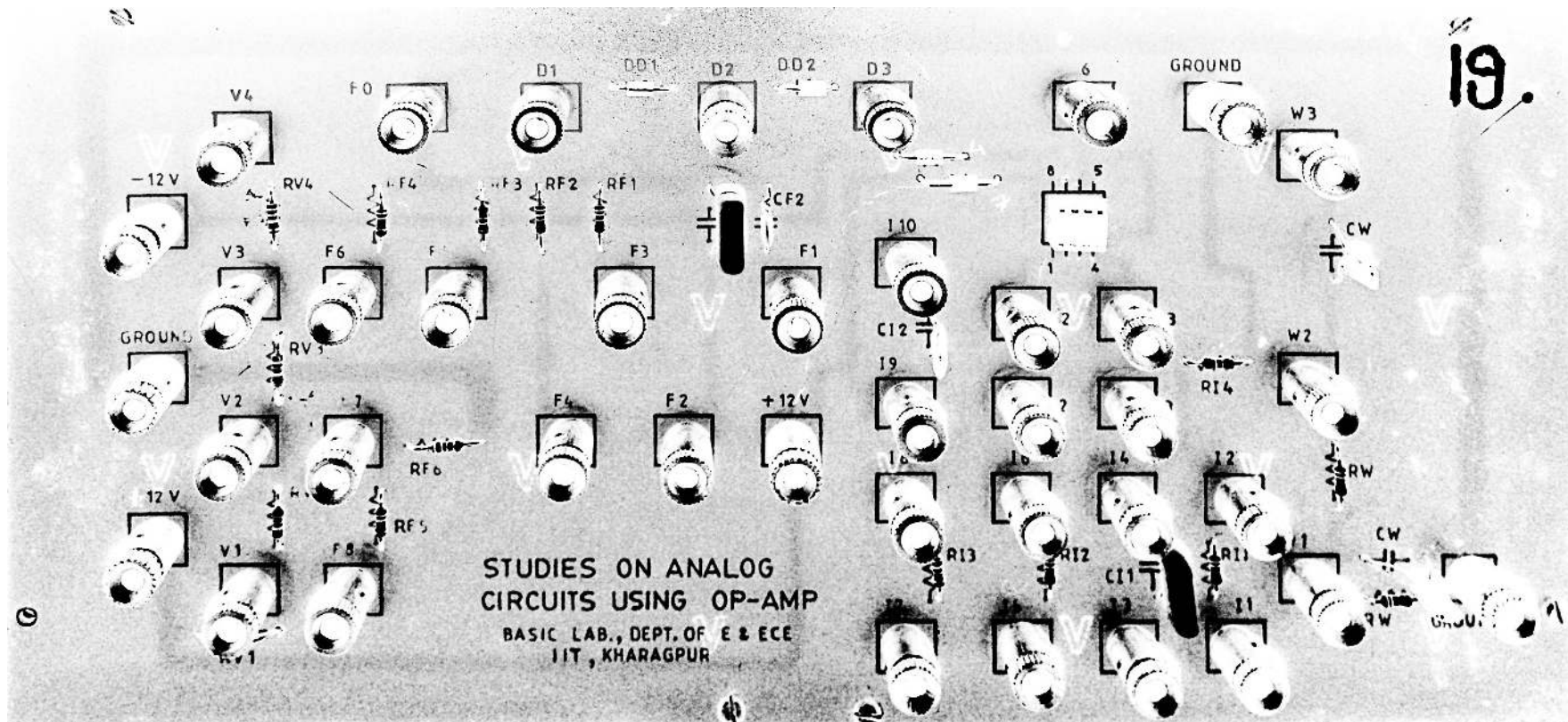


Fig.10



**BASIC ELECTRONICS LABORATORY**  
**EXPERIMENT NO: 6**  
**STUDIES ON LOGIC GATES**

**A Note On the circuit layout:** The board consists of 6 IC's. These are all quad two-input TTL logic gate IC's. The input/output pins of all IC's except 7402 (NOR) are same.

These IC's are from top to bottom: 7408 (AND), 7432 (OR), 7400 (NAND), 7400 (NAND), 7402 (NOR), 7486 (XOR).

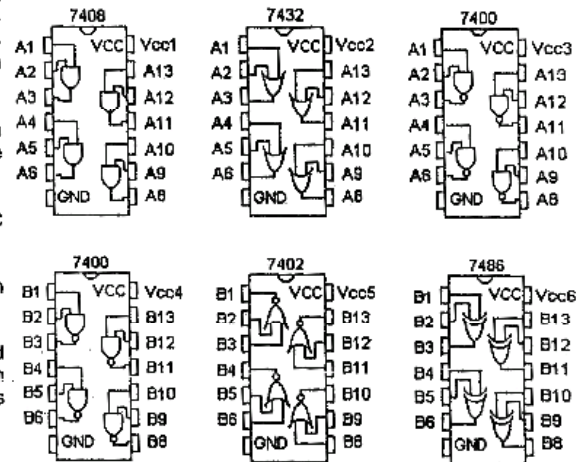
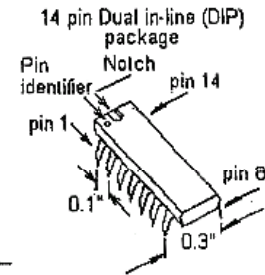
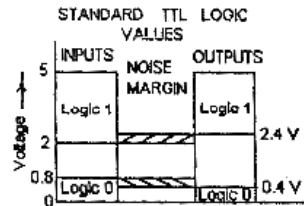
The top (bottom) three IC's form the group A (B) where each IC has its pins 1 to 6 connected to terminals A1 to A6 (B1 to B6) respectively. The pins 8 to 13 are connected to terminals A8 to A13 (B8 to B13) respectively.

Pin 7 of all six IC's are grounded. The V<sub>cc</sub> pin 14 of each IC is individually connected to the respective terminals V<sub>cc</sub>1 to V<sub>cc</sub>6.

Applying a +5V supply to the V<sub>cc</sub> pin of an IC activates (selects) it.

**Logic Inputs:** The available voltage for Logic High (Low) input is +5V (0V).

**Caution:** Atmost two IC may be selected simultaneously, provided only one of the top A (bottom B) group of IC's 7408, 7432 or 7400 (group of IC's 7400, 7402 or 7486) is activated at any given time.

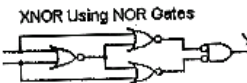
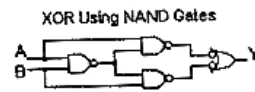


**Experiment:** In the following experiments consider all possible combinations of input logic levels. Note down in tabular form the measured voltages and then the corresponding logic levels. Connect the output to the LED input and then record the corresponding output voltage/logic levels. Thus obtain the truth table. Note that the LED lights up when the LED input is high. The Logic Gate diagrams below are drawn such that they have their inputs on the left and outputs on the right.

(i) Realize AND, OR, NOT, NOR, XOR logic elements using only NAND gates.

XOR gate as controlled inverter:

- (i) Apply a 1 KHz (TTL compatible) square waveform to one of the inputs (A) of an XOR gate (which could be any one of the four XOR gates available in IC 7486).
- (ii) Keep the other input (instead of B lets call it INVERT) to the XOR gate low and compare the output (Y) and (A) input waveforms.
- (iii) Keep the INVERT input high and compare the output (Y) and the (A) input waveforms. Observe the controlled inversion feature.



(ii) Realize AND, OR, NOT, NAND, XNOR logic elements using only NOR gates.

(iii) Verification of De Morgan's Theorems: Implement the following:

(a)  $F = (X + Y)'$  using IC 7402 and compare with  $F = X' \cdot Y'$  realized using IC 7400/7408.

(b)  $F = (X \cdot Y)'$  using IC 7400 and compare with  $F = X' + Y'$  realized using ICs 7400/7432.

(iv) Verification of Theorems in Switching Algebra:

Realize

(a)  $F = X + X \cdot Y$  using IC 7400 and compare with  $F = X$ .

(b)  $F = X \cdot (X + Y)$  using IC 7402 and compare with  $F = X$ .

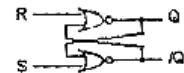
(c)  $F = X + X' \cdot Y$  using IC 7400 and compare with  $F = X + Y$  realized using IC 7400.

(d)  $F = (X + Y) \cdot (X + Z)$  using IC 7400 and compare with  $F = X + Y \cdot Z$  realized using IC 7400.

P.T.O.

(V) LATCHES:

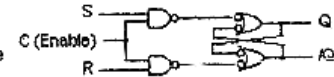
- (a) Realize the S, R latch using IC 7402. Obtain the truth table.  
 (i) Apply  $S=1, R=1$  and determine  $Q=?$ ,  $\bar{Q}=?$ .  
 (ii) Next apply  $S=0, R=0$  and determine the new outputs  $Q=?$ ,  $\bar{Q}=?$ .  
 (iii) Repeat steps (i), (ii) with variations of the sequence in which  $S=0, R=0$  is applied. Explain the results.



- (b) Realize the  $\bar{S}, \bar{R}$  latch using IC 7400. Obtain the truth table.  
 (i) Apply  $\bar{S}=0, \bar{R}=0$  and determine  $Q=?$ ,  $\bar{Q}=?$ .  
 (ii) Next apply  $\bar{S}=1, \bar{R}=1$  and determine the new outputs  $Q=?$ ,  $\bar{Q}=?$ .  
 (iii) Repeat steps (i), (ii) with variations of the sequence in which  $\bar{S}=1, \bar{R}=1$  is applied. Explain the results.



- (c) Realize the S, R latch with enable using IC 7400. Obtain the truth table.

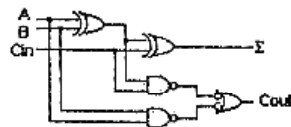


- (i) Observe the outputs for the following sequence of inputs:  
 $C=0, S=1, R=1$ ;  $C=1, S=1, R=1$ ; and then  $C=0, S=1, R=1$ .  
 (ii) Repeat step (i) and explain your results.

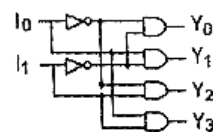


- (d) Realize the D latch using ICs 7400.

- (VI) Realize the Full Adder using IC 7400 and IC 7486.

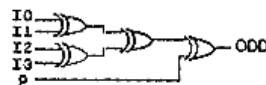


- (VII) Realize the 2 to 4 Decoder using IC 7408 and IC 7400.

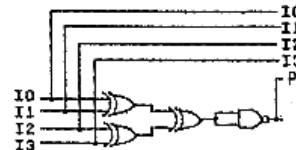


- (VIII) Parity Generator/Checker: Error detecting codes use an extra bit called parity bit, to detect errors in the transmission and storage of data. In an Odd Parity code, the parity bit (P) is chosen so that the total number of 1 bits in a code word is odd.

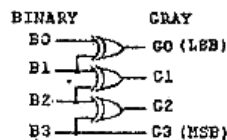
- (a) Realize an Odd Parity Checker for a 5 bit input word using IC 7486.



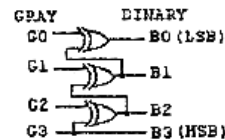
- (b) Realize a Parity generator if the parity of the 5 bit code  $I_0, I_1, I_2, I_3$  & P is Odd independent of the 4 bit input word.



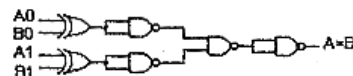
- (IX) Realize 4 bit binary to Gray code conversion logic using IC 7486.



- (X) Realize 4 bit Gray code to binary conversion logic using IC 7486.



- (XI) Comparators: Realize using IC 7486 and IC 7400 a logic circuit to compare binary numbers containing two bits.



- (XII) Multiplexer (data selector): Realize the 2- input multiplexer using IC 7400

