Lovely Professional University, Punjab

Course Code	Course Title	Course Planner	Lectures	Tutorials	Practicals	Credits
CSE211	COMPUTER ORGANIZATION AND DESIGN	23368::Umer Iqbal Wani	3	1	0	4
Course Weightage	ATT: 5 CA: 25 MTT: 20 ETT: 50	**Exam Category: 55: Mid Term Exam: All Subjective – End Term Exam: All Subjective**				
Course Orientation	COMPETITIVE EXAMINATION (Higher Education), KNOWLEDGE ENHANCEMENT					

Course Outcomes :Through this course students should be able to

CO1 :: review the structure and functioning of a digital computer and understand its overall system architecture.

CO2 :: describe and understand the generic principles that underlie the building of a digital computer, digital logic and memory hierarchy

CO3 :: analyze the working of memory unit and study the examples of mapping techniques for different cache memory systems

CO4 :: understand functioning of the basic building blocks of a computer

CO5 :: visualize the underlying architecture and connection of various hardware components of a computer

CO6 :: develop innovative architectural designs of computers based on the common and fundamental concepts

	TextBooks (T)		
Sr No	**Title**	**Author**	**Publisher Name**
T-1	COMPUTER SYSTEM ARCHITECTURE	MORRIS MANO	PRENTICE HALL

	Reference Books (R)		
Sr No	**Title**	**Author**	**Publisher Name**
R-1	COMPUTER ARCHITECTURE A QUANTITATIVE APPROACH	HENNESSY,J.L,DAVID A PATTERSON, AND GOLDBERG	PEARSON
R-2	COMPUTER ORGANIZATION AND ARCHITECTURE-DESIGNING FOR PERFORMANCE	WILLIAM STALLINGS	PRENTICE HALL

LTP week distribution: (LTP Weeks)	
Weeks before MTE	7
Weeks After MTE	7
Spill Over (Lecture)	7

Detailed Plan For Lectures

Week Number	Lecture Number	Broad Topic(Sub Topic)	Chapters/Sections of Text/reference books	Other Readings, Relevant Websites, Audio Visual Aids, software and Virtual Labs	Lecture Description	Learning Outcomes	Pedagogical Tool Demonstration/ Case Study / Images / animation / ppt etc. Planned	Live Examples
Week 1	Lecture 1	Basics Of Digital Electronics(Logic gates)	T-1 R-2		Introduction to the course Introduction of digital computer, Logic gates and flip flops	Students will understand about course contents and basic of digital electronics	Demonstration with PPT	Digital electronics is based entirely on the fundamental principles of Boolean logic. Consider the following devices: i . A soda machine which accepts coins and dispenses cans of soda ii. a microwave oven with programmable power levels and timers iii. a hand-held calculator

Week 1	Lecture 1	Basics Of Digital Electronics(Introduction to combinational circuit)	T-1 R-2		Introduction to the course Introduction of digital computer, Logic gates and flip flops	Students will understand about course contents and basic of digital electronics	Demonstration with PPT	Digital electronics is based entirely on the fundamental principles of Boolean logic. Consider the following devices: i . A soda machine which accepts coins and dispenses cans of soda ii. a microwave oven with programmable power levels and timers iii. a hand-held calculator
		Basics Of Digital Electronics(introduction to sequential circuits)	T-1		Introduction to the course Introduction of digital computer, Logic gates and flip flops	Students will understand about course contents and basic of digital electronics	Demonstration with PPT	Digital electronics is based entirely on the fundamental principles of Boolean logic. Consider the following devices: i . A soda machine which accepts coins and dispenses cans of soda ii. a microwave oven with programmable power levels and timers iii. a hand-held calculator
	Lecture 2	Basics Of Digital Electronics(Multiplexers and De multiplexers)	T-1 R-2		Introduction to multiplexers, Decoders, Flip flops	Students will understand how Muxs, Decoders, Flip flops function	Demonstration with diagrams	

Week 1	Lecture 2	Basics Of Digital Electronics(Decoder and Encoder)	T-1		Introduction to multiplexers, Decoders, Flip flops	Students will understand how Muxs, Decoders, Flip flops function	Demonstration with diagrams	
		Basics Of Digital Electronics(Flip flops)	T-1 R-2		Introduction to multiplexers, Decoders, Flip flops	Students will understand how Muxs, Decoders, Flip flops function	Demonstration with diagrams	
	Lecture 3	Register Transfer and Micro Operations(Register Transfer Language and Register Transfer)	T-1		Discussion on Bus and Memory Transfers, Bus selection and three state bus buffers	i. Students will understand transfer between Processor registers through buses ii. Understand transfer between Processor register and memory through buses	Demonstration with images	
Week 2	Lecture 4	Register Transfer and Micro Operations(register transfer)	T-1		Operations are performed on the binary data stored in the register	Student will learn about the 16 Logical micro-operations and practice its applications	Peer Learning	

Week 2	Lecture 5	Register Transfer and Micro Operations(Logic Micro Operations)	T-1 R-2		Discussion on Shift registers (left and right shift registers etc.)	.Students will understand about data storage in shift registers. ii. Understand the movement of data in shift registers.	Demonstration with PPT	The most common uses of a shift register is to convert between serial and parallel interfaces. This is useful as many circuits work on groups of bits in parallel, but serial interfaces are simpler to construct. ii. Shift registers can be used as simple delay circuits. iii. Bidirectional shift registers could be connected in parallel for a hardware implementation of a stack.
	Lecture 6	Register Transfer and Micro Operations(arithmetic microoperations)	T-1		Introduction of micro-operations and internal hardware organization of a digital computer.	i. Students will understand about processing task of digital hardware modules. ii. Understand the Micro-operations of system.	Discussion with Images	Internal hardware organization of a digital computer
Week 3	Lecture 7	Register Transfer and Micro Operations(Shift Micro Operations)	T-1		Discussion on Arithmetic and logical shift unit	Students will learn about the working of ALSU	Peer Learning	
	Lecture 8	Computer Organization (instruction codes)	T-1		Introduction to basic computer organization and show how its operation can be specified with register transfer statement.	i. Students will understand about internal registers,control structure and instruction . ii. Understanding of Common bus system	Discussions with images and PPT	

Week 3	Lecture 9	Computer Organization (computer registers)	T-1		Introduction to basic computer organization and show how its operation can be specified with register transfer statement.	i. Students will understand about internal registers,control structure and instruction . ii. Understanding of Common bus system	Discussions with images and PPT	
Week 4	Lecture 10	Computer Organization (common bus system)	T-1		Discussion on basic computer instruction format and timing for register	Students will understand the elements of modern instructions sets and explain their impact on processor desig	Discussion with images	Control Unit of a computer system
	Lecture 11	Computer Organization (instruction cycle)	T-1		Explain the basics of instruction execution on a computer.	. Understand the characteristics of an instruction set and how it maps to underlying hardware. ii. Identify and analyze the design and function of the basic instruction execution elements of a modern processo	discussions with image	
	Lecture 12	Computer Organization (memory reference instructions)	T-1		Discussion on memory reference instructions and interrupt cycle	Students will identify and analyze the design and function of the basic instruction execution elements of a modern processor	Discussion thorough knowledge and understanding of key concepts	
		Computer Organization (input-output and interrupt)	T-1		Discussion on memory reference instructions and interrupt cycle	Students will identify and analyze the design and function of the basic instruction execution elements of a modern processor	Discussion thorough knowledge and understanding of key concepts	
Week 5	Lecture 13				Test 1			
	Lecture 14	Central Processing Unit (General Register Organization)	T-1		Introduction to various data processing operations performed in CPU and storage device that store information	i) Understand the organization and architecture of CPU. ii) To understand stack based processor organization. ii. Instruction set of a stack organized processor	Discussion with examples	

An instruction plan is only a tentative plan. The teacher may make some changes in his/her teaching plan. The students are advised to use syllabus for preparation of all examinations. The students are expected to keep themselves updated on the contemporary issues related to the course. Upto 20% of the questions in any examination/Academic tasks can be asked from such issues even if not explicitly mentioned in the instruction plan.

Week 5	Lecture 15	Central Processing Unit (Data Transfer and Manipulation)	T-1		Describing about different modes of transfer and categories of computer instruction including program control instructions	Students will learn about computer instruction and data transfer instruction	Peer Learning	
		Central Processing Unit (Program control)	T-1		Describing about different modes of transfer and categories of computer instruction including program control instructions	Students will learn about computer instruction and data transfer instruction	Peer Learning	
Week 6	Lecture 16	Central Processing Unit (Addressing Modes)	T-1		Describing about different modes of transfer and categories of computer instruction	Students will learn about computer instruction and data transfer instruction	Students will learn about computer instruction and data transfer instruction	
	Lecture 17	Central Processing Unit (Complex instruction set computer)	T-1		CISC and RISC variable length instructions in multiple cycles	Students will understand the CISC and RISC Architecture	peer learning	
	Lecture 18	Central Processing Unit (Reduced instruction set computer)	T-1		CISC and RISC variable length instructions in multiple cycles	Students will understand the CISC and RISC Architecture	peer learning	
Week 7	Lecture 19	Central Processing Unit (Reduced instruction set computer)	T-1		CISC and RISC variable length instructions in multiple cycles	Students will understand the CISC and RISC Architecture	peer learning	
		SPILL OVER						
Week 7	Lecture 20				Spill Over			
	Lecture 21				Spill Over			
		MID-TERM						
Week 8	Lecture 22	Input-Output Organization (Input Output Interface)	T-1		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Discussion with images	

Week 8	Lecture 22	Input-Output Organization (Data transfer schemes)	T-1		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Discussion with images	
	Lecture 23	Input-Output Organization (Direct memory access transfer)	T-1		Discussion on types of data transfer schemes and Discussion on DMA used when multiple bytes are to be transferred between memory and IO devices	. Students will understand the concept of Direct memory access to memory for data transfers ii. Learn how DMA used when multiple bytes are to be transferred between memory and IO devices iii. Learn DMA Data transfer mechanism between I/O devices and system memory with the least processor intervention using DMAC	Discussion with Image	A sound card may need to access data stored in the computer's RAM, but since it can process the data itself, it may use DMA to bypass the CPU. Video cards that support DMA can also access the system memory and process graphics without needing the CPU. Ultra DMA hard drives use DMA to transfer data faster than previous hard drives that required the data to first be run through the CPU

Week 8	Lecture 23	Input-Output Organization (Input/Output processor.)	T-1		Discussion on types of data transfer schemes and Discussion on DMA used when multiple bytes are to be transferred between memory and IO devices	. Students will understand the concept of Direct memory access to memory for data transfers ii. Learn how DMA used when multiple bytes are to be transferred between memory and IO devices iii. Learn DMA Data transfer mechanism between I/O devices and system memory with the least processor intervention using DMAC	Discussion with Image	
	Lecture 24	Input-Output Organization (Input/Output processor.)	T-1		Discussion on types of data transfer schemes and Discussion on DMA used when multiple bytes are to be transferred between memory and IO devices	. Students will understand the concept of Direct memory access to memory for data transfers ii. Learn how DMA used when multiple bytes are to be transferred between memory and IO devices iii. Learn DMA Data transfer mechanism between I/O devices and system memory with the least processor intervention using DMAC	Discussion with Image	
Week 9	Lecture 25	Input-Output Organization (Priority interrupt)	T-1		Introduction to input output subsystem of a compute	Students will understand the mode of communication between the central system and out side environment	Discussion with images	
		Input-Output Organization (modes of data transfer)	T-1		Introduction to input output subsystem of a compute	Students will understand the mode of communication between the central system and out side environment	Discussion with images	

Week 9	Lecture 26	Memory hierarchy(main memory)	T-1		Describing about RAM and ROM chips , Auxiliary memory is also discussed. Associative memory- Describing about Argument register Match Logic etc	Students will learn about content addressable memory	Peer discusion	Content addressable memory is often used in computer networking devices. For example, when a network switch receives a data frame from one of its ports, it updates an internal table with the frame's source MAC address and the port it was received on. It then looks up the destination MAC address in the table to determine what port the frame needs to be forwarded to, and sends it out on that port. The MAC address table is usually implemented with a binary CAM so the destination port can be found very quickly, reducing the switch's latency

Week 9	Lecture 26	Memory hierarchy(auxiliary memory)	T-1		Describing about RAM and ROM chips , Auxiliary memory is also discussed. Associative memory- Describing about Argument register Match Logic etc	Students will learn about content addressable memory	Peer discusion	Content addressable memory is often used in computer networking devices. For example, when a network switch receives a data frame from one of its ports, it updates an internal table with the frame's source MAC address and the port it was received on. It then looks up the destination MAC address in the table to determine what port the frame needs to be forwarded to, and sends it out on that port. The MAC address table is usually implemented with a binary CAM so the destination port can be found very quickly, reducing the switch's latency

Week 9	Lecture 26	Memory hierarchy (associative memory)	T-1		Describing about RAM and ROM chips , Auxiliary memory is also discussed. Associative memory- Describing about Argument register Match Logic etc	Students will learn about content addressable memory	Peer discusion	Content addressable memory is often used in computer networking devices. For example, when a network switch receives a data frame from one of its ports, it updates an internal table with the frame's source MAC address and the port it was received on. It then looks up the destination MAC address in the table to determine what port the frame needs to be forwarded to, and sends it out on that port. The MAC address table is usually implemented with a binary CAM so the destination port can be found very quickly, reducing the switch's latency
	Lecture 27				Test 2			
Week 10	Lecture 28	Memory hierarchy(cache memory)	T-1		Discussion on types of mapping techniques in cache memory	Students will learn about basic concepts of cache memory	Peer Learning	
	Lecture 29	Memory hierarchy(virtual memory)	T-1		Discussion on page table ,memory mapping table	Students will understand about how to manage memory space and address space	Discussion with images	

Week 10	Lecture 30	Introduction to Parallel Processing(Pipelining)	T-1		Detailed discussion on instruction pipelining in computer.	Introduction to pipelining and its types	Peer Learning	
Week 11	Lecture 31	Introduction to Parallel Processing(Pipelining)	T-1		Detailed discussion on instruction pipelining in computer.	Introduction to pipelining and its types	Peer Learning	
	Lecture 32	Introduction to Parallel Processing(Characteristics of multiprocessors)	T-1 R-1		Introduction to parallel processing and multiprocessors	Amdahl's law , chracteristics of multiprocessors	Discussion with examples	
		Introduction to Parallel Processing(parallel processing)	T-1 R-1		Introduction to parallel processing and multiprocessors	Amdahl's law , chracteristics of multiprocessors	Discussion with examples	
	Lecture 33	Introduction to Parallel Processing(Interconnection Structures)	T-1 R-1		Various multiprocessor interconnection structures	Students will learn about Time-shared, Multiport memory, crossbar switch, hypercube interconnection	Discussions with images and diagrams	
Week 12	Lecture 34				Test 3			
	Lecture 35	Multiprocessors (Categorization of multiprocessors (SISD,MIMD,SIMD.SPMD) , Introduction to GPU)	T-1 R-1		Different categories of multiprocessors, introduction to GPU	Students will learn about multiprocessor calssification, and GPU	Discussion with images	
	Lecture 36	Multiprocessors (Categorization of multiprocessors (SISD,MIMD,SIMD.SPMD) , Introduction to GPU)	T-1 R-1		Different categories of multiprocessors, introduction to GPU	Students will learn about multiprocessor calssification, and GPU	Discussion with images	
Week 13	Lecture 37	Latest technology and trends in computer architecture (multi-cores processor.)	T-1 R-1		Latest processor architecture study is done	Student will learn about latest processor architectures	Demonstration and discussions	
		Latest technology and trends in computer architecture (microarchitecture)	T-1 R-1		Latest processor architecture study is done	Student will learn about latest processor architectures	Demonstration and discussions	
	Lecture 38	Latest technology and trends in computer architecture (latest processor for smartphone or tablet and desktop)	T-1 R-1		Discussion on new nonvolatile memory technology and discussion on various processors	Students will learn about new processor and new memory technology with there architectures	Peer Learning	
	Lecture 39	Latest technology and trends in computer architecture (latest processor for smartphone or tablet and desktop)	T-1 R-1		Discussion on new nonvolatile memory technology and discussion on various processors	Students will learn about new processor and new memory technology with there architectures	Peer Learning	

Week 14	Lecture 40	Latest technology and trends in computer architecture (next generation processors architecture)	T-1 R-1		Latest processor architecture study is done	Student will learn about latest processor architectures	Demonstration and discussion	
		SPILL OVER						
Week 14	Lecture 41				Spill Over			
	Lecture 42				Spill Over			
Week 15	Lecture 43				Spill Over			
	Lecture 44				Spill Over			
	Lecture 45				Spill Over			

Scheme for CA:

CA Category of this Course Code is:A0203 (2 best out of 3)

Component	Weightage (%)	Mapped CO(s)
Test 1	50	CO1, CO2
Test 2	50	CO2, CO4, CO5
Test 3	50	CO3, CO5, CO6

Details of Academic Task(s)

Academic Task	Objective	Detail of Academic Task	Nature of Academic Task (group/individuals)	Academic Task Mode	Marks	Allottment / submission Week
Test 1	To check the subject understanding and learning ability of the students	Will be covering syllabus from Week 1 to Week 5. All questions should be of 5 marks each or in multiples of 5	Individual	Offline	30	4 / 5
Test 2	To check the subject understanding and learning ability of the students	Will be covering syllabus from Week 6 to Week 8. All questions should be of 5 marks each or in multiples of 5	Individual	Offline	30	8 / 9
Test 3	To check the subject understanding and learning ability of the students	Will be covering syllabus from Week 9 to Week 11. All questions should be of 5 marks each or in multiples of 5	Individual	Offline	30	11 / 12

Plan for Tutorial: (Please do not use these time slots for syllabus coverage)

Tutorial No.	Lecture Topic	Type of pedagogical tool(s) planned (case analysis,problem solving test,role play,business game etc)
Tutorial1	Problem Solving on Logic Gates	Problem Solving
Tutorial2	Problems based on Bus and Memory transfer and Arithmetic and shift Micro operations	Problem Solving
Tutorial3	Problem Solving on Register transfer and Register transfer language and Instruction Codes	Problem Solving
Tutorial4	Problem Solving on Control Timing Signals and Instruction Cycle	Problem Solving
Tutorial5	Problem Solving on Memory Reference Instructions and Input Output interrupt	Problem Solving
Tutorial6	Problem Solving on program and Micro Program Control,	Problem Solving
Tutorial7	Problem Solving on Data Transfer, Manipulation and Addressing Modes	Problem Solving
After Mid-Term		
Tutorial8	Problem Solving on Data Transfer Schemes, Program Control and Interrupts	Problem Solving
Tutorial9	Problem Solving on Direct Memory Access and Memory Hierarchy	Problem Solving
Tutorial10	Problem Solving on Cache Memory, Associative Memory and Virtual Memory	Problem Solving
Tutorial11	Problem Solving on Addition and Subtraction algorithm	Problem Solving
Tutorial12	Problem Solving on Multiplication algorithm	Problem Solving
Tutorial13	Problem Solving on Booth Multiplication algorithm	Problem Solving
Tutorial14	Problem Solving on Division Algorithm	Problem Solving