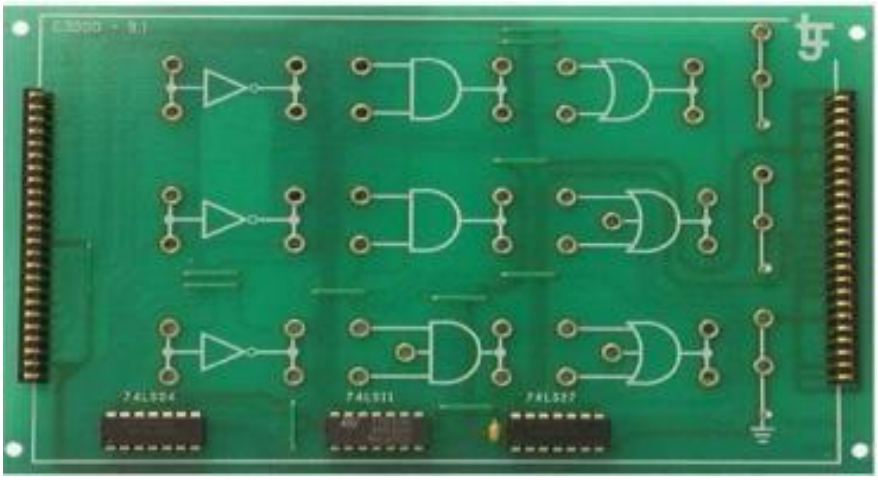
LABORATORY MANUAL

ECE216

Digital Electronics Laboratory



Name of the Student……..
Registration Number/Roll No…….
Section and Group……..
School of Electronics and Electrical Engineering

LOVELY PROFESSIONAL UNIVERSITY
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General guidelines for the students

Lab Safety:

• Avoid contacting circuits with wet hands or wet materials.

• All current transmitting parts of any electrical devices must be enclosed.

• Maintain a work space clear of extraneous material such as books, papers, and clothes.

• Never change wiring with circuit plugged into power source.

• Place the IC's properly in the bread board, Don't break the IC pins by forcefully inserting in bread board.

• Switch off the power supply when not in use.

• Always cut wire leads so the clipped wire falls on table top and not towards others.

• Use only tools and equipment with non-conducting handles when working with electrical devices.

• When checking an operating circuit, keep one hand either in a pocket or behind your back to avoid making a closed circuit through the body.

• Never plug leads into power source unless they are connected to an established circuit.

Table of Content

Experiment 1

1. Aim: To analyze and implement Boolean Expressions using Basic Logic Gates (AND, OR, NOT, NOR, NAND and XOR gates).

Apparatus Required: IC 7408, 7432, 7404, IC 7486, 7400, 7402, 7486 and Digital Training Kit.

2. Learning Objectives: This experiment enables a student to learn

- How to analyze logic gates
- How to express Boolean expression using logic gates
- How to check equivalence of two Boolean expressions using logic gates
- How to check equivalence of two logic circuits consisting of multiple gates

3. Theory: Analysis of Logic gates using 7408, 7432, 7404 Power Supply. Diagrams of each chip are shown in figures

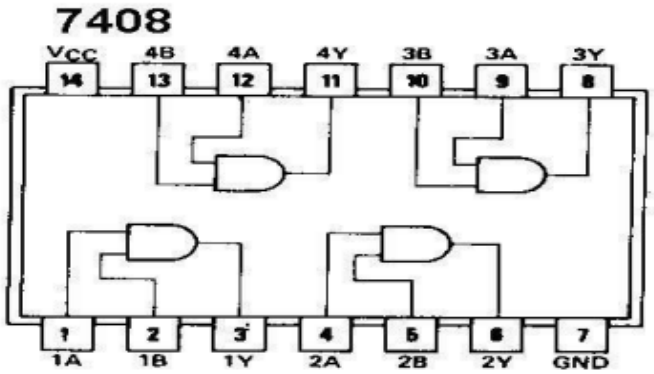


Figure1

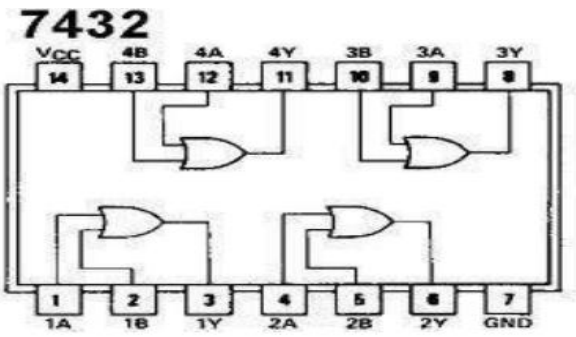


Figure2

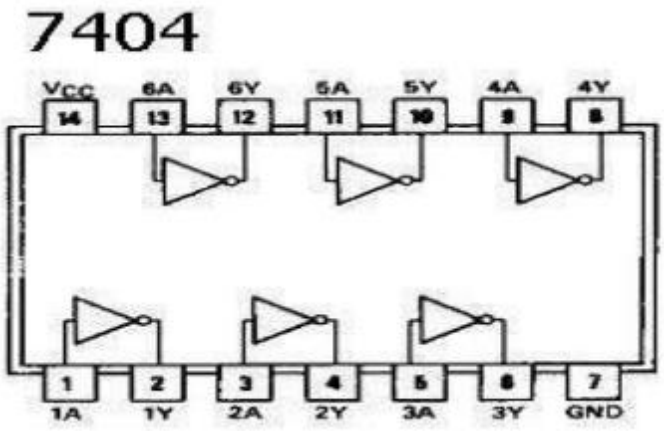


Figure 3

Fig: 1 .7408(quad 2 input AND gates) Fig: 3. 7432 (quad 2 input OR gates) Fig: 3. 7404(HEX inverter)

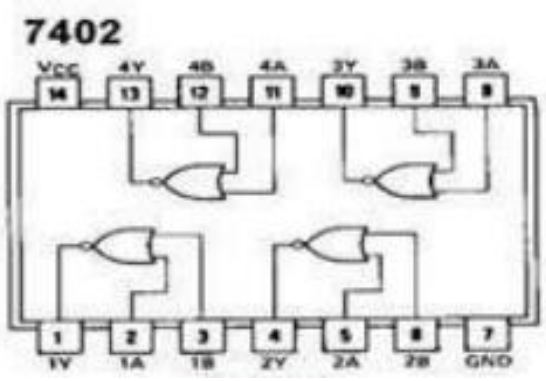


Figure 4

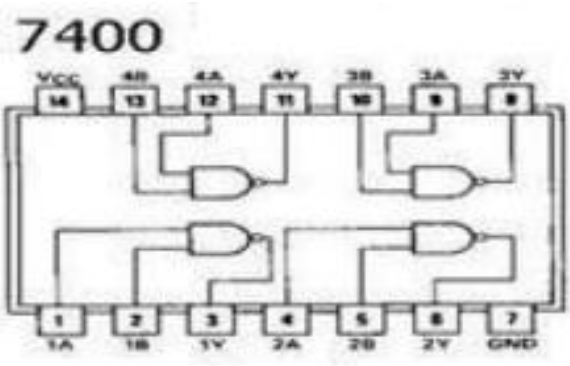


Figure 5

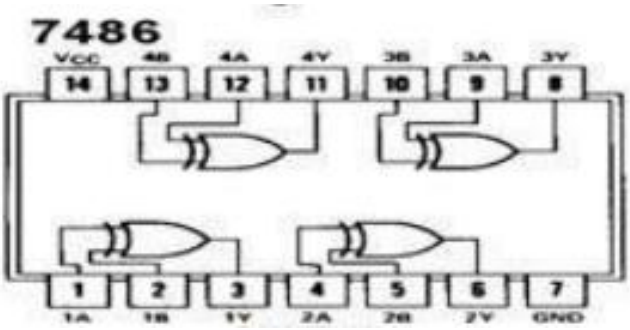
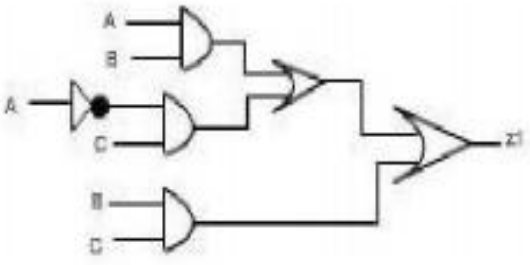


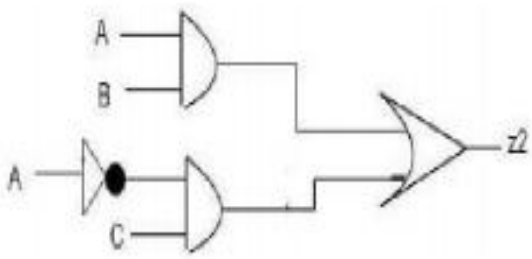
Figure 6

Fig: 4.7432(quad 2 input NOR gates) Fig: 5. 7400 (quad 2 input NAND gates) Fig: 6. 7486(quad 2 input XOR gates)

(a) AB+A'C+BC=AB+A'C

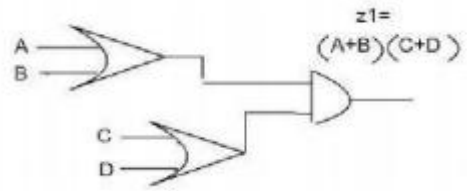
According to consensus theorem, the Boolean identity holds.

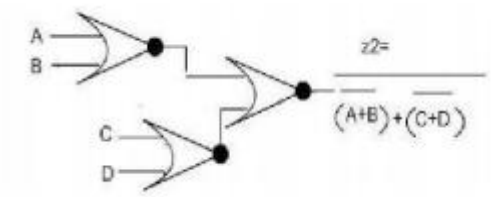




In the above picture both circuits are equivalent.

(b) Verify equivalence of OR-AND and NOR-NOR structure





In the above picture both circuits are equivalent. Student may be asked to wire up the network of gates shown in the above figures. They can next verify that the output of the two circuits, viz z1 and z2.

4. Procedure: Follow these steps to do the experiment.

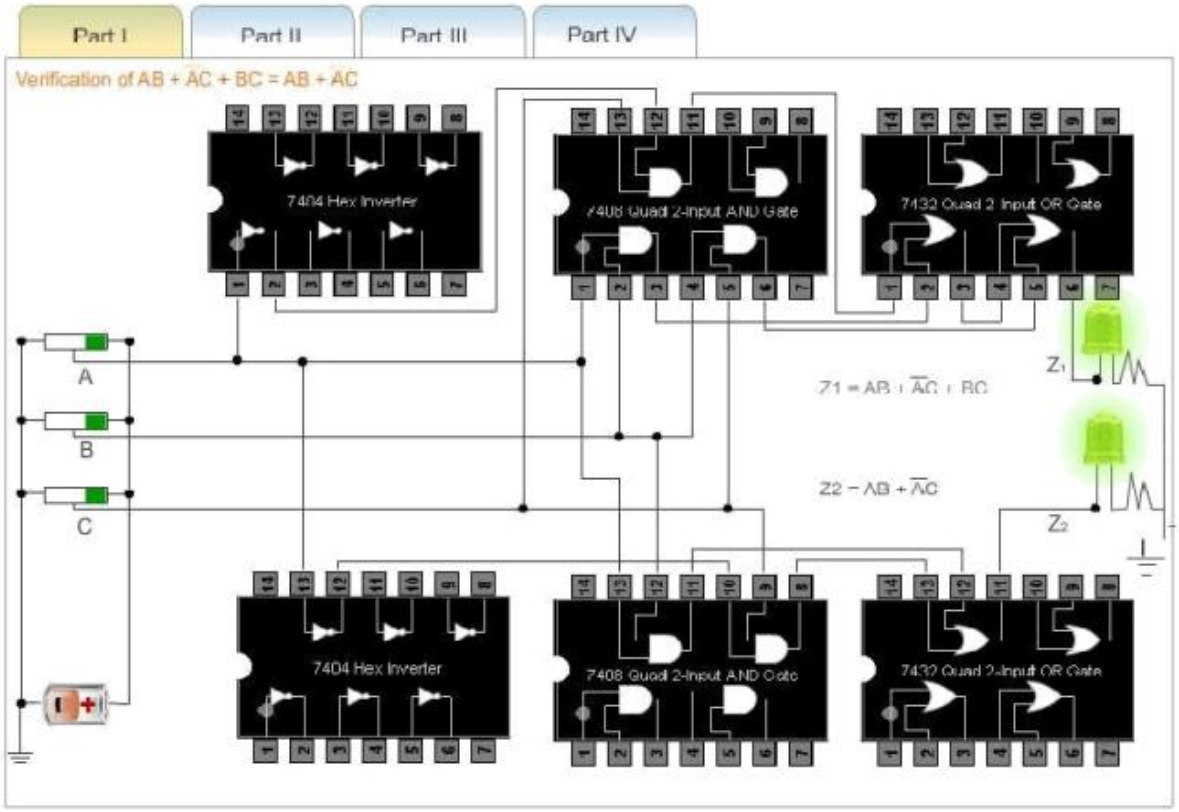
1. At first go through the structure of 7404 Hex inverter, 7408(quad 2-input AND gates), 7432(quad 2-input OR gates).

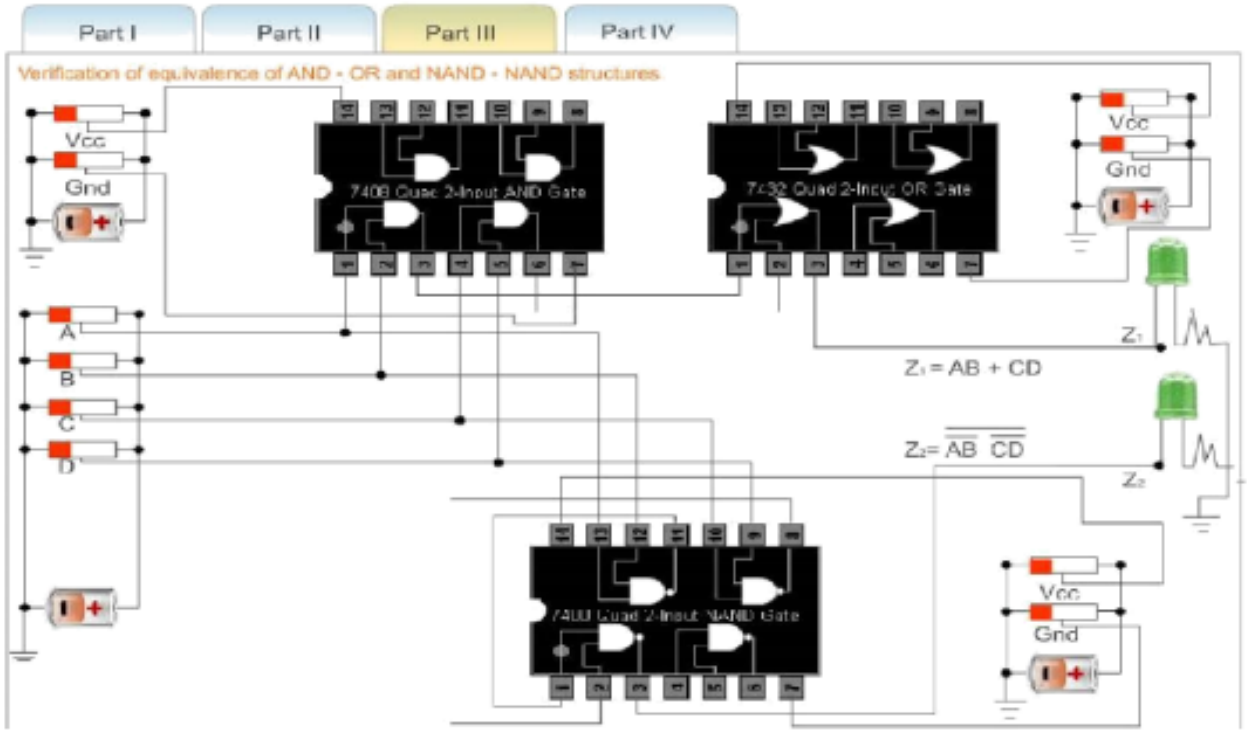
2. Next, apply a high level voltage to all the inputs A, B, C.

3. Next, check that both LEDs glow. This is because both the outputs z1 and z2 attain the same value.

4. Thus, AB+A'C+BC=AB+A'C holds for the condition A=B=C="1".

5. For all the combinations of the variables A, B, and C verify that both the LEDs are glowing or not glowing. If the LED glows, it indicates that the corresponding output has reached logic 1 level. Similarly, a dark LED indicates low level output voltage.





5. Required Results:

A	B	B	Z1	Z2
L	L	L	L	L
L	L	H	H	H
L	H	L	L	L
L	H	H	H	H
H	L	L	L	L
H	L	H	L	L
H	H	L	H	H
H	H	H	H	H

6. Precautions:

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit.
4. Avoid the heating of IC 7.

7. Learning Outcomes: Students will be able to understand the analysis and synthesis of Boolean expressions.

Date of Performance **Worksheet of the student** **Registration Number:**

Aim:

Observation Table: For solving the following expression

AB+A'C+BC=AB+A'C

S.No.	A	B	C	Z1	Z2

Learning Outcomes (what I have learnt):

To be filled in by Faculty

S.No.	Parameter	Marks obtained	Max. Marks
1	Understanding of the student about the procedure/apparatus.		20
2	Observations and analysis including learning Outcomes		20
3	Completion* of experiment, Discipline and Cleanliness		10
	Signature of Faculty	**Total marks obtained**	

Experiment 2

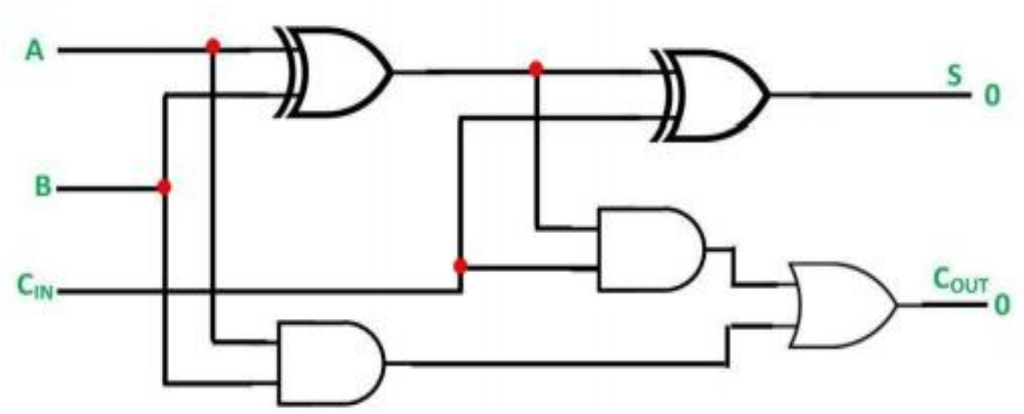
Aim: To design a circuit for Full adder and full subtractor using X-OR and basic gates

1. **Apparatus Required: -** IC 7486, IC 7432, IC 7408, IC 7400, IC 7404 etc.
2. **Learning objective**:
    a) How to realize the functionality full adder.
3**. Theory:**

1) Using X – OR and Basic Gates to implement full Adder:

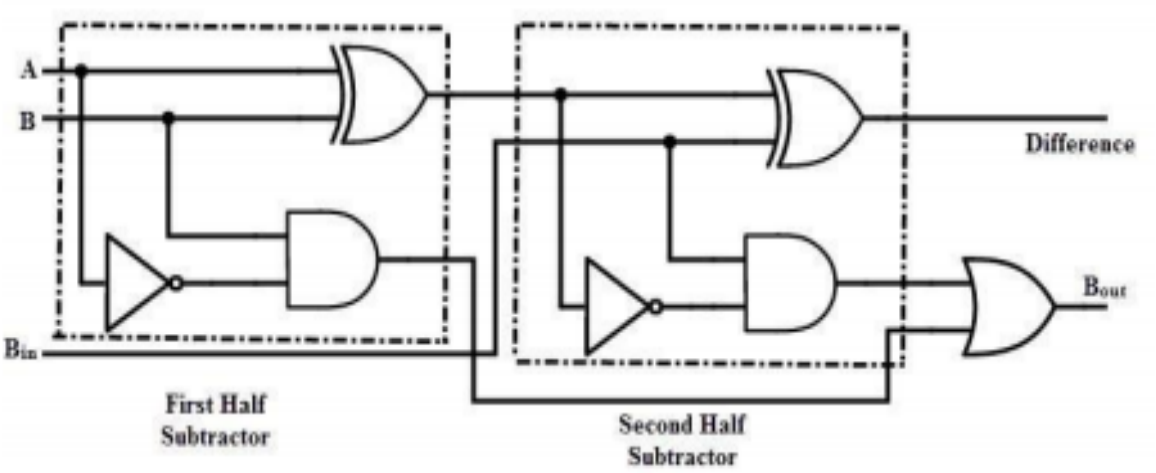
A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and Cin ; A and B are the operands, and Cin is a bit carried in from the next less significant stage. The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers. The circuit produces a two-bit output sum typically represented by the signals Count and S.
In this implementation, the final OR gate before the carry-out output may be replaced by an XOR gate without altering the resulting logic. Using only two types of gates is convenient if the circuit is being implemented using simple IC chips which contain only one gate type per chip. In this light, Cout can be implemented as. A full adder can be constructed from two half adders by connecting A and B to the input of one half adder, connecting the sum from that to an input to the second adder, connecting Ci to the other input and OR the two carry outputs. Equivalently, S could be made the three-bit XOR of A, B and Ci, and Cout could be made the three-bit majority function of A, B, and Ci.

Full Adder using half adders:



Using X – OR and Basic Gates to implement Full Subtractor:

As in the case of the addition using logic gates, a full subtractor is made by combining two half subtractors and an additional OR-gate. A full subtractor has the borrow in capability (denoted as B_{IN} in the diagram below) and so allows cascading which results in the possibility of multi-bit subtraction. The circuit diagram for a full subtractor is given below.



5. Procedure:

1. Verify the gates.
2. Make the connections as per the circuit diagram
3. Switch on VCC and apply various combinations of input according to the truth table.
4. Note down the output readings for half/full adder sum and the carry bit for different combinations of inputs.

6. Cautions:

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit.
4. Avoid the heating of IC.

7. Learning Outcomes: Students will be able to understand the implementation of adders with the help of logic gates.

Date of Performance **Worksheet of the student** Registration Number:

Aim:

Observation Table1: Truth table for Full adder

S.No.	A	B	Ci	Su m	C_{out}

Learning Outcomes (what I have learnt):

To be filled in by Faculty

S.No.	Parameter	Marks obtained	Max. Marks
1	Understanding of the student about the procedure/apparatus.		20
2	Observations and analysis including learning Outcomes		20
3	Completion* of experiment, Discipline and Cleanliness		10
	Signature of Faculty	**Total marks obtained**	

Experiment-3

1. Aim: To design a circuit to implement Boolean functions using Multiplexers.

Apparatus required: Multiplexer ICs (dual 4:1 mux 74153),7404, Chords.

2. Learning objectives:

a) How to realize functionality of Dual 4 Line to 1 Line Multiplexer using 74153 IC.

b) How Dual 4 Line to 1 Line Multiplexer select the particular input to be sent to the output.

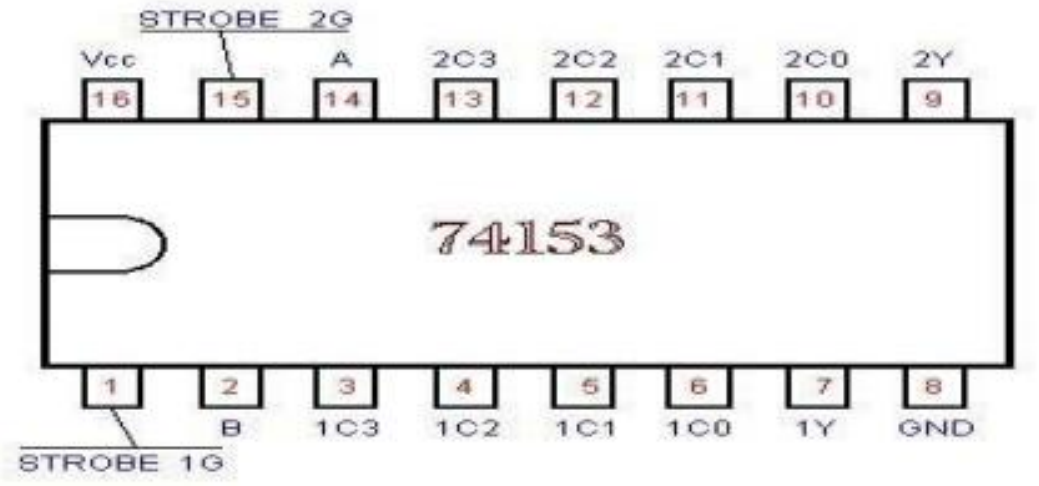
3. Theory:

It quite often happens, in the design of large-scale digital systems, that a single line is required to carry two or more different digital signals. Of course, only one signal at a time can be placed on the one line. What is required is a device that will allow us to select, at different instants, the signal we wish to place on this common line. Such a circuit is referred to as a Multiplexer.

A multiplexer performs the function of selecting the input on any one of 'n' input lines and feeding this input to one output line.

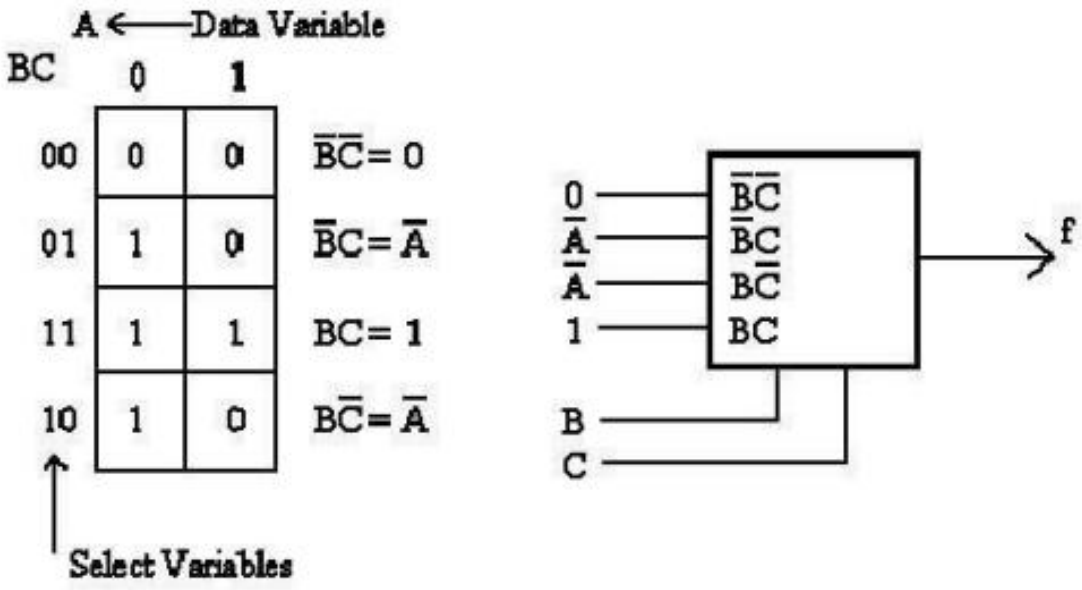
Multiplexers are used as one method of reducing the number of integrated circuit packages required by a particular circuit design. This in turn reduces the cost of the system.

Assume that we have four lines, C0, C1, C2 and C3, which are to be multiplexed on a single line, Output (Y). The four input lines are also known as the Data Inputs. Since there are four inputs, we will need two additional inputs to the multiplexer, known as the Select Inputs, to select which of the C inputs is to appear at the output. Call these select lines A and B. The gate implementation of a 4-line to 1-line multiplexer is shown below:



Implementation of a Boolean function using 4:1 mux:

Consider the function: In this example we could have picked any variable to be the data variable and the other two as select variables. Suppose one were to take A as the data variable. The corresponding Karnaugh map is then:

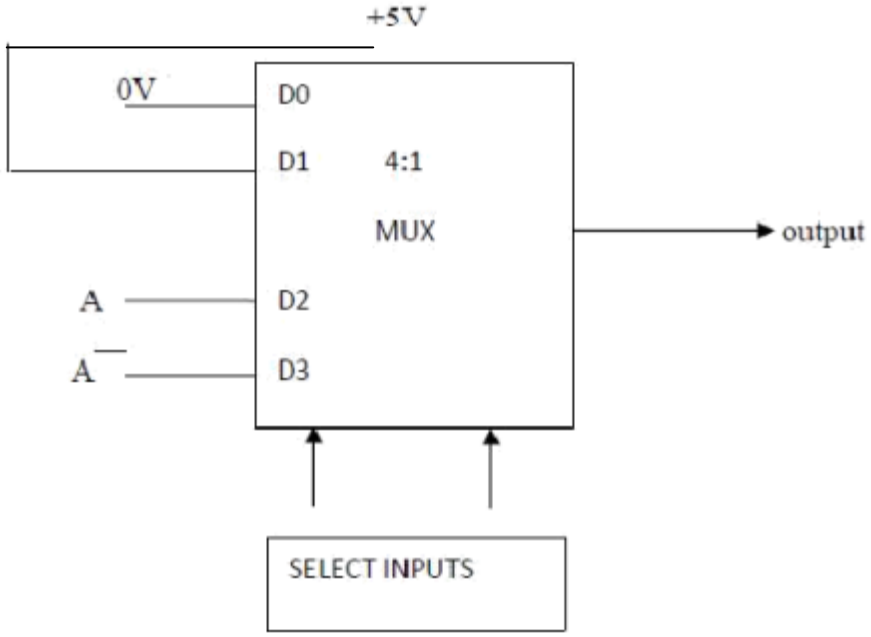


Alternate method:

Implementation of a following function using 4:1 mux: F(A,B,C)= Σ(1,3,5,6)

The given function has three variables. Hence, it can be implemented using a multiplexer with two select inputs and four data inputs. The implementation table of the given function as shown in table below:

	D_0	D_1	D_2	D_3
$\bar{A}$	0	(1)	2	(3)
A	4	(5)	(6)	7
	0	1	$\bar{A}$	$\bar{A}$



4. Procedure

a) At first go through the structure of 74153.Then apply high level voltage to Vcc and low level voltage to GND. If Vcc and ground are not connected properly then error message will be shown and no output will be generated.
b) Next, apply high level voltage to Strobe1G or strobe 2G. If STROBE 1G is low, 1st Multiplexer is activated. If STROBE 2G is low, then 2nd Multiplexer is activated.
c) Next, apply low level voltage to the select inputs A and B (A Most Significant Bit, B Less significant bit). Then apply a high level voltage to 2C0. Now check that how Dual 4 Line to 1 Line Multiplexer select the particular input to be multiplexed and to be applied to the output IY {1 = 1, 2}.
d) For all the combinations of the select inputs A, B verify that both the LEDs are glowing or not glowing. If the LED glows, it indicates that the corresponding output has reached logic 1 level. Similarly, a dark LED indicates low level output voltage.
e) If both the Strobe inputs are low then both Multiplexers are activated.

5. Cautions:

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit.
4. Avoid the heating of IC.

Date of Performance **Worksheet of the student** Registration Number:

Aim:

Observation Table: Truth Table for 4:1 Mux

S.No.	D0	D1	D2	D3	X	Y	Output

Learning Outcomes (what I have learnt):

To be filled in by Faculty

S.No.	Parameter	Marks obtained	Max. Marks
1	Understanding of the student about the procedure/apparatus.		20
2	Observations and analysis including learning Outcomes		20
3	Completion* of experiment, Discipline and Cleanliness		10
	Signature of Faculty	**Total marks obtained**	

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Experiment 4

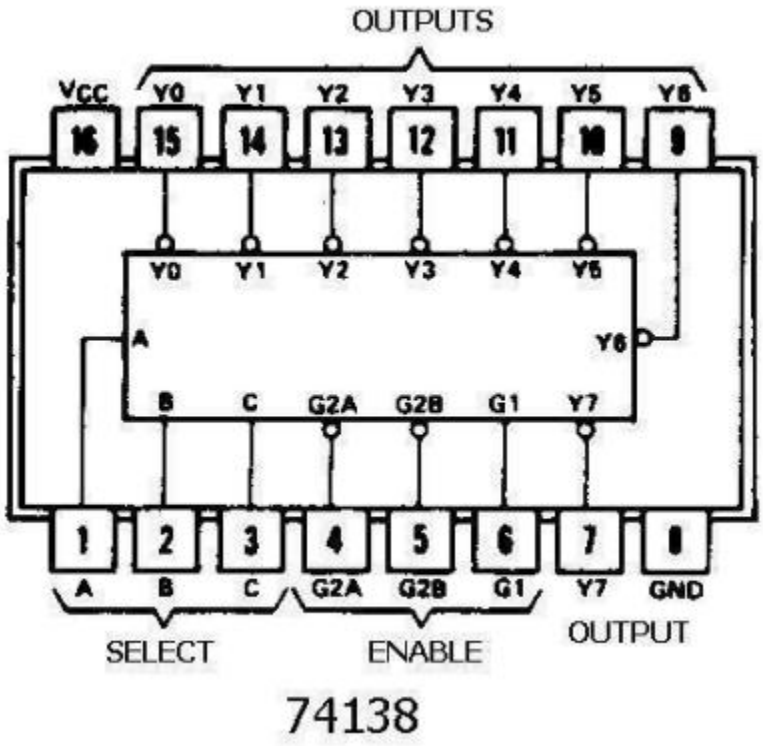
1. Aim: To design a circuit to implement Boolean functions using Decoders.

Apparatus required: IC 74138, 7404, 7432,7400,7408,7410 and LEDs.

2. Learning Objectives: This experiment enables a student to learn:

How to realize functionality of a 3-to-8-line active low Decoder viz. 74138 IC. That is on setting the two-active low and one active high enable inputs to proper level, one can verify that one and only one of the eight active low outputs is asserted based on the values assigned to three select input.

3. Theory: IC 74138 works as a 3-to-8 active low decoder, based on the values assigned to three select inputs of the three enable inputs, G1 must be made high value while G2A and G2B must be low. The eight active low inputs (Y0 to Y7) correspond to eight max terms (M0 to M7) or in other words, component of the corresponding min terms m0-m7. For example, Y0 = component of C B A = C+B+A.



G2A	G2B	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	L	H	0	0	0	0	1	1	1	1	1	1	1
L	L	H	0	0	1	1	0	1	1	1	1	1	1
L	L	H	0	1	0	1	1	0	1	1	1	1	1
L	L	H	0	1	1	1	1	1	0	1	1	1	1
L	L	H	1	0	0	1	1	1	1	0	1	1	1
L	L	H	1	0	1	1	1	1	1	1	0	1	1
L	L	H	1	1	0	1	1	1	1	1	1	0	1
L	L	H	1	1	1	1	1	1	1	1	1	1	0

4. Procedure

1. At first go through the structure of 74138. Then apply high level voltage to VCC and apply low level voltage to GND and also apply high level voltage to G1.
2. Next, apply low level voltage to all the three select inputs (C B A). Now check that Y0 is at low state. Other outputs are at high state.
3. Apply low level voltage to C and B and apply high level voltage to A. Now check that Y1 is at low state. Other outputs are at high state.
4. Apply low level voltage to C and A and apply high level voltage to B. Now check that Y2 is at low state. Other outputs are at high state.
5. Apply low level voltage to C and apply high level voltage to B and A. Now check that Y3 is at low state. Other outputs are at high state.
6. Next, apply high level voltage to C and apply low level voltage to B and A. Now check that Y4 is at low state. Other outputs are at high state.
7. Apply high level voltage to C and A and apply low level voltage to B. Now check that Y5 is at low state. Other outputs are at high state.
8. Next, apply high level voltage to C and B high and apply low level voltage to A. Now check that Y6 is at low state. Other outputs are at high state.
9. Next, apply high level voltage to all the select inputs (C,B,A). Now check that Y7 is at low state. Other outputs are at high state.

5. Cautions

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit.
4. Avoid the heating of IC.

6. Learning Outcomes: Students will be able to understand the analysis and synthesis of logic functions with the help of decoders.

Date of Performance **Worksheet of the student** **Registration Number:**

Aim:

Observation Table: Truth Table for 3:8 decoder

G2A	G2B	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7

Learning Outcomes (what I have learnt):

To be filled in by Faculty

S.No.	Parameter	Marks obtained	Max. Marks
1	Understanding of the student about the procedure/apparatus.		20
2	Observations and analysis including learning Outcomes		20
3	Completion* of experiment, Discipline and Cleanliness		10
	Signature of Faculty	Total marks obtained	

Experiment 5

1. Aim: To implement and simulate the combinational and sequential circuits using Software (DSCH/Proteus).

Equipments Required: Laptop with DSCH/Proteus installed.

2. Learning Objectives: This experiment enables a student to learn

- How to implement the combinational and sequential circuit on virtual platform.
- Student will learn the simulation of the digital circuits.
- Students will learn the software usage in circuit implementation and the benefits of that.

3. Outline of the procedure:

1. Open the DSCH software on your laptop
2. Pick the desired components from the library.

Fig 1. Symbol Library

3. Drag and Drop the component on the Virtual work place.

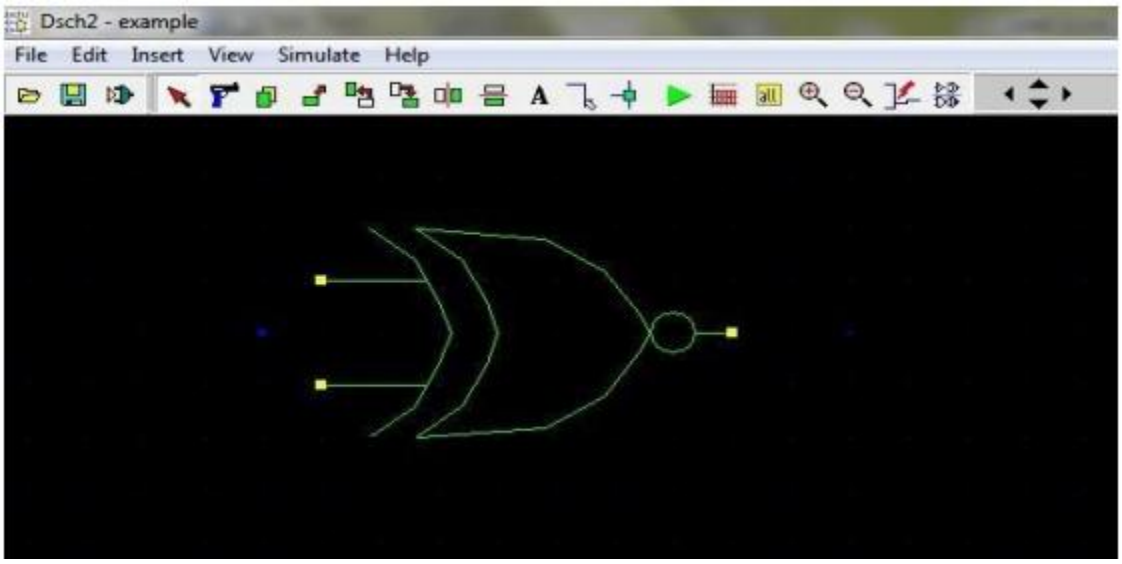


Fig 2. Component placed on virtual workplace

4. Similarly place all the components as per the design.
5. Connect them through the wire tool.

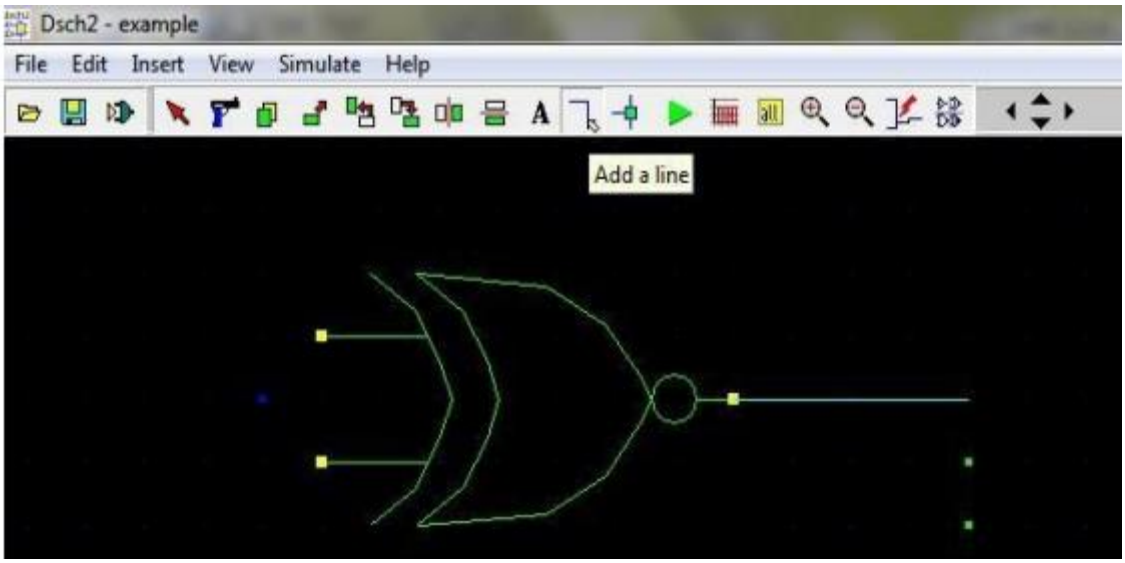


Fig 3. Click on symbol to add the wires between components.

6. Connect the input switches and output devices.
7. Click on run simulation.

Fig 4. To run the simulation of designed circuit.

8. Finally you can check the change in output with respect to input signal variation.

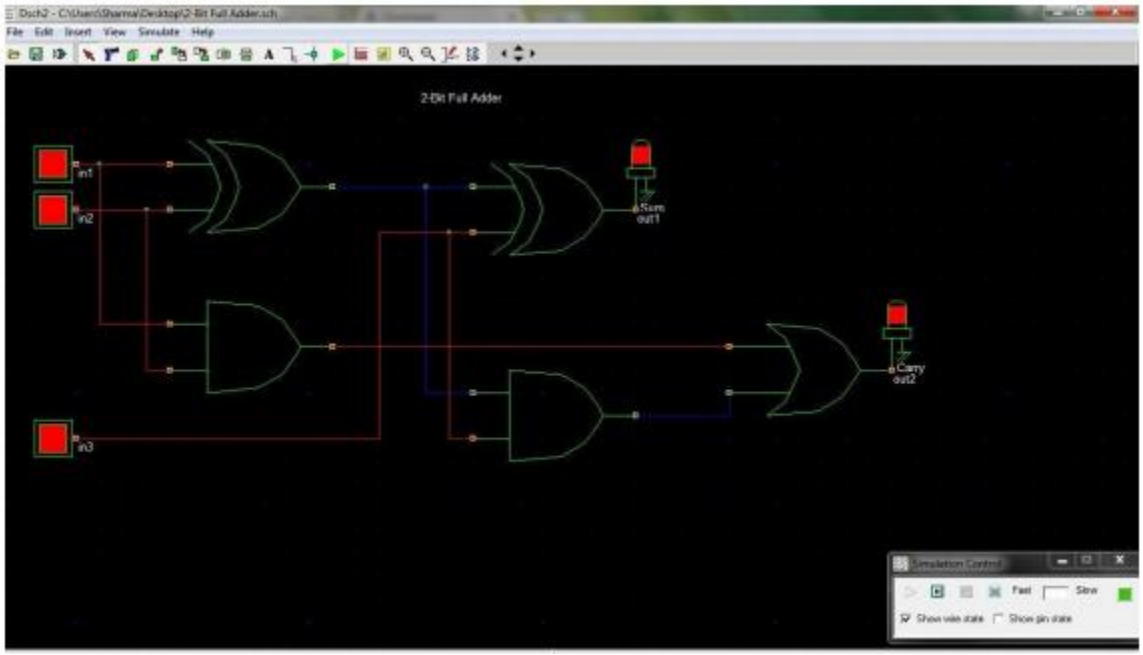


Fig 5. Circuit implemented using basic logic gates.

5. Cautions

1. Choose the component properly by checking symbols.
2. Check the connections before simulation.
3. There should not any short circuit in the circuit.

Date of Performance **Worksheet of the student** Registration Number:

Aim:

Observation: (Show & paste the result using DSCH)

Learning Outcomes:

To be filled in by Faculty

S.No.	Parameter	Marks obtained	Max. Marks
1	Understanding of the student about the procedure/apparatus.		20
2	Observations and analysis including learning Outcomes		20
3	Completion of experiment, Discipline and Cleanliness		10
	Signature of Faculty	**Total marks obtained**	

Experiment 6

1. AIM: The Aim of the experiment is to fully understand the functionality of J-K Flip-Flop.

Apparatus required: IC 7400, IC 7410, Power supply and LEDs.

2. Learning Objectives: How to realize the functionality of sequential circuits using basic flip-flops

3. Theory The logic circuits whose outputs at any instant of time depend not only on the present input but also on the past outputs are called sequential circuits.
The simplest kind of sequential circuit which is capable of storing one bit of information is called latch. The operation of basic latch can be modified, by providing an additional control input that determines, when the state of the circuit is to be changed. The latch with additional control input is called the Flip-Flop. The additional control input is either the clock or enable input.

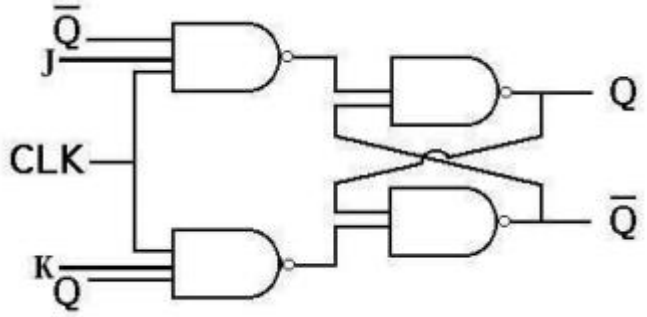
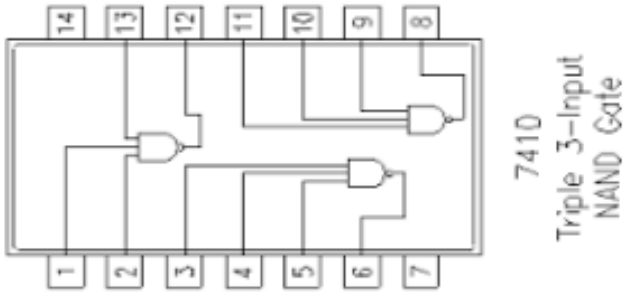


Fig 1: J-K Flip flop using NAND gate



J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\bar{Q}$ (t)

Fig 2: Truth Table of J-K Flip Flop and Pin configuration of 7410

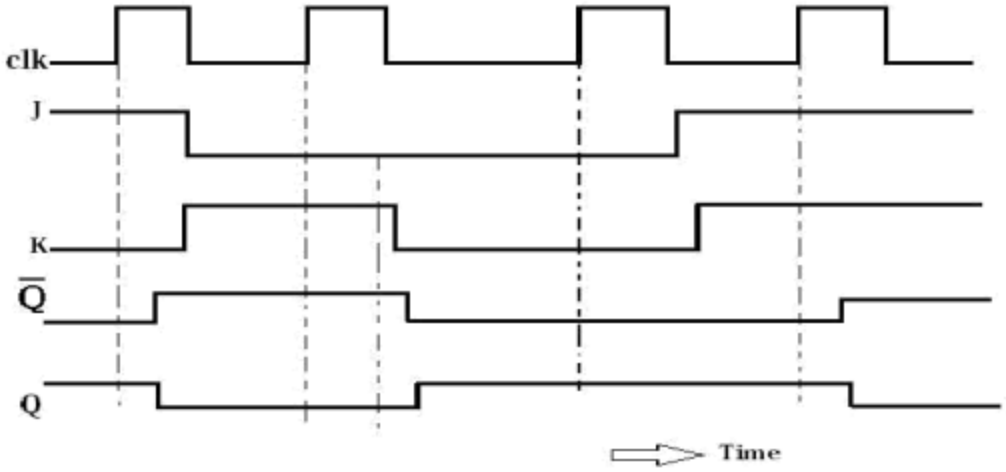


Figure 3: Typical wave-form in J-K FlipFlop

4. Procedure

1. At first apply high voltage to Vcc1 & Vcc2.So that the "Clock Start" button will be enabled.
2. Next, start the clock pulse by clicking on the "Clock Start" button and after generation of some clock pulses stop the clock pulse by clicking on the"clock Stop" button.
3. Now apply high voltage to D input and set "No of clock pulses" to 1.See the changes at output (Q and Q) at positive clock edge. 4. Now apply low voltage to D input and start the clock pulse. See the changes at output (Q and Q) at positive clock edge.

5. Cautions:

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit.
4. Avoid the heating of IC.
5. Provide proper clock pulse.

6. Learning Outcomes: Student will be able to learn working of flip flop

Date of Performance **Worksheet of the student** **Registration Number**

Aim:

Observation Table for J-K Flip Flop

J	K	Q(t)	Q(t+1)

Learning Outcomes (what I have learnt):

To be filled in by Faculty

S.No.	Parameter	Marks obtained	Max. Marks
1	Understanding of the student about the procedure/apparatus.		20
2	Observations and analysis including learning Outcomes		20
3	Completion of experiment, Discipline and Cleanliness		10
	Signature of Faculty	**Total marks obtained**	

Experiment 7

1. Aim: To design a 3 bit binary up/down counter using flip flop.

Apparatus required: IC 74LS76, Power supply, LEDs and Function generator.

2. Learning Objectives: To learn to realize the functionality of sequential circuits using basic flipflops.

3. Theory: A sequential circuit that goes through a prescribed sequence of states upon the application of input pulses is called a counter. The input pulses, called count pulses, may be clock pulses. In a counter, the sequence of states may follow a binary count or any other sequence of states. Counters are found in almost all the equipment containing digital logic. They are used for counting the number of occurrences of an event and are useful for generating timing sequences to control operations in a digital system.

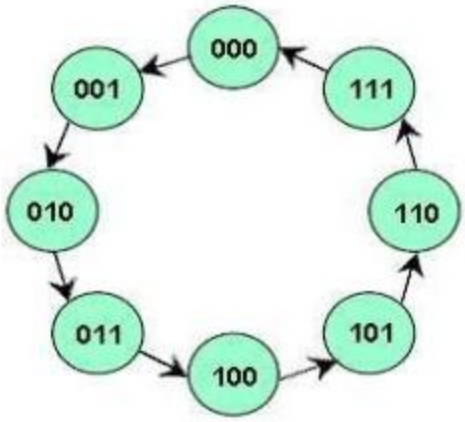


Fig: State diagram of 3-bit binary up counter

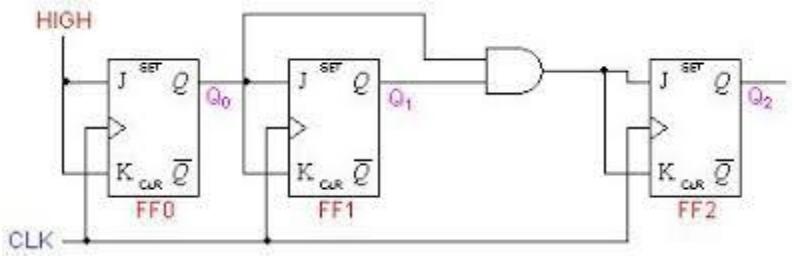
Present State			Next State		
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Fig: Truth Table of 3-bit binary up counter

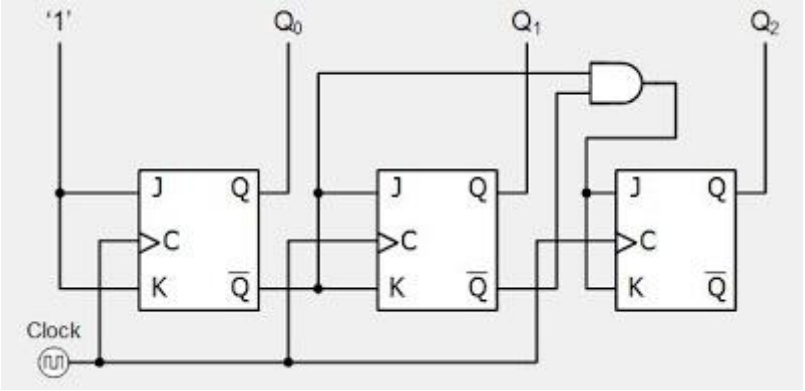
4. Procedure:

1. Design the circuit as given below.

Circuit diagram of 3 bit up counter



Circuit diagram of 3 bit down counter

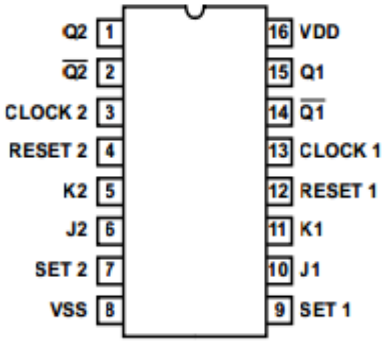


2. Apply clock pulse of 1 Hz frequency and check the output on Q0, Q1 and Q2.

5. Cautions:

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit.
4. Avoid the heating of IC.
5. Provide proper clock pulse.

Pin configuration of IC 7476



Pin configuration of IC 4027

6. Learning Outcomes: Student will be able to design counter using flip flop.

Date of Performance **Worksheet of the student** **Registration Number**

Aim:

Observation Table for J-K Flip Flop

J	K	Q(t)	Q(t+1)

Learning Outcomes (what I have learnt):

To be filled in by Faculty

S.No.	Parameter	Marks obtained	Max. Marks
1	Understanding of the student about the procedure/apparatus.		20
2	Observations and analysis including learning Outcomes		20
3	Completion of experiment, Discipline and Cleanliness		10
	Signature of Faculty	**Total marks obtained**	

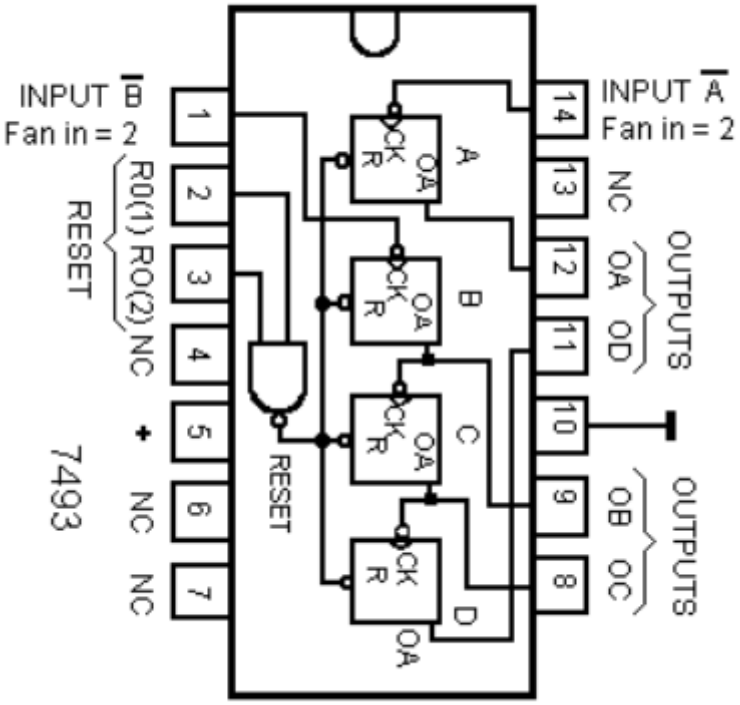
Experiment 8

1. Aim: To visualize the output of decade counter on seven segment display.

Apparatus required: IC 74LS93, IC 7447 Decoder Power supply, Seven Segment display and Function generator.

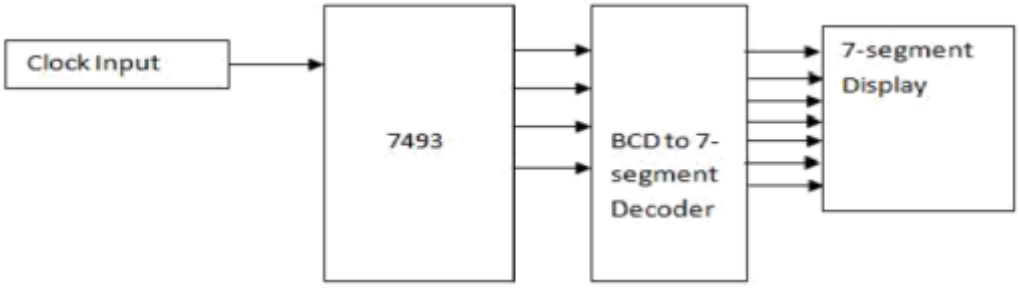
2. Learning Objectives: To design decade counter using binary counter and display it on seven segment.

3. Theory: A decade counter requires resetting to zero when the output count reaches the decimal value of 10, i.e. when 1010 and to do this we need to feed this condition back to the reset input. A counter with a count sequence from binary 0000 through to 1001 is generally referred to as a BCD binary code decimal counter because its ten state sequences is that of BCD code.



4. Procedure:

1. Connect the circuit as given below.



2. Apply clock pulse of Frequency 1 Hz
3. Check the output on seven segment display for every clock pulse.

5. Cautions: Connect all wire connection properly and provide proper input sequence.

6. Learning Outcomes: Student will be able to learn use of decoder and seven segment display.

Date of Performance **Worksheet of the student** **Registration Number**

Aim:

Observation Table for J-K Flip Flop

J	K	Q(t)	Q(t+1)

Learning Outcomes (what I have learnt):

To be filled in by Faculty

S.No.	Parameter	Marks obtained	Max. Marks
1	Understanding of the student about the procedure/apparatus.		20
2	Observations and analysis including learning Outcomes		20
3	Completion of experiment, Discipline and Cleanliness		10
	Signature of Faculty	**Total marks obtained**	

Experiment 9

Aim: Design and Implementation of application based projects-1

Title:

a. To design a line following robot using basic gates.
b. To design 4 bit digital calculator which can perform addition and multiplication and display using 7 segment.
c. To design a circuit this can generate random number and display using 7 segment.
d. To design a circuit for humidity and temperature monitoring.
e. To design a circuit for secure locking mechanism.

Implement anyone from listed above

Date of Performance **Worksheet of the student** **Registration Number**

Aim:

Learning Outcomes:

To be filled in by Faculty

S.No.	Parameter	Marks obtained	Max. Marks
1	Understanding of the student about the procedure/apparatus.		20
2	Observations and analysis including learning Outcomes		20
3	Completion of experiment, Discipline and Cleanliness		10
	Signature of Faculty	**Total marks obtained**	

Experiment 10

Aim: Design and Implementation of application based projects-2

Title:

a. To design a system for solar tracking.
b. To design a up and down fading lights (different colored LEDs) with specified delays using flip-flops /counters
c. Design a universal counter which can perform different shift operations using multiplexer.
d. Design a digital calculator which can implement subtraction and division functions, and display output in 7-segment display unit

Implement anyone from listed above

Date of Performance **Worksheet of the student** **Registration Number**

Aim:

Learning Outcomes:

To be filled in by Faculty

S.No.	Parameter	Marks obtained	Max. Marks
1	Understanding of the student about the procedure/apparatus.		20
2	Observations and analysis including learning Outcomes		20
3	Completion of experiment, Discipline and Cleanliness		10
	Signature of Faculty	**Total marks obtained**	