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100-ft Ring Road, Bengaluru – 560 085, Karnataka, India

Project report on

'Implementation of Inductorless DC-DC Buck Convertor'

Submitted by

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Aug 2020 – May 2021

under the guidance of

Internal guide

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FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PROGRAM B. TECH

CERTIFICATE

This is to certify that the report entitled

Implementation of Inductorless DC -DC Buck Convertor

is a bonafide work carried out by

Dhanush Abhinand R B (PES1201700977)

Likhith Kumar Shetty (PES1201701337)

In partial fulfillment for the completion of 8th-semester course work in the Program of Study B.Tech in Electronics and Communication Engineering, under rules and regulations of PES University, Bengaluru during the period Aug 2020-May 2021.It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report. The dissertation has been approved as it satisfies the 8th-semester academic requirements in respect of project work.

M. S. Sunita 20/5/2021

Signature with date & Seal
Prof. M.S.Sunita
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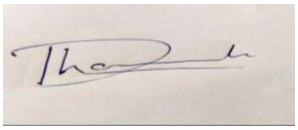
Declaration

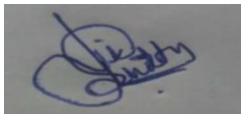
We, **Dhanush Abhinand R B , Likhith Kumar Shetty** ,hereby declare that the report entitled, ***Implementation of Inductorless DC-DC buck convertor,*** is an original work done by us under the guidance of **Prof. M S Sunita**, *Associate Professor*, ECE Department and is being submitted in partial fulfillment of the requirements for completion of 8th Semester course work in the Program of Study, B.Tech in Electronics and Communication Engineering.

PLACE: Bengaluru, Karnataka, India

DATE: 25/05/2021

NAME AND SIGNATURE OF THE CANDIDATES

1. **Dhanush Abhinand R B** 

2. **Likhith Kumar Shetty** 

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ABSTRACT

In Analog circuits there is a requirement for a DC-DC converter to supply to various parts of the circuit either to perform Buck operation or Boost operation. Conventional Linear DC Convertor There are disadvantages in the Size and output ripple ,power loss in the circuit .In our project we have implemented the Inductorless DC -DC converter with the switched capacitor technique along with single boundary hysteretic control method. The objective is to build a power efficient circuit and to get output voltage with minimum ripple. Simulations are carried out in cadence virtuoso software. Here the energy storing element is the capacitor and it is responsible to transfer the Voltage to the output load capacitance through charge sharing. Also we can build the circuit in a small integrated circuit chip.

ACKNOWLEDGEMENT

We would like to express our gratitude and thank all those who made this project possible. We sincerely thank our internal guide Prof.M.S.Sunita , Professor of the Department of Electronics and Communication Engineering for providing us the opportunity to take up this project and providing us with support, guidance and motivation which helped us to complete our project.We would also like to sincerely thank Prof. Anuradha.M, Head of the Department of Electronics and Communication Engineering for her encouragement and support. During the course of this project we have learnt a lot from various sources and are indebted to all.

We would also like to express our gratitude to Dr. M.R Doreswamy,Chancellor,PES University, Prof. Jawahar Doreswamy, Pro-Chancellor, PES University ,Dr Suryaprasad J, Vice Chancellor, PES University for the support and encouragement.

Chapter 1. INTRODUCTION

Due to the rapid development in Semiconductor industry ,It lead to the development and demand for Small scale Integrated chips ,Sensors. These integrated circuits have developed a rapid advancement in size over the years and power management as these will consume very low power and size efficient ,and to provide portability, reliability , to extend battery operation ,to import hardware debugging technology. Our main focus will be on cost,area,power and performance.

These Integrated circuit chips can also be mounted into the printed circuit boards. So from the conventional linear DC-DC convertor Inductor is responsible to store as energy storing element in basic Buck and boost convertor .But in these type of converters Inductor will consume large power dissipation also in resistors and large size which will also develops large output ripple during discontinuous mode of operation.

1.1 Motivation

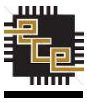
The DC-DC converter will shift the voltage level from one level to the other level either it will perform step up operation or step down operation. Because of the disadvantage of the conventional linear regulator circuit we have motivation to develop an Inductorless circuit where we replace the Inductor with the main energy storing element and transferring element with the capacitor using Switched capacitor technique

1.2)Problem Statement

To implement a DC-DC step down voltage Convertor using the switched capacitor circuit for power regulation and supply for small scale electronic components or circuits.

Target objective

- To build a power efficient circuit.
- Obtain stable output voltage with minimum ripple.
- Size efficient circuit, incorporable on an IC.
- Fast transient response and high efficiency over a wide load current change.
- To show optimal output voltage ripple by matching the sampling clock with the convertor switching frequency.
- To implement Single boundary hysteretic control method along with the modified circuit.



1.3)LITERATURE SURVEY

1)Z. Xiao, A. K. Bui and L. Siek, "A Hysteretic Switched-Capacitor DC–DC Converter With Optimal Output Ripple and Fast Transient Response," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 11, pp. 2995-3005, Nov. 2017, doi: 10.1109/TVLSI.2017.2728606.

The above paper is the base paper which we have used in the project ,In this paper we have obtained the detailed explanation for the single boundary hysteretic control method With feedback and without feedback and the modified hysteretic control method with the updated hysteretic control loop method which controls the switching frequency of the clock signal which is required for the sampling of output signal according to the amount of output ripple which is generated.

2)H. Le, S. R. Sanders and E. Alon, "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," in IEEE Journal of Solid-State Circuits, vol. 46, no. 9, pp. 2120-2131, Sept. 2011, doi: 10.1109/JSSC.2011.2159054.

The switched capacitor technique we will use control both the charging phases and discharging but turning ON and OFF both PMOS and NMOS .The gate voltage to these devices are provided by the implementation of Startup circuit , Gate driver circuit , Dead time generator circuit ,Level shifter .The above paper explains the implementation of these circuit. Level Shifter is used to drive the voltage level from one DC level to the other DC voltage level .Dead time generator induces a small amount of deadtime that is both phased (non overlapping) signals should turn OFF for a small duration of time .

3)T. M. Van Breussegem and M. S. J. Steyaert, "Monolithic Capacitive DC-DC Converter With Single Boundary–Multiphase Control and Voltage Domain Stacking in 90 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 46, no. 7, pp. 1715-1727, July 2011, doi: 10.1109/JSSC.2011.2144350.

The above paper explains the single boundary hysteretic control method with the implementation of power efficient circuit and power analysis .Here they have explained the different configuration of DC-DC convertor switched capacitor circuit where they have have implemented the stepup and stepdown operation which will provide a gain of 1:3 , 1:2, 2:1, 3:1 and the explanation of modified hysteretic control method which is the extension of single boundary hysteretic control method

4)B. Kinger, S. Suman, K. G. Sharma and P. K. Ghosh, "Design of Improved Performance Voltage Controlled Ring Oscillator," 2015 Fifth International Conference on Advanced Computing & Communication Technologies, 2015, pp. 441-445, doi: 10.1109/ACCT.2015.127.

Voltage control oscillator is a device where the output voltage periodic signal which is generated is controlled by the input signals DC voltage .Hence we will get voltage variation that is converted into the frequency variation. Eg ;- For certain input voltage V1 it will generate a periodic signal of frequency f1 and for V2 we get f2. In this paper we have obtained the transistor level design of VCO using 180nm technology .The VCO is responsible to generate clock signal which is fed as an input to the dynamic comparator circuit and sample the output signal

5)X. Fu, K. El-Sankary and Y. Yadong, "A Pulse injection background calibration technique for charge pump PLLs," 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 98-101, doi: 10.1109/NEWCAS49341.2020.9159782.

Charge pump integrator is the part of PLL (Phase locked loop) .In our design we have obtained the charge pump integrator and VCO combination where charge pump integrator drive output node voltage .These output will be a very small variation as from the output of the comparator is given to the VCO the Increment and decrement signal will be passed to the input of charge pump circuit.,when the increment signal raises the output node voltage as the capacitor will start charging and output node voltage increases by a small amount and similarly during the decrement cycle the output voltage will decrease.

Chapter : 2 Voltage regulators

There are different types of voltage regulators Linear regulators use passive power consuming components to distribute power among loads, a simple example is the resistor based voltage regulator circuit Then there are Inductor and capacitor based converters that use their property of energy storage and transfer to regulation voltage by switching methods

2.1)Basic Inductor based Buck converter

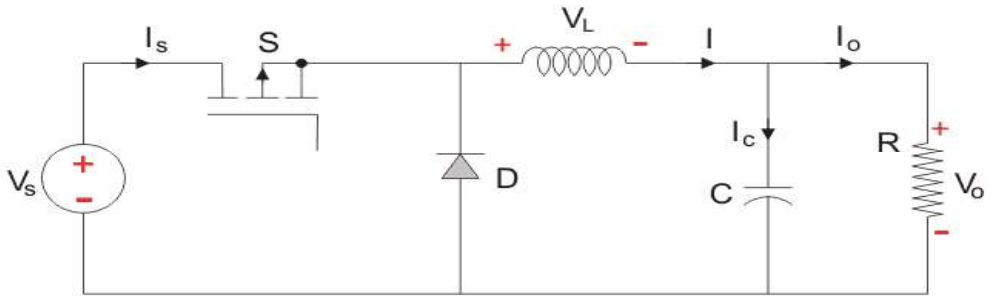


Fig 1.1 Buck converter circuit with NMOS acting as switch and diode,capacitor,Resistor

The Basic Buck Converter is a DC-DC converter where we perform a step down operation. The amplitude of the output voltage is less than the input voltage .Eg:- 1:2 represents the gain of the circuit where Vout is half of the input voltage. It's a low cost circuit .

There are 2 working states: Switch ON -State1 and Switch OFF -State 2 .

- During Switch ON states we give the periodic Rectangular pulse to the switch ,where here is the N-mosfet .The positive cycle will turn On the Mosfet it enters into a linear region and acts like a short circuit.

- During Switch Off state The Negative half cycle of periodic pulse will drive the mosfet to the cutoff region.

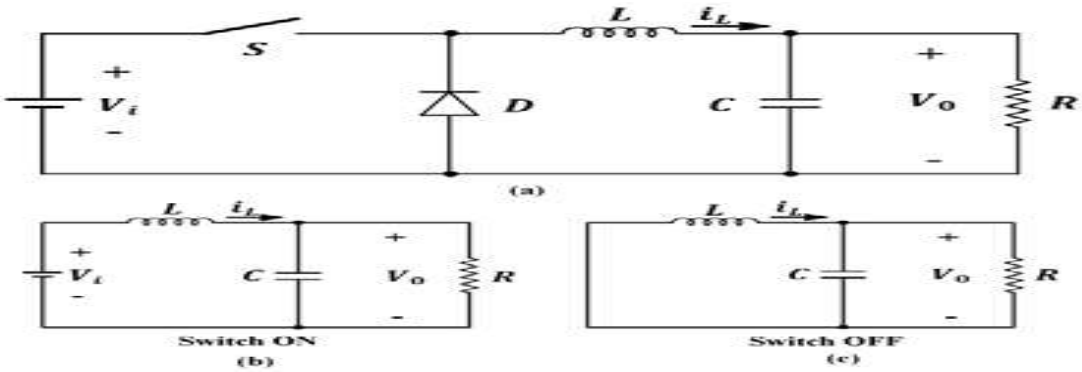


Fig 1.2 Shows the two working condition Switch ON and Switch off phase

- During State 1 Nmos is turned ON and the Diode will be reverse biased(open circuit) and The inductor ,Capacitor will start charging as current flows in the circuit and increases.
- Inductor will undergo sudden change in current ,also the inductor starts charging and it will store the energy in the form of a magnetic field.
- In the waveform we can observe Inductor current raising,till the end of state 1.
- During State 2 Nmos is off and Diode will be forward biased (Short circuit) the supply voltage is not attached as the Inductor has completely charged to 100% it will act like a current source.
- At this stage the inductor will start discharging , the voltage across the inductor decreases, the rate of change of current decreases and hence the voltage across the resistor ,which is load, will start increasing.
- The output voltage developed in this case is less than the input voltage hence it performs step down operation

- The same process continues after State 2,State 1 begins where inductor will start charging again .There are two modes here continuous and discontinuous mode .

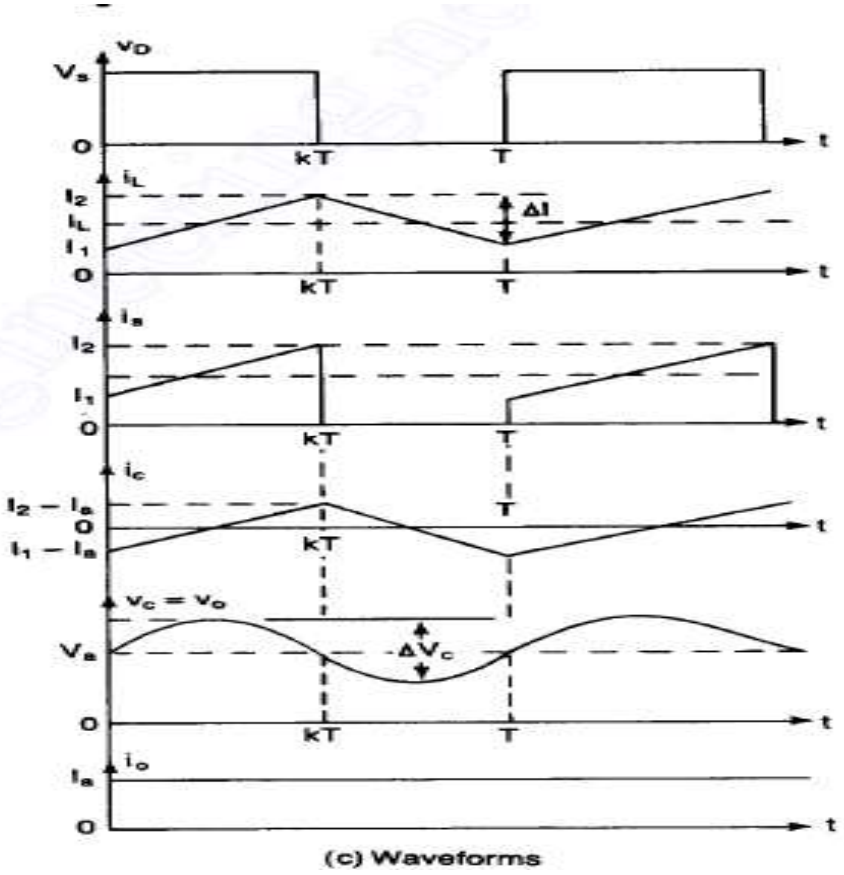


Fig 1.3 represents the voltage source Vs ,Current across the Inductor ,Source,Capacitor and voltage across capacitor

2.2)Preference of Switched capacitor dc-dc converter over an inductor based converter

Though the inductor based converters are robust and efficient and are widely used for higher scale power regulation, but when it comes to designing a small scale converter that can be incorporated on an IC the inductor based converter poses a lot of difficulties.The inductor being a bulky magnetic component causes cannot be shrunk in size effectively it produces magnetic lines that can cause flux interference with neighbouring components in the small scale. Therefore a capacitor based switching converter can be used to overcome these disadvantages where small sized MIM capacitors can be fabricated on CMOS technology. The switched capacitor converter generally requires more switching making is slightly inefficient, there other methods such as converters with of off-chip inductors being used as well

2.3)Basic Switched capacitor dc-dc converter working theory

Switched capacitor converters work on the principle of energy storage and transfer.

The energy storage elements are capacitors, they accumulate and dissipate charges.

A switched capacitor voltage step down(buck) converter uses a set of flying capacitors to regulate voltage across an RC load

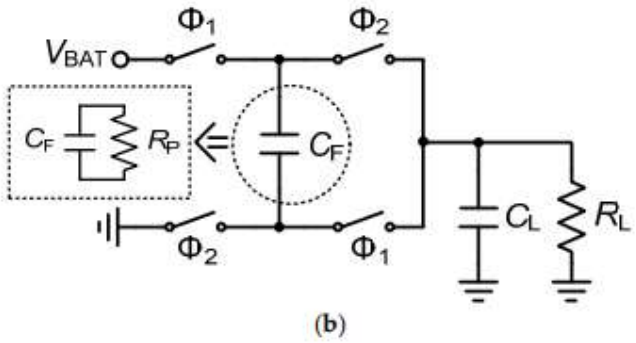


Fig 2.1 represents the simple 1:2 Switched capacitor circuit

General working principle

During the charging phase(o1) capacitors get charged, current to the load is supplied by source. During the discharge(o2) Cf is connected in parallel to RC load, Cf transfers the same amount of charge acquired to the load, load current is supplied by Cf and Cl .

2.4)Control architecture mechanisms for monitoring voltage ripple and overall converter efficiency

The 3 most commonly used techniques to reduce output ripple under varying load current in SW-DC converters are:

Frequency control - in this method the switching frequency is varied with varying load . under light load values, the capacitors discharge faster, hence frequency has to be Increased to prevent current drop and reduce ripple. To increase switching frequency, controller(oscillator) energy required increases

Duty cycle control- this method modulates the output current/voltage by varying connection time to o/p node.for light loads ,duty cycle is increased as load increases.

Capacitance control.-In this method the value of the flying capacitance is varied According to the load. As the load decreases, additional flying capacitances are added in parallel to increase capacitance across load to maintain high RC value and reduce output voltage drop.

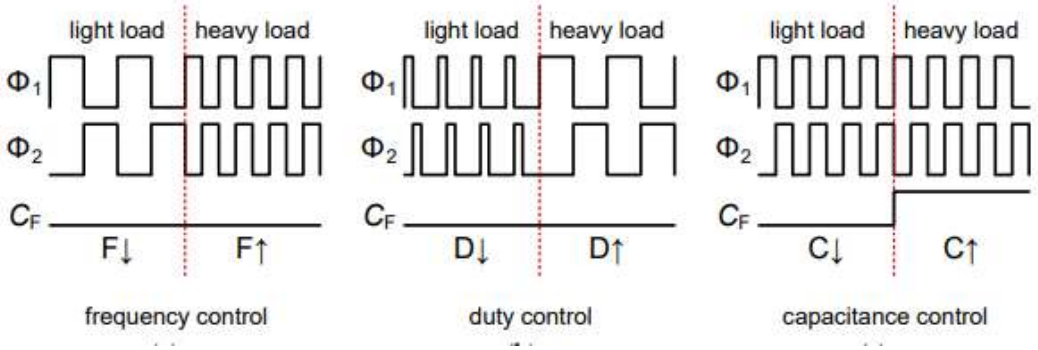


Fig 2.2 represents the 3 different types of control technique used in switched Capacitor DC-DC Convertor

2.5)Hysteretic control method

A technique where the output voltage of SC-dc converter is compared with reference voltage levels and accordingly switch between phases.

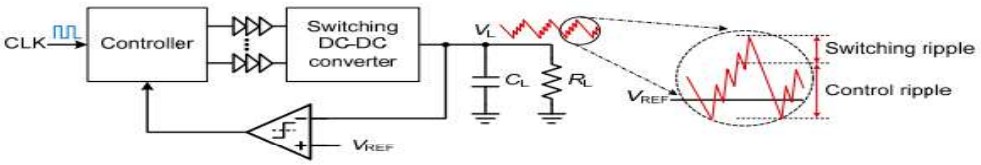


Figure 3. Block diagram of the switched-capacitor (SC) DC–DC converter using one-boundary hysteresis feedback and its output ripple voltage.

Fig 2.3 represents the block diagram of switched DC-DC convertor using single boundary hysteresis control method with feedback

Two commonly used types depending on the value of the load capacitor

1)Single boundary hysteretic control technique: In this control technique the voltage output of the SWDC converter is compared with a reference voltage, if the output drops below this reference voltage, the control architecture switches phase mostly used when Cout(load capacitor)~=Cfly(flying capacitors). Below figure shows typical waveforms It shows output voltage Vout being compared with reference VL in synchronous with the sample clock. The converter switches phase whenever Vout goes below VL and the cycle repeats. Converter clock signal indicates the phase of the converter(charging or discharging)

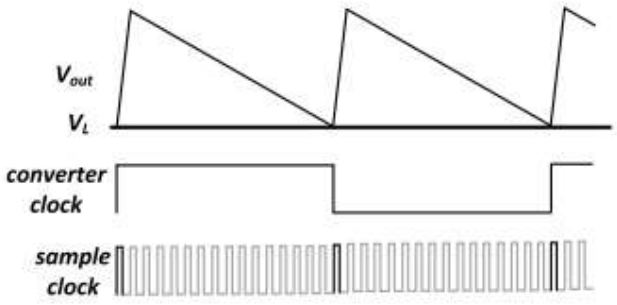


Fig 2.4 represents the output voltage and reference voltage VL ,Converter clock signal and sample clock

2)Double boundary hysteretic control: this method is used when Cout is of much greater value than Cfly.There are two modes of operation enable and the disable mode.In enable mode, Vout gets incremented in small steps during each charge and discharge cycle due to the high value of Cout used. When Vout rises above the upper boundary(VH) the converter enters the disable mode where the Converter operates in the discharge phase the output voltage eventually falls below the lower boundary(Vl) and the controller enters enable mode ,the cycle repeats

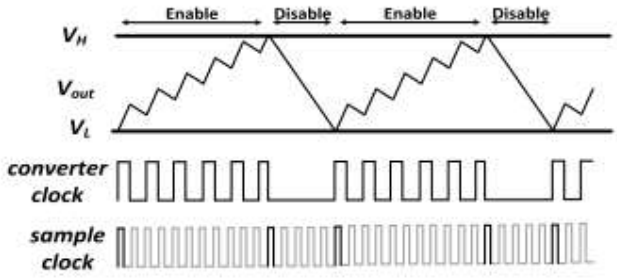


Fig 2.5 represents the Vout with Convertor clock showing enable mode and disable mode and sample clock

2.6)Single boundary hysteretic control for a 1:2 step down SW-dc-dc converter

A two phase SC-dc-dc converter with voltage conversion ratio of 2:1 is shown in fig Cfly - charge transfer capacitor, Cout-load capacitor .To achieve a voltage gain of 2:1 Cout The same order of Cfly is used(to divide voltage equally) as Cout~=Cfly output ripple is significant. Therefore single boundary hysteretic control is used.

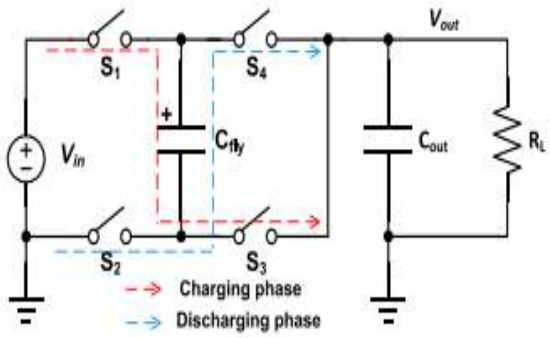


Fig 2.6 Charging and discharging phase of SWDC

During charging phase: Charge transfer to both capacitors are impulsive,then Cout

discharges through Rl, supplying current to the load.consequently Vout decreases, Vcfly Increases when Vout drops below Vref ,control architecture switches phase

During Discharge phase : Cout and Cfly are connected in parallel across load Rl. Charge sharing takes place(impulsive transfer) Vout increases to Voutmax, Vcfly drops to Voutmax, The capacitors discharge supplying load current across RL, Vout eventually drops below Vref and controller switches to charging phase

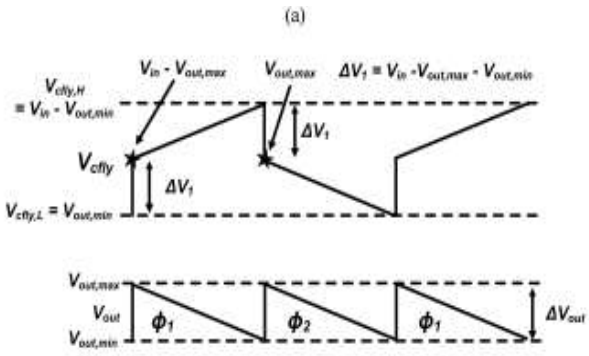


Fig 2.7 represents the output voltage and flying capacitor voltage

Steady state equations:

The same amount of charge acquired by Cfly in the charging phase is transferred to RC load in the discharge phase.

Charge transfer is given by $Q = C_{fly} \Delta V_{cfly}$

Average output current is given by $I_{out} = 2 f_{sw} C_{fly} \Delta V_{cfly}.$

Output voltage ripple can be calculated $$\Delta V_{out} = V_{out,max} - V_{out,min} = \frac{I_{out}}{2 f_{sw} (C_{fly} + C_{out})}.$$

Chapter 3: Block diagram of control architecture and implementation of a single boundary hysteretic controller

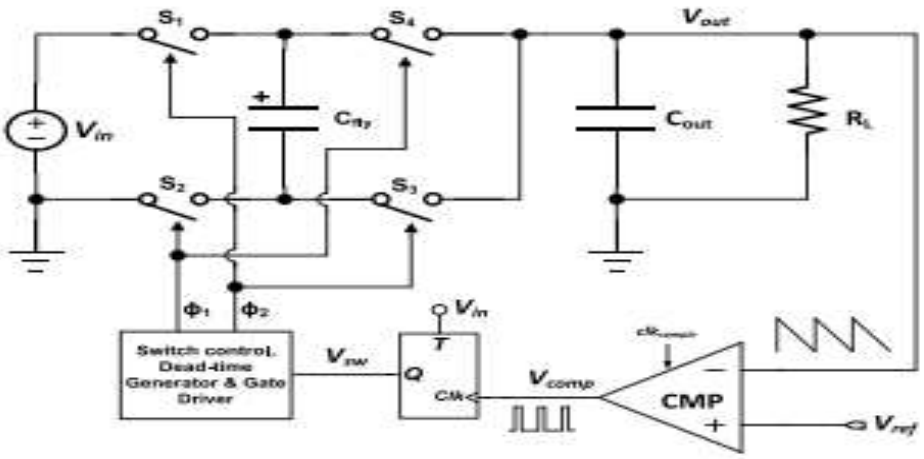


Fig 2.8 represents the Single boundary hysteretic control method

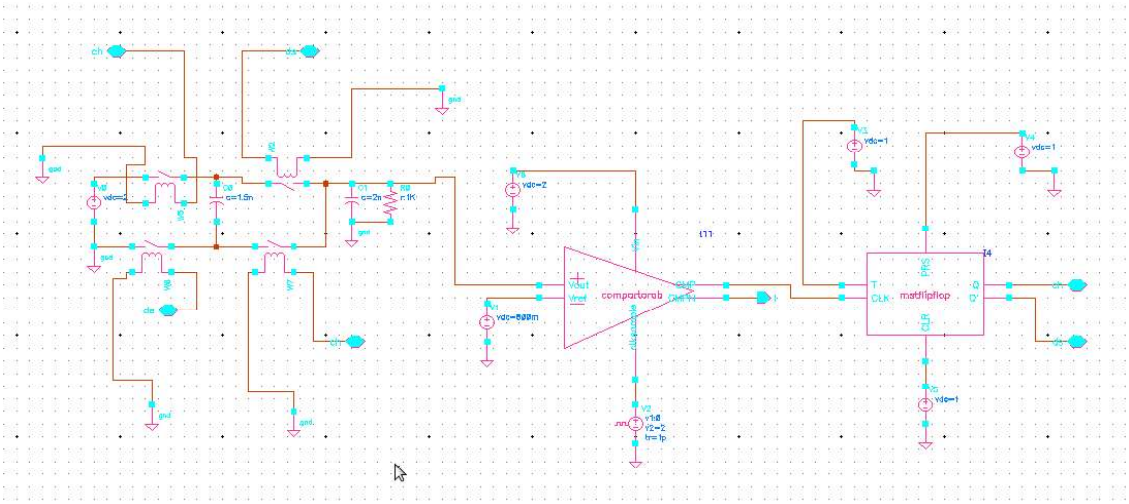


Fig 2.9 represents the simulation of a single boundary Hysteretic control method in Cadence Virtuoso.

The above figure shows the block diagram of a switched capacitor converter that uses single boundary hysteretic control for its switching purpose. The output voltage is fed to a dynamic clocked comparator where it is compared with a reference voltage signal. In synchronization with the sample clock signal, the comparator outputs a pulse whenever the output voltage drops below the specified reference voltage. This pulse is used to toggle the state of the T-flip flop which is used to switch between the charging and discharging phase. The output of the T-flip flop is fed to the switches(MOSFETS) of the converter via a gate driver Circuit. The Gate driver block provides dead time generation between the complementary Signals to prevent overlap during phase transition. It also does level shifting operation to minimize the gate driving losses of the MOSFETS that are being driven and ensures that MOSFETs have sufficient turn on voltage between their gate and source terminals.

3.1)IMPLEMENTATIONS

Testing of 1:2 Switched capacitor in cadence:

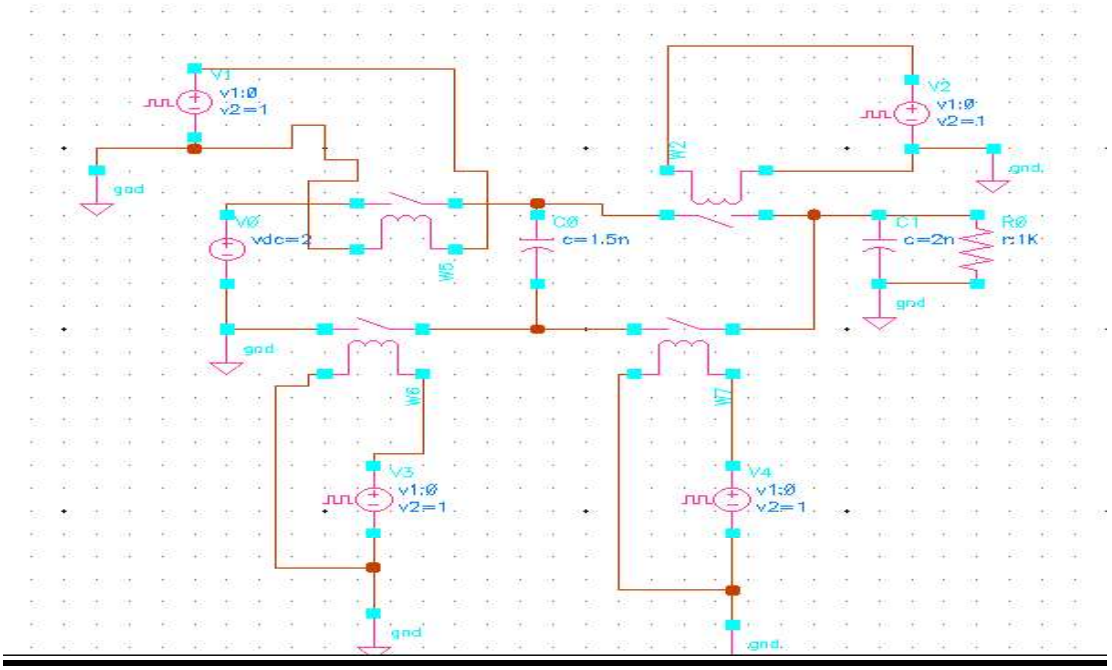
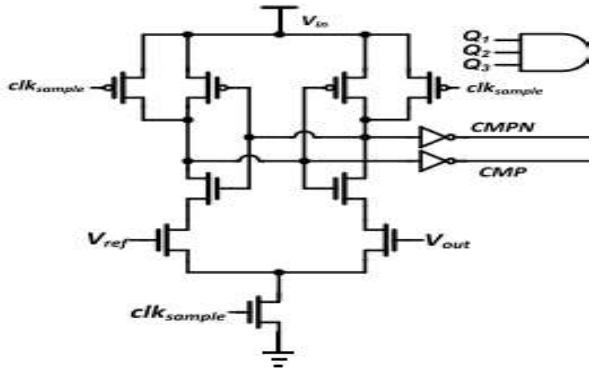


Fig 3.1 represents the implementation of Switched capacitor DC-DC convertor without Feedback Vin =2V Cfly =1.5nF C load =2nF R load=1K ohm Switching period =1us.

3.2)Output Voltage Ripple :

In single boundary Hysteretic control method the output the voltage which we feed into the Comparator as clock signal that is the periodic rectangular pulse with duty cycle 0.5 has the fixed frequency .Hence the sampling period of the output will remain same and we sample it when Vout is less than the reference voltage.

3.3)Implementation of DynamicComparator in Cadence



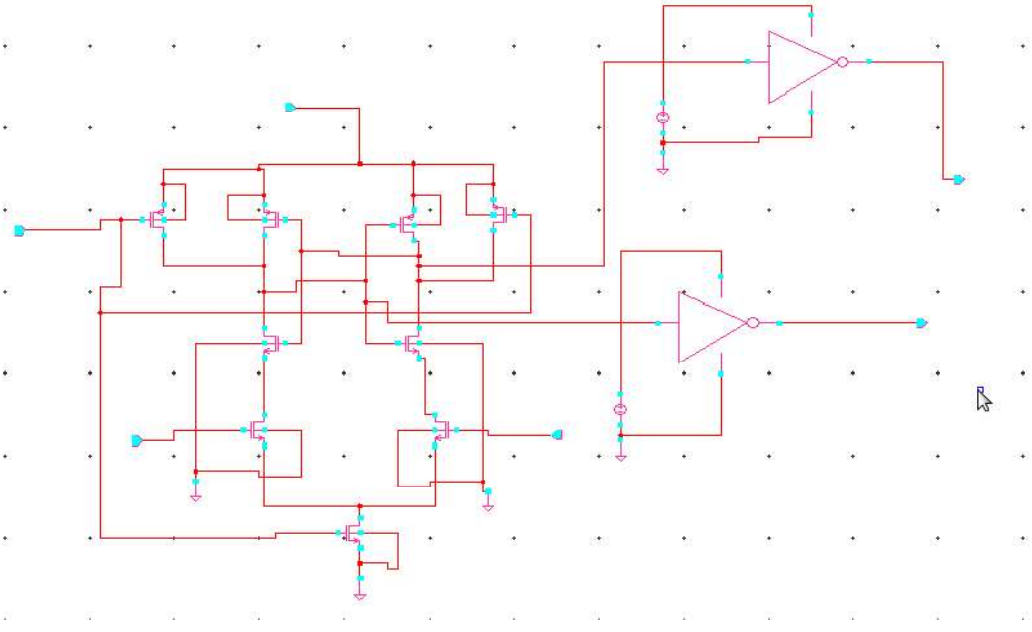


Fig3.2 represents the representation and simulation of Transistor level implementation of

Dynamic comparator in Cadence Virtuoso

The above figures show the circuit diagram of the dynamic comparator. The inputs

clk(sampling clock) ,Vref(reference voltage), Vout(output voltage)are applied to the gates

of the transistors as shown . The inner 4 transistors form a back to back inverter or latch. The circuit works on the principle of Domino logic ,during the precharge phase clk sample low nodes of the latch are pulled up and the outputs(CMP,CMPN) are low. In the evaluation phase clk sample is high , depending on the value of the output voltage the pull down strength of the two transistors gated by Vref and Vout change ,thereby one node will get pulled down to ground faster and the other, and the node will be high due to the back to back inverting action.

3.4)Testbench Circuit

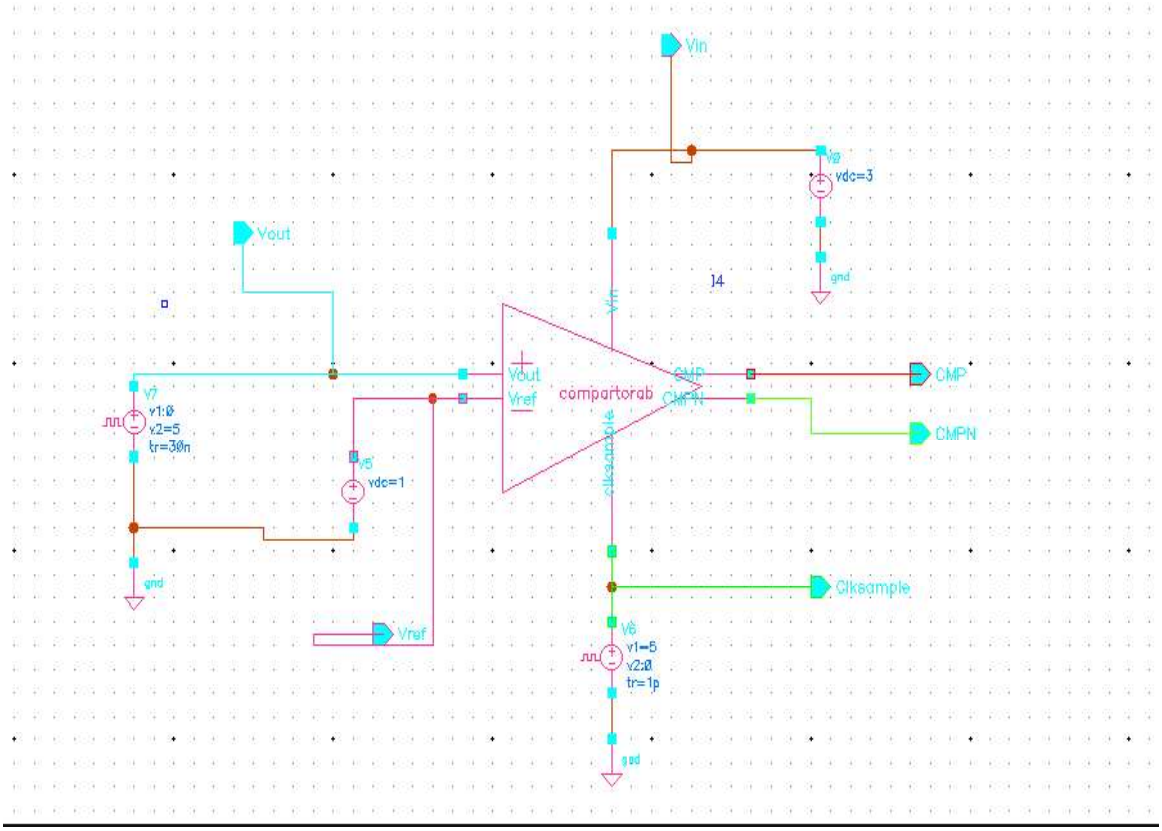


Fig 3.3 represents the testbench simulation of dynamic comparator circuit

3.5) T flip flop Using Master slave J-K flip flop with preset and clear input

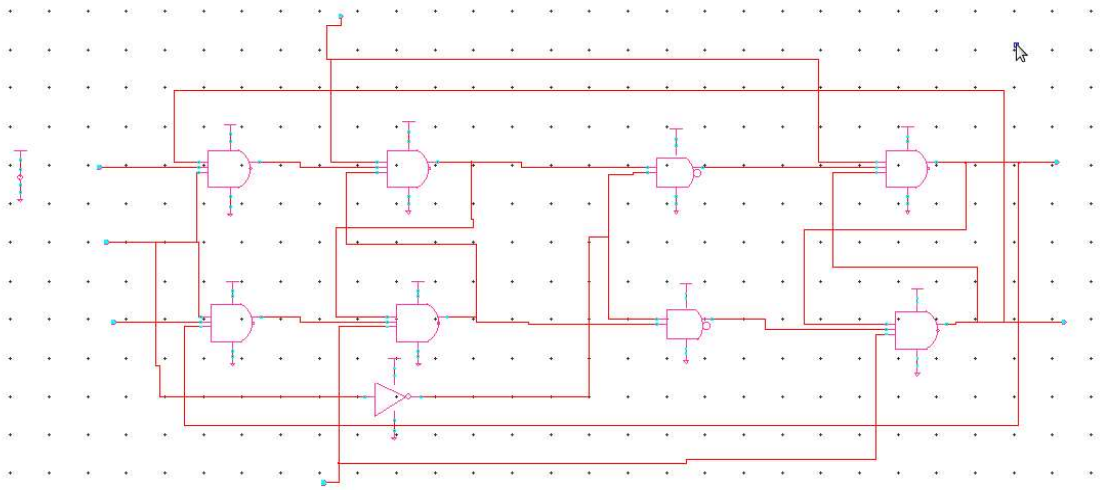


Fig 3.4 represents the simulation of Master Slave J-K flip flop with asynchronous preset and clear signal

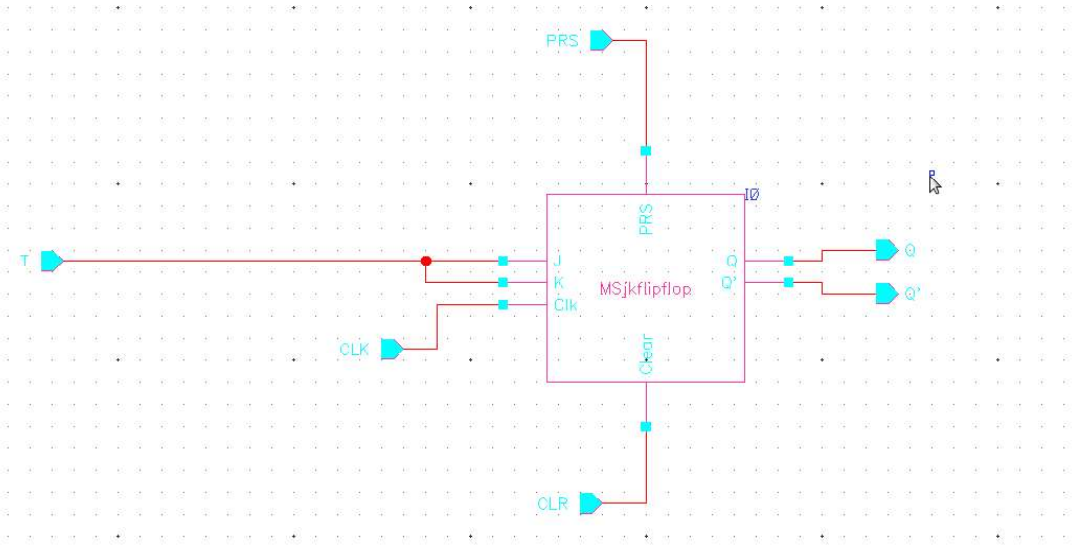


Fig 3.5 represents the simulation of T flip flop using Master Slave J-K flip flop

3.6)Implementation of Single boundaryHysteretic controller by replacing The Ideal switch by PMOS and NMOS :

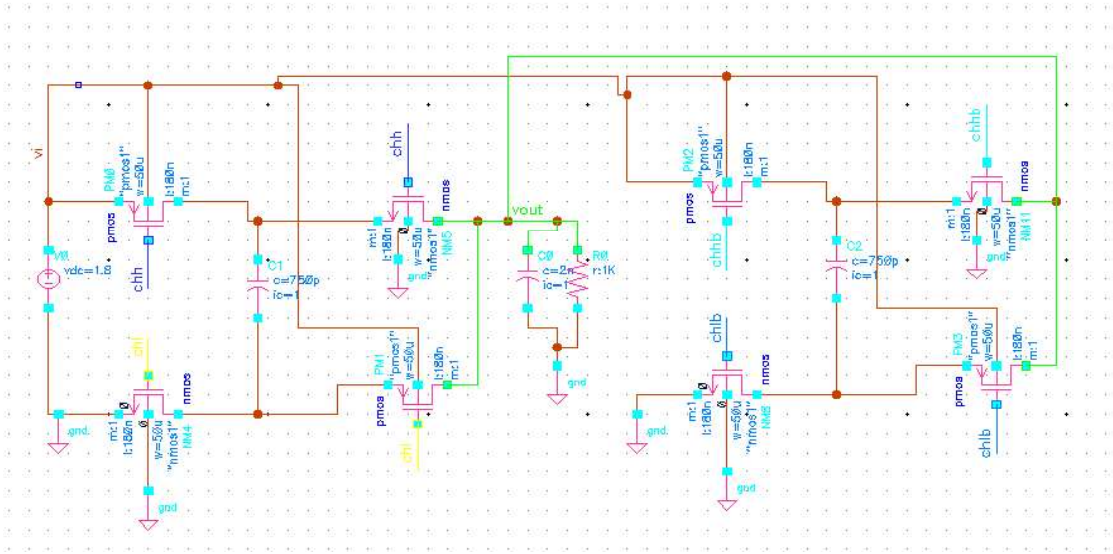


Fig 3.6 represents the Single boundary hysteric control circuit with Mosfet as switch

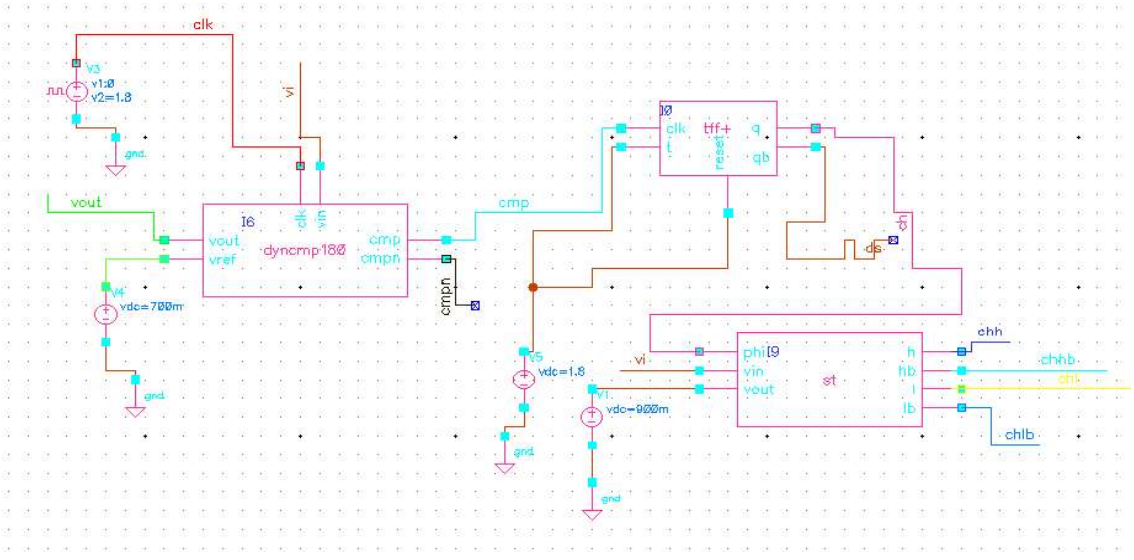


Fig 3.7 represents the Dynamic comparator circuit ,T flip flop and level shifter circuit generate voltage signals to the inputs of Mosfets

Here in the above circuit we have replaced Ideal Switch with Mosfets The switches S1,1, S1,3, S2,1, and S2,3 are replaced by p-type MOSFETs whereas S1,2, S1,4, S2,2, and S2,4 are implemented as n-type MOSFETs .The working is same as the Single boundary hysteretic control method .These Gate signals are generated from the startup circuit where we have level Shifter ,dead time generator .Level shifter will cause the phased signals to move from one voltage level to the other level.

Chapter 4) Modified Hysteretic controllerBlocks/Working/Schematics(Cadence 180nm):

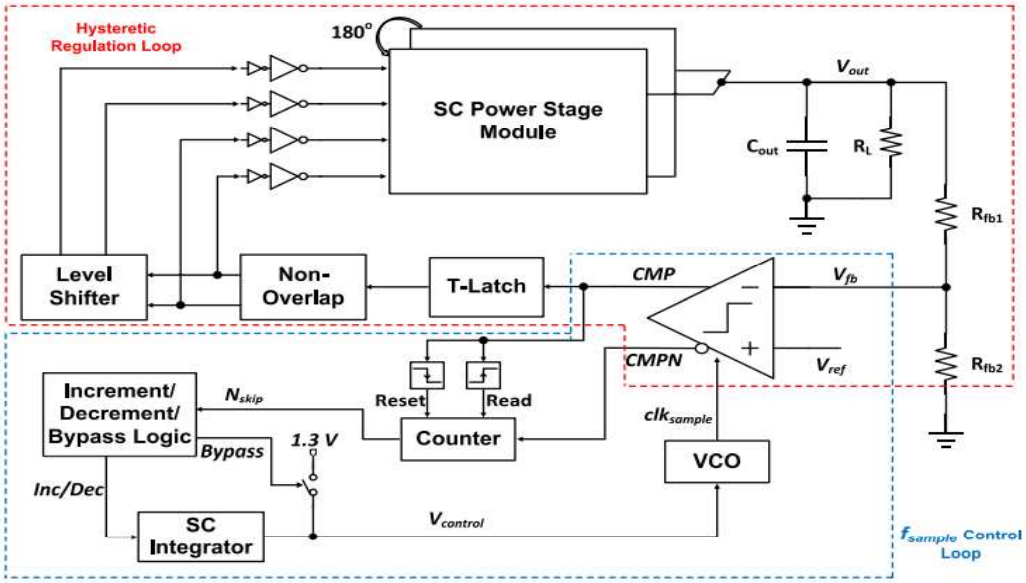
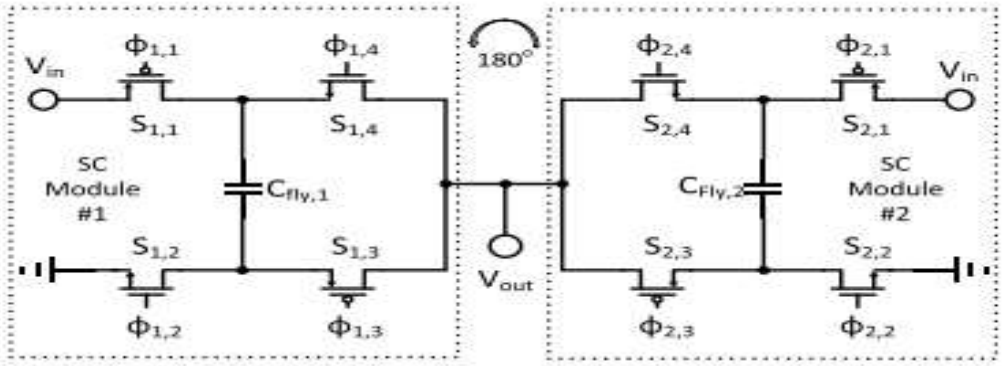


Fig 4.1 represents the block diagram of modified hysteretic controller

The above diagram shows the modified hysteretic controller, the main purpose of this modification is for the converter to automatically adjust the sampling clock frequency given to the dynamic comparator, so as to conserve power being consumed by the VCO that generates it in reference to certain tolerable voltage ripple observed at output, to avoid non-uniform ripple in the output as explained earlier. The sampling clock frequency to the Dynamic comparator is generated by a VCO, the CMPN signals from the dynamic comparator is being counted by a 3 bit counter the value being Nskip, if the N-skip count is above a reference value, an



increment decrement bypass block is used to generate inc/dec signals, here a 3 bit magnitude comparator is used to compare the value of Nskip with a reference Nskip value Nref, so when Nskip is less than reference value the frequency of VCO must be increased , to avoid non uniform ripple, when Nskip is greater than Nref the frequency fromVCO must be reduced must to minimize its current consumption and increase efficiency, the sampling frequency pulse from the VCO is generated by adjusting its control voltage, this control voltage is supplied from a charge pump circuit whose output voltage can be increased or decreased from the inc/dec signals from the 3 bit comparator.

4.1)SWDC MODULE:

Fig 4.2 represents the circuit diagram of a 2 phase 1:2 step down swdc converter

The figure shows a two phase operation of a switched capacitor converter, while one converter is in the charging phase the other converter is in the discharging phase, this allows even charge distribution on the output RC load. Same circuit was explained earlier for a simple hysteretic controller.

4.2)Level shifter , Dead time generator

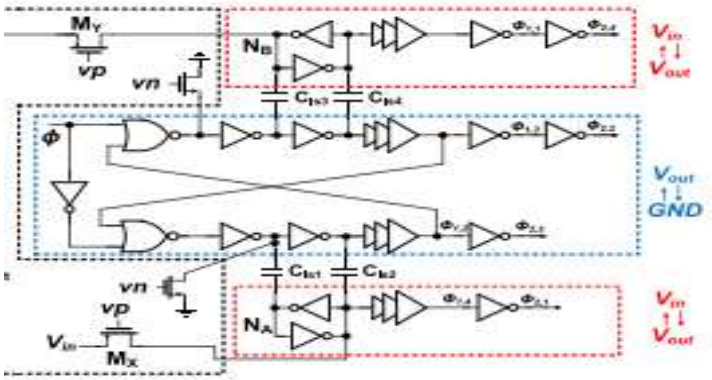


Fig 4.3 represents the circuit diagram of a level shifter,dead time generator

The above figure shows a level shifter circuit to drive the gates of 2 the SWDC module circuit , The phi is the clock signal that is output of T Latch, the circuit outlined in blue, make an SR latch with delays due to inverters/buffers, so that one output changes before the other causing a deadtime between each output, this deadtime between outputs is required to prevent both charge and discharge paths to be on at the same instant, causing a path from input to ground due to which current spikes and lowers efficiency.

4.3)Level shifter , Dead time generator Schematic

The below fig shows the implementation of the level shifter, deadtime generator circuit same as in circuit diagram, Transistor widths for each gate, W=5u,Vin=1.8V, Vout = 900mv for testing Level shifting capacitor used =2pF

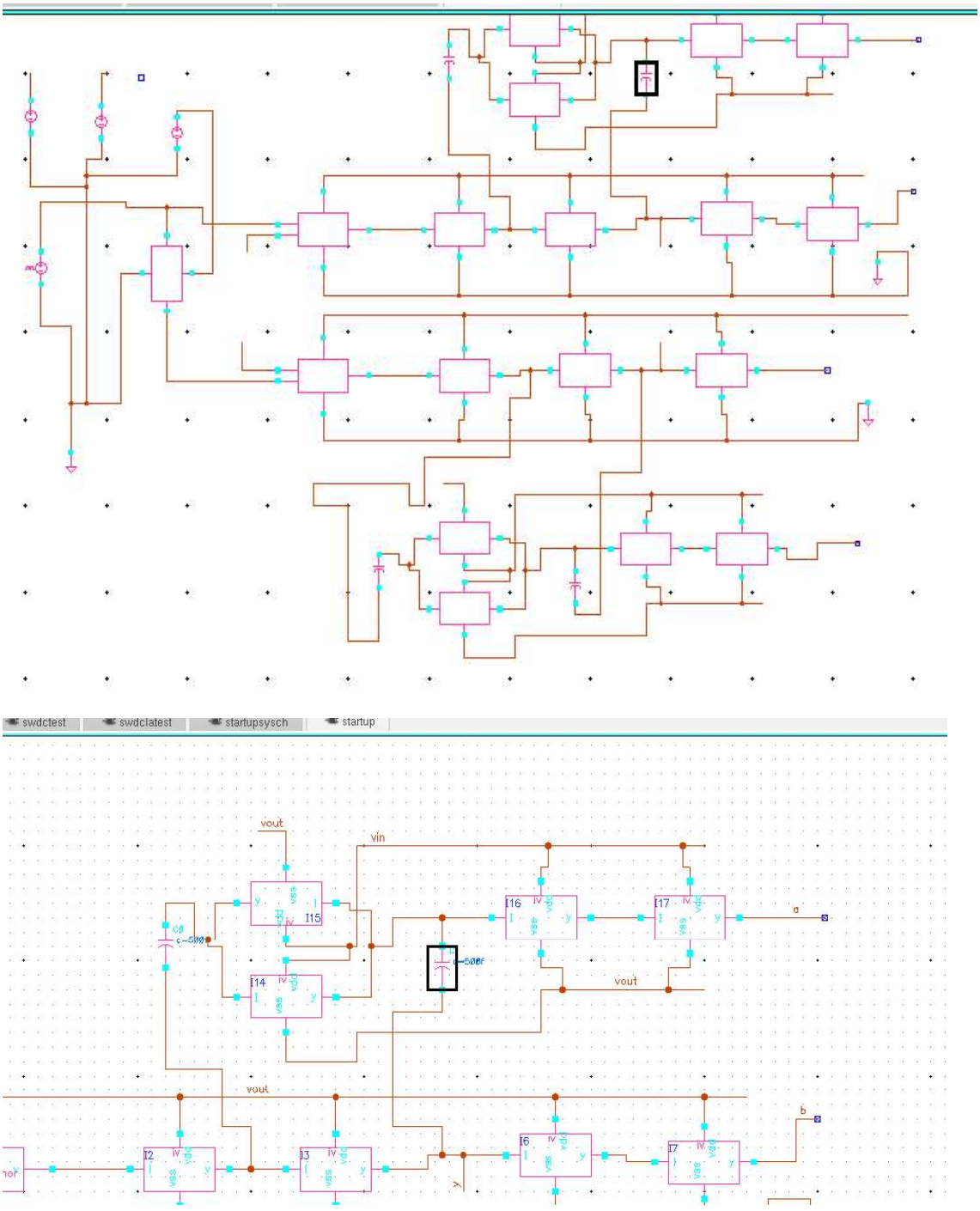


Fig 4.4 represents the schematic of a level shifter,dead time generator

4.4)Voltage Controlled Oscillator

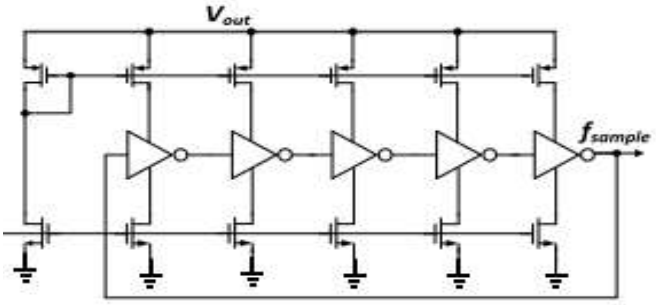


Fig 4.5 represents the circuit diagram of a Voltage controlled oscillator

The above fig show circuit diagram of a current starved VCO, the name current starved means current controlled, the back to back inverters shown make a ring oscillator, the input voltage is applied to the gates of all nmos, the input voltage controls current in branch and the current is mirrored to all pmos, thereby controlling the pull up current to the ring oscillator(current starving),

Reducing current increases the delay to charge the gates between inverter mosfets, so the output time period of pulse increases and fsample decreases.

4.5)Voltage Controlled Oscillator Schematic

Below figure is the transistor level implementation of VCO, ring oscillator mosfets have W=1u pull up/pull down mosfets have W=2u, a trigger pulse is used to start the oscillation, and inverter is used at out to obtain a square wave signal.

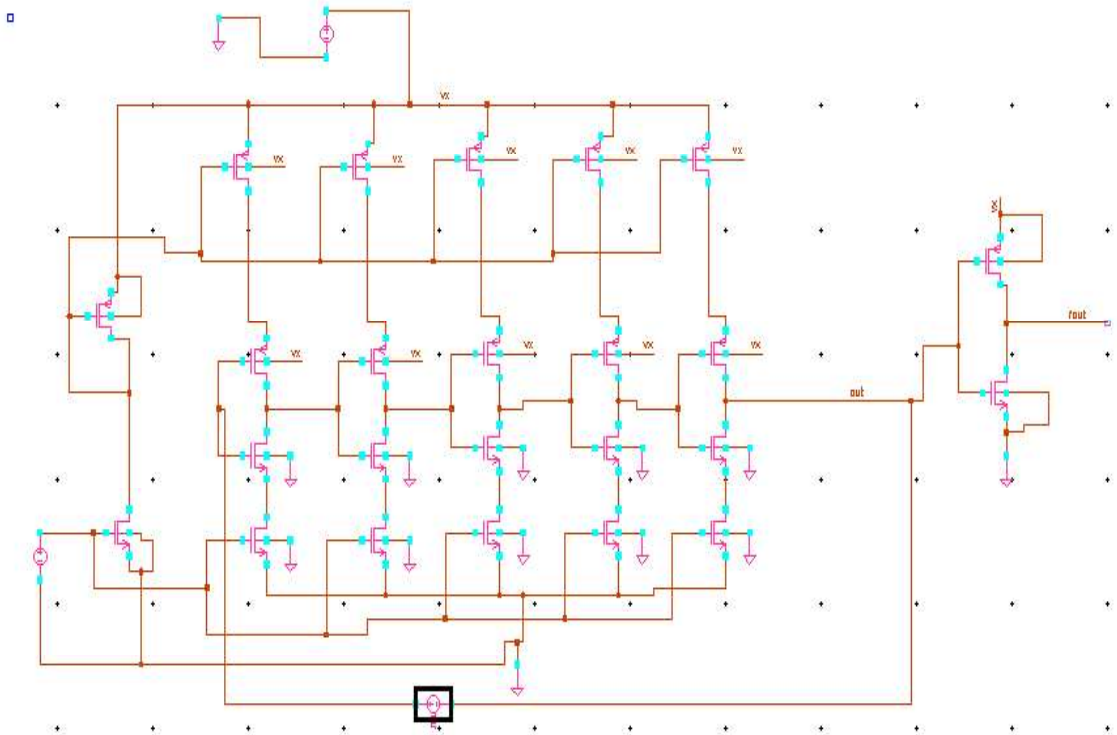


Fig 4.6 represents the schematic of a Voltage controlled oscillator

4.6) N-Skip counter

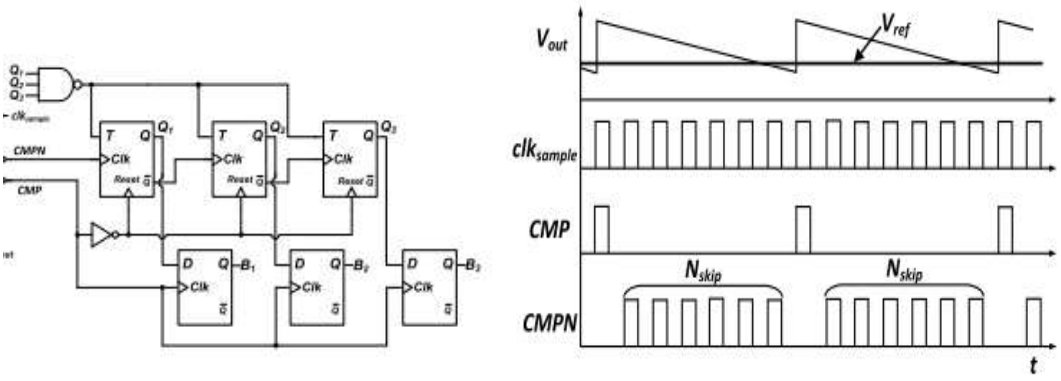


Fig 4.7 represents the circuit and waveforms of an Nskip counter

The above fig shows the circuit of Nskip counter, the T Flip Flops make an up counter it counts the no. of CMPN pulses that come from the dynamic comparator, when the CMP signal arrives the counter resets and the current count value is loaded parallely to the D'Flip Flops and stored, the counter stops counting after it reaches a maximum of 7 which is Q0Q1Q2=111 the nand gate sets T to 0, and T Flip Flops become inactive.

4.7) Nskip counter Schematic

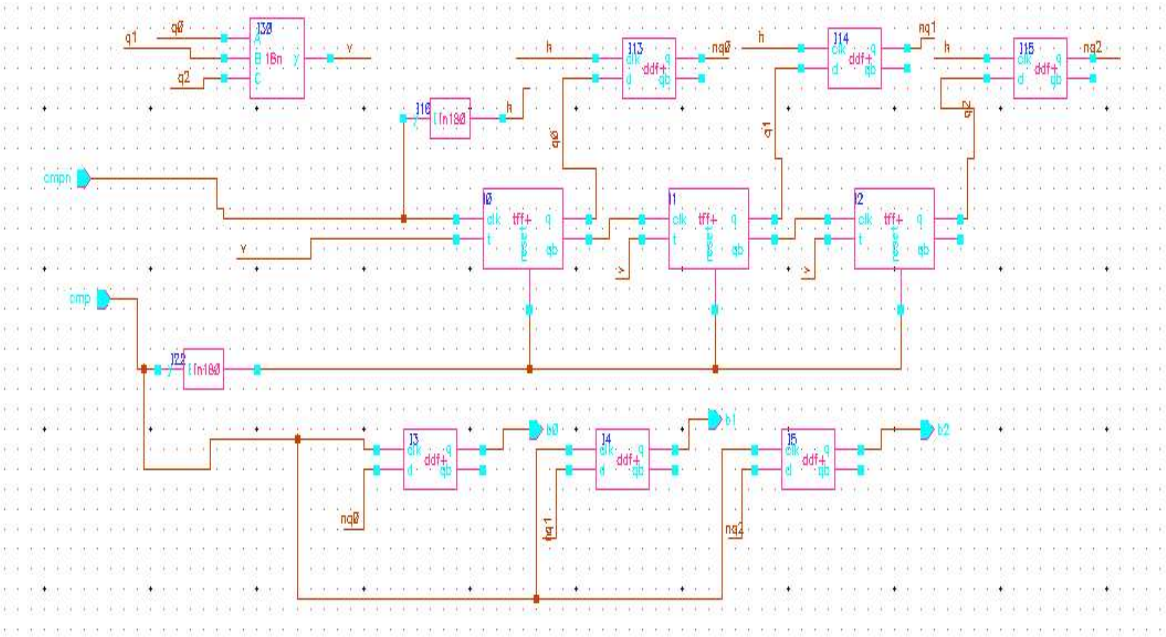


Fig 4.8 represents the schematic of an Nskip counter

The above schematic show implementation of the Nskip counter positive edge triggered T and D flip flops are used, with asynchronous reset, to achieve same action as positive edge triggered reset as in circuit diagram additional D Flip Flops are added above to capture q values before it gets asynchronously reseted.

4.8)Increment/Decrement Bypass logic and Charge pump circuit

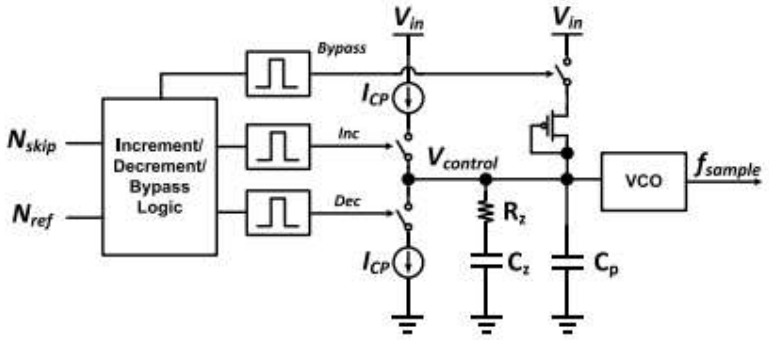


Fig 4.9 represents the circuit diagram of an inc/dec bypass logic

In the above figure the increment and decrement Bypass logic is a 3 bit magnitude comparator, that generates inc high when Nksip<Nref, dec high when Nskip > Nref, Nref is a reference count value to be set(here must be less than 7), when inc is high the capacitor Cp gets charged by current source and output voltage is incremented , when dec is high capacitor Cp disharges output voltage decrements, this output voltage is given as control input to the VCO

4.9)Increment/Decrement Bypass logic and Charge pump circuit Schematic

The below is the implementation of the charge pump circuit , it is started with an initial condition of 350mV, it is adjusted for voltage change of 10mV/0.1us by the equation I=C(dV/dt) and by choosing C=1uF and setting current source I=10mA.

The below waveforms shows voltage increments/decrements wrt to inc/dec signals.

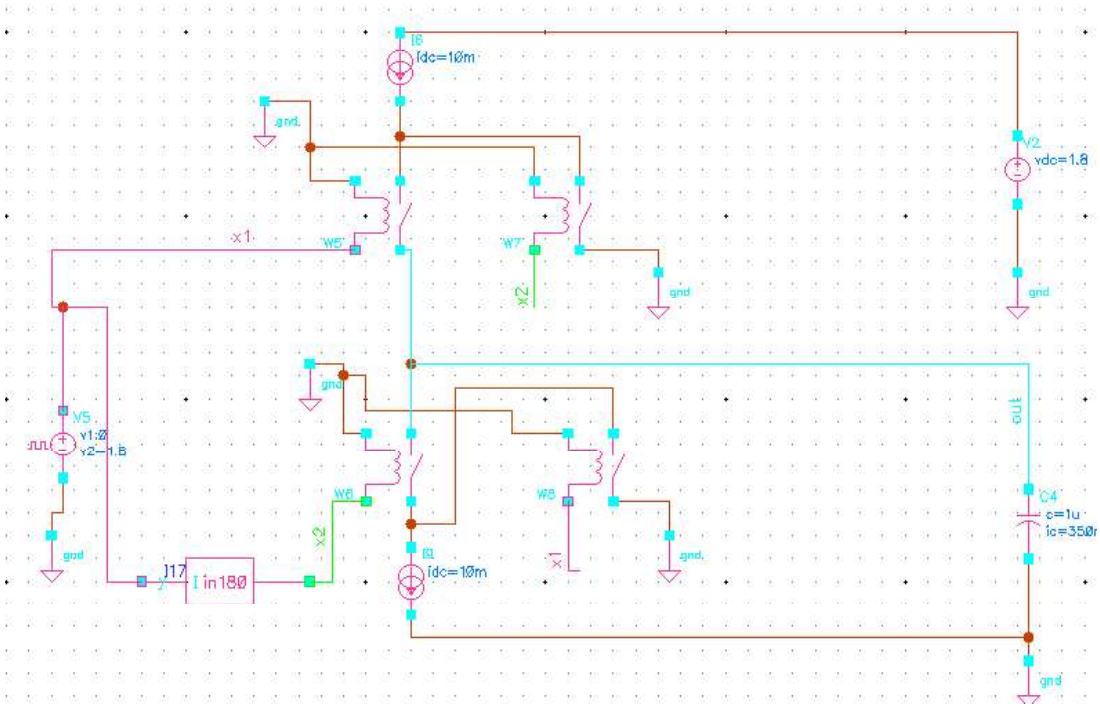


Fig 4.10 represents the schematic of the charge pump circuit

4.10)3 bit magnitude comparator schematic(inc/dec bypass logic)

The below schematic show a 3 bit magnitude comparator implemented for Inc/dec logic

Outputs A greater than B ,A less than B ,A equal to B are designed as per equations

A>B = A3B3' + (A3 Ex-Nor B3) A2B2' + (A3 Ex-Nor B3) (A2 Ex-Nor B2) A1B1' + (A3 Ex-Nor B3) (A2 Ex-Nor B2) (A1 Ex-Nor B1) A0B0'

A<B = A3'B3 + (A3 Ex-Nor B3) A2'B2 + (A3 Ex-Nor B3) (A2 Ex-Nor B2) A1'B1 + (A3 Ex-Nor B3) (A2 Ex-Nor B2) (A1 Ex-Nor B1) A0'B0

The output of the3 bit comparator act as a input to increment ,decrement signals to the charge pump integrator

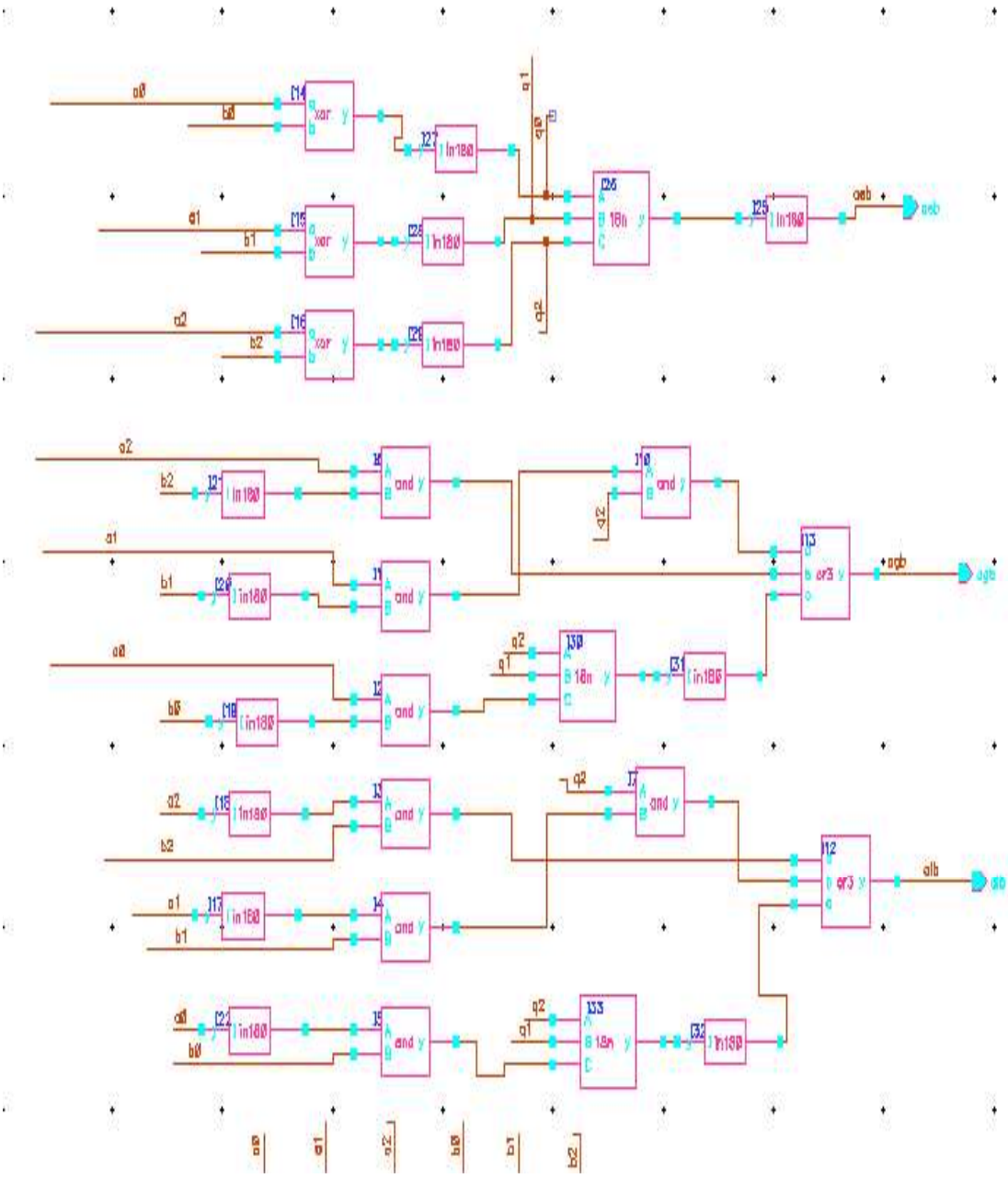


Fig 4.11 represents the schematic of the 3 bit magnitude comparator

Chapter 5)Final Assembly of Blocks for Modified Hysteretic controller Schematics and Resulting waveforms/Power analysis:

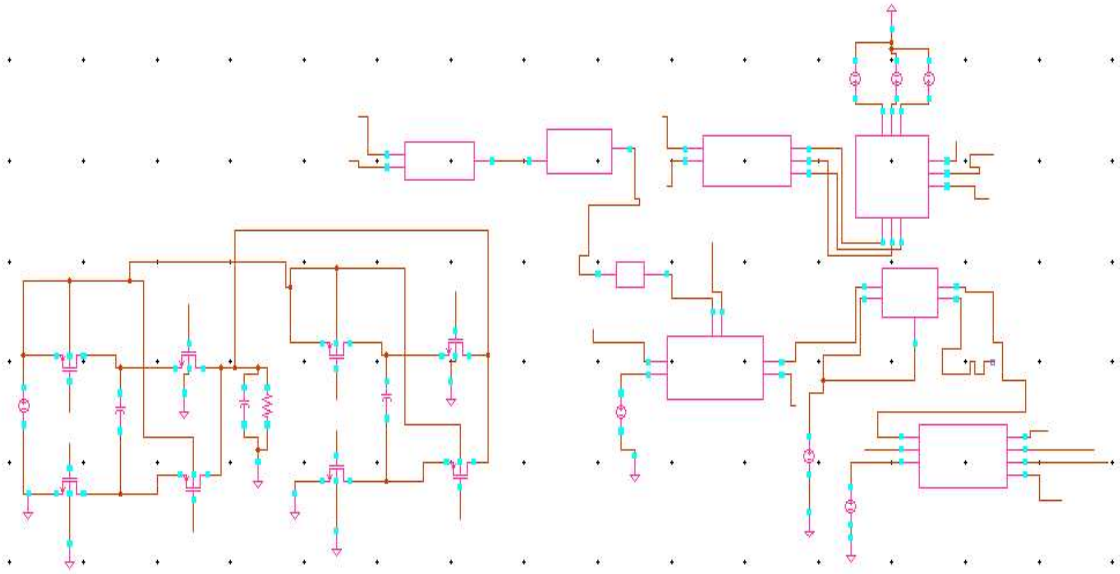


Fig 5.1 represents the schematic of modified hysteretic controller

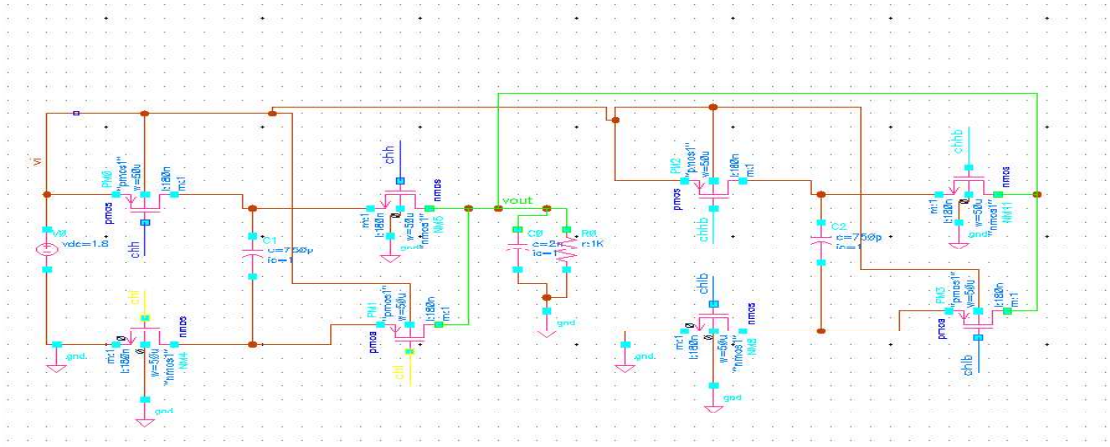


Fig 5.2 represents the schematic of 2 phase switched capacitor module

Input voltage Vdc given is 1.8V, flying capacitors of 0.75nF are used,

Load capacitor = 2nF, resistive load =1k ohms.

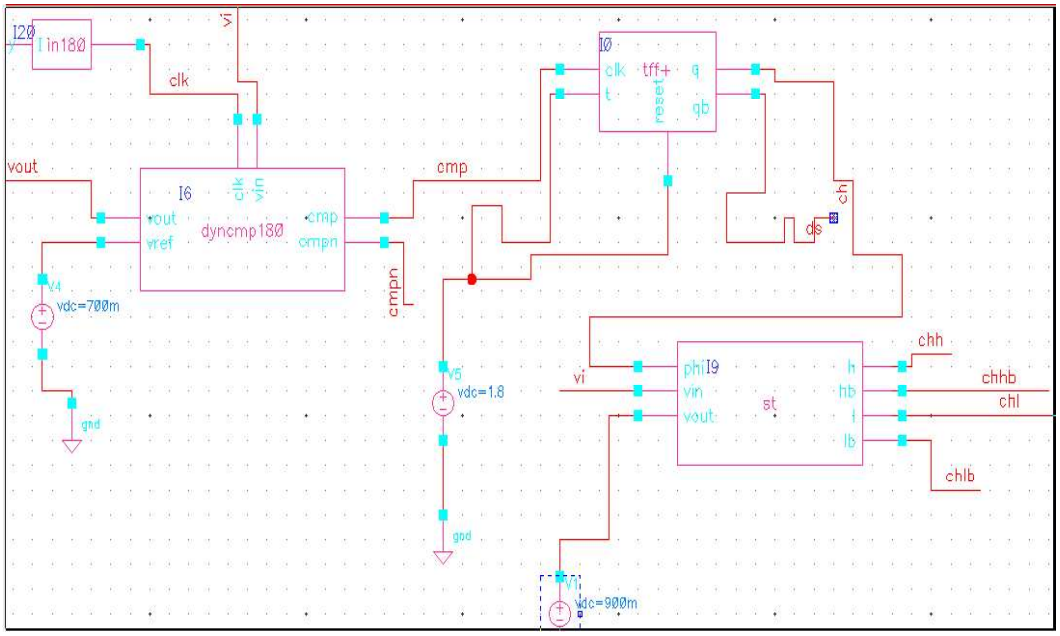


Fig 5.3 represents the Dynamic comparator(dyncmp180), T Flip flop(tff+), level shifter(st)

The above fig shows the Vout net connected to dynamic comparator, the input clock signal from VCO can be seen given to the dynamic comparator, which was a manually generated signal in the simple hysteretic controller circuit shown earlier, the cmp signal is given to T flip flop to change phase(between charging and discharging).The output of T flip flop is given to level shifter that generates the high/low side gate signals to be given to mosfet gates. The cmpn signa is given to the nksip counter for counting.skipped pulses.

The cmpn signal is given to the Nskip counter it count the no. of skipped pulses, this 3 bit value is given to the 3 bit comparator and compared with the reference set

to 101(5) here, it sets inc or dcc high based on comparison and this is given to charge pump, which generates vcont voltage control for VCO

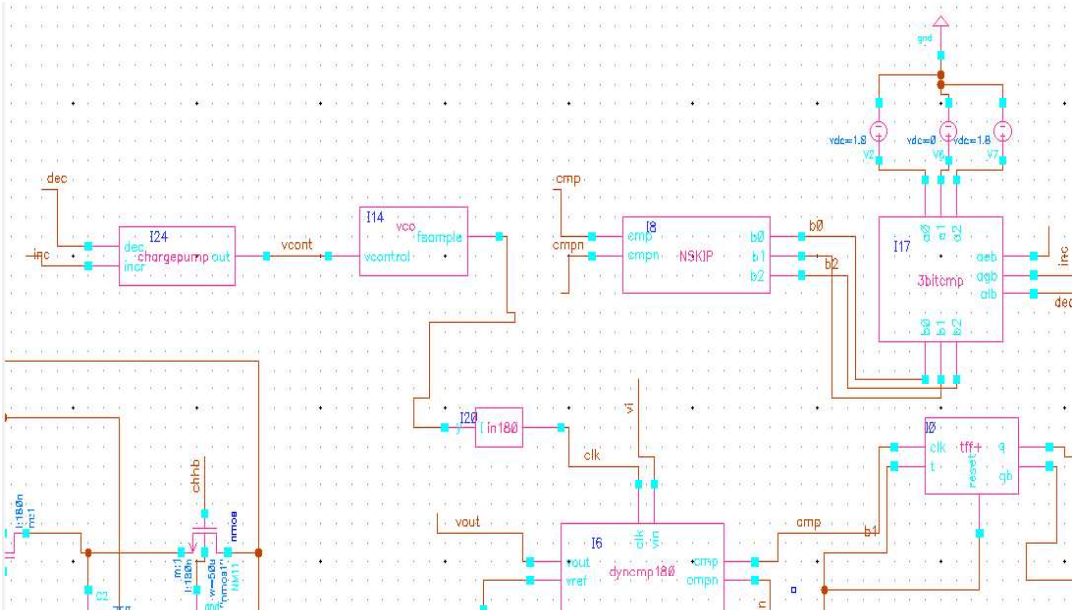


Figure 5.4 shows Nskip counter, 3 bit comparator, charge pump, VCO

5.1)Resulting waveforms and converter working verification

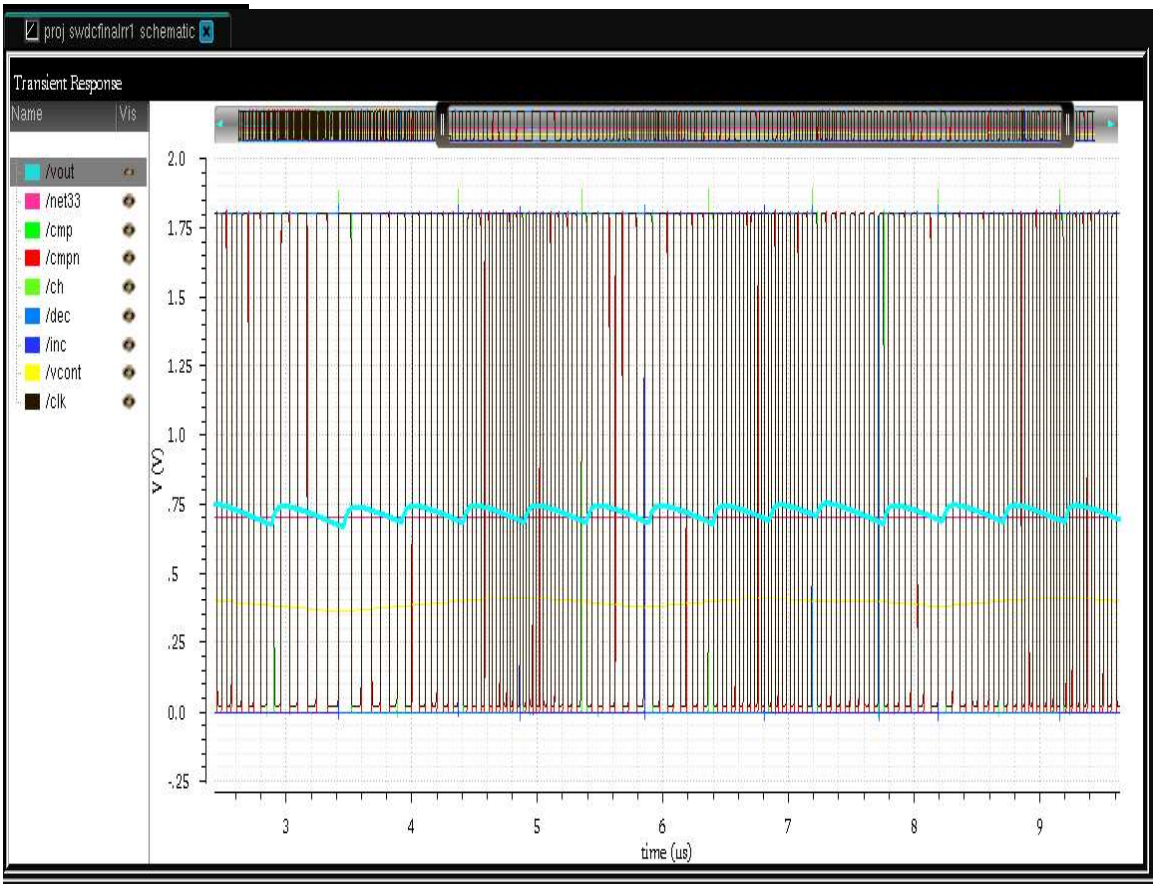


Figure 5.5 shows waveform of simulated modified hysteretic controller schematic

This waveform shows the simulated results for the previous circuit schematic, the converter was started with its capacitors precharged to 1V, so that it can transition to steady state and waveforms can be verified. The output voltage(vout) is shown in red, and has a ripple of ~60mV, the cmp and cmpn signals are depending on whether Vout is above or below Vref(=700mV), the cmpn signals are counted and inc/dec signals go high as per

number of cmpn pulses, vcont signal varies and sampling clock frequency(clk) variation is seen , both inc/dec are low when cmpn count is 5 ie the Nref value, but the charge pump capacitor discharges due the switch resistances used and the converter adjusts to N-skip count values around 5, to ensure that non uniform output voltage ripple is minimized.

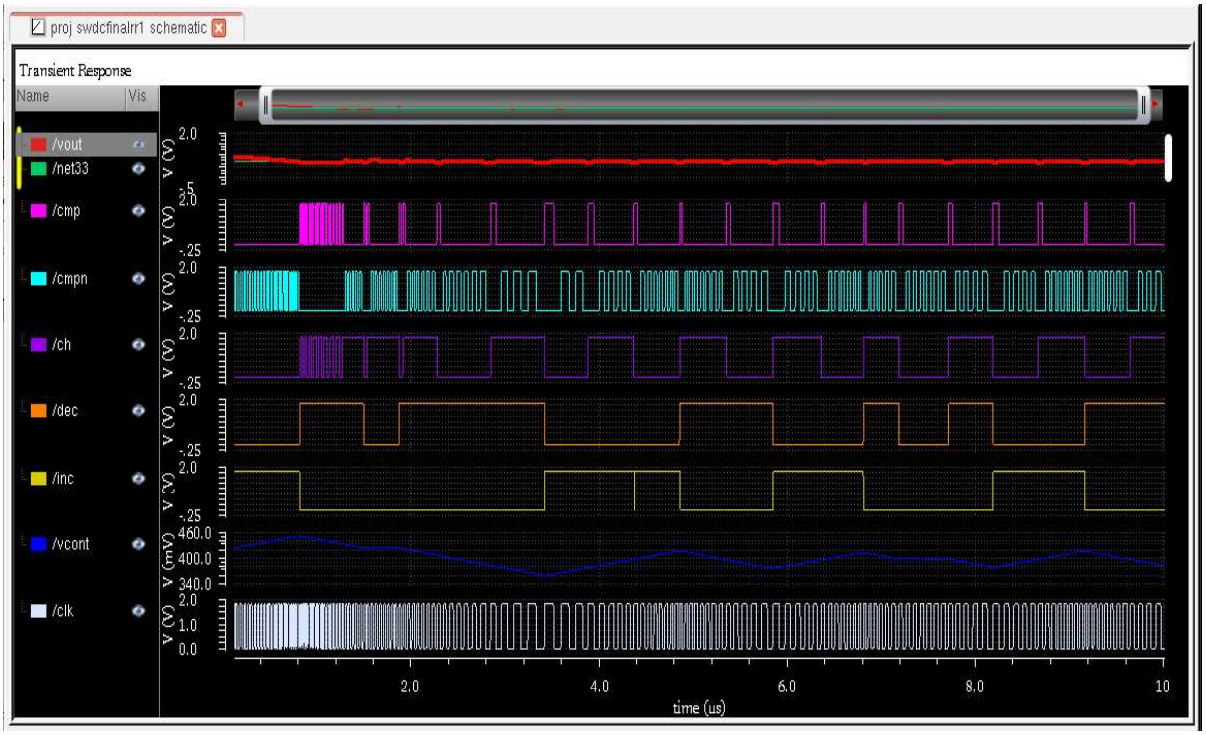


Figure 5.6 shows waveform of simulated modified hysteretic controller schematic

5.2)Power analysis and efficiency calculation:

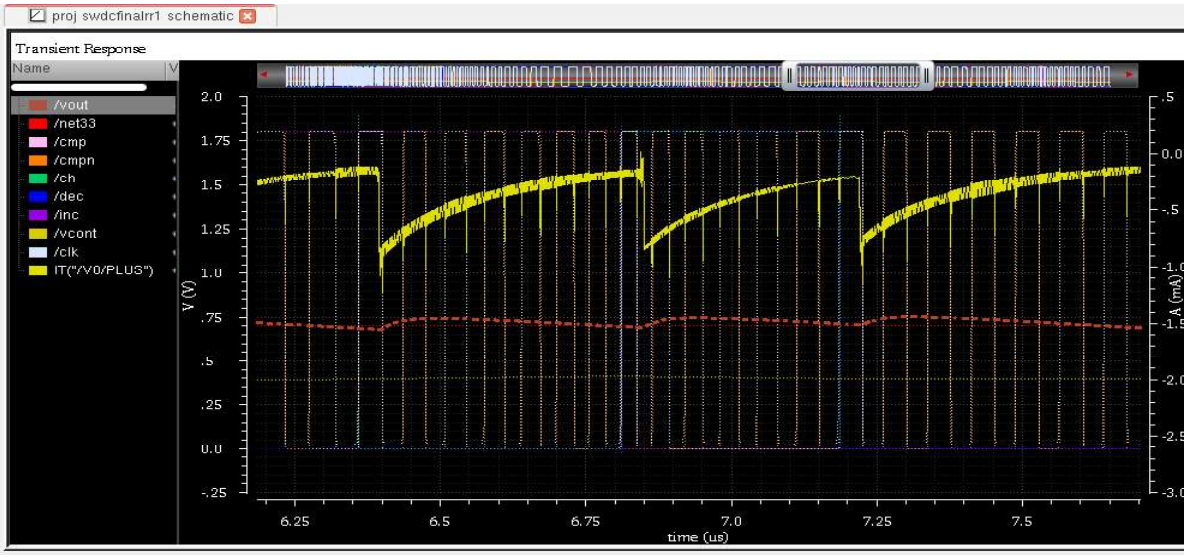


Figure 5.7 shows waveform with input current plots for approximate power calculation

In the above graph instantaneous for the same circuit, input current at input net is plotted in yellow.

Average input power calculation:

Over one half cycle (charging/discharging) voltage and current at input node is measured at 3 points and averaged.

The points are (V,I)(volts,mA) (1.8, 0.8) , (1.8, 0.3) , (1.8, 0.1)

The average input power calculated = 0.72mW

Average output power calculation:

The output is stepped down to a steady value above 700mV with ~60mV ripple

Average output voltage is taken as 730mV, resistive load = 1kohm

Therefore output power = (Vout)^2 / R = 0.49mW

Efficiency calculation: Dividing the output power by input power the efficiency of converter was found to be 85.9% Thus 1:2 voltage step down action is achieved with 85.9% power efficiency.

Chapter 6)Simulated Waveforms of Schematic:

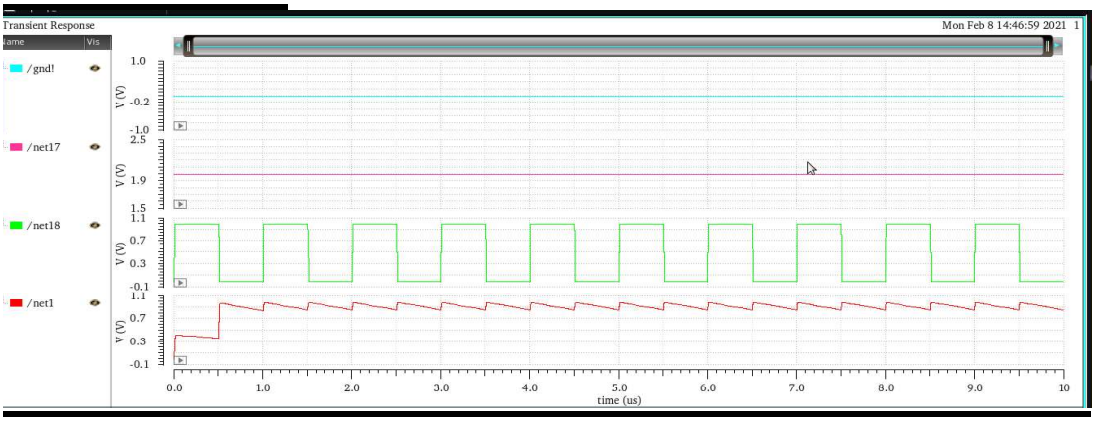


Fig 6.1 represents the output of 1:2 switched capacitor in cadence virtuoso

Here above waveform represent the input signal Vin , input clock signal to the ideal switch and the output voltage obtained .Input voltage =2v Output voltage=~0.9V ,with ripple =~0.1V for 1 Mhz switching frequency

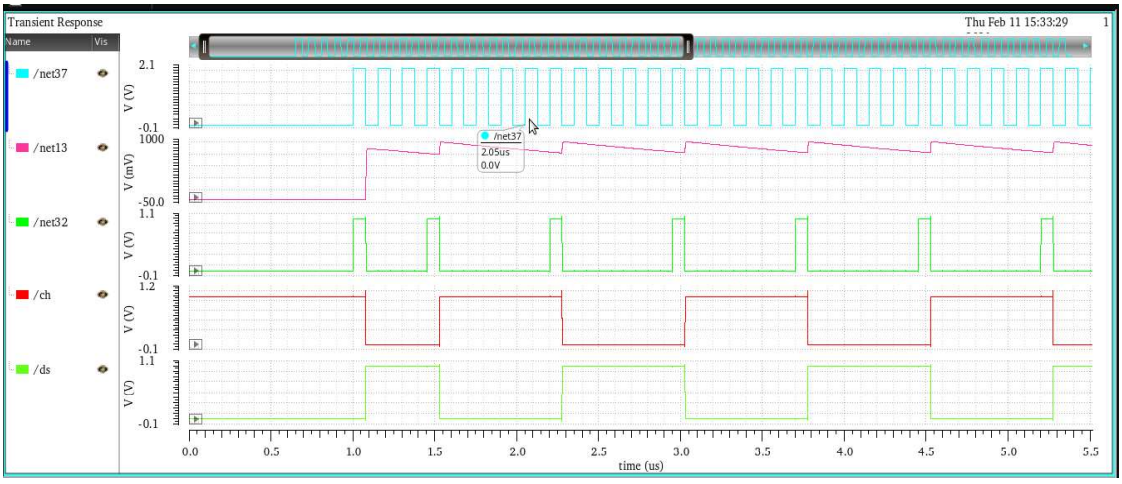


Fig 6.2 represents the output waveform of single boundary hystertic controller

The above waveform represents the output 1:2 switched capacitor with single boundary hysteretic method Net37 represents Sample clock signal which is input to dynamic comparator Net32 is the dynamic comparator output Net13 is the output voltage ch ,ds - it is complementary MS Tflip-flop output signal which is again fed back to the ideal switch

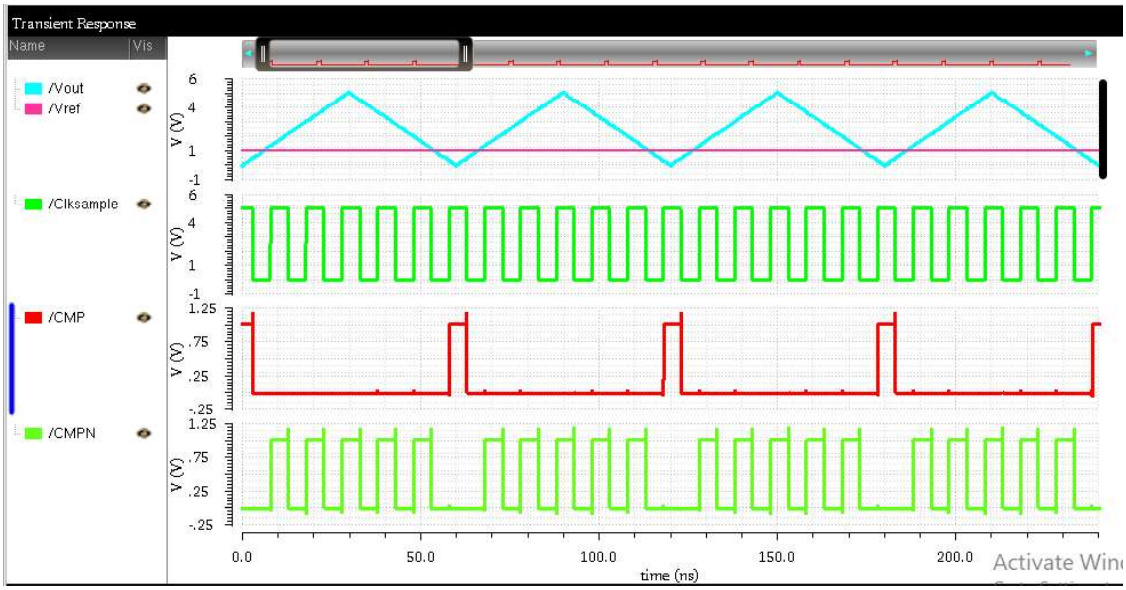


Fig 6.3 represents the testbench simulation output of dynamic comparator

The above waveform is the dynamic comparator input and output signals. We have a triangular reference signal of 6V amplitude and reference voltage of 1V and input clk signal to the dynamic comparator where it samples at the positive edge and output CMP and CMPN signals.

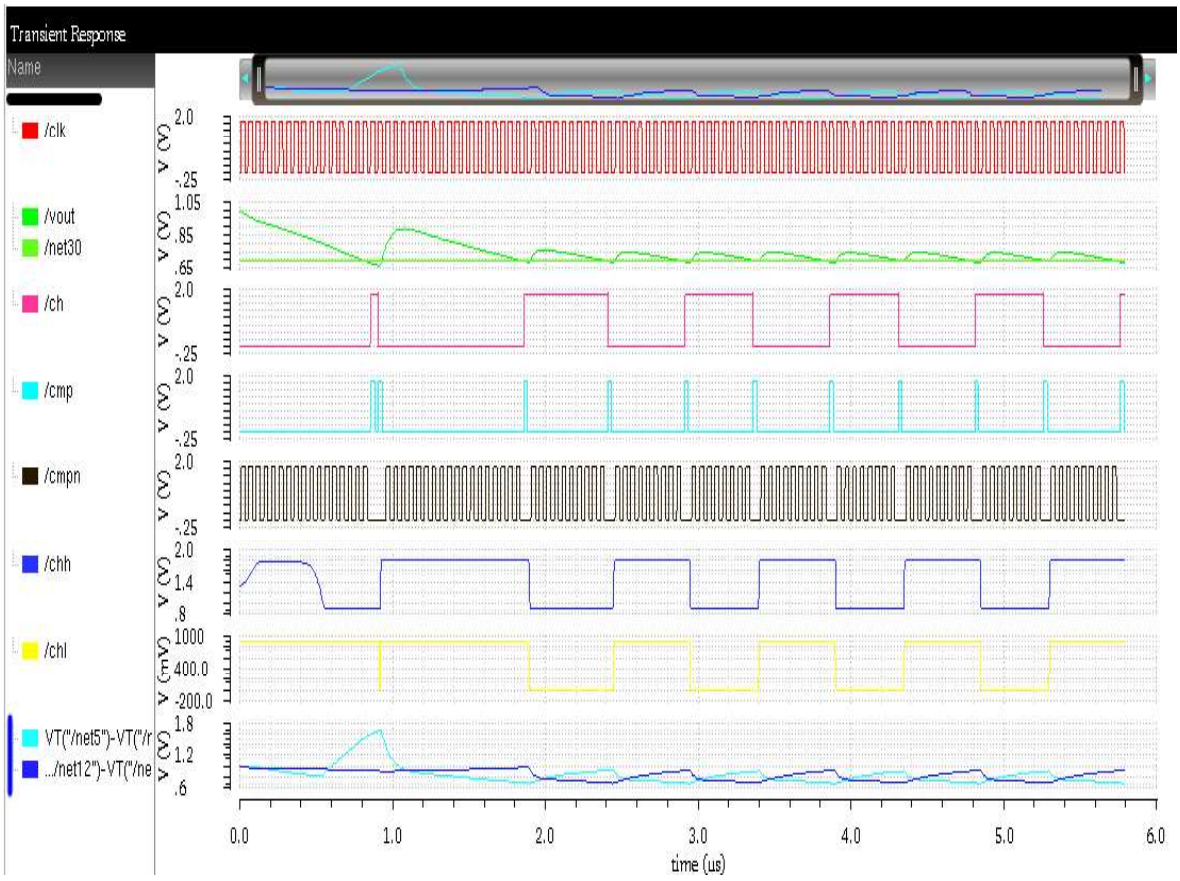


Fig 6.4 represents single boundary hysteretic control by replacing ideal switch with mosfet

The above waveform we replace ideal switch with Mosfet in single boundary hysteretic control method and there is clock signals to the input comparator and output of comparator CMP and CMPN is obtained for vout less than vref Here Vin =2V ,Vout = 0.85V with 0.25 V output ripple , chh and ch1 represent level shifter output signals generated from the level shifter.

6.1)Simulation of Level shifter circuit ,Voltage controlled oscillator and charge pump Integrator

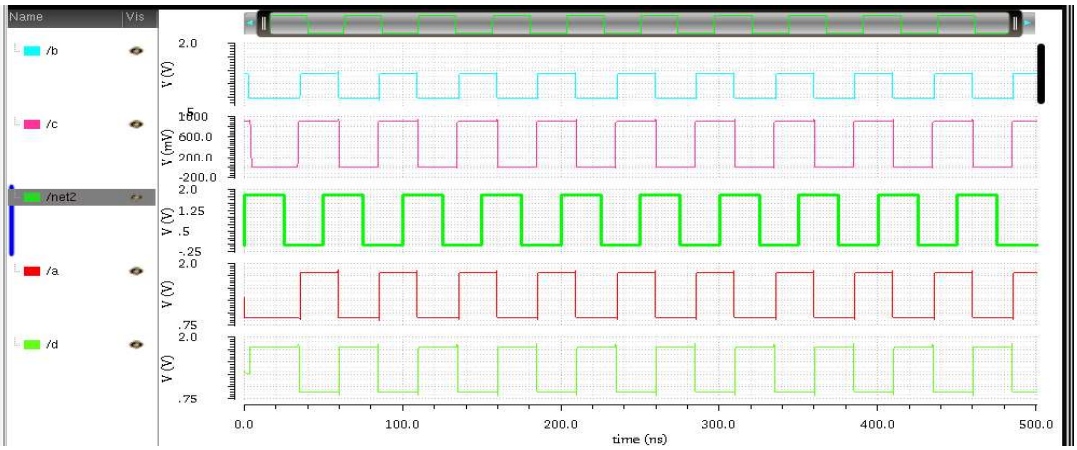


Fig 6.4 represents the waveforms of Level shifter circuit

Above are waveforms obtained the a,d are the level shifted signals(vary from Vout to Vin) b,c vary are low side signals vary from 0 to Vout, net2 is the input clock signal.

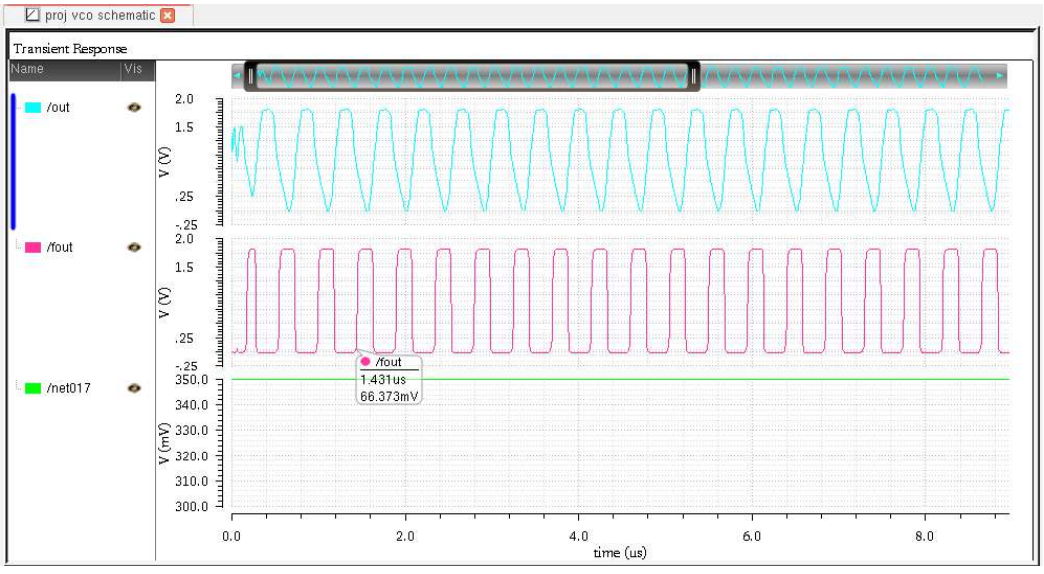


Fig 6.5 represents the waveforms of voltage controlled oscillator

The waveforms in blue show output at net out, pink show waveform at inverter o/p (fout), for a DC input voltage of 350mV a square wave of 0.6us period was obtained as seen.

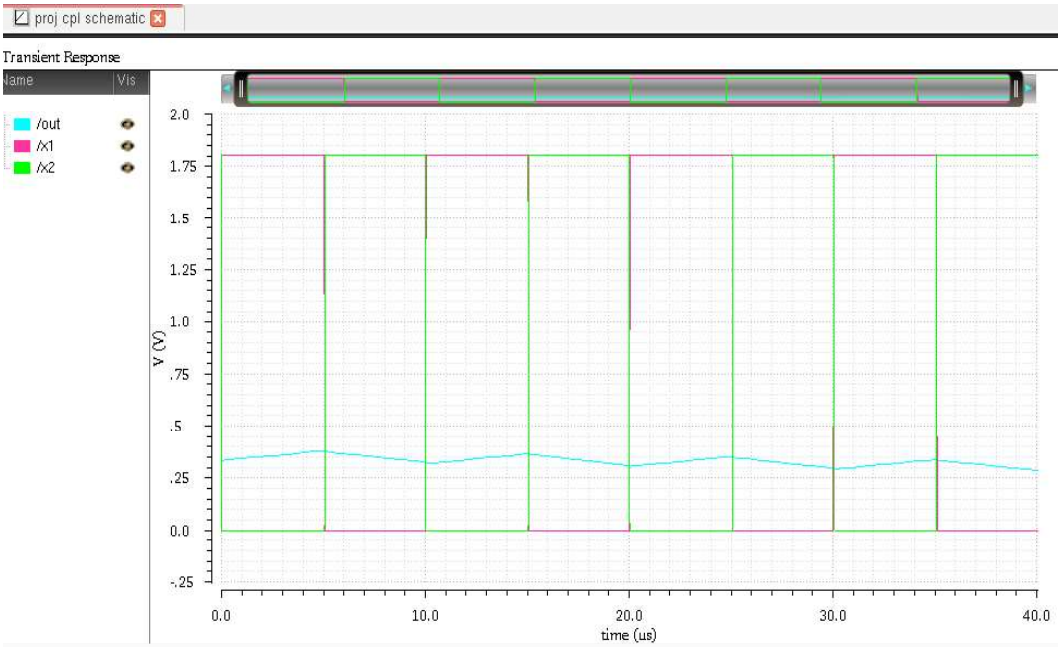


Fig 6.6 represents the waveforms of charge pump circuit

The above is the simulation of charge pump circuit , it is started with an initial condition of 350mV, it is adjusted for voltage change of 10mV/0.1us by the equation I=C(dV/dt) and by choosing C=1uF and setting current source I=10mA.

The below waveforms shows voltage increments/decrements wrt to inc/dec signals having a voltage increments/decrements in steps of 10mV/0.1us.

6.4)Simulation of N-skip counter schematic:

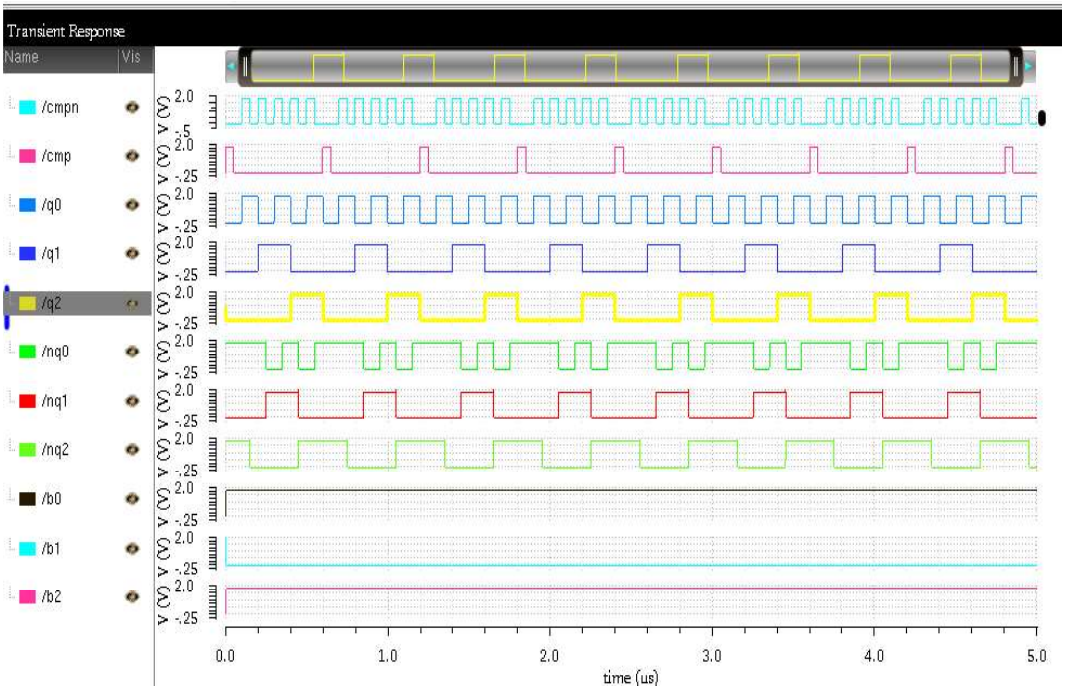


Fig 6.7 represents the waveforms of Nskip counter

The above simulation of Nskip counter schematic shows resulting waveforms, Cmp test signals are applied as above and the q0,q1,q2 counting values are observed, and b0,b1,b2 holds the value 101 indicating 5 cmpn pulses.

6.5)References:

1)Z. Xiao, A. K. Bui and L. Siek, "A Hysteretic Switched-Capacitor DC–DC Converter With Optimal Output Ripple and Fast Transient Response," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 11, pp. 2995-3005, Nov. 2017, doi: 10.1109/TVLSI.2017.2728606.

2)Jiaming Liu, Hao Meng and Degang Chen, "Switched-compensation technique in switched-capacitor circuit for achieving fast settling performance," 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS), Fort Collins, CO, 2015, pp. 1-4, doi: 10.1109/MWSCAS.2015.7282162.

3)T. M. Van Breussegem and M. S. J. Steyaert, "Monolithic Capacitive DC-DC Converter With Single Boundary–Multiphase Control and Voltage Domain Stacking in 90 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 46, no. 7, pp. 1715-1727, July 2011, doi: 10.1109/JSSC.2011.2144350.

4)X. Fu, K. El-Sankary and Y. Yadong, "A Pulse injection background calibration technique for charge pump PLLs," 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 98-101, doi: 10.1109/NEWCAS49341.2020.9159782.

5)B. Kinger, S. Suman, K. G. Sharma and P. K. Ghosh, "Design of Improved Performance Voltage Controlled Ring Oscillator," 2015 Fifth International Conference on Advanced Computing & Communication Technologies, 2015, pp. 441-445, doi: 10.1109/ACCT.2015.127.