Design Project Report

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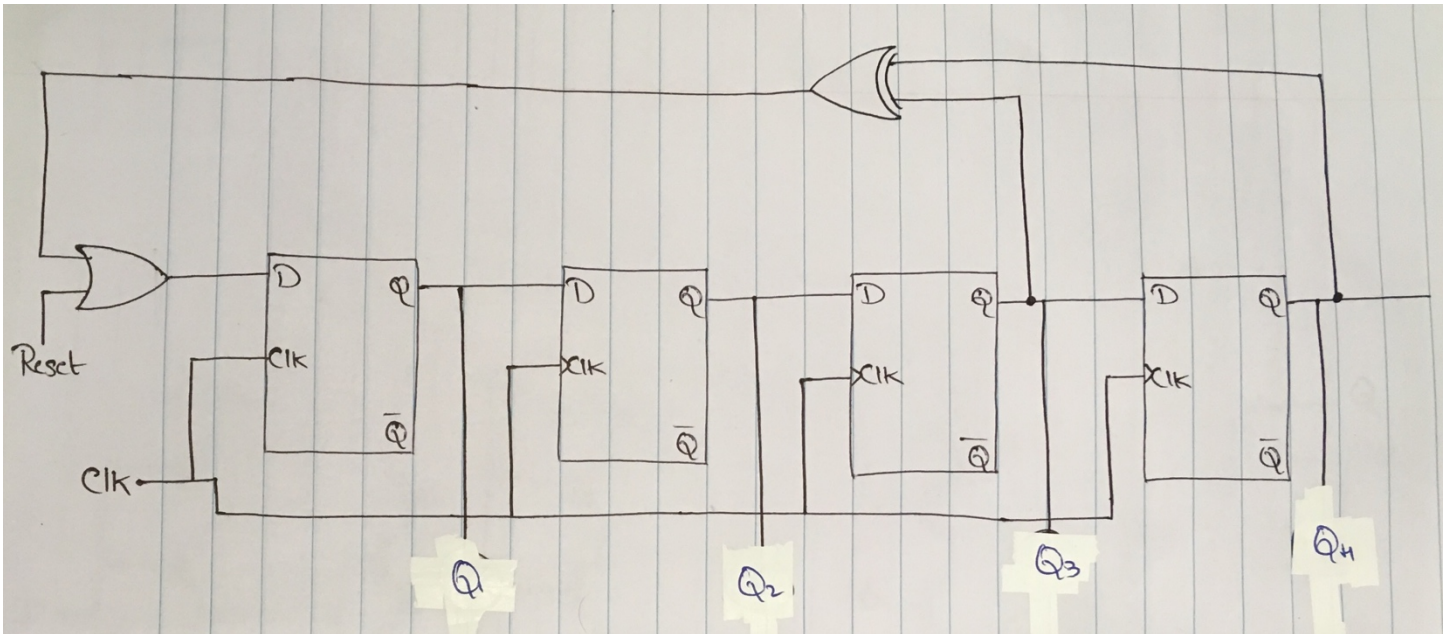
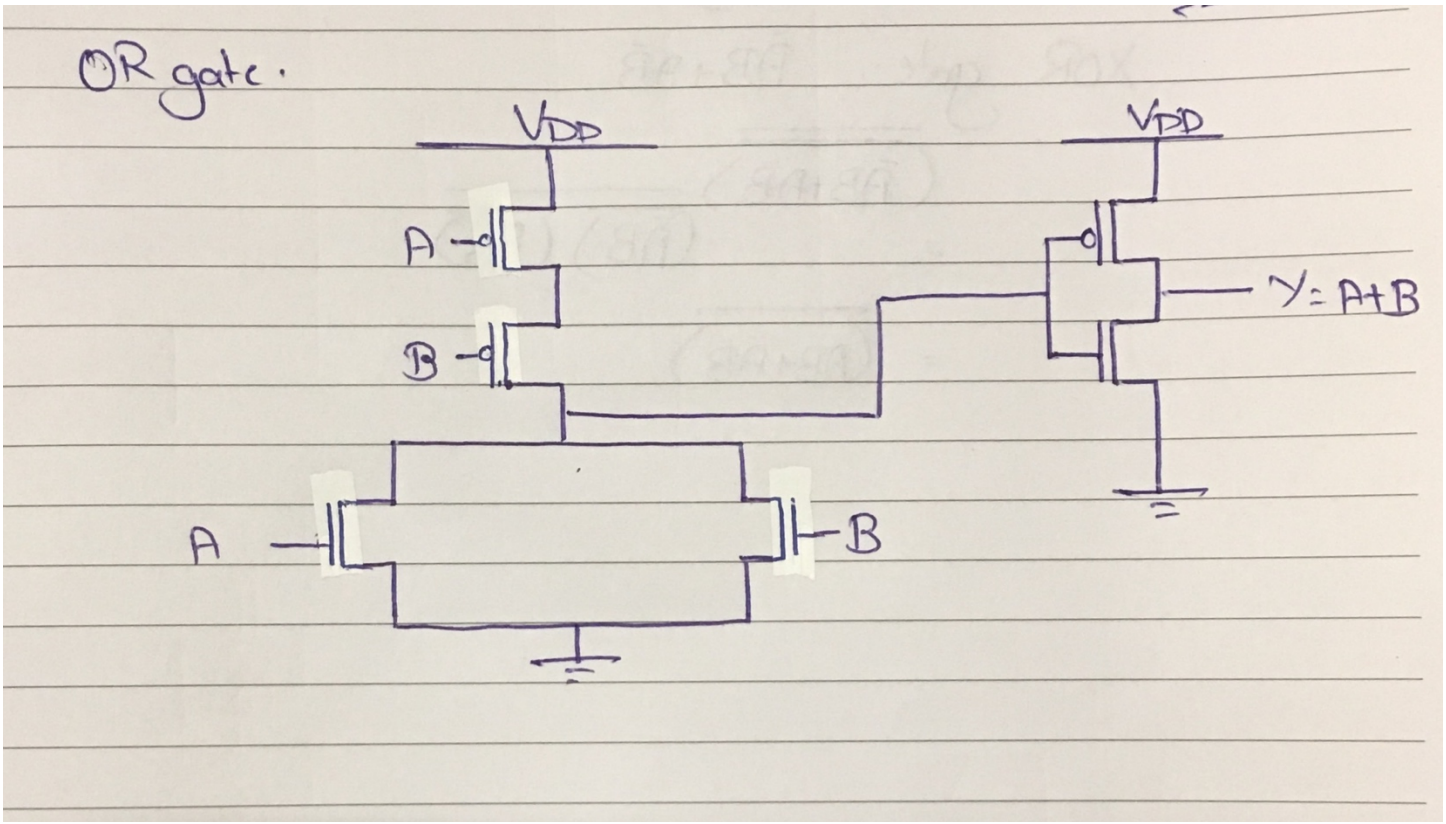
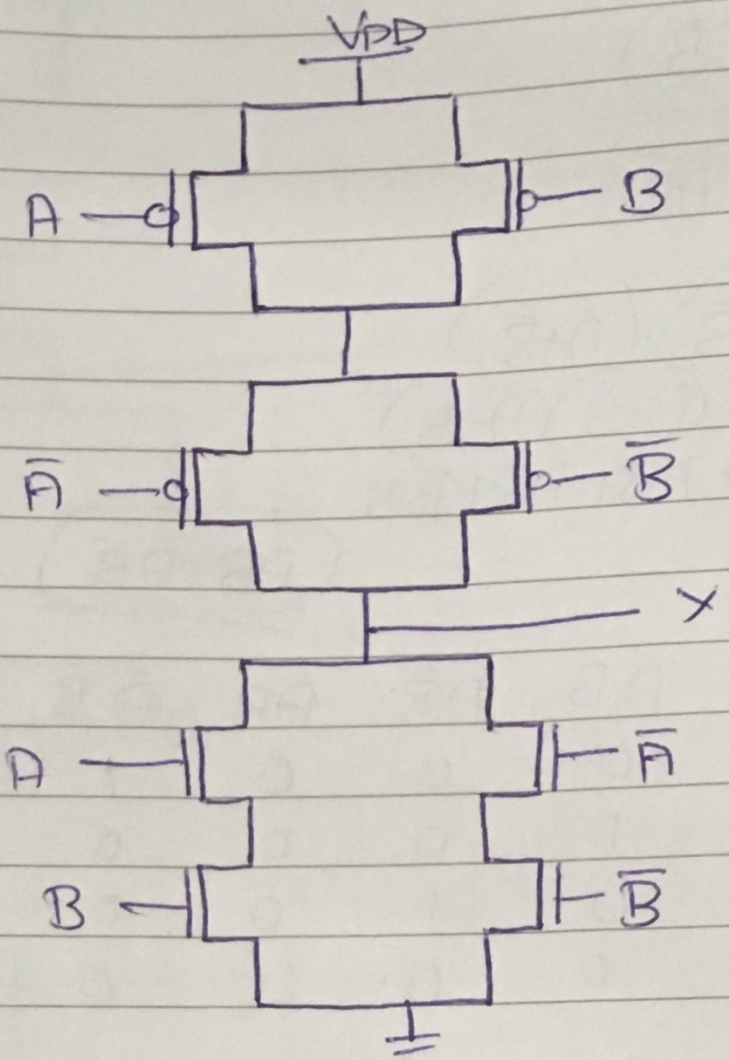


Schematic of a Pseudo Random Noise Generator constructed using D-Flipflops



Transistor Schematic of OR Gate

$\overline{A\bar{B}+\bar{A}B}$

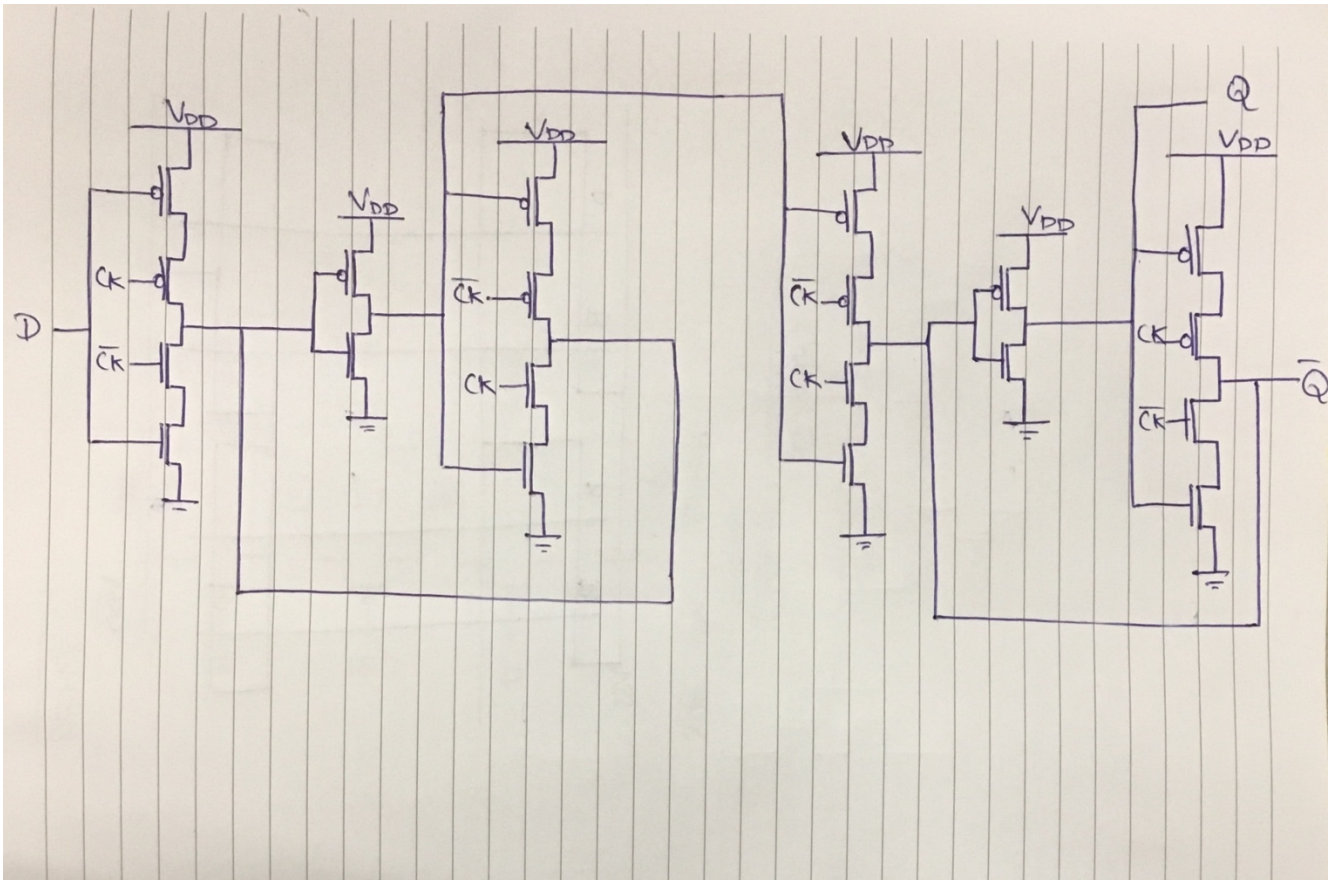


XOR gate: $\bar{A}B+A\bar{B}$

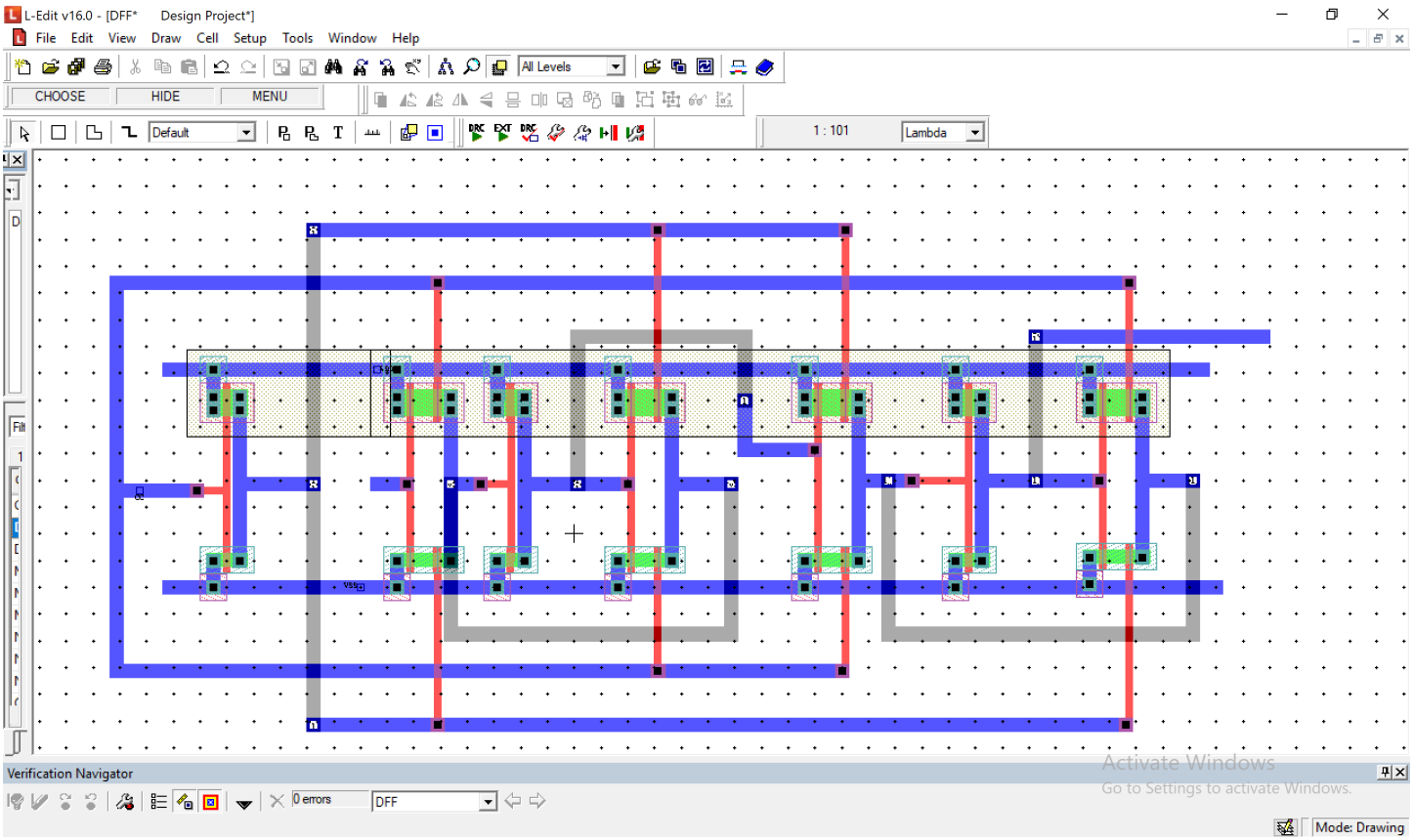
$$\overline{(\bar{A}B+A\bar{B})} = \overline{(\bar{A}B)}\,\overline{(A\bar{B})}$$

$$= \overline{(AB+\bar{A}\bar{B})}$$

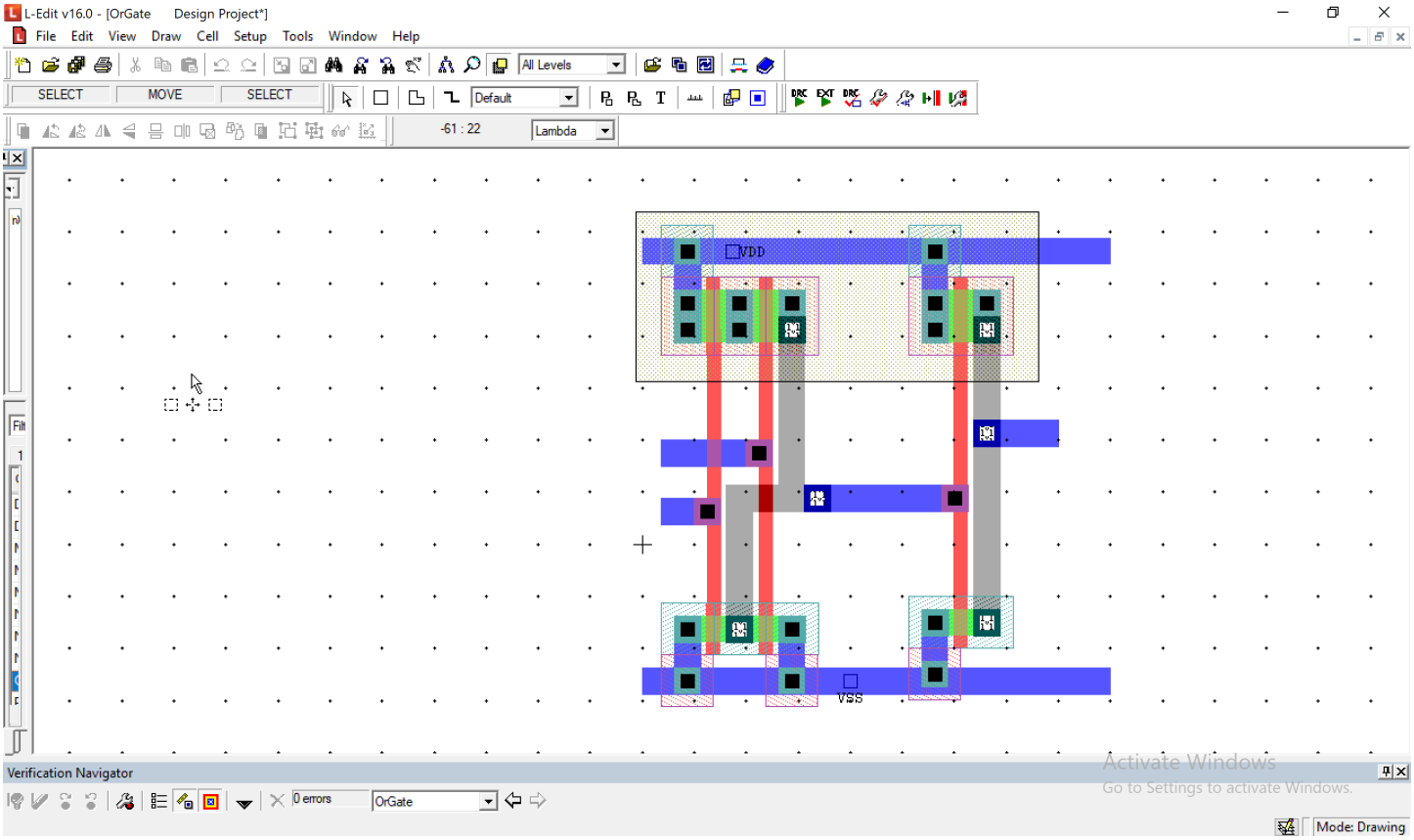
Transistor Schematic of XOR Gate



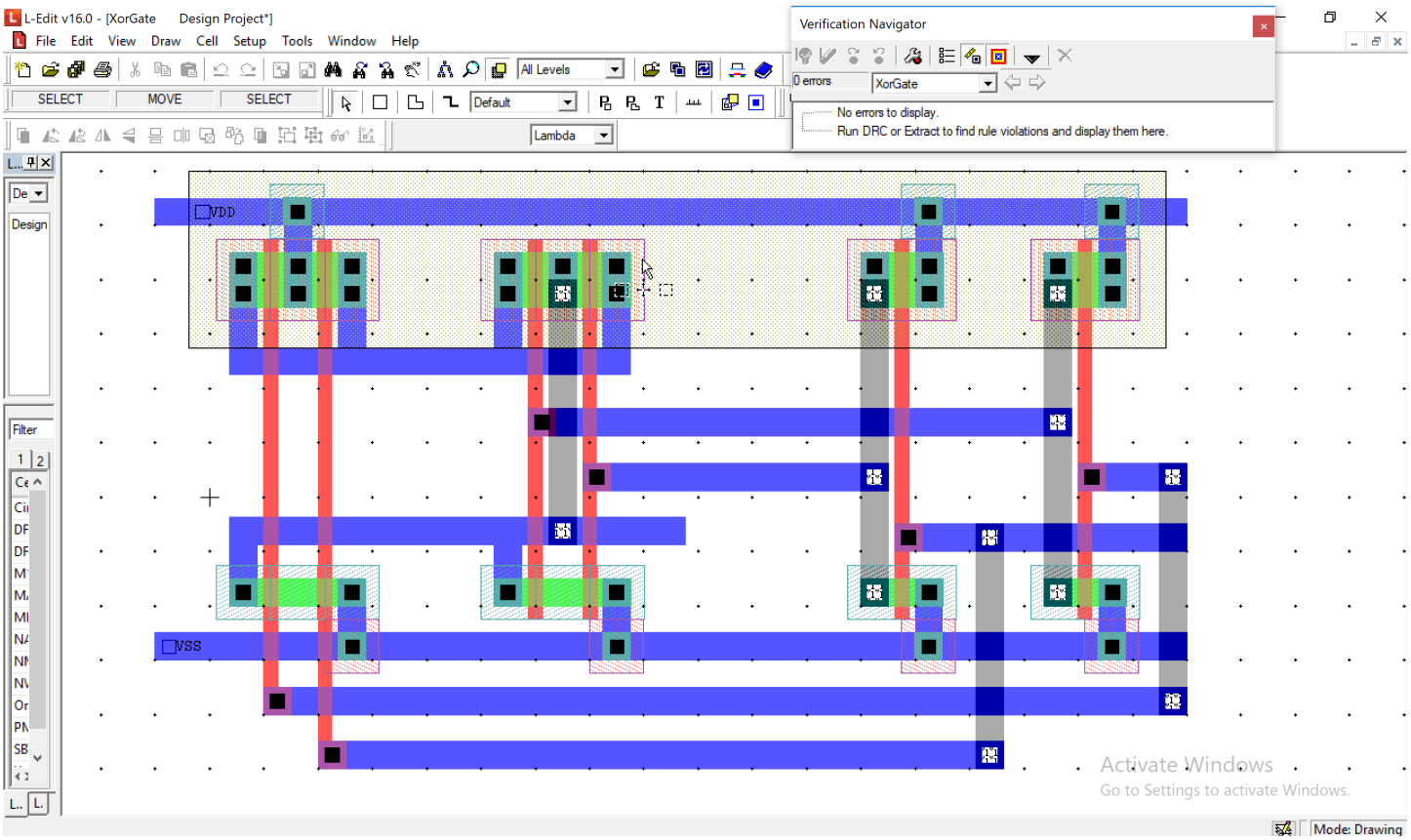
Transistor Schematic of D-Flipflop



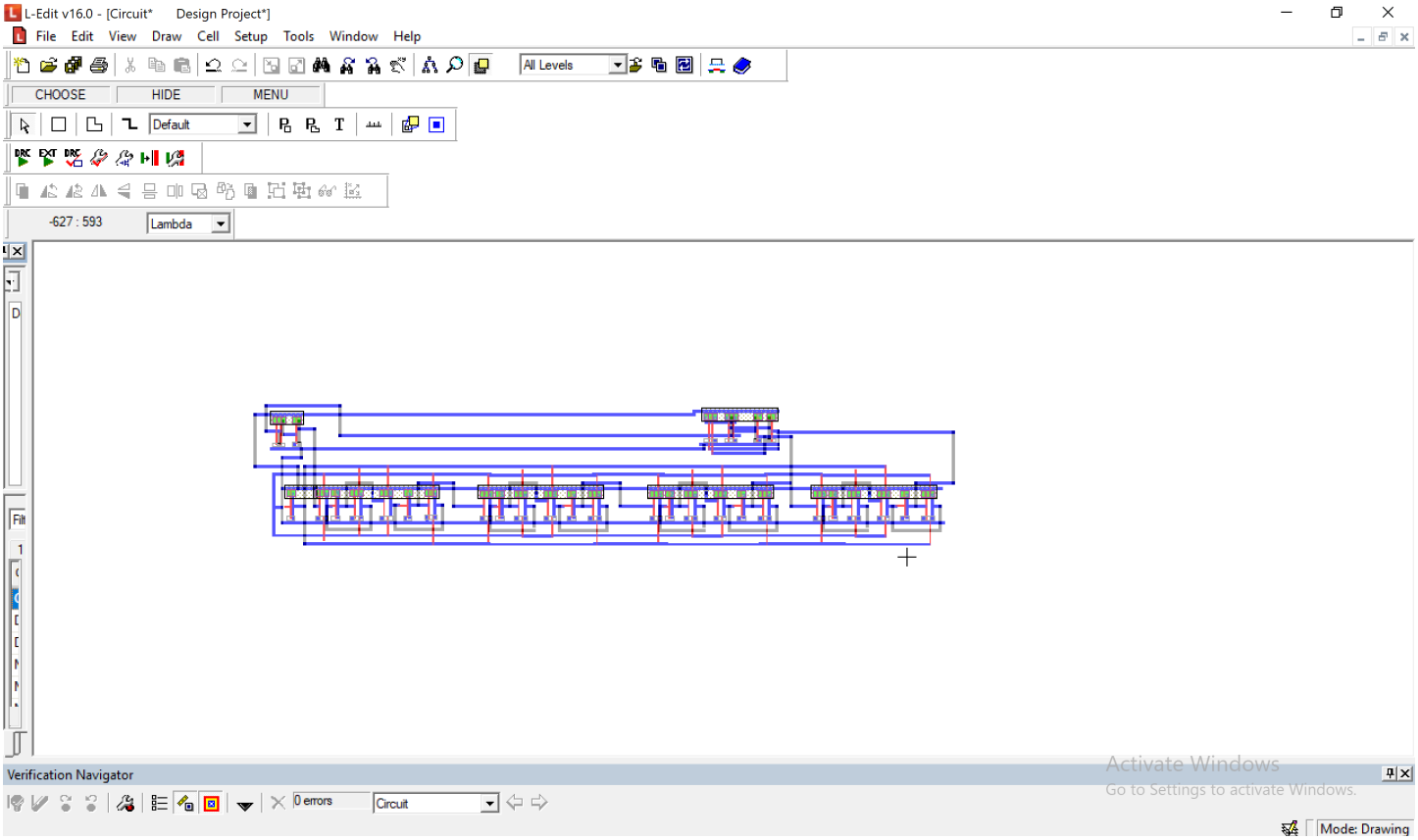
Layout of D-Flipflop after performing DRC



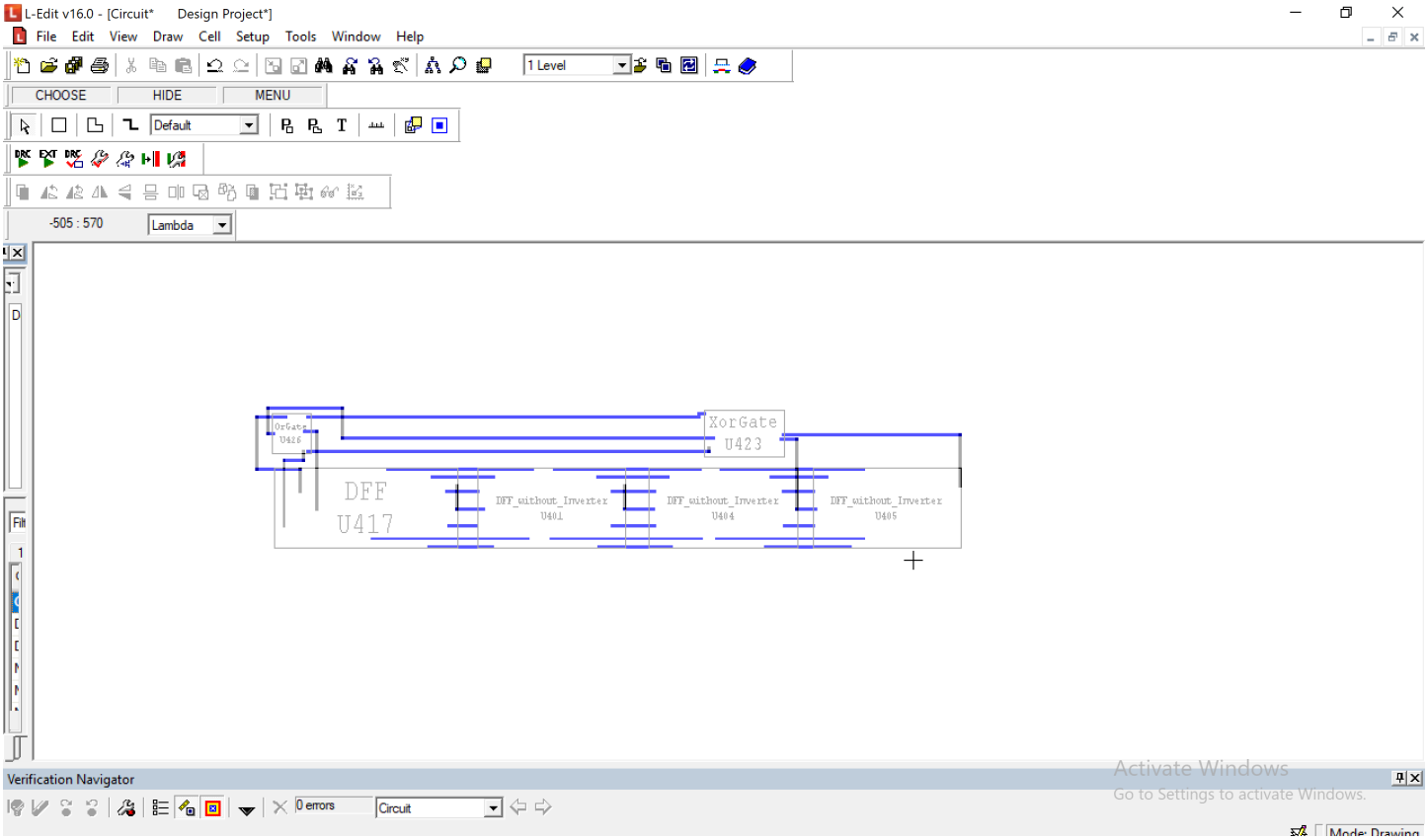
Layout of OR Gate after performing DRC



Layout of XOR Gate after performing DRC

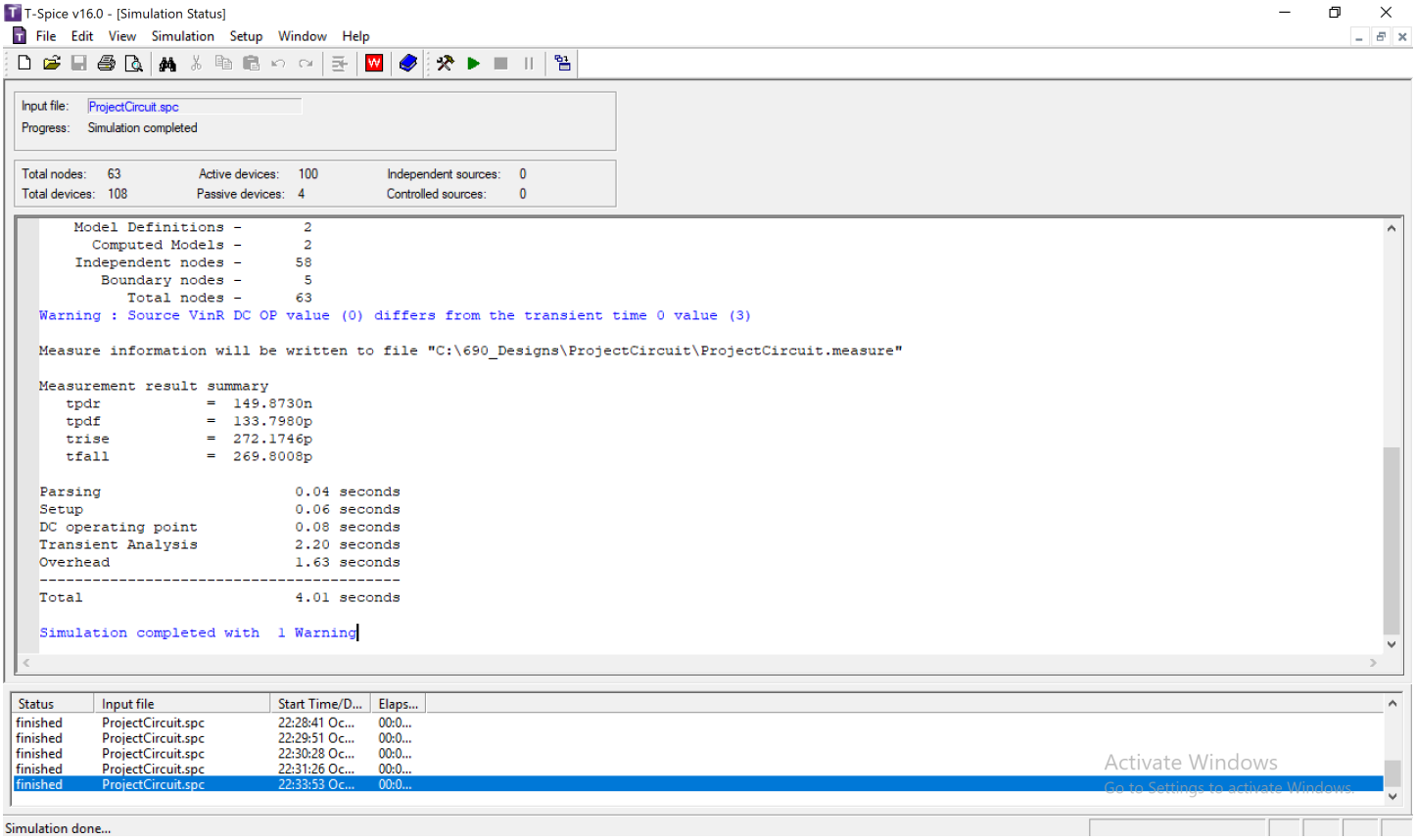


Layout of entire circuit after performing DRC (1)

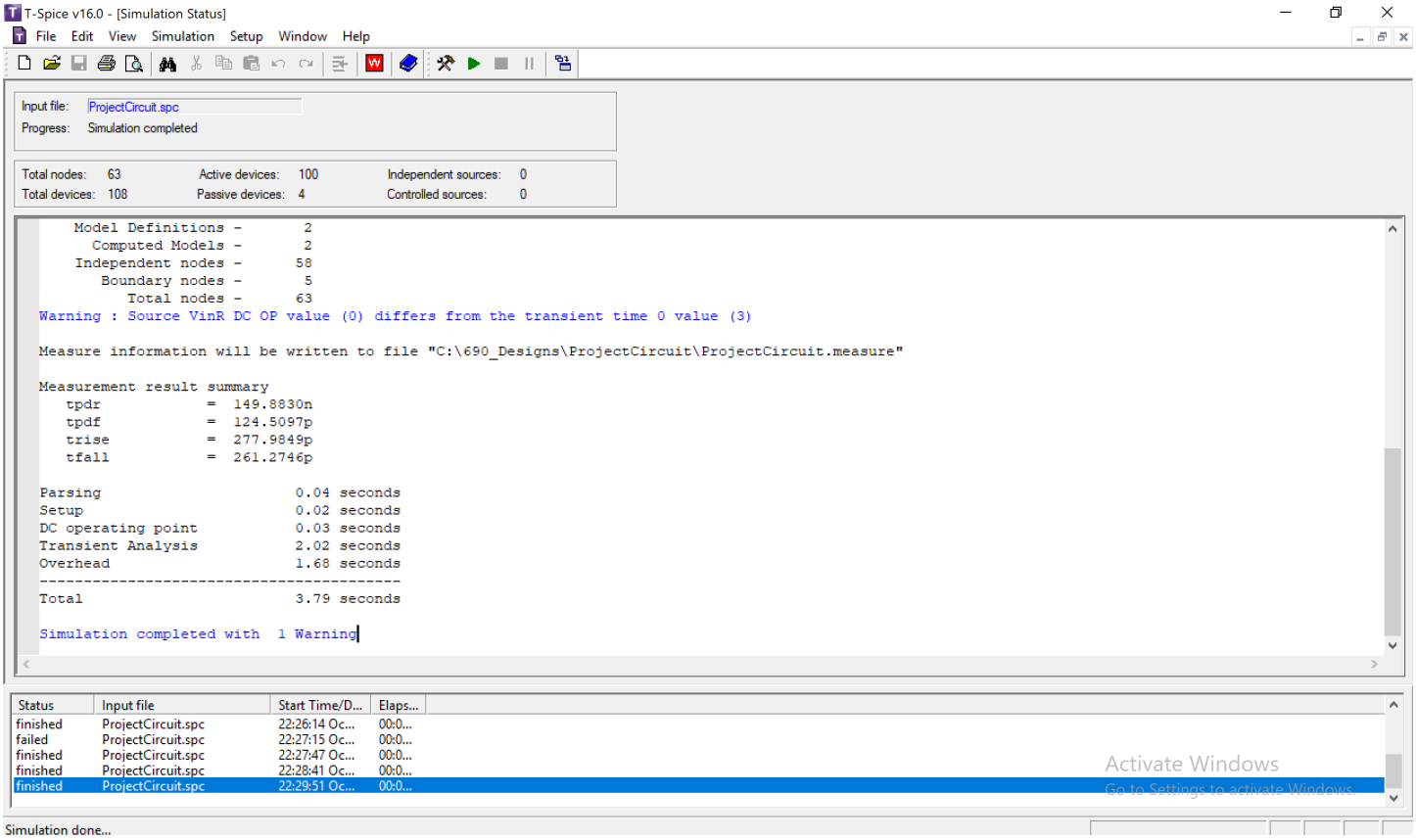


Layout of Circuit after performing DRC (2)

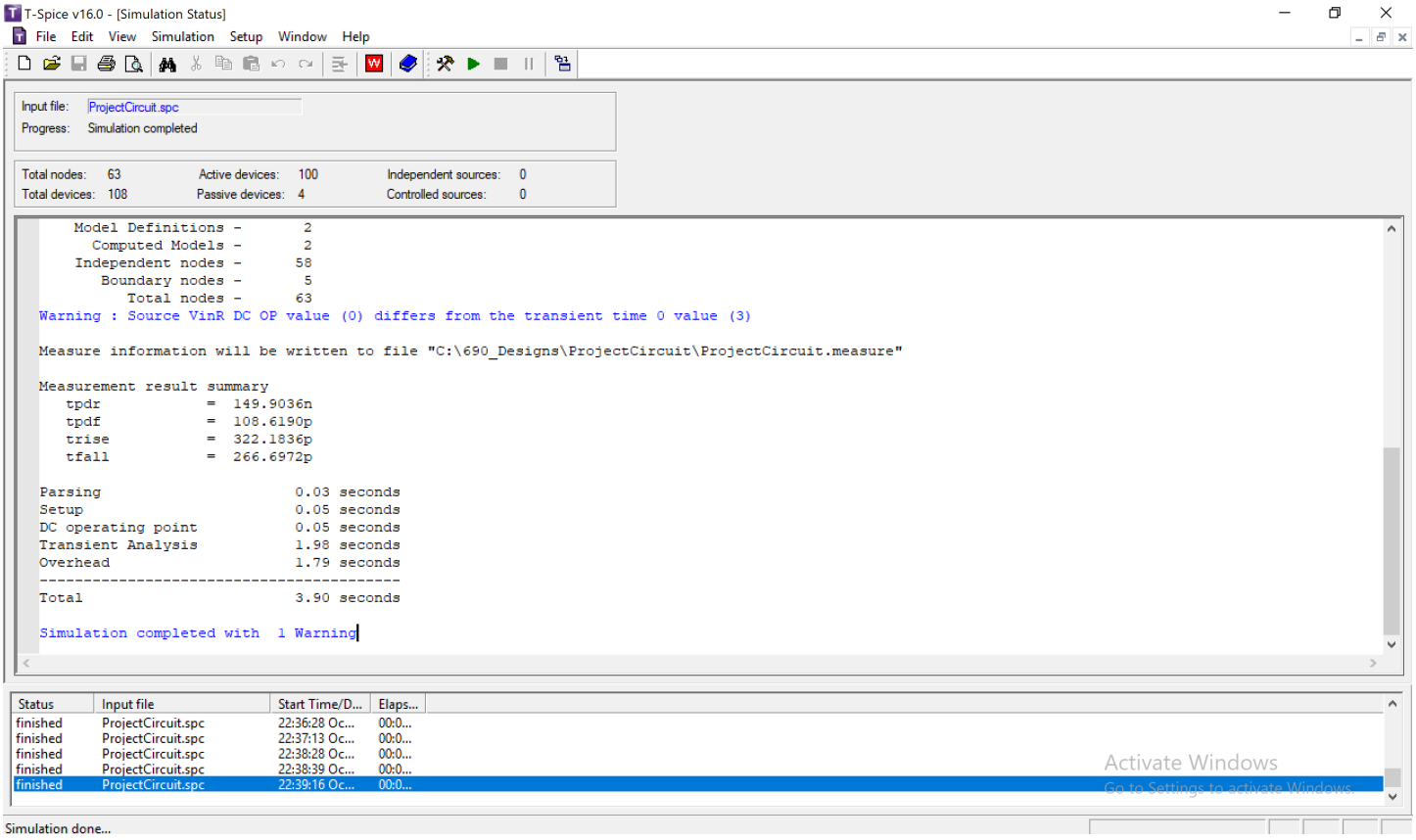
Timing Diagram of the circuit



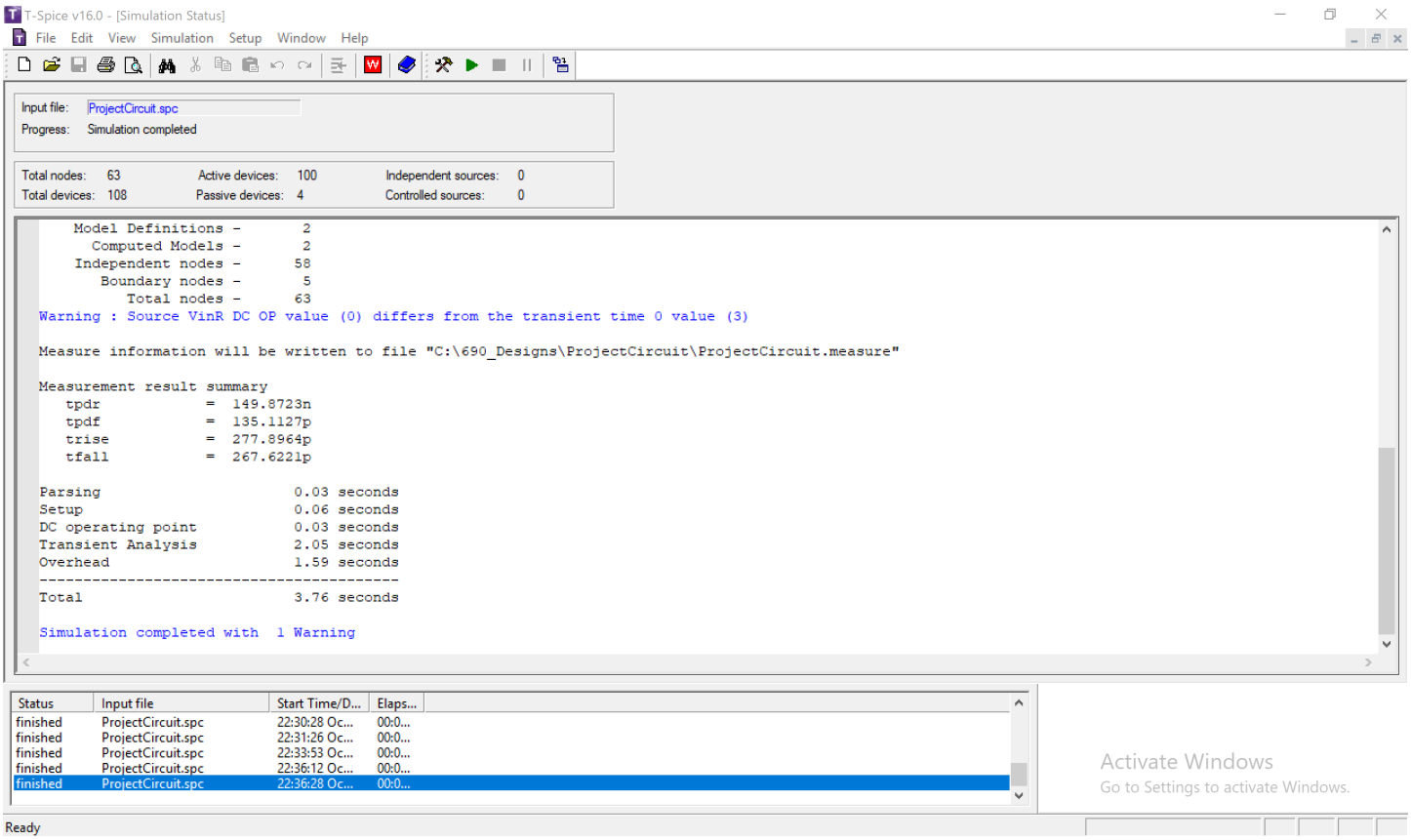
Delay at -25°C and 3.5V



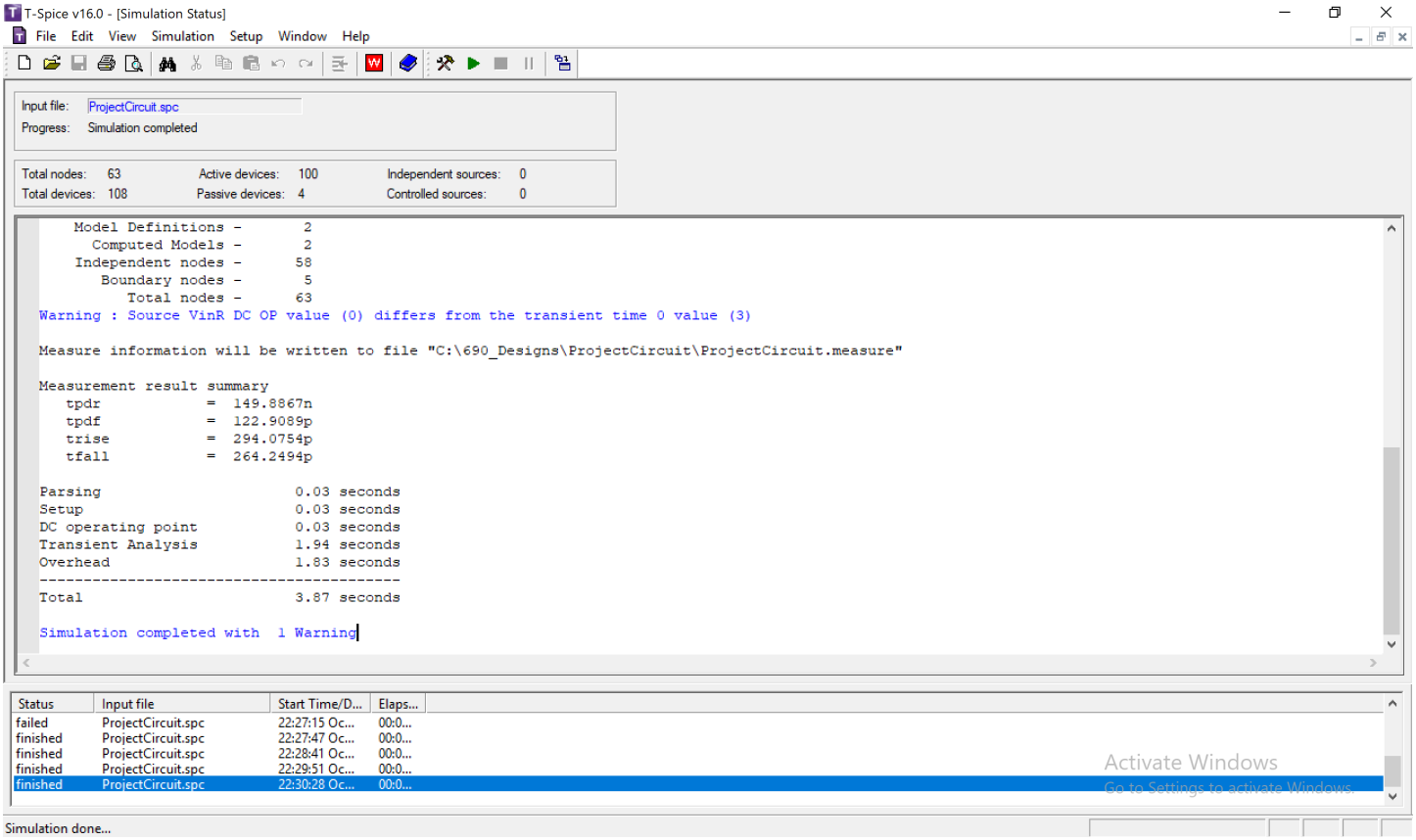
Delay at -25°C and 3V



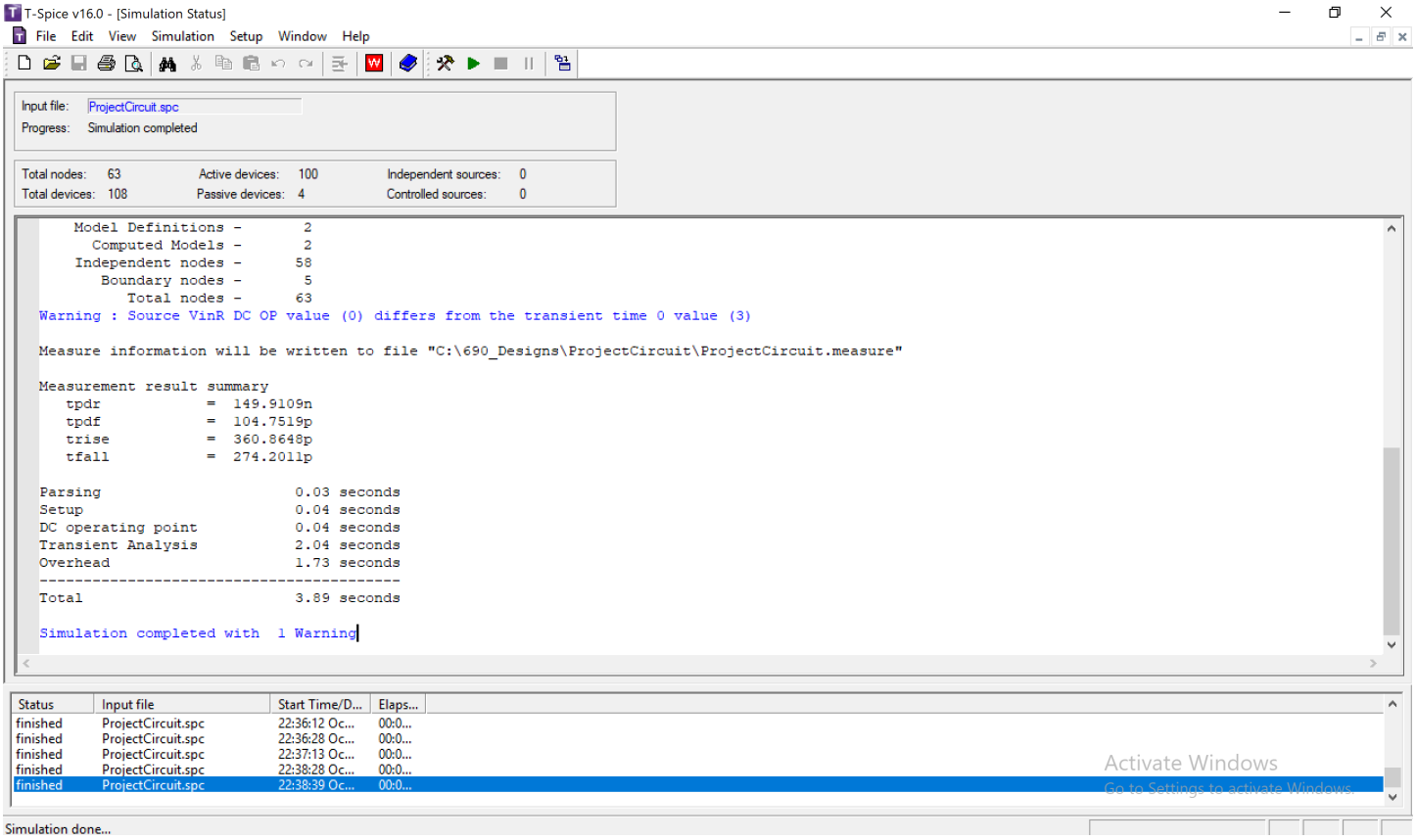
Delay at 25°C and 2.5V



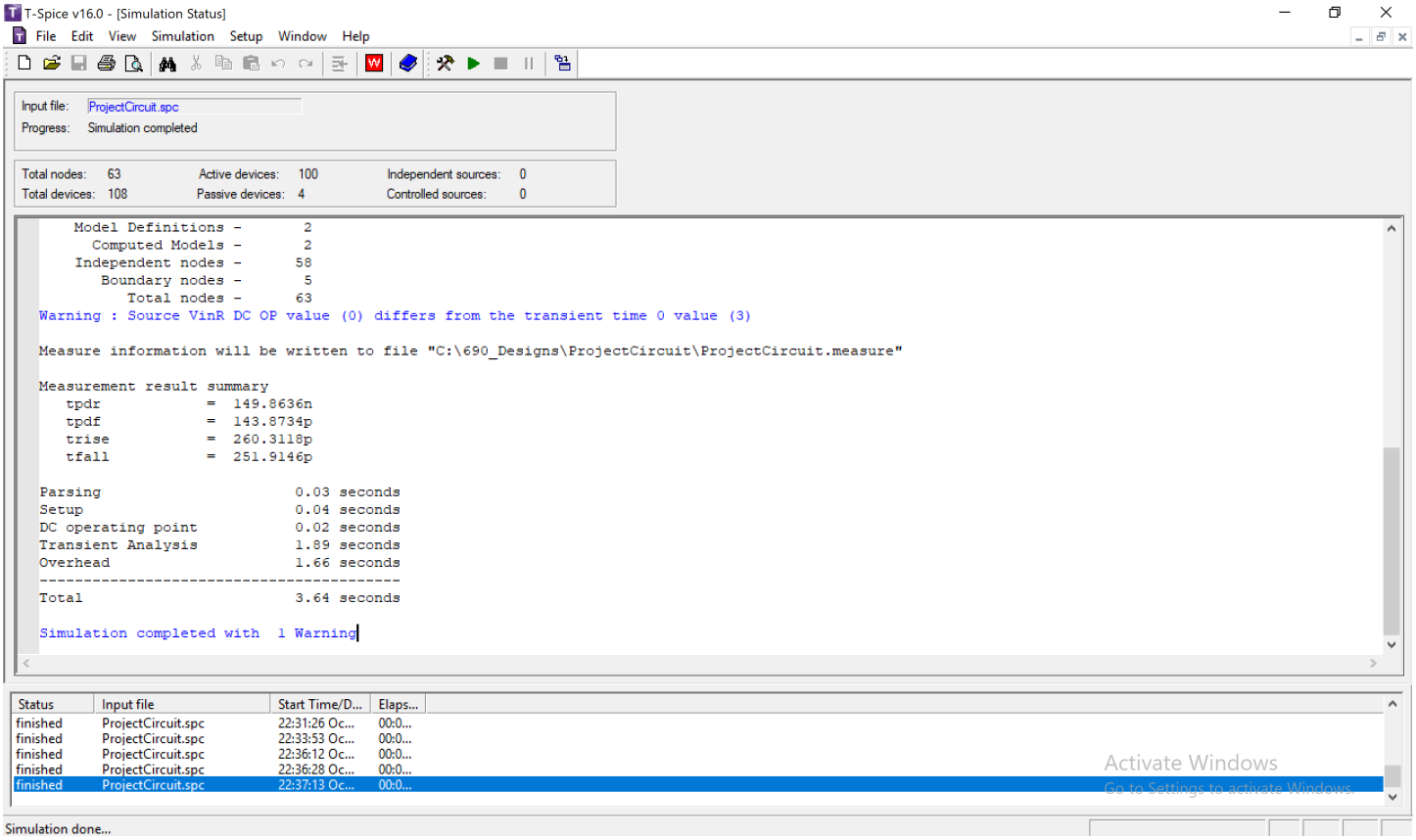
Delay at 25°C and 3.5V



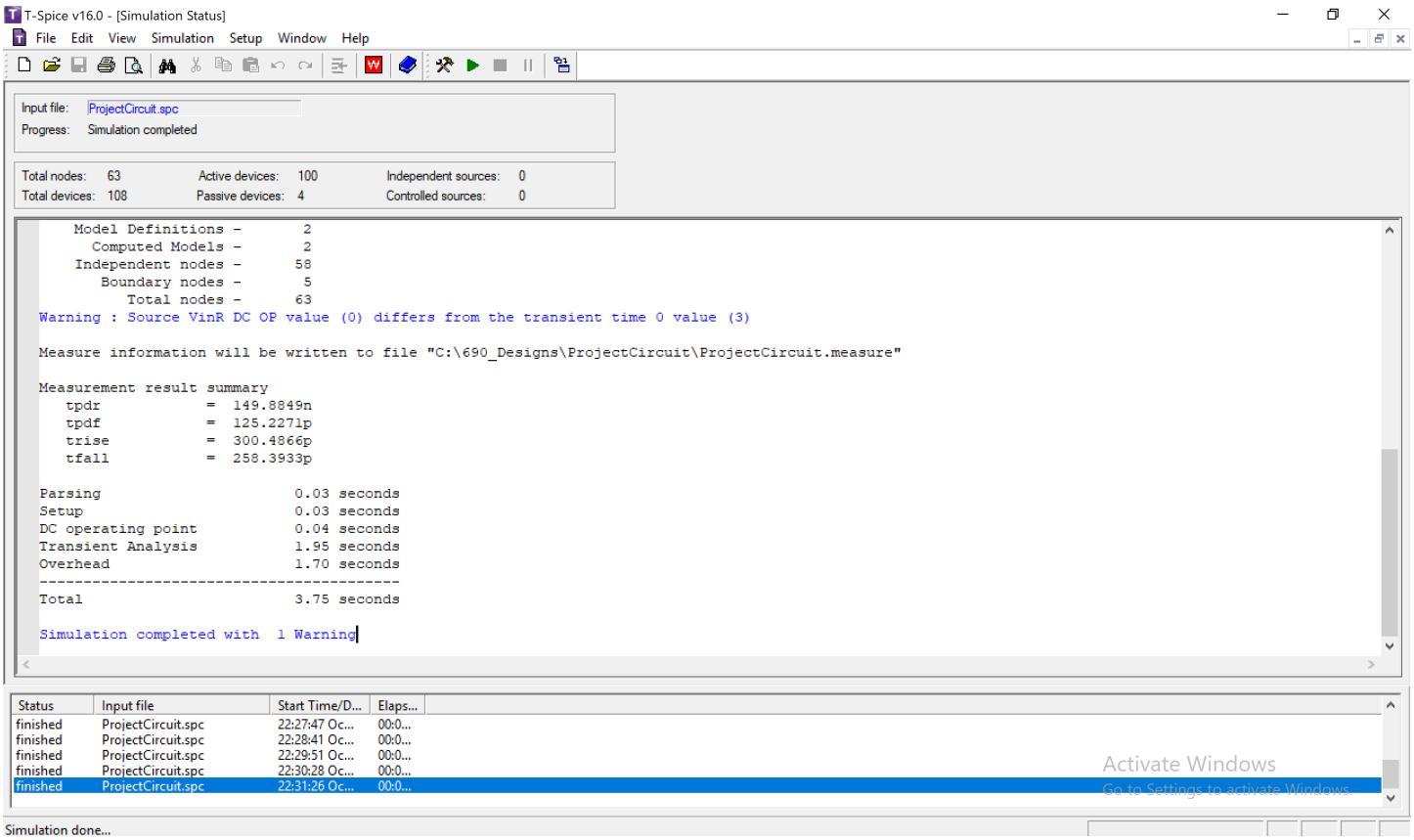
Delay at 25°C and 3V



Delay at 100°C and 2.5V



Delay at 100°C and 3.5V



Delay at 100°C and 3V

I first designed the circuit in a block diagram fashion and broke it down into 3 circuits: 1) D-Flipflop 2) XOR Gate 3) OR Gate. I simulated the individual circuits to check for their proper functioning and did a DRC as I proceeded along. The last step was to cascade all the individual circuits into the Pseudo-Random Noise generator as shown in the first circuit schematic.