Introduction to Digital Design and Computer Architecture

3. Sequential Logic

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Introduction to Sequential Logic

- Sequential logic circuits have memory.
- Outputs depend on:
  - Current input values
  - Prior states of the system
- Key Definitions:
  - **State**: Information necessary to determine future behavior.
  - **State elements**: Latches and flip-flops storing bits of state.
  - **Synchronous circuits**: Combine logic with a bank of flip-flops.

State Elements in Digital Circuits

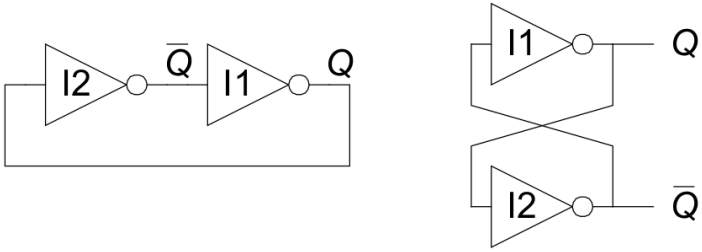
The state of a circuit influences its future behavior

- State elements store state:
  - Bistable circuit
  - SR Latch
  - D Latch
  - D Flip-flop

Bistable Circuit

Fundamental building block of other state elements

- Two outputs: Q, $\bar{Q}$
- No inputs



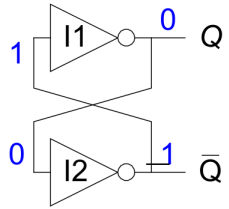
Behavior of a Bistable Circuit

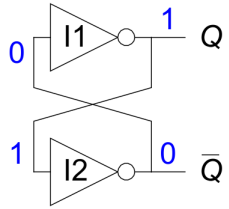
Consider the two possible cases:

- **Q = 0:** then $Q = 1$, $\bar{Q} = 0$ (consistent)
- **Q = 1:** then $Q = 0$, $\bar{Q} = 1$ (consistent)

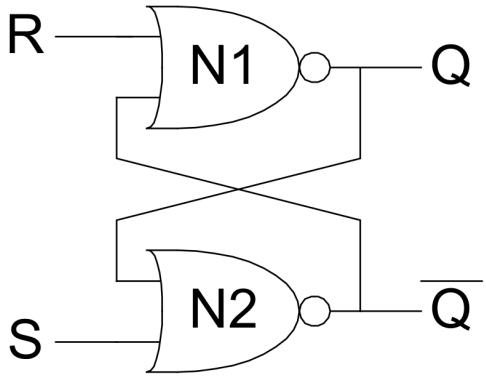
Stores 1 bit of state in the state variable, Q (or $\bar{Q}$)

But there are no inputs to control the state.



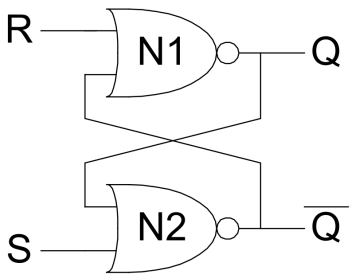


SR (Set/Reset) Latch



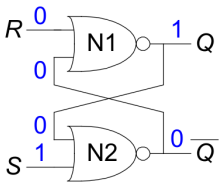
SR (Set/Reset) Latch

- **SR Latch**
- Consider the four possible cases:
  - $S = 1, R = 0$
  - $S = 0, R = 1$
  - $S = 0, R = 0$
  - $S = 1, R = 1$

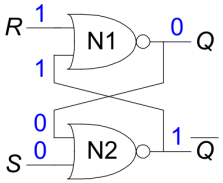


SR Latch Analysis

- $S = 1, R = 0$:
  then $Q = 1$ and $\bar{Q} = 0$



- $S = 0, R = 1$:
  then $Q = 0$ and $\bar{Q} = 1$



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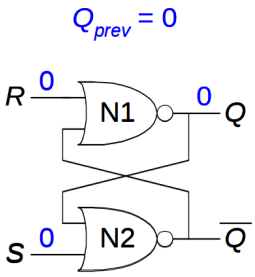

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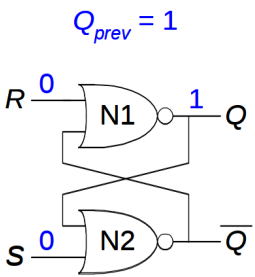

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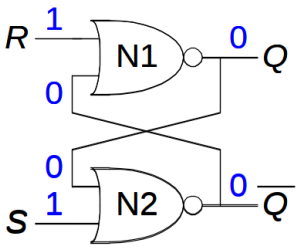


SR Latch Analysis

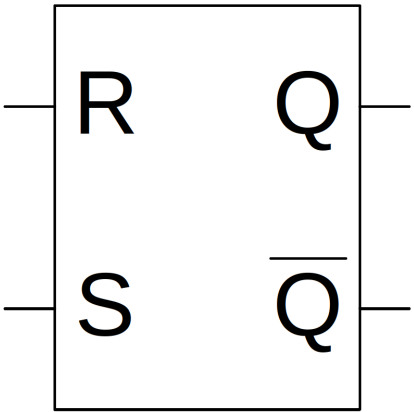
- $S = 1, R = 0$:
  then $Q = 1$ and $\overline{Q} = 0$
- Memory!:

- $S = 0, R = 1$:
  then $Q = 0$ and $\overline{Q} = 1$
- Invalid State:

SR Latch Symbol

- **SR** stands for *Set/Reset Latch*:
  - Stores one bit of state (Q).
- **Control what value is being stored with S, R inputs:**
  - Set: Make the output 1
    ($S = 1, R = 0, Q = 1$)
  - Reset: Make the output 0
    ($S = 0, R = 1, Q = 0$)

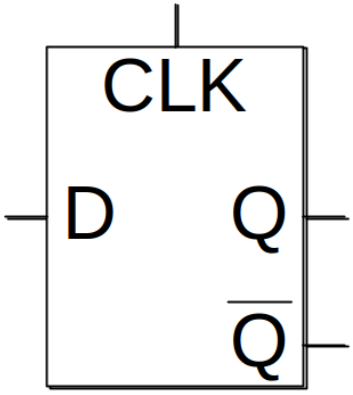
Must do something to avoid invalid states!



SR Latch Invalid States

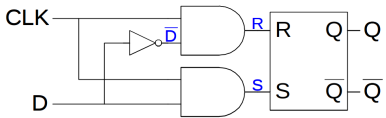
- **Invalid State:**
  - Occurs when $S = 1, R = 1$.
  - This leads to both $Q = 0$ and $\bar{Q} = 0$, violating the fundamental rule that $\bar{Q} \neq Q$.
- **Solution:**
  - Avoid $S = 1$ and $R = 1$ inputs in practical implementations.
  - Use additional circuitry (e.g., clocked latches or flip-flops) to handle edge cases.

Always ensure $S = 0$ or $R = 0$ to maintain valid states.



D Latch Internal Circuit

- The D Latch stores data based on the input D and the clock CLK.
- When CLK $= 1$:
  - If $D = 0$, $Q = 0$, $\bar{Q} = 1$.
  - If $D = 1$, $Q = 1$, $\bar{Q} = 0$.
- When CLK $= 0$, the output remains unchanged (previous state is held).



CLK	D	$\bar{D}$	S	R	Q
0	X				
1	0				
1	1				

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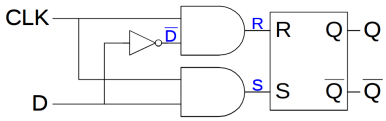
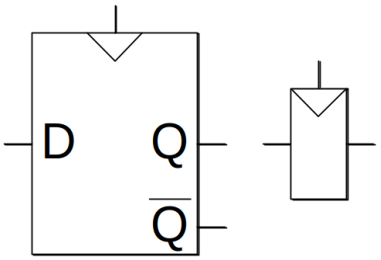


CLK	D	$\bar{D}$	S	R	Q
0	X	$\bar{x}$	0	0	Q_{prev}
1	0	1	0	1	0
1	1	0	1	0	1

D Flip-Flop

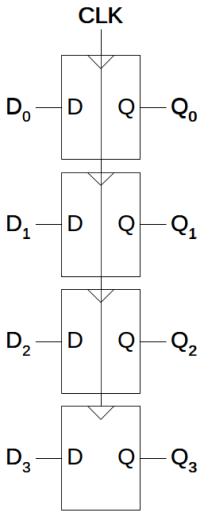
Inputs: *CLK*, *D*

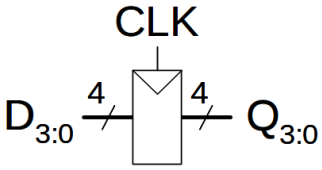
- **Function:**
  - Samples *D* on the **rising edge** of CLK.
  - When CLK rises from 0 to 1:
    - *D* passes through to *Q*.
  - Otherwise, *Q* holds its **previous value**.
  - *Q* changes **only** on the rising edge of CLK.
- Called **edge-triggered**.
- Activated on the clock edge.



Flip-Flop Symbols

Registers



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