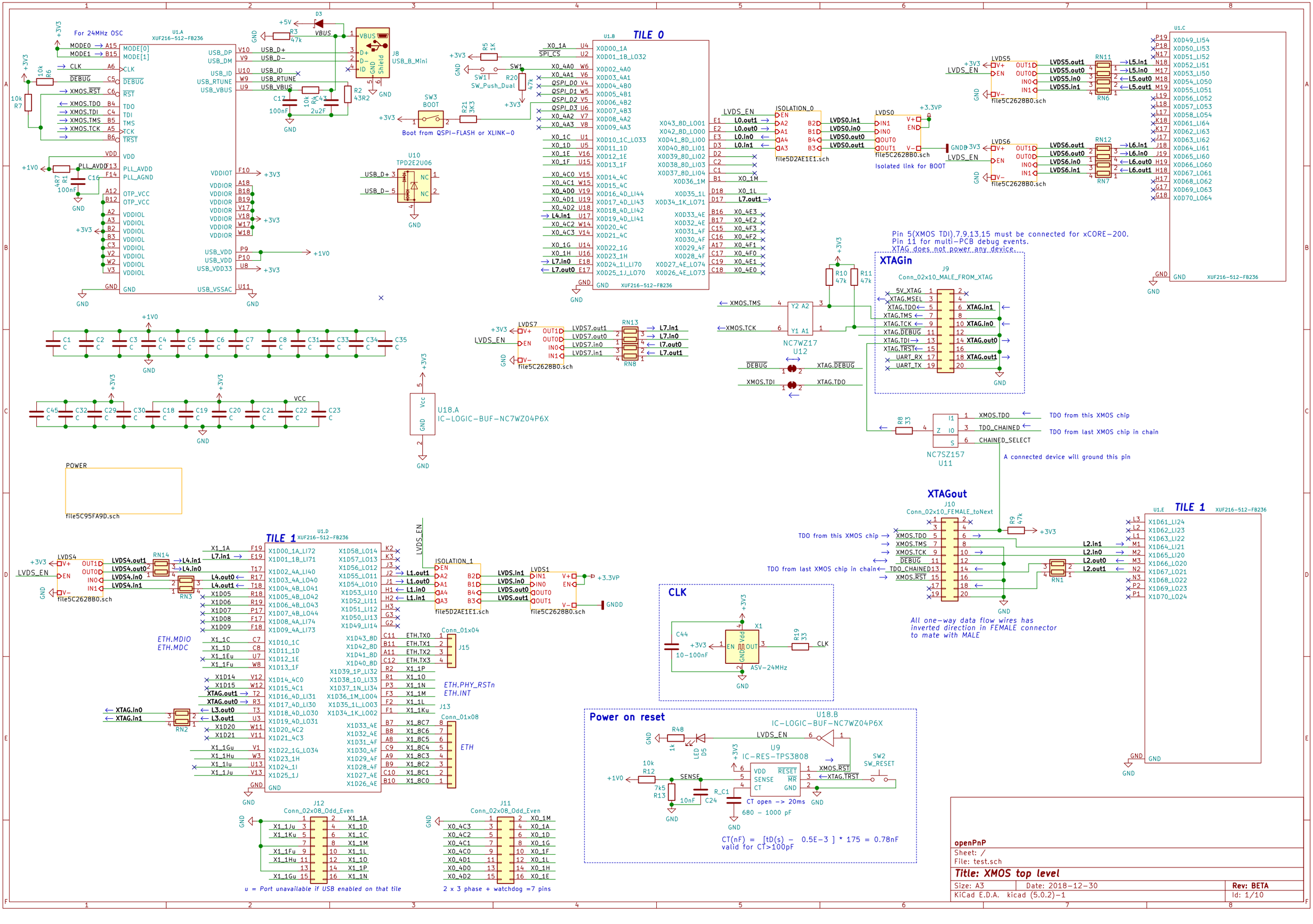
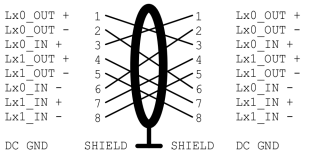
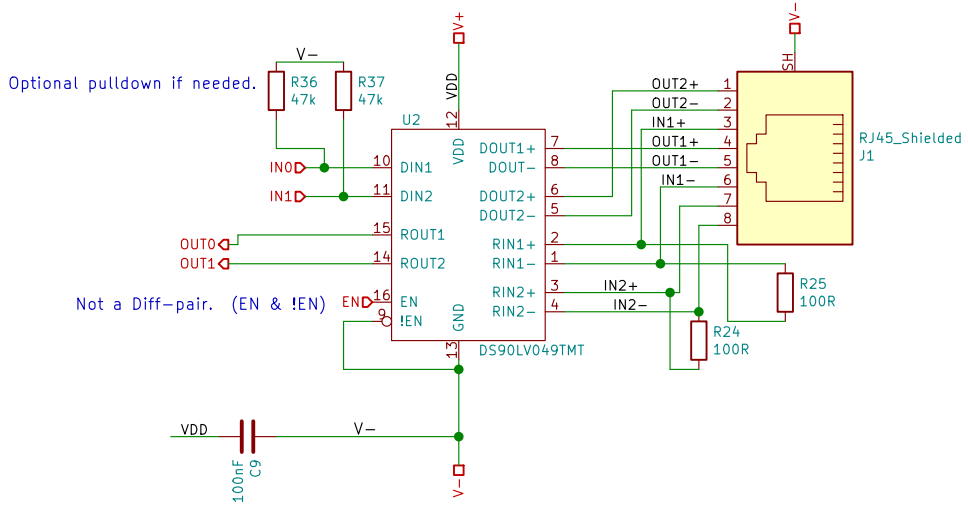

TILE 0
U1.A
XUF216-512-FB236
For 24MHz OSC
MODE0
MODE1
CLK
DEBUG
XMOS.RST
XMOS.TDO
XMOS.TDI
XMOS.TMS
XMOS.TCK
PLL_AVDD
PLL_AGND
OTP_VCC
VDDIOL
VDDIOT
VDDIOR
USB_DP
USB_DM
USB_ID
USB_RTUNE
USB_VBUS
USB_VDD
USB_VDD33
USB_VSSAC
USB_D+
USB_D-
J8
USB_B_Mini
D3
SW1
SW_Push_Dual
SW3
BOOT
Boot from QSPI-FLASH or XLINK-0
U10
TPD2E2U06
U1.B
LVDS_EN
ISOLATION_0
file5D2AE1E1.sch
LVDS0
file5C2628B0.sch
Isolated link for BOOT
U1.C
LVDS5
LVDS6
RN11
RN12
RN6
RN7
Pin 5(XMOS TDI),7,9,13,15 must be connected for xCORE-200.
Pin 11 for multi-PCB debug events.
XTAG does not power any device.
XTAGin
J9
Conn_02x10_MALE_FROM_XTAG
NC7WZ17
U12
U18.A
IC-LOGIC-BUF-NC7WZ04P6X
LVDS7
RN13
RN8
XTAGout
J10
Conn_02x10_FEMALE_toNext
TDO from this XMOS chip
TDO from last XMOS chip in chain
All one-way data flow wires has
inverted direction in FEMALE connector
to mate with MALE
NC7SZ157
U11
TDO from this XMOS chip
TDO_CHAINED
TDO from last XMOS chip in chain
CHAINED_SELECT
A connected device will ground this pin
POWER
file5C95FA9D.sch
TILE 1
U1.D
XUF216-512-FB236
LVDS4
RN14
RN3
ISOLATION_1
file5D2AE1E1.sch
LVDS1
file5C2628B0.sch
ETH.MDIO
ETH.MDC
ETH.PHY_RSTn
ETH.INT
ETH
J15
J13
Conn_01x04
Conn_01x08
XTAG.in0
XTAG.in1
XTAG.out0
XTAG.out1
RN2
CLK
ASV-24MHz
Power on reset
U18.B
IC-LOGIC-BUF-NC7WZ04P6X
U9
IC-RES-TPS3808
SW2
SW_RESET
CT open -> 20ms
680 - 1000 pF
CT(nF) = [tD(s) - 0.5E-3] * 175 = 0.78nF
valid for CT>100pF
J12
Conn_02x08_Odd_Even
u = Port unavailable if USB enabled on that tile
J11
2 x 3 phase + watchdog =7 pins
TILE 1
U1.E
XUF216-512-FB236
openPnP
Sheet: /
File: test.sch
Title: XMOS top level
Size: A3
Date: 2018-12-30
Rev: BETA
KiCad E.D.A. kicad (5.0.2)-1
Id: 1/10

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

openPnP		
Sheet: /LVDS0/		
File: file5C2628B0.sch		
Title: LVDS <-> Xlinks		
Size: A4	Date: 2018-12-30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 2/10

RJ45 PINOUT:

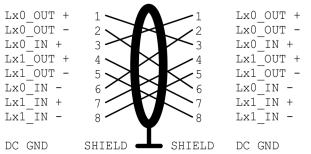
1/2 Lx0_OUT +/-

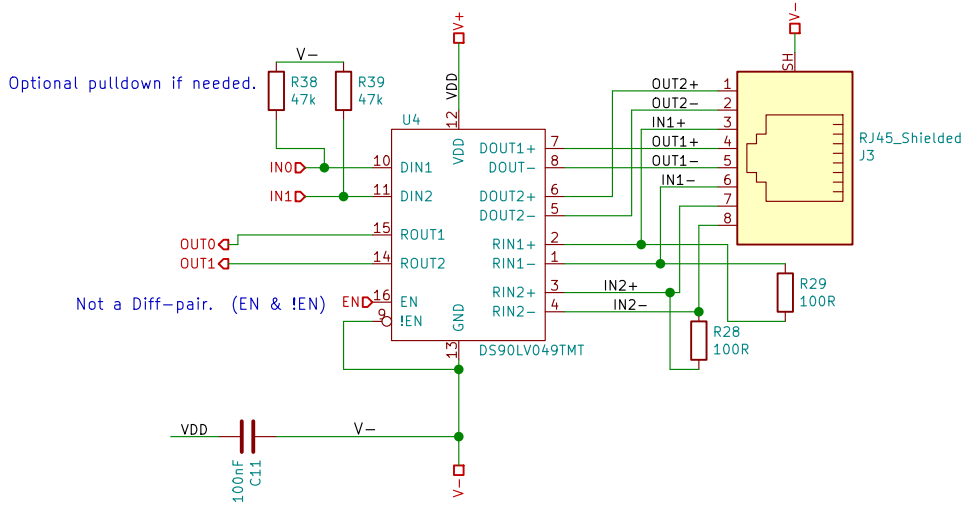
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

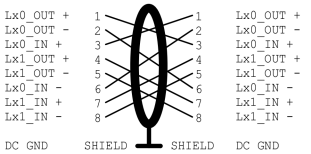
This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

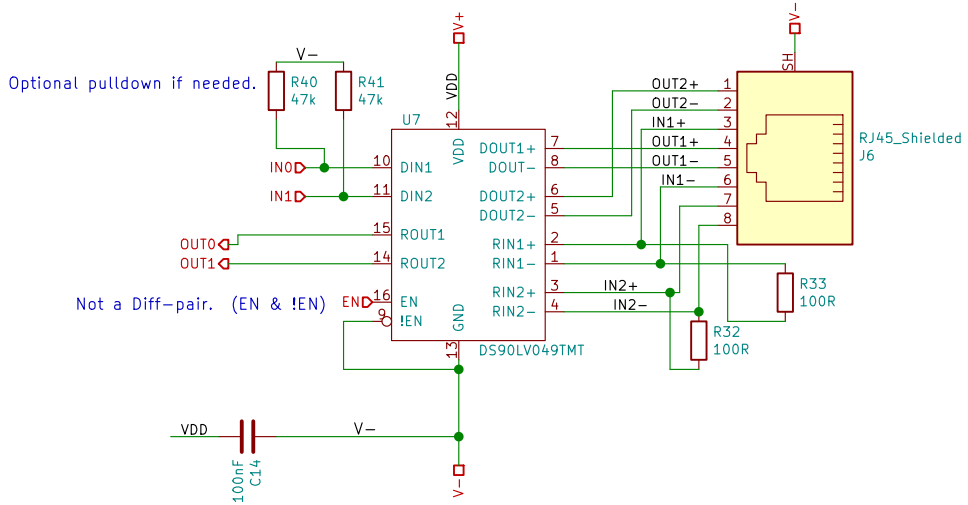
openPnP		
Sheet: /LVDS4/		
File: file5C2628B0.sch		
Title: LVDS <−> Xlinks		
Size: A4	Date: 2018−12−30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 3/10

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

openPnP		
Sheet: /LVDS6/		
File: file5C2628B0.sch		
Title: LVDS <−> Xlinks		
Size: A4	Date: 2018−12−30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 4/10

RJ45 PINOUT:

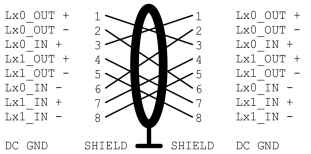
1/2 Lx0_OUT +/-

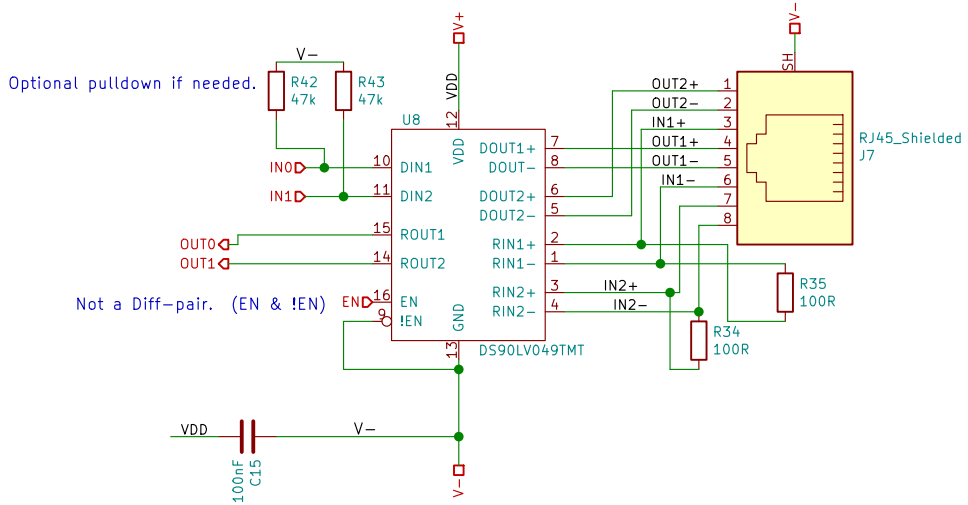
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





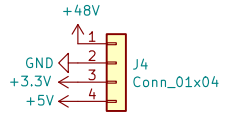
Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

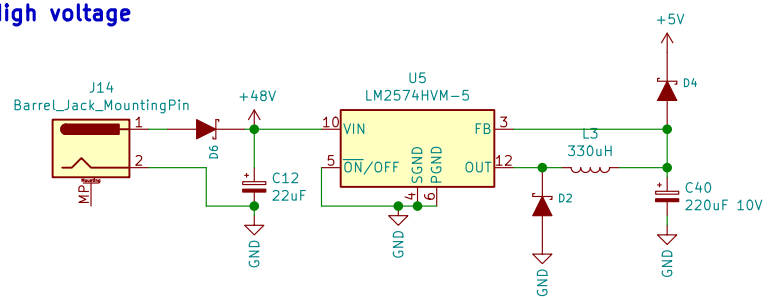
openPnP		
Sheet: /LVDS7/		
File: file5C2628B0.sch		
Title: LVDS <−> Xlinks		
Size: A4	Date: 2018−12−30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 5/10

Cards can be power by USB or by the barrel jack 8–48V.
Alternative "+48V" can come from a connected daugther card.
Both USB and +48V should not be connected on the same PCB.
USB ground should be isolated from power ground for PC safety.

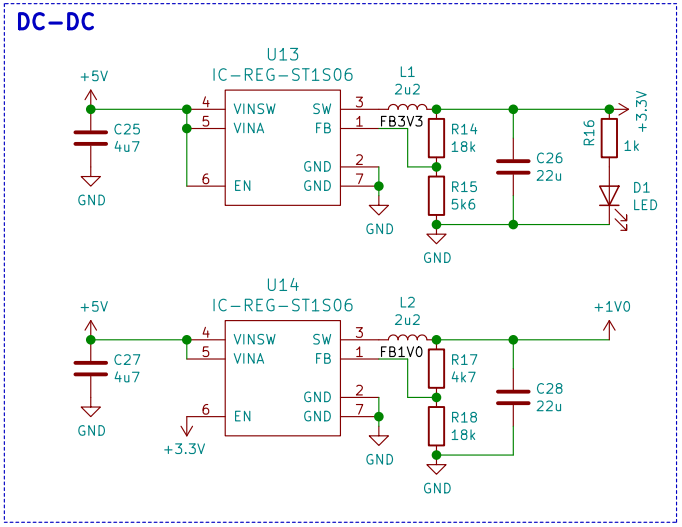
Power ports are Global in the schematics.



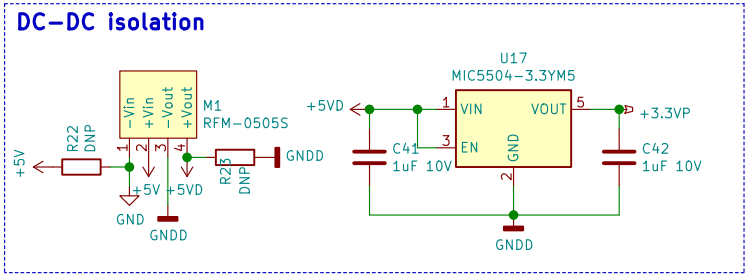
High voltage



DC–DC

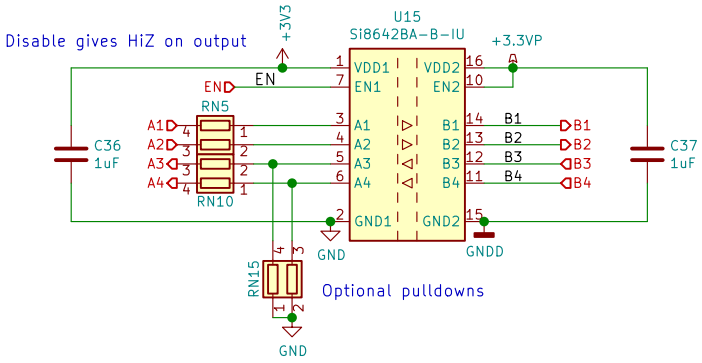


DC–DC isolation



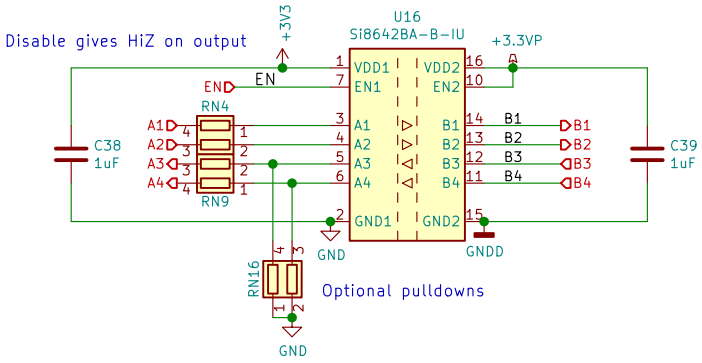
VDDIO/OTP_VCC and VDD can ramp up independently.
In order to reduce stresses on the device, it is preferable to make them ramp up in a short time frame of each other, no more than 50 ms apart.
RST_N and TRST_N should be kept low until all power supplies are stable and within tolerances of their final voltage.
If your design is powered by VBUS, then RST_N should go high within 10 ms of attaching to VBUS in order to ensure that USB timings are met.
RST_N should be at least 1 ms after VDDIO good to enable the built–in flash to settle

openPnP		
Sheet: /POWER/		
File: file5C95FA9D.sch		
Title: Power		
Size: A4	Date: 2018–12–30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)–1		Id: 6/10



On XLinks-2 wire, only one transition per clock cycle can happen within the pair, to avoid jitter/skew sensitivity.

openPnP		
Sheet: /ISOLATION_0/		
File: file5D2AE1E1.sch		
Title: Isolation		
Size: A4	Date: 2018-12-30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 7/10



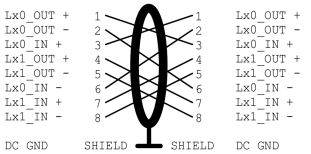
On XLinks-2 wire, only one transition per clock cycle can happen within the pair, to avoid jitter/skew sensitivity.

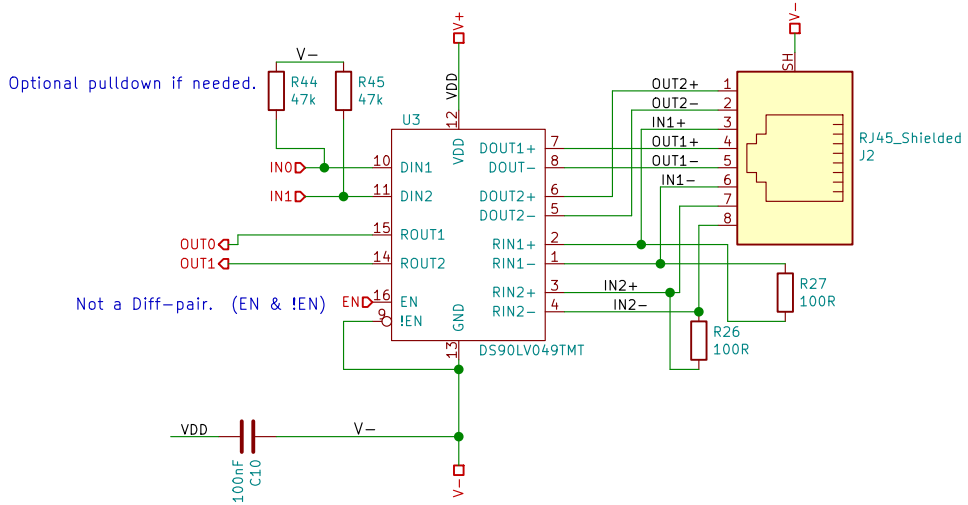
openPnP		
Sheet: /ISOLATION_1/		
File: file5D2AE1E1.sch		
Title: Isolation		
Size: A4	Date: 2018-12-30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 8/10

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

openPnP

Sheet: /LVDS1/
File: file5C2628B0.sch

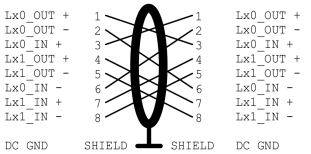
Title: LVDS <−> Xlinks

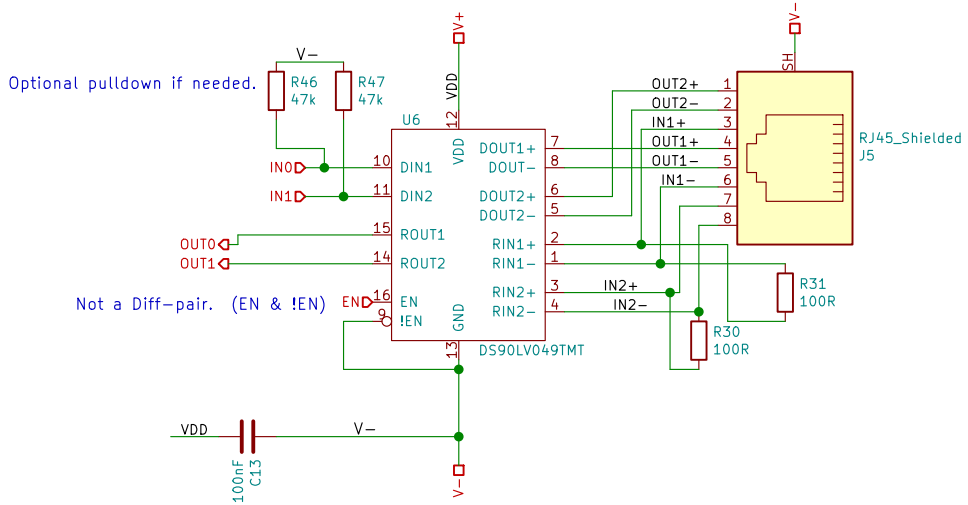
Size: A4	Date: 2018−12−30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 9/10

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

openPnP		
Sheet: /LVDS5/		
File: file5C2628B0.sch		
Title: LVDS <−> Xlinks		
Size: A4	Date: 2018−12−30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 10/10