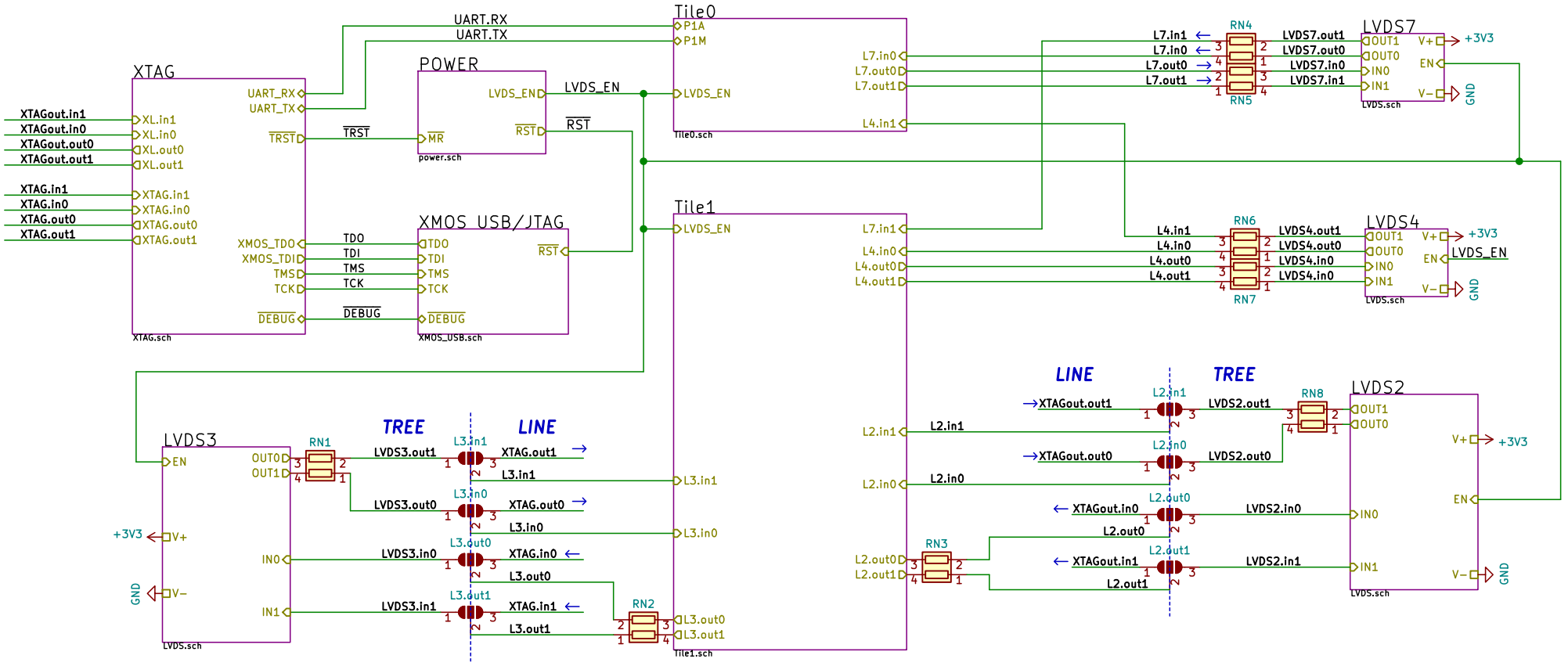
Board can be configured for Line or Tree/Star network.

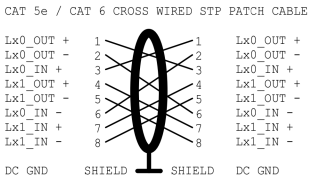


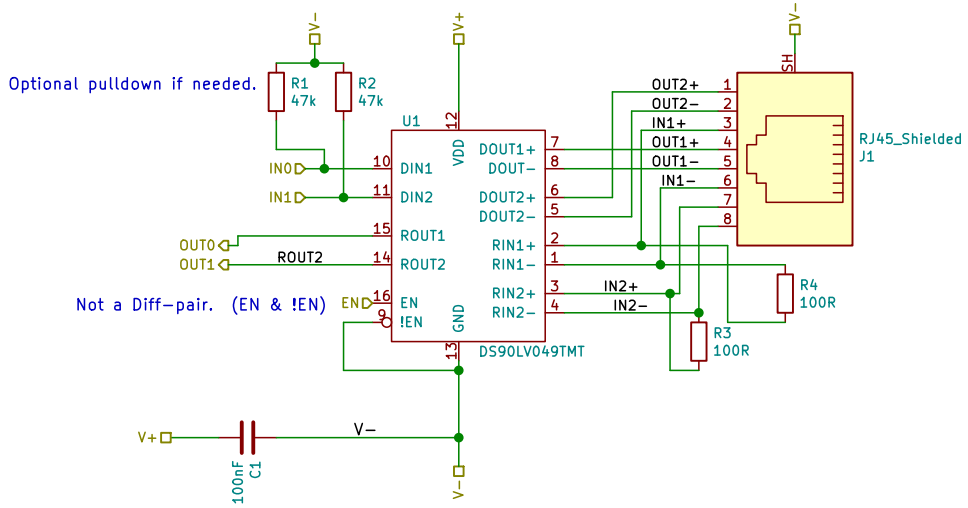
Open Source **openPnP**		
Sheet: / File: XMOS_XUF216_FB236.sch		
Title: XMOS top level		
Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 1/16

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

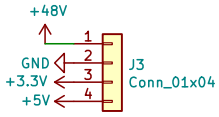
Sheet: /LVDS7/
File: LVDS.sch

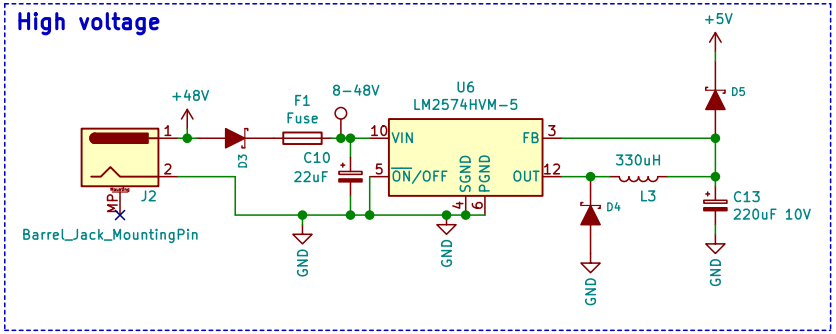
Title: LVDS <-> Xlinks

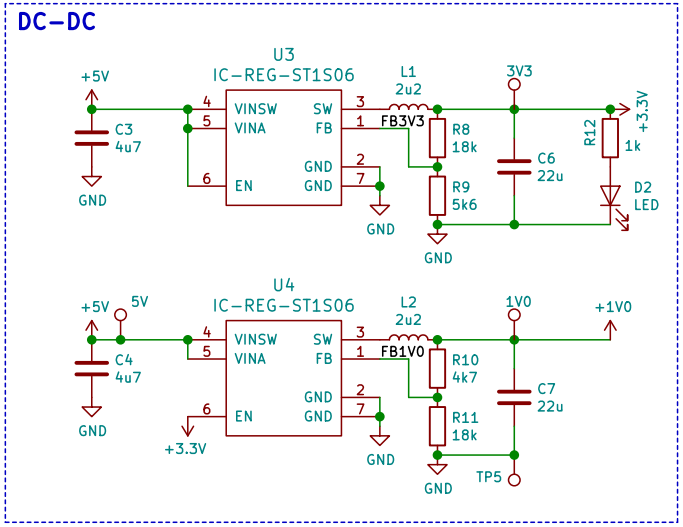
Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 2/16

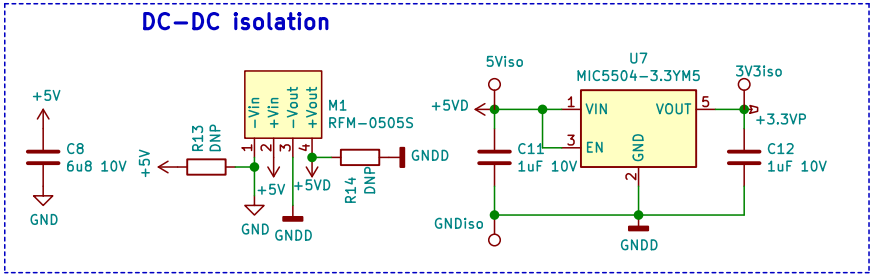
Cards can be power by USB or by the barrel jack 8–48V.
Alternative "+48V" can come from a connected daugther card.
Both USB and +48V should not be connected on the same PCB.
USB ground should be isolated from power ground for PC safety.

Power ports are Global in the schematics.

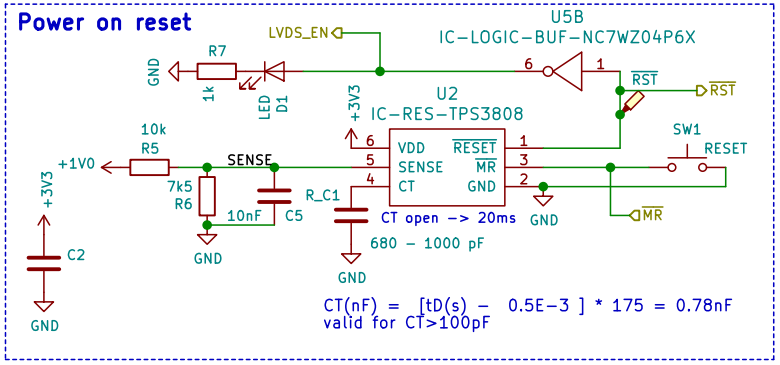


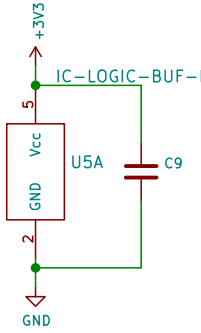






VDDIO/OTP_VCC and VDD can ramp up independently.
In order to reduce stresses on the device, it is preferable to make them ramp up in a short time frame of each other,
no more than 50 ms apart.
RST_N and TRST_N should be kept low until all power supplies are stable and within tolerances of their final voltage.
If your design is powered by VBUS, then RST_N should go high within 10 ms of attaching to VBUS in order to ensure that USB timings are met.
RST_N should be at least 1 ms after VDDIO good to enable the built–in flash to settle





Open Source
openPnP
Sheet: /POWER/
File: power.sch

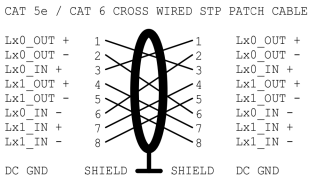
Title: Power

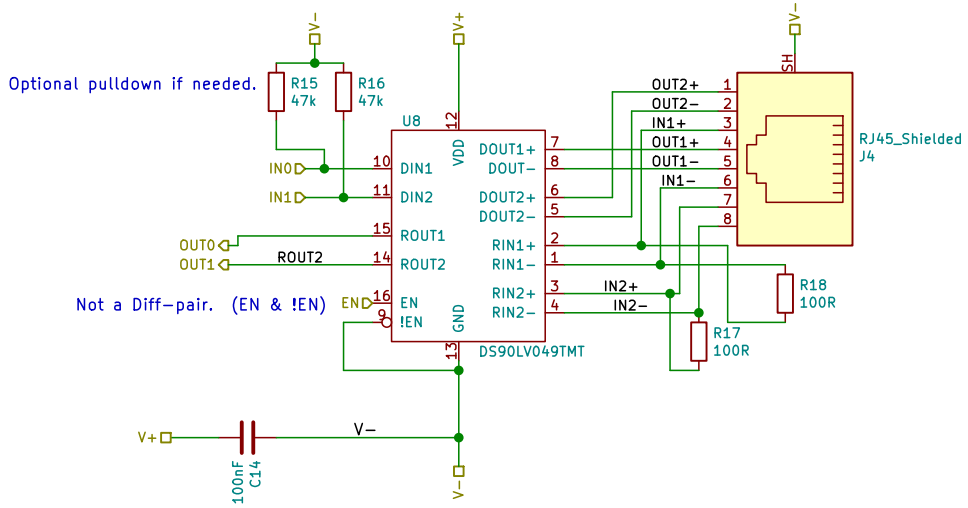
Size: A4	Date: 2019–01–01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)–1		Id: 3/16

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

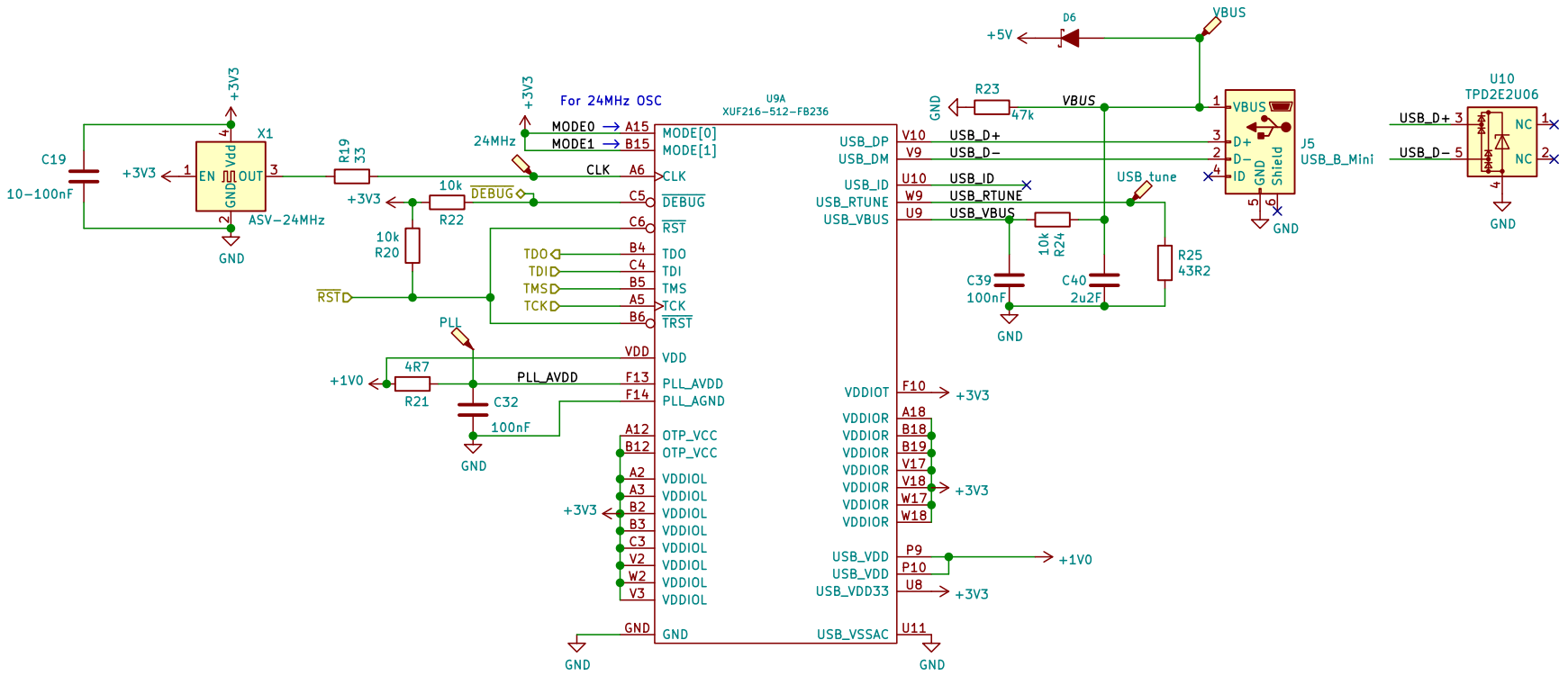
This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

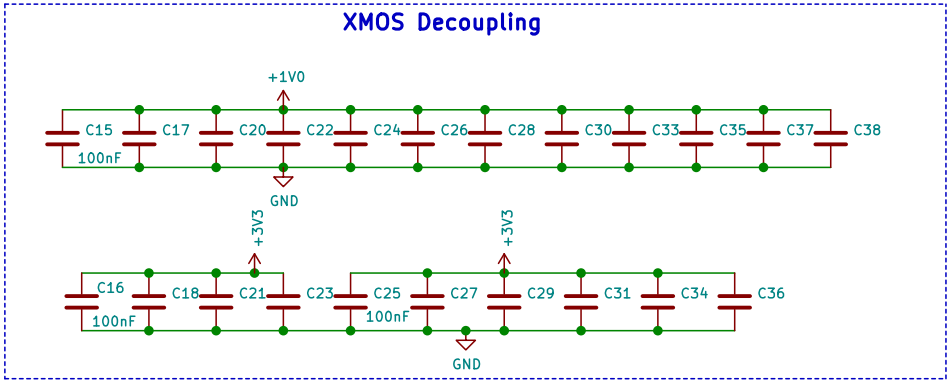
Open Source
openPnP

Sheet: /LVDS2/
File: LVDS.sch

Title: LVDS <-> Xlinks

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 4/16



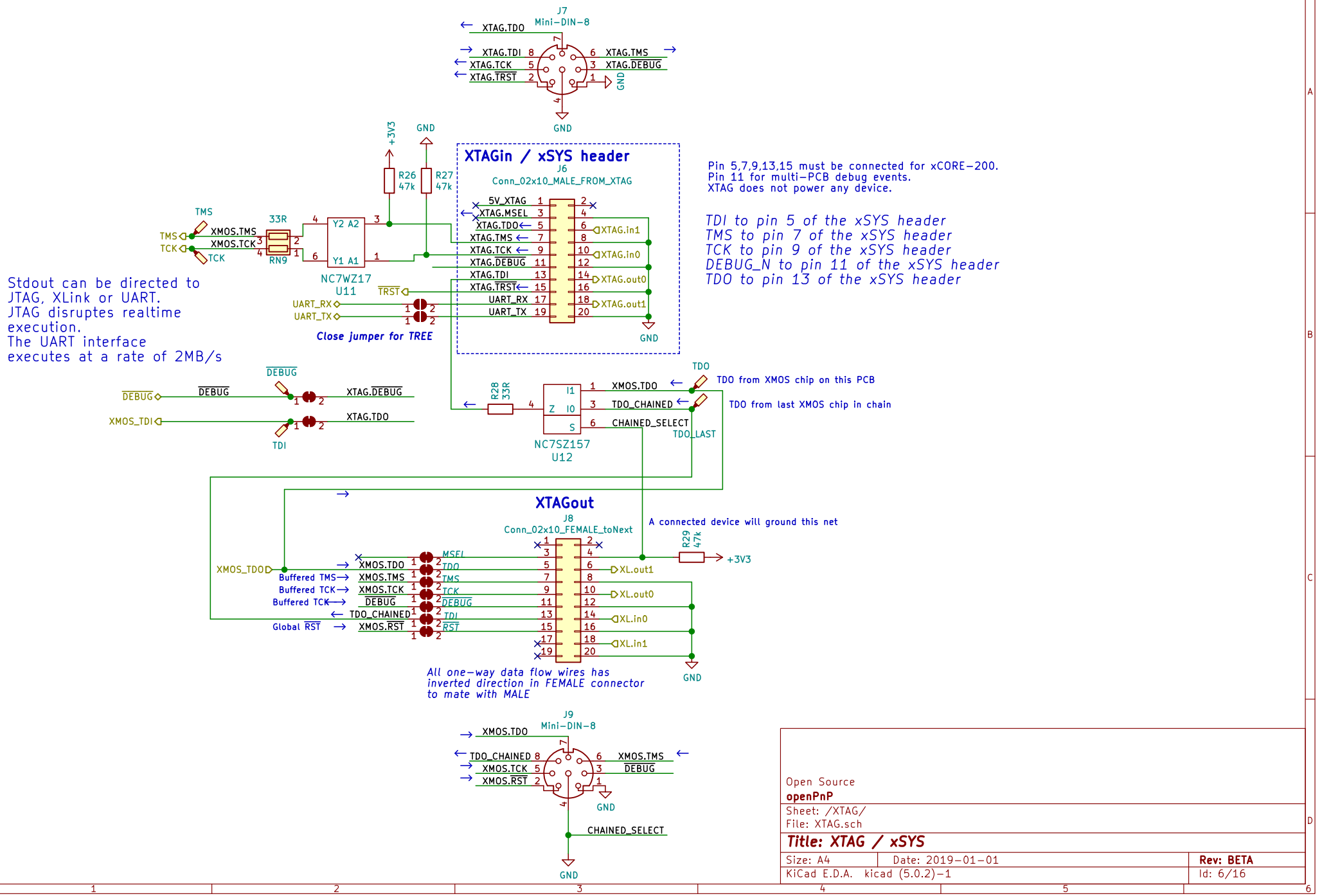


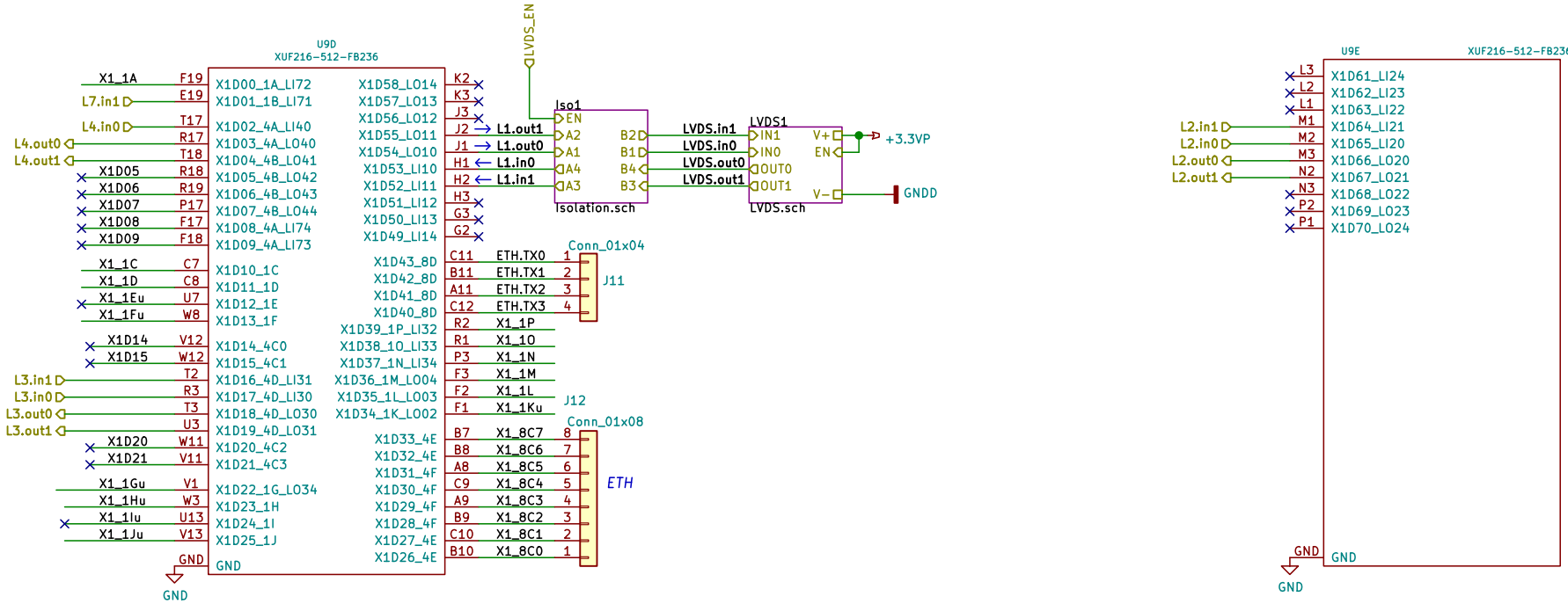
Open Source
openPnP

Sheet: /XMOS USB/JTAG/
File: XMOS_USB.sch

Title: XTAG & XMOS USB

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 5/16


J7
Mini-DIN-8
XTAG.TDO
XTAG.TDI
XTAG.TCK
XTAG.TRST
XTAG.TMS
XTAG.DEBUG
GND
XTAGin / xSYS header
J6
Conn_02x10_MALE_FROM_XTAG
5V_XTAG
XTAG.MSEL
XTAG.in1
XTAG.in0
XTAG.out0
XTAG.out1
UART_RX
UART_TX
Pin 5,7,9,13,15 must be connected for xCORE-200.
Pin 11 for multi-PCB debug events.
XTAG does not power any device.
TDI to pin 5 of the xSYS header
TMS to pin 7 of the xSYS header
TCK to pin 9 of the xSYS header
DEBUG_N to pin 11 of the xSYS header
TDO to pin 13 of the xSYS header
+3V3
R26 47k
R27 47k
33R
RN9
Y2 A2
Y1 A1
NC7WZ17
U11
TRST
Close jumper for TREE
Stdout can be directed to
JTAG, XLink or UART.
JTAG disrupts realtime
execution.
The UART interface
executes at a rate of 2MB/s
R28 33R
NC7SZ157
U12
TDO
TDO from XMOS chip on this PCB
TDO from last XMOS chip in chain
TDO_LAST
CHAINED_SELECT
XTAGout
J8
Conn_02x10_FEMALE_toNext
A connected device will ground this net
R29 47k
XMOS_TDO
Buffered TMS
Buffered TCK
Global RST
All one-way data flow wires has
inverted direction in FEMALE connector
to mate with MALE
J9
Mini-DIN-8
XMOS.TDO
TDO_CHAINED
XMOS.TCK
XMOS.RST
XMOS.TMS
DEBUG
CHAINED_SELECT
Open Source
openPnP
Sheet: /XTAG/
File: XTAG.sch
Title: XTAG / xSYS
Size: A4
Date: 2019-01-01
Rev: BETA
KiCad E.D.A. kicad (5.0.2)-1
Id: 6/16

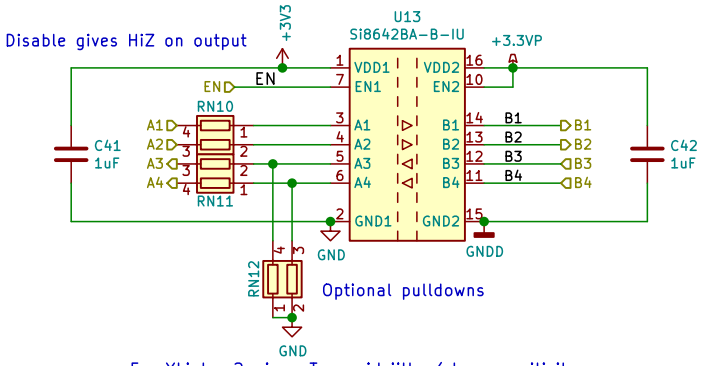


Open Source
openPnP

Sheet: /Tile1/
File: Tile1.sch

Title: XMOS Tile1

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 7/16



For XLinks-2 wire: To avoid jitter/skew sensitivity,
only one transition per clock cycle can happen within the pair.

Open Source
openPnP

Sheet: /Tile1/Iso1/
File: Isolation.sch

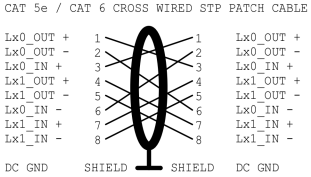
Title: Isolation

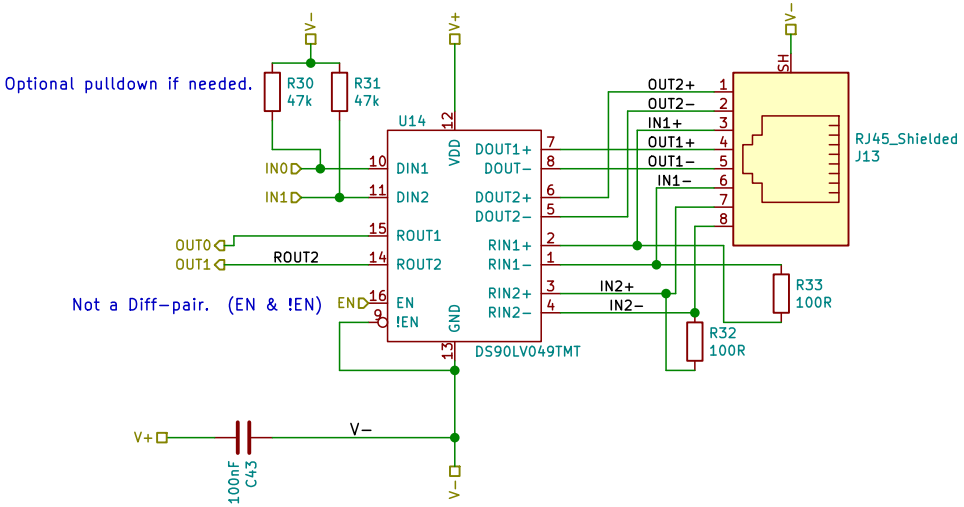
Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 8/16

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /Tile1/LVDS1/
File: LVDS.sch

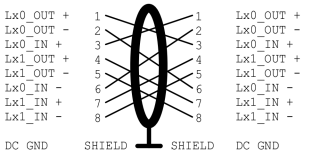
Title: LVDS <-> Xlinks

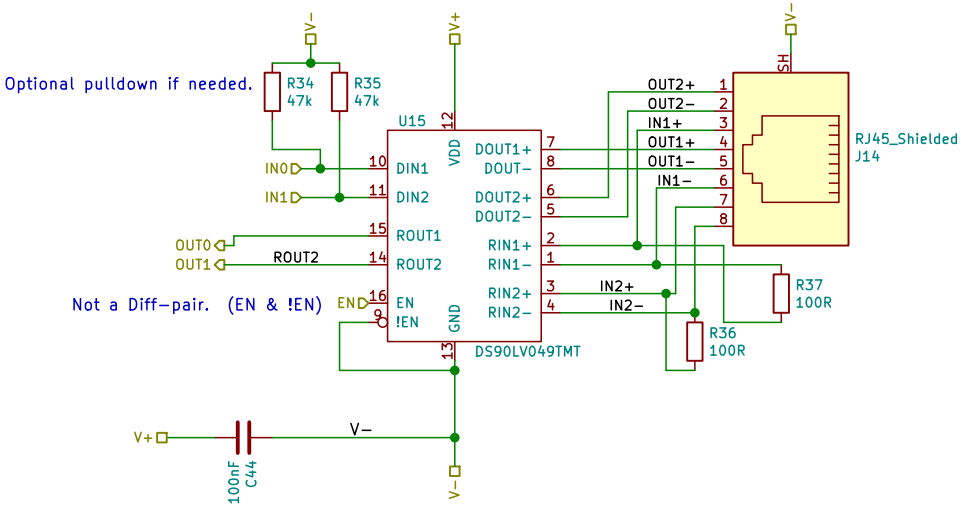
Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 9/16

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

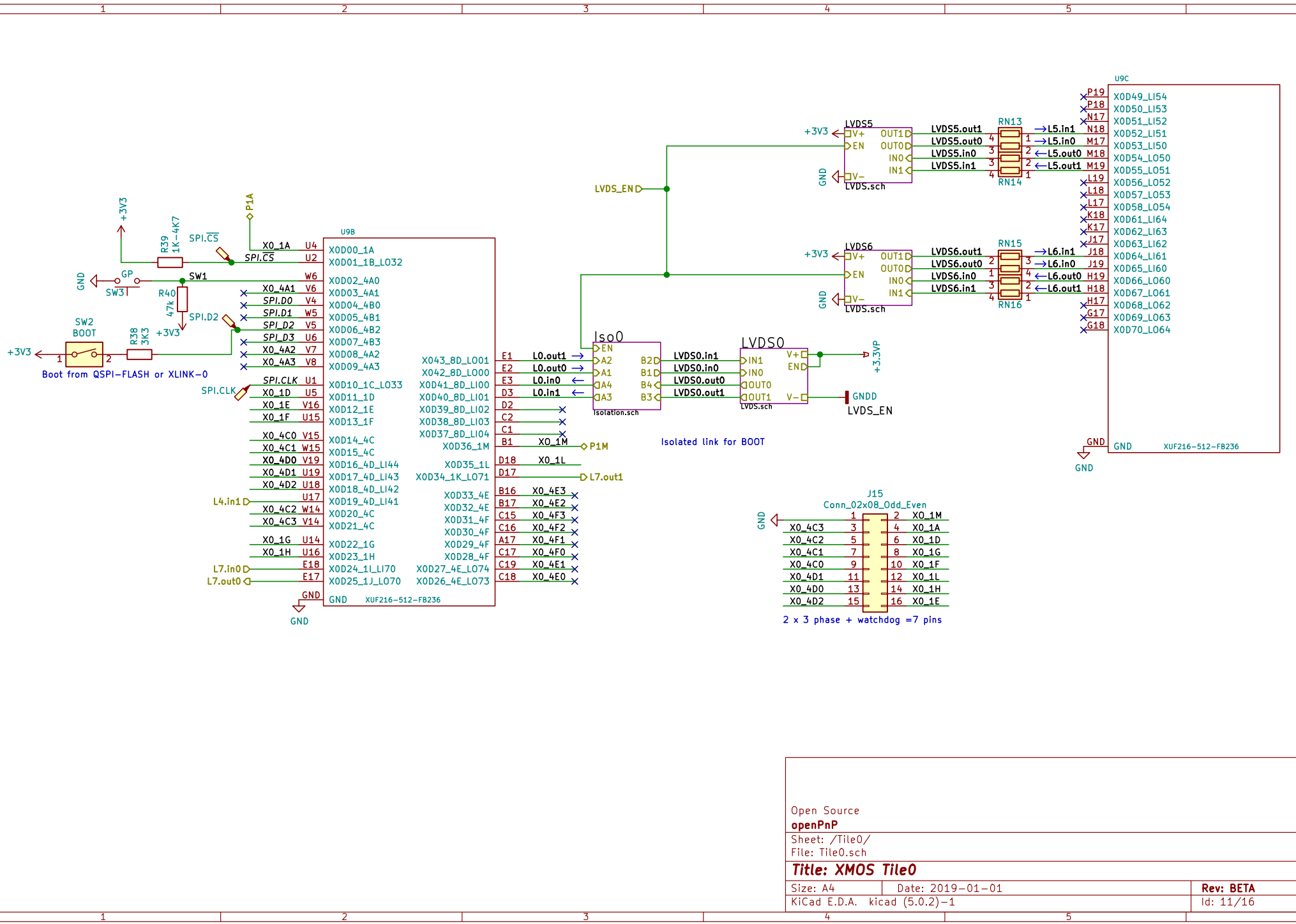
This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /LVDS4/
File: LVDS.sch

Title: LVDS <-> Xlinks

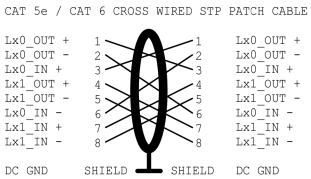
Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 10/16

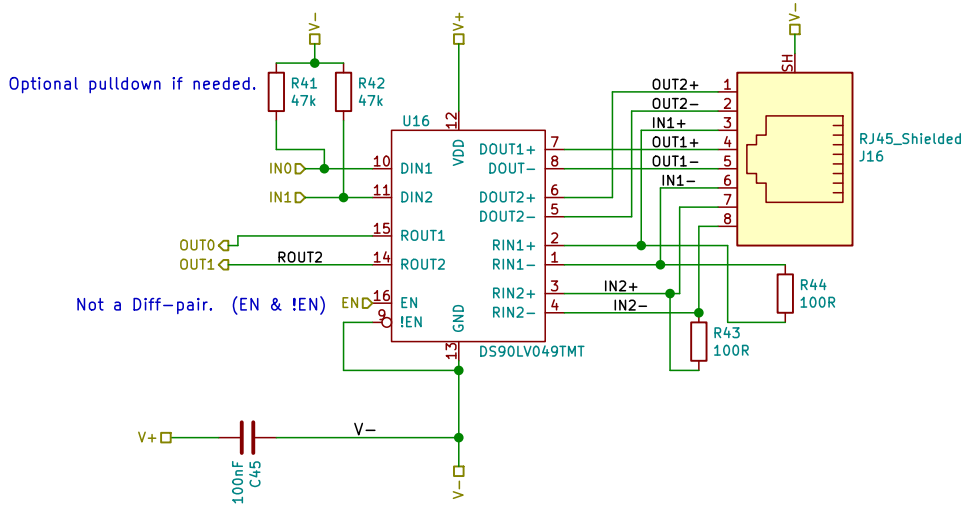

U9B
U9C
SW1
SW2
BOOT
R39
1K-4K7
R40
47k
R38
3K3
SPI.CS
SPI.D0
SPI.D1
SPI.D2
SPI.D3
SPI.CLK
+3V3
GND
P1A
Boot from QSPI-FLASH or XLINK-0
Iso0
Isolation.sch
LVDS0
LVDS.sch
LVDS5
LVDS6
LVDS_EN
+3.3VP
GNDD
Isolated link for BOOT
RN13
RN14
RN15
RN16
J15
Conn_02x08_Odd_Even
2 x 3 phase + watchdog =7 pins
XUF216-512-FB236
Open Source
openPnP
Sheet: /Tile0/
File: Tile0.sch
Title: XMOS Tile0
Size: A4
Date: 2019-01-01
Rev: BETA
KiCad E.D.A. kicad (5.0.2)-1
Id: 11/16

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /Tile0/LVDS6/
File: LVDS.sch

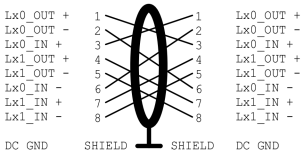
Title: LVDS <-> Xlinks

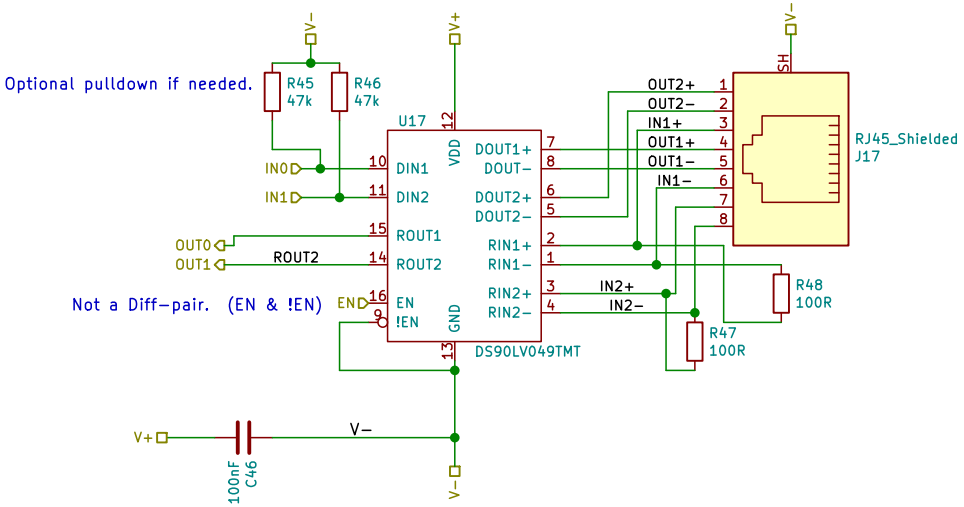
Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 12/16

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /Tile0/LVDS5/
File: LVDS.sch

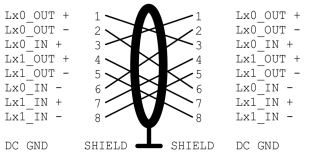
Title: LVDS <-> Xlinks

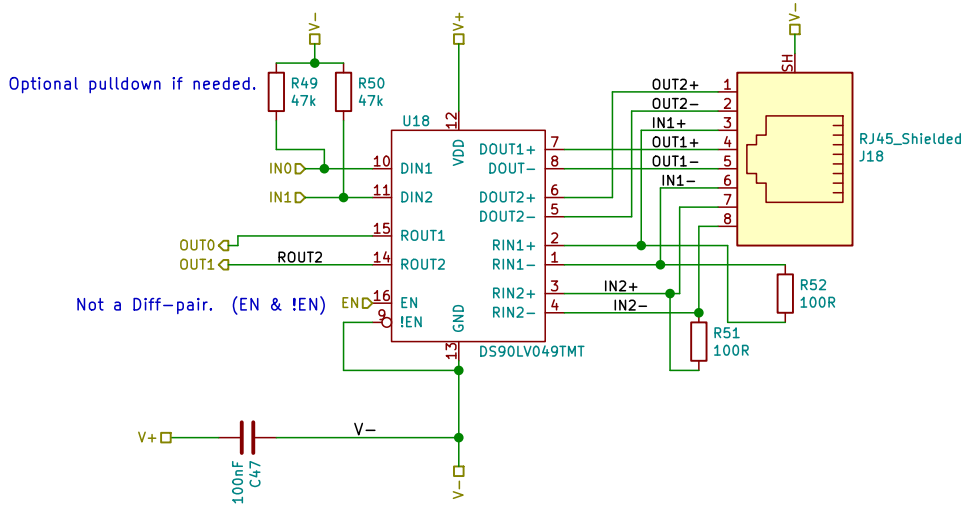
Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 13/16

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

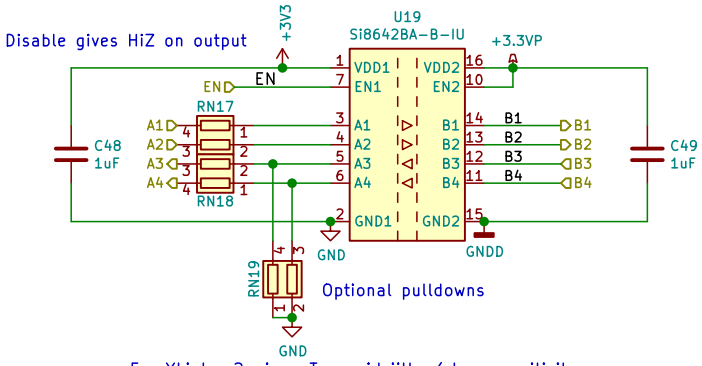
This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /Tile0/LVDS0/
File: LVDS.sch

Title: LVDS <-> Xlinks

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 14/16



For XLinks-2 wire: To avoid jitter/skew sensitivity,
only one transition per clock cycle can happen within the pair.

Open Source
openPnP

Sheet: /Tile0/Iso0/
File: Isolation.sch

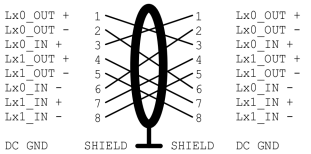
Title: Isolation

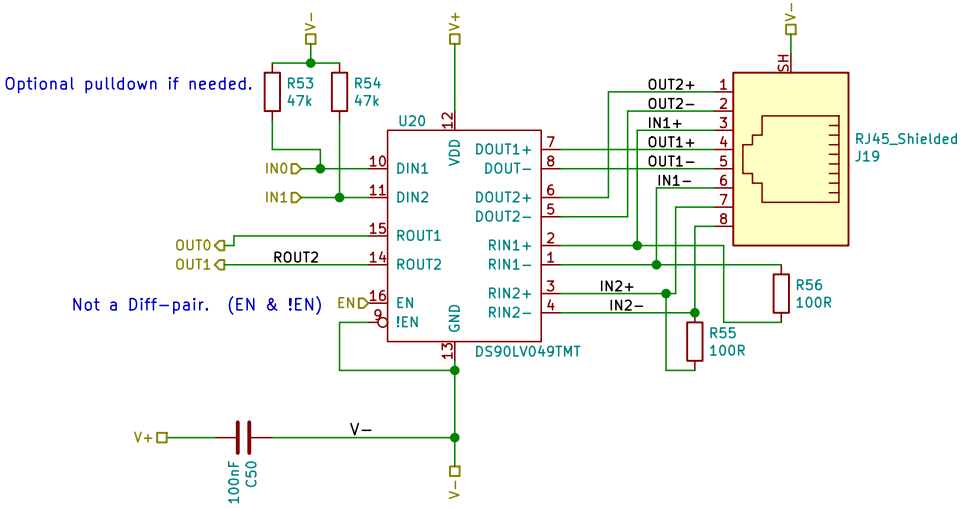
Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 15/16

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /LVDS3/
File: LVDS.sch

Title: LVDS <-> Xlinks

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 16/16