Board can be configured for Line or Tree/Star network.

TILE 0

U1.A XUF216-512-FB236

For 24MHz OSC

24MHz

MODE0 A15
MODE1 B15
CLK A6
DEBUG C5
XMOS.RST C6
XMOS.TDO B4
XMOS.TDI C4
XMOS.TMS B5
XMOS.TCK A5
B6
PLL
VDD
PLL_AVDD F13
PLL_AGND F14
OTP_VCC A12 B12
VDDIOL A2 A3 B2 B3 C3 V2 W2 V3
GND
MODE[0] MODE[1] CLK DEBUG RST TDO TDI TMS TCK TRST VDD PLL_AVDD PLL_AGND OTP_VCC VDDIOL GND

USB_DP V10
USB_DM V9
USB_ID U10
USB_RTUNE W9
USB_VBUS U9
VDDIOT F10
VDDIOR A18 B18 B19 V17 V18 W17 W18
USB_VDD P9 P10
USB_VDD U8
USB_VSSAC U11
USB_D+ USB_D- USB_ID USB_RTUNE USB_VBUS USB_VDD33 USB_VSSAC

+5V D3 VBUS
R3 47k
J8 USB_B_Mini
R4 10k
R2 43R2
C17 100nF
C43 2u2F
USB_tune

U10 TPD2E2U06
USB_D+ 3
USB_D- 5
NC 1 NC 2 4

SW3 BOOT
R21 3K3
SW1 GP
R20 47k
R5 1K-4K7
SPI.CS
Boot from QSPI-FLASH or XLINK-0

U1.B TILE 0

X0_1A U4
SPI.CS U2
X0_4A1 V6
SPI.D0 V4
SPI.D1 W5
SPI_D2 V5
SPI_D3 U6
X0_4A2 V7
X0_4A3 V8
SPI.CLK U1
X0_1D U5
X0_1E V16
X0_1F U15
X0_4C0 V15
X0_4C1 W15
X0_4D0 V19
X0_4D1 U19
X0_4D2 U18
L4.in1 U17
X0_4C2 W14
X0_4C3 V14
X0_1G U14
X0_1H U16
L7.in0 E18
L7.out0 E17
GND

X0D00_1A
X0D01_1B_LO32
X0D02_4A0
X0D03_4A1
X0D04_4B0
X0D05_4B1
X0D06_4B2
X0D07_4B3
X0D08_4A2
X0D09_4A3
X0D10_1C_LO33
X0D11_1D
X0D12_1E
X0D13_1F
X0D14_4C
X0D15_4C
X0D16_4D_LI44
X0D17_4D_LI43
X0D18_4D_LI42
X0D19_4D_LI41
X0D20_4C
X0D21_4C
X0D22_1G
X0D23_1H
X0D24_1I_LI70
X0D25_1J_LO70
X0D26_4E_LO73
X0D27_4E_LO74
X0D28_4F
X0D29_4F
X0D30_4F
X0D31_4F
X0D32_4E
X0D33_4E
X0D34_1K_LO71
X0D35_1L
X0D36_1M
X0D37_8D_LI04
X0D38_8D_LI03
X0D39_8D_LI02
X0D40_8D_LI01
X0D41_8D_LI00
X0D42_8D_LO00
X0D43_8D_LO01
X0D44_1P
X0D45_1N
X0D46_1M
X0D47_1L
X0D48_8C
X0D49_4I_LI73
X0D50_1I_LI13
X0D51_1I_LI12
X0D52_1I_LI11
X0D53_1I_LI10
X0D54_1I_LO10
X0D55_1I_LO11
X0D56_1I_LO12
X0D57_1I_LO13
X0D58_1I_LO14
X0D59_1I_LO15
X0D60_1I_LO16
X0D61_1I_LO17
X0D62_1I_LO18
X0D63_1I_LO19
X0D64_1I_LO20
X0D65_1I_LO21
X0D66_1I_LO22
X0D67_1I_LO23
X0D68_1I_LO24
X0D69_1J_LO23
X0D70_1J_LO24

E1 L0.out1
E2 L0.out0
E3 L0.in0
D3 L0.in1
D2
C2
C1
B1 X0_1M
D18 X0_1L
D17 L7.out1
B16 X0_4E3
B17 X0_4E2
C15 X0_4F3
C16 X0_4F2
A17 X0_4F1
C17 X0_4F0
C19 X0_4E1
C18 X0_4E0

LVDS_EN
ISOLATION_0 EN A2 A1 A4 A3
B2 LVDS0.in1
B1 LVDS0.in0
B4 LVDS0.out0
B3 LVDS0.out1
file5D2AE1E1.sch
LVDS0 IN1 IN0 OUT0 OUT1 V+ EN V-
+3.3VP
GNDD
file5C2628B0.sch
Isolated link for BOOT

J16 Mini-DIN-8
XTAG.TDO 7
XTAG.TDI 8
XTAG.TCK 5
XTAG.TRST 2
XTAG.TMS 6
XTAG.DEBUG 3
GND 1 4

Pin 5(XMOS TDI),7,9,13,15 must be connected for xCORE-200.
Pin 11 for multi-PCB debug events.
XTAG does not power any device.

XTAGin / xSYS header

J9 Conn_02x10_MALE_FROM_XTAG

5V_XTAG 1
XTAG.MSEL 3
XTAG.TDO 5
XTAG.TMS 7
XTAG.TCK 9
XTAG.DEBUG 11
XTAG.TDI 13
XTAG.TRST 15
UART_RX 17
UART_TX 19
2 4 6 XTAG.in1 8 10 XTAG.in0 12 14 XTAG.out0 16 18 XTAG.out1 20
GND

TDI to pin 5 of the xSYS header
TMS to pin 7 of the xSYS header
TCK to pin 9 of the xSYS header
DEBUG_N to pin 11 of the xSYS header
TDO to pin 13 of the xSYS header

close for TREE

The UART interface executes at a rate of 2MB/s

R10 47k
R11 47k
33R
RN17
Y2 A2 Y1 A1
NC7WZ17 U12
X0_1A X0_1M

TMS XMOS.TMS XMOS.TCK TCK
DEBUG DEBUG XTAG.DEBUG
XMOS.TDI XTAG.TDO TDI

Stdout can be directed to JTAG, XLink or UART.
JTAG disruptes realtime execution.

R8 33R
NC7SZ157 U11
I1 I0 Z S
XMOS.TDO
TDO_CHAINED
CHAINED_SELECT
TDO
TDO from this XMOS chip
TDO_RETURN
TDO from last XMOS chip in chain
A connected device will ground this net

U18.A IC-LOGIC-BUF-NC7WZ04P6X

C1 C2 C3 C4 C5 C6 C7 C8 C31 C33 C34 C35 100nF
C45 C32 C29 C30 C18 C19 C20 C21 C22 C23 100nF
VCC +1V0 +3V3 GND

POWER
file5C95FA9D.sch

LVDS5 RN11 LVDS5.out1 LVDS5.out0 LVDS5.in0 LVDS5.in1 L5.in1 L5.in0 L5.out0 L5.out1 RN6 file5C2628B0.sch
LVDS6 RN12 LVDS6.out1 LVDS6.out0 LVDS6.in0 LVDS6.in1 L6.in1 L6.in0 L6.out0 L6.out1 RN7 file5C2628B0.sch

U1.C
P19 P18 N17 N18 M17 M18 L19 L18 L17 K18 K17 J17 J18 J19 H19 H18 H17 G17 G18
X0D49_LI54 X0D50_LI53 X0D51_LI52 X0D52_LI51 X0D53_LI50 X0D54_LO50 X0D55_LO51 X0D56_LO52 X0D57_LO53 X0D58_LO54 X0D61_LI64 X0D62_LI63 X0D63_LI62 X0D64_LI61 X0D65_LI60 X0D66_LO60 X0D67_LO61 X0D68_LO62 X0D69_LO63 X0D70_LO64
GND GND XUF216-512-FB236

LVDS7 RN13 LVDS7.out1 LVDS7.out0 LVDS7.in0 LVDS7.in1 L7.in1 L7.in0 L7.out0 L7.out1 RN8 file5C2628B0.sch

TILE 1

U1.D XUF216-512-FB236

LVDS4 RN14 LVDS4.out1 LVDS4.out0 LVDS4.in0 LVDS4.in1 L4.in1 L4.in0 L4.out0 L4.out1 RN3 file5C2628B0.sch

X1D05 R18
X1D06 R19
X1D07 P17
X1D08 F17
X1D09 F18
X1D10_1C C7
X1D11_1D C8
X1D12_1E U7
X1D13_1F W8
X1D14_4C0 V12
X1D15_4C1 W12
L3.in1 T2
L3.in0 R3
T3
U3
X1D20 W11
X1D21 V11
X1D22_1G_LO34 V1
X1D23_1H W3
X1D24_1I U13
X1D25_1J V13

X1D58_LO14 K2
X1D57_LO13 K3
X1D56_LO12 J3
X1D55_LO11 J2
X1D54_LO10 J1
X1D53_LI10 H1
X1D52_LI11 H2
X1D51_LI12 H3
X1D50_LI13 G3
X1D49_LI14 G2
X1D43_8D C11
X1D42_8D B11
X1D41_8D A11
X1D40_8D C12
X1D39_1P_LI32 R2
X1D38_1O_LI33 R1
X1D37_1N_LI34 P3
X1D36_1M_LO04 F3
X1D35_1L_LO03 F2
X1D34_1K_LO02 F1
X1D33_4E B7
X1D32_4E B8
X1D31_4F A8
X1D30_4F C9
X1D29_4F A9
X1D28_4F B9
X1D27_4E C10
X1D26_4E B10

LVDS_EN
ISOLATION_1 EN A2 A1 A4 A3
B2 LVDS.in1
B1 LVDS.in0
B4 LVDS.out0
B3 LVDS.out1
file5D2AE1E1.sch
LVDS1 IN1 IN0 OUT0 OUT1 V+ EN V-
+3.3VP
GNDD
file5C2628B0.sch

L1.out1 L1.out0 L1.in0 L1.in1

Conn_01x04 J15
ETH.TX0 1
ETH.TX1 2
ETH.TX2 3
ETH.TX3 4

Conn_01x08 J13 ETH
X1_1P 1
X1_1N 2
X1_1O 3
X1_1M 4
X1_1L 5
X1_1Ku 6
X1_8C7 7
X1_8C6 8

LVDS3 RN18 LVDS3.out1 LVDS3.out0 LVDS3.in0 LVDS3.in1 file5C2628B0.sch

L3.out0 L3.out1 RN5
X1D20
X1_1Gu
X1_1Hu
X1_1Iu
X1_1Ju

TREE LINE
L3.in1 LVDS3.out1 XTAG.out1
L3.in0 LVDS3.out0 XTAG.out0
L3.out0 LVDS3.in0 XTAG.in0
L3.out1 LVDS3.in1 XTAG.in1

J12 Conn_02x08_Odd_Even
X1_1Ju 3 X1_1A 2
X1_1Ku 5 X1_1D 4
7 X1_1C 6
X1_1Fu 9 X1_1M 8
X1_1Hu 11 X1_1L 10
13 X1_1O 12
X1_1Gu 15 X1_1P 14
X1_1N 16
ETH.MDC
ETH.MDIO
ETH.INT
ETH.PHY_RSTn
u = Port unavailable if USB enabled on that tile

J11 Conn_02x08_Odd_Even
X0_4C3 3 X0_1M 2
X0_4C2 5 X0_1A 4
X0_4C1 7 X0_1D 6
X0_4C0 9 X0_1G 8
X0_4D1 11 X0_1F 10
X0_4D0 13 X0_1L 12
X0_4D2 15 X0_1H 14
X0_1E 16
2 x 3 phase + watchdog =7 pins

XTAGout

J10 Conn_02x10_FEMALE_toNext

TDO from this XMOS chip
TDO from last XMOS chip in chain
MSEL XMOS.TDO TDO XMOS.TMS TCK XMOS.TCK DEBUG XMOS.RST TDI TDO_CHAINED RST
2 4 6 XTAGout.out1 8 10 XTAGout.out0 12 14 XTAGout.in0 16 18 XTAGout.in1 20
R9 47k
+3V3
GND
All one-way data flow wires has inverted direction in FEMALE connector to mate with MALE

J17 Mini-DIN-8
XMOS.TDO
TDO_CHAINED
XMOS.TCK
XMOS.RST
XMOS.TMS
DEBUG
CHAINED_SELECT

TILE 1

U1.E XUF216-512-FB236

L2.in1 L2.in0 L2.out0 L2.out1 RN1
L3 L2 L1 M1 M2 M3 N2 N3 P2 P1
X1D61_LI24
X1D62_LI23
X1D63_LI22
X1D64_LI21
X1D65_LI20
X1D66_LO20
X1D67_LO21
X1D68_LO22
X1D69_LO23
X1D70_LO24
GND GND

CLK

C44 10-100nF
X1 ASV-24MHz
R19 33
CLK

Power on reset

U18.B IC-LOGIC-BUF-NC7WZ04P6X

R48 1k
LED D5
LVDS_EN
U9 IC-RES-TPS3808
SW2 RESET
R12 10k
R13 7k5
C24 10nF
R_C1
CT open -> 20ms
680 - 1000 pF
XMOS.RST
XTAG.TRST

CT(nF) = [tD(s) - 0.5E-3] * 175 = 0.78nF
valid for CT>100pF

TREE LINE

L2.in1 XTAGout.out1 L2.in1
L2.in0 XTAGout.in0 L2.in0
L2.out0 XTAGout.out0 L2.out0
L2.out1 XTAGout.in1 L2.out1

LVDS2 RN? LVDS2.out1 LVDS2.out0 LVDS2.in0 LVDS2.in1 file5C2628B0.sch

Open Source
openPnP
Sheet: /
File: test.sch

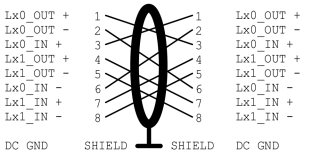
Title: XMOS top level

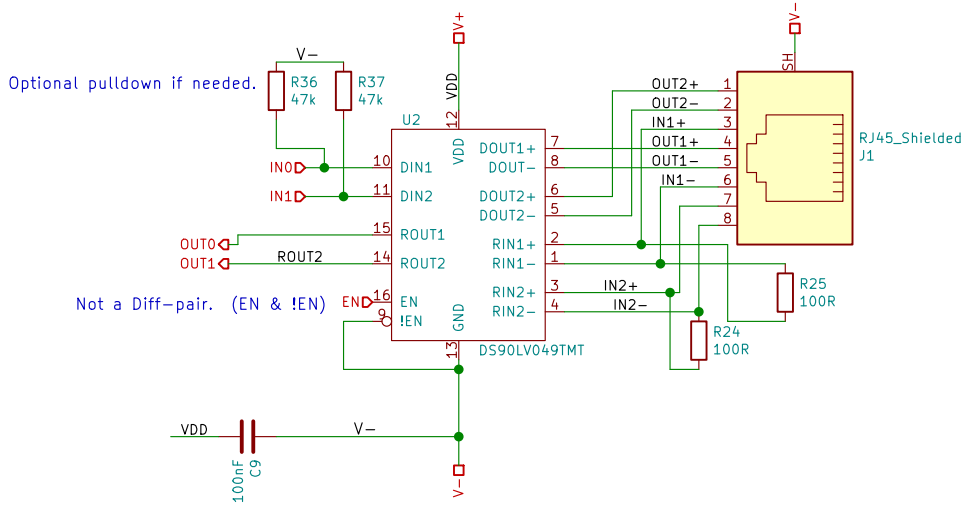
Size: A3	Date: 2018-12-31	Rev: BETA
KiCad E.D.A. kicad (5.0.2)-1		Id: 1/12

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /LVDS0/
File: file5C2628B0.sch

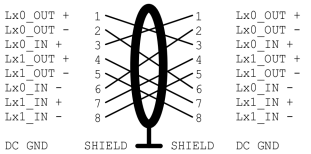
Title: LVDS <−> Xlinks

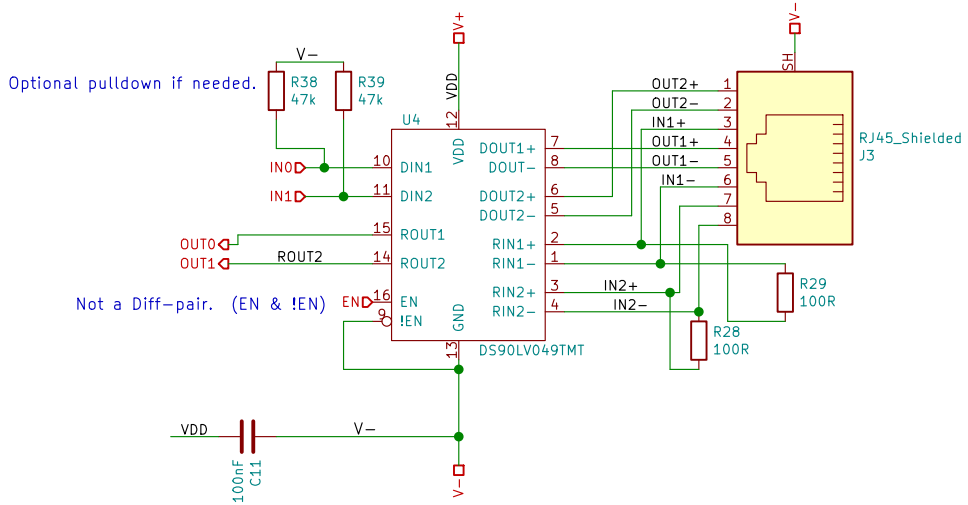
Size: A4	Date: 2018−12−31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 2/12

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /LVDS4/
File: file5C2628B0.sch

Title: LVDS <−> Xlinks

Size: A4	Date: 2018−12−31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 3/12

RJ45 PINOUT:

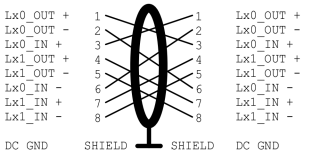
1/2 Lx0_OUT +/-

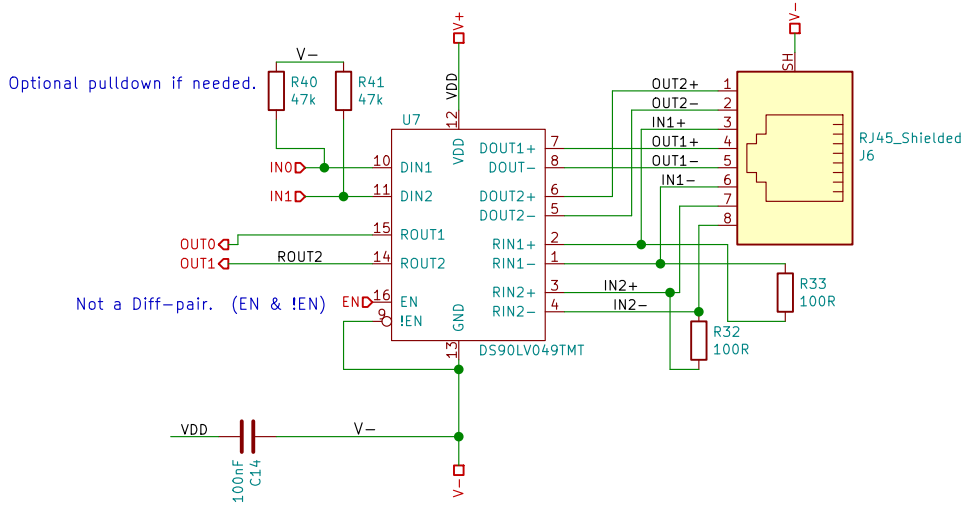
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /LVDS6/
File: file5C2628B0.sch

Title: LVDS <−> Xlinks

Size: A4	Date: 2018−12−31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 4/12

RJ45 PINOUT:

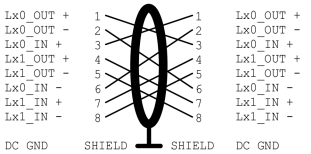
1/2 Lx0_OUT +/-

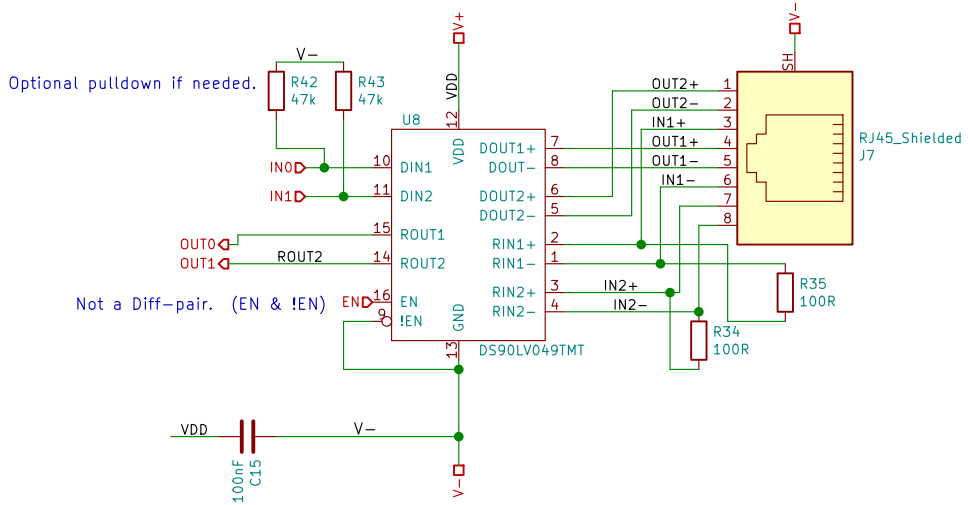
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

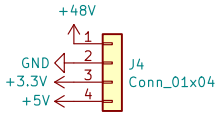
Sheet: /LVDS7/
File: file5C2628B0.sch

Title: LVDS <–> Xlinks

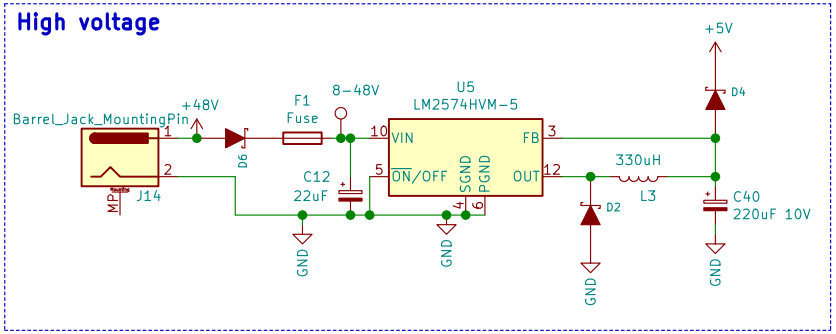
Size: A4	Date: 2018–12–31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)–1		Id: 5/12

Cards can be power by USB or by the barrel jack 8–48V.
Alternative "+48V" can come from a connected daugther card.
Both USB and +48V should not be connected on the same PCB.
USB ground should be isolated from power ground for PC safety.

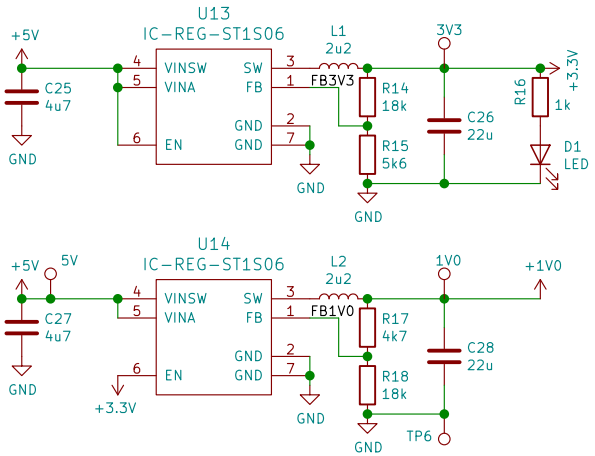
Power ports are Global in the schematics.



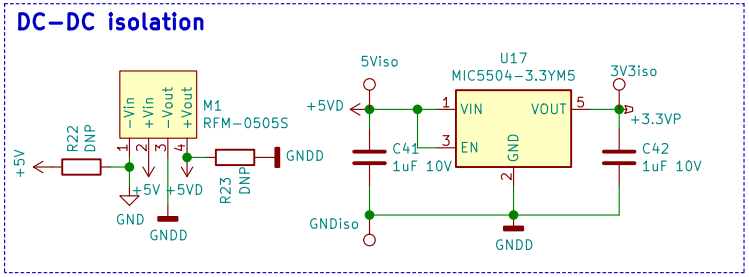
High voltage



DC–DC



DC–DC isolation

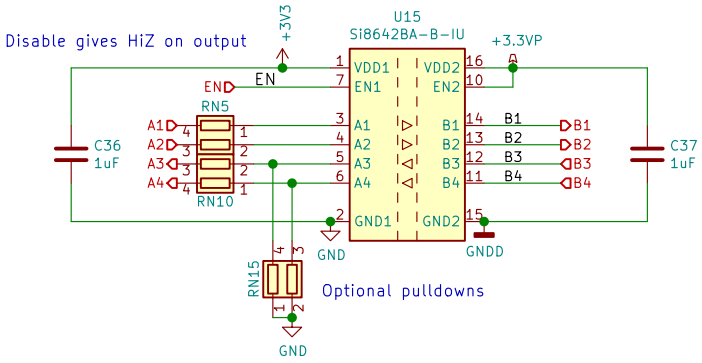


VDDIO/OTP_VCC and VDD can ramp up independently.
In order to reduce stresses on the device, it is preferable to make them ramp up in a short time frame of each other,
no more than 50 ms apart.
RST_N and TRST_N should be kept low until all power supplies are stable and within tolerances of their final voltage.
If your design is powered by VBUS, then RST_N should go high within 10 ms of attaching to VBUS in order to ensure that USB timings are met.
RST_N should be at least 1 ms after VDDIO good to enable the built–in flash to settle

Open Source
openPnP
Sheet: /POWER/
File: file5C95FA9D.sch

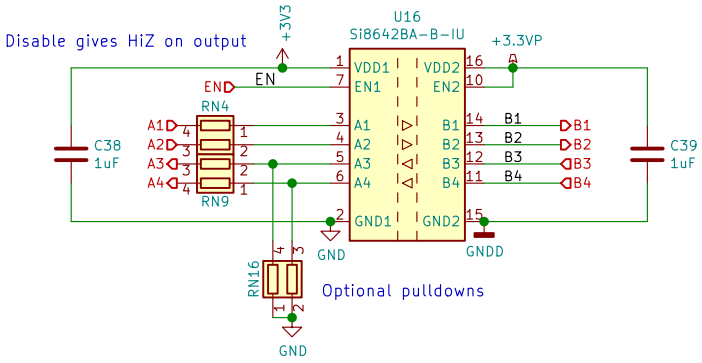
Title: Power

Size: A4	Date: 2018–12–31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)–1		Id: 6/12



On XLinks-2 wire, only one transition per clock cycle can happen within the pair, to avoid jitter/skew sensitivity.

Open Source **openPnP**		
Sheet: /ISOLATION_0/ File: file5D2AE1E1.sch		
Title: Isolation		
Size: A4	Date: 2018-12-31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 7/12



On XLinks-2 wire, only one transition per clock cycle can happen within the pair, to avoid jitter/skew sensitivity.

Open Source
openPnP

Sheet: /ISOLATION_1/
File: file5D2AE1E1.sch

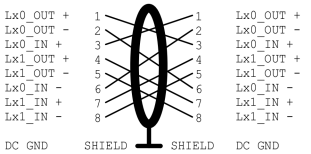
Title: Isolation

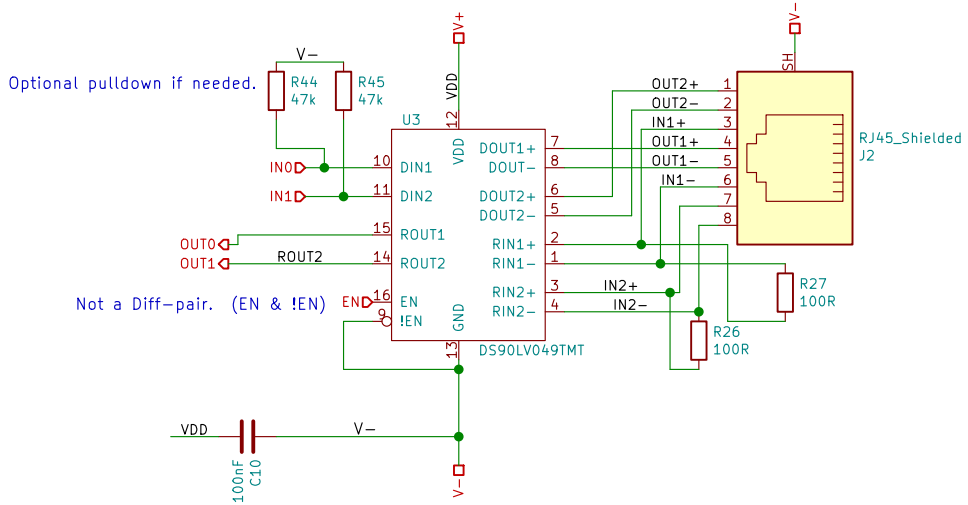
Size: A4	Date: 2018-12-31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 8/12

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /LVDS1/
File: file5C2628B0.sch

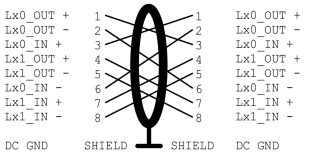
Title: LVDS <−> Xlinks

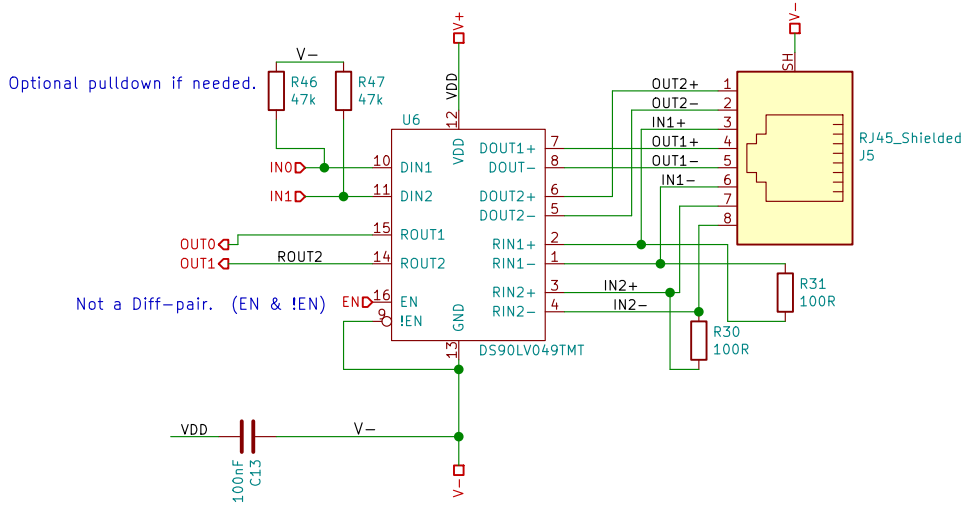
Size: A4	Date: 2018−12−31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 9/12

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /LVDS5/
File: file5C2628B0.sch

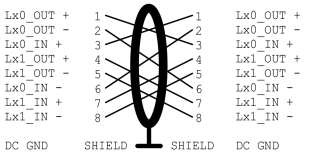
Title: LVDS <–> Xlinks

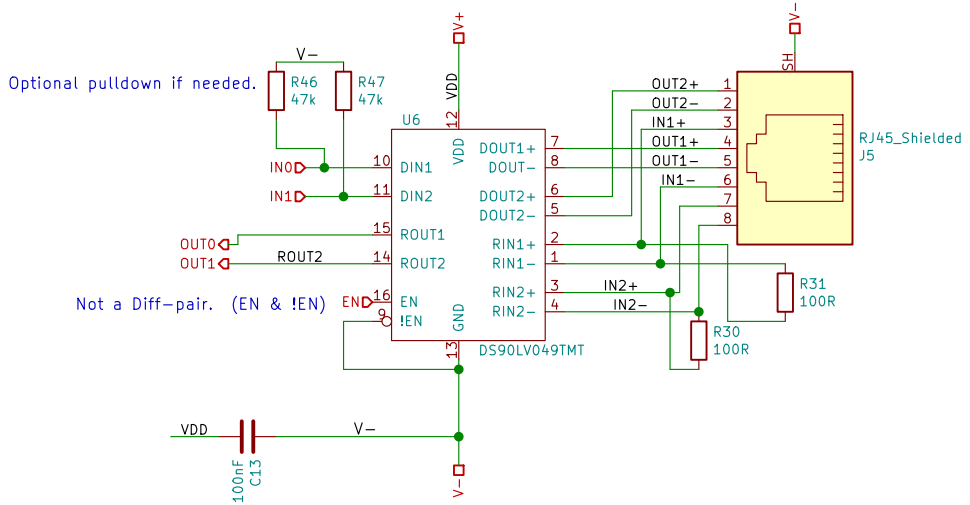
Size: A4	Date: 2018−12−31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 10/12

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /LVDS3/
File: file5C2628B0.sch

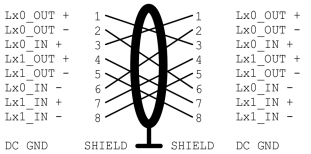
Title: LVDS <−> Xlinks

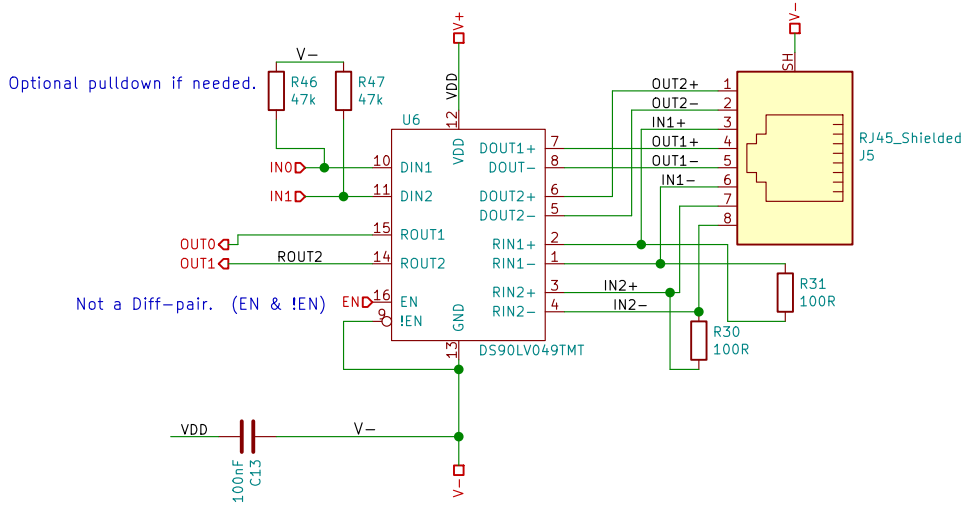
Size: A4	Date: 2018−12−31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 11/12

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /LVDS2/
File: file5C2628B0.sch

Title: LVDS <–> Xlinks

Size: A4	Date: 2018−12−31	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 12/12