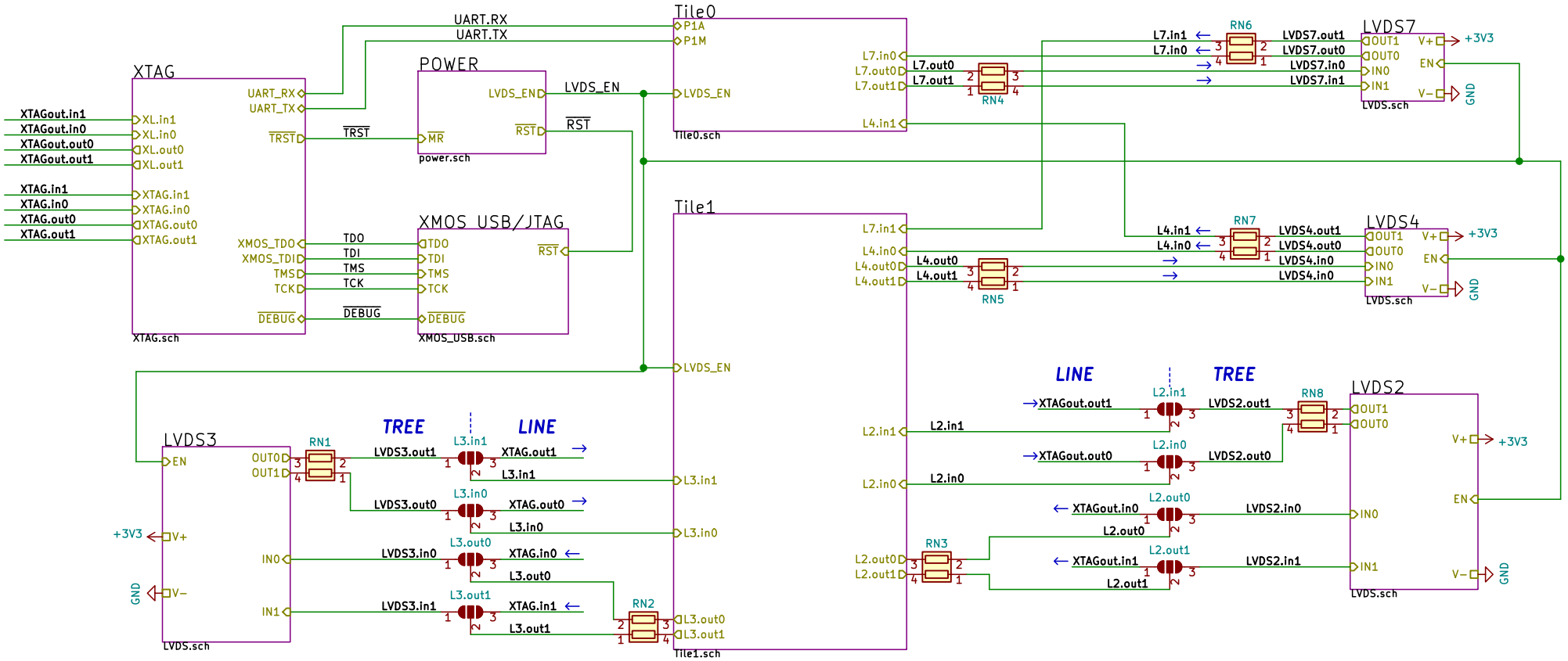
Board can be configured for Line or Tree/Star network.



Open Source
openPnP

Sheet: /
File: XMOS_XUF216_FB236.sch

Title: XMOS top level

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 1/16

RJ45 PINOUT:

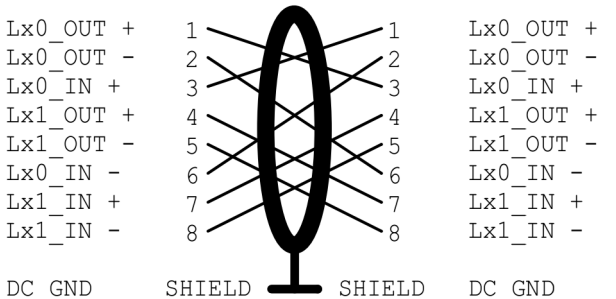
1/2 Lx0_OUT +/-

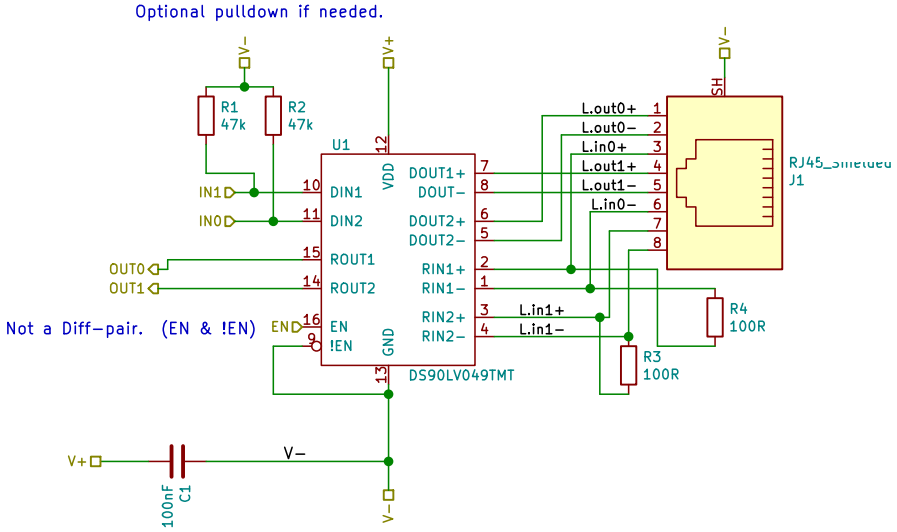
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

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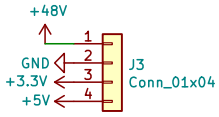
Sheet: /LVDS7/
File: LVDS.sch

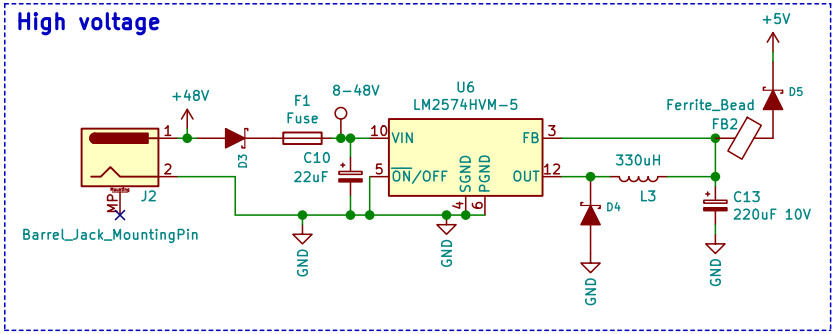
Title: LVDS <-> Xlinks

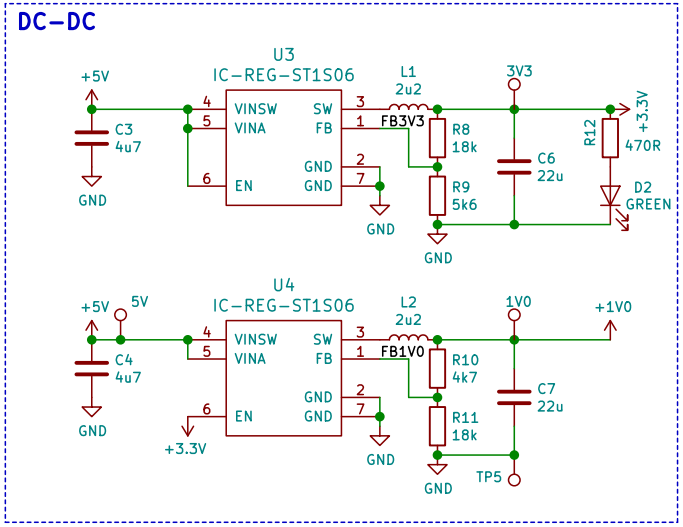
Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 2/16

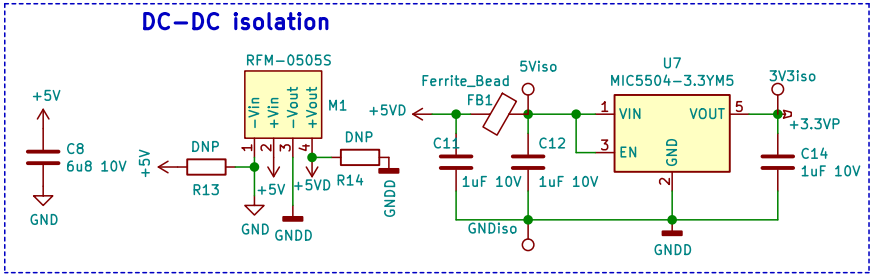
Cards can be power by USB or by the barrel jack 8–48V.
Alternative "+48V" can come from a connected daugther card.
Both USB and +48V should not be connected on the same PCB.
USB ground should be isolated from power ground for PC safety.

Power ports are Global in the schematics.

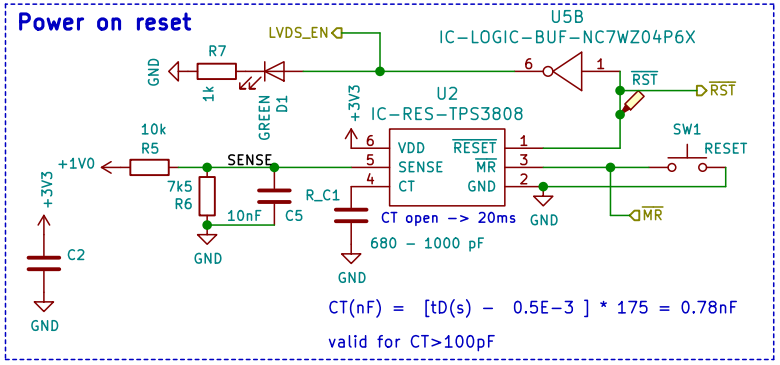


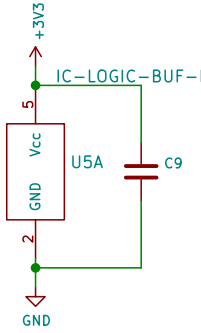






VDDIO/OTP_VCC and VDD can ramp up independently.
In order to reduce stresses on the device, it is preferable to make them ramp up in a short time frame of each other,
no more than 50 ms apart.
RST_N and TRST_N should be kept low until all power supplies are stable and within tolerances of their final voltage.
If your design is powered by VBUS, then RST_N should go high within 10 ms of attaching to VBUS in order to ensure that USB timings are met.
RST_N should be at least 1 ms after VDDIO good to enable the built–in flash to settle





Open Source
openPnP

Sheet: /POWER/
File: power.sch

Title: Power

Size: A4	Date: 2019–01–01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)–1		Id: 3/16

RJ45 PINOUT:

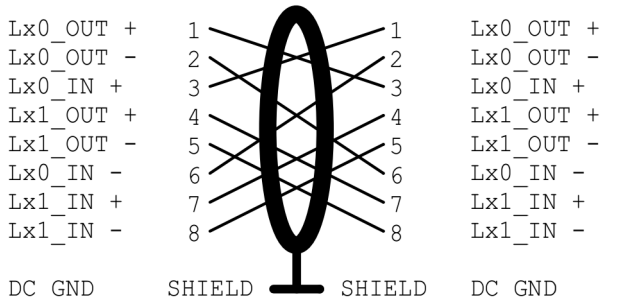
1/2 Lx0_OUT +/-

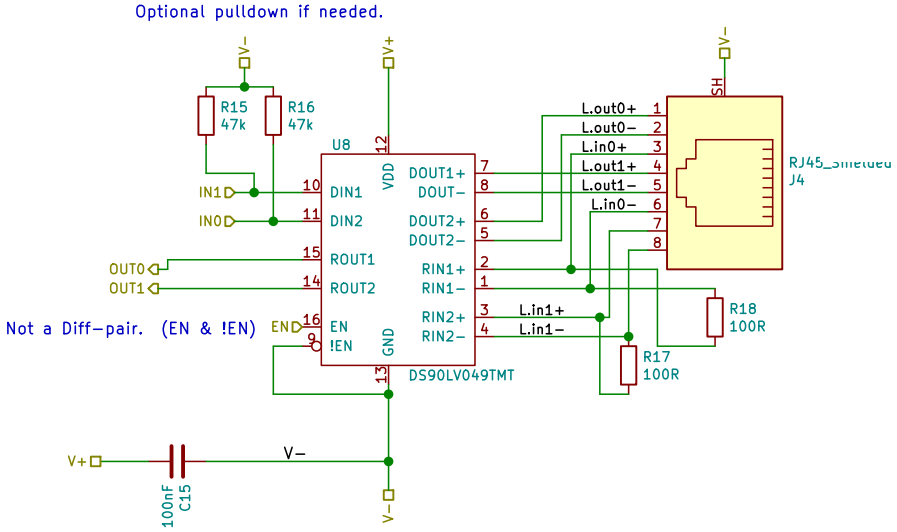
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

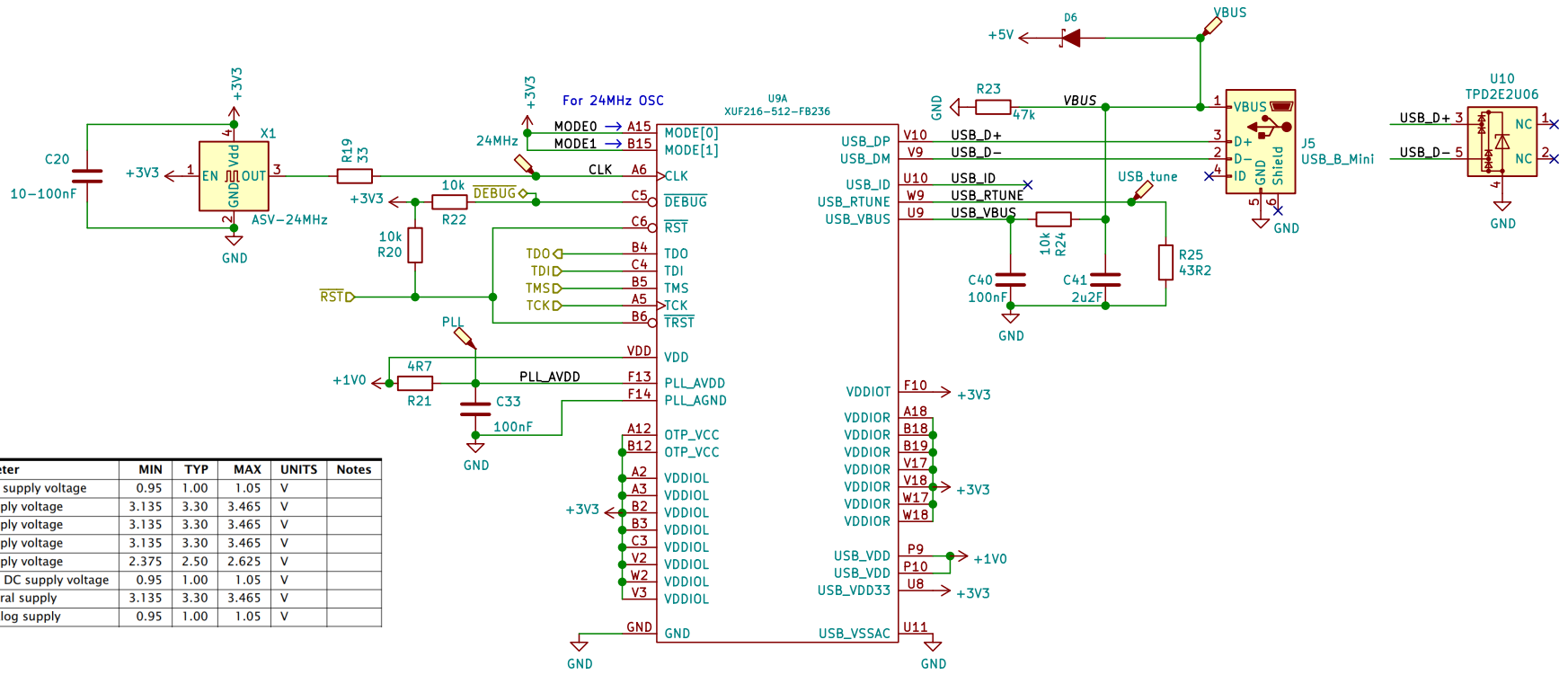
This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

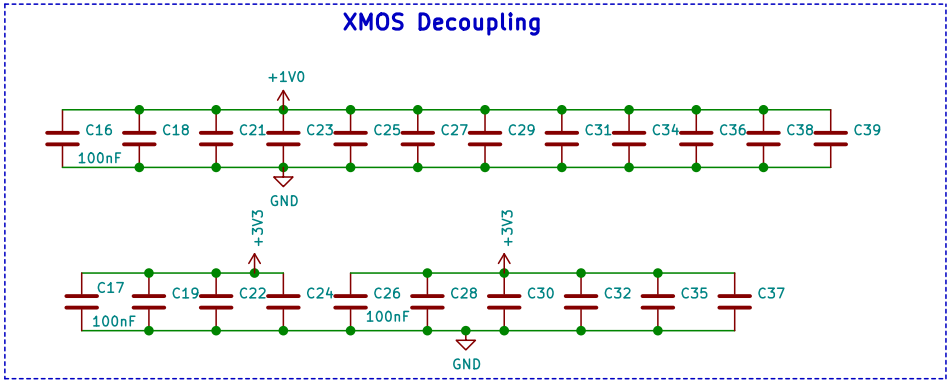
Sheet: /LVDS2/
File: LVDS.sch

Title: LVDS <-> Xlinks

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 4/16



Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD	Tile DC supply voltage	0.95	1.00	1.05	V	
VDDIOL	I/O supply voltage	3.135	3.30	3.465	V	
VDDIOR	I/O supply voltage	3.135	3.30	3.465	V	
VDDIOT 3v3	I/O supply voltage	3.135	3.30	3.465	V	
VDDIOT 2v5	I/O supply voltage	2.375	2.50	2.625	V	
USB_VDD	USB tile DC supply voltage	0.95	1.00	1.05	V	
VDD33	Peripheral supply	3.135	3.30	3.465	V	
PLL_AVDD	PLL analog supply	0.95	1.00	1.05	V	

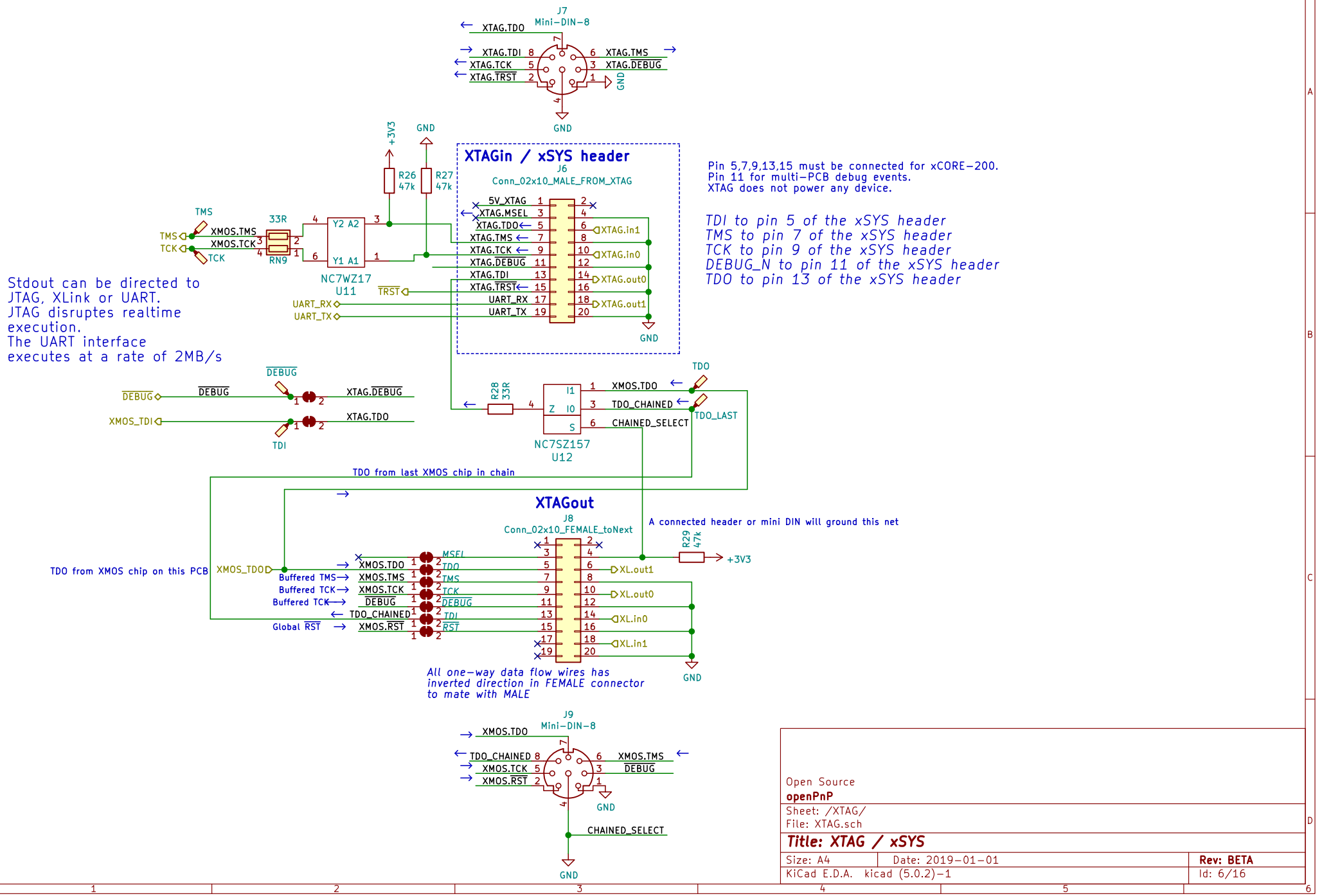


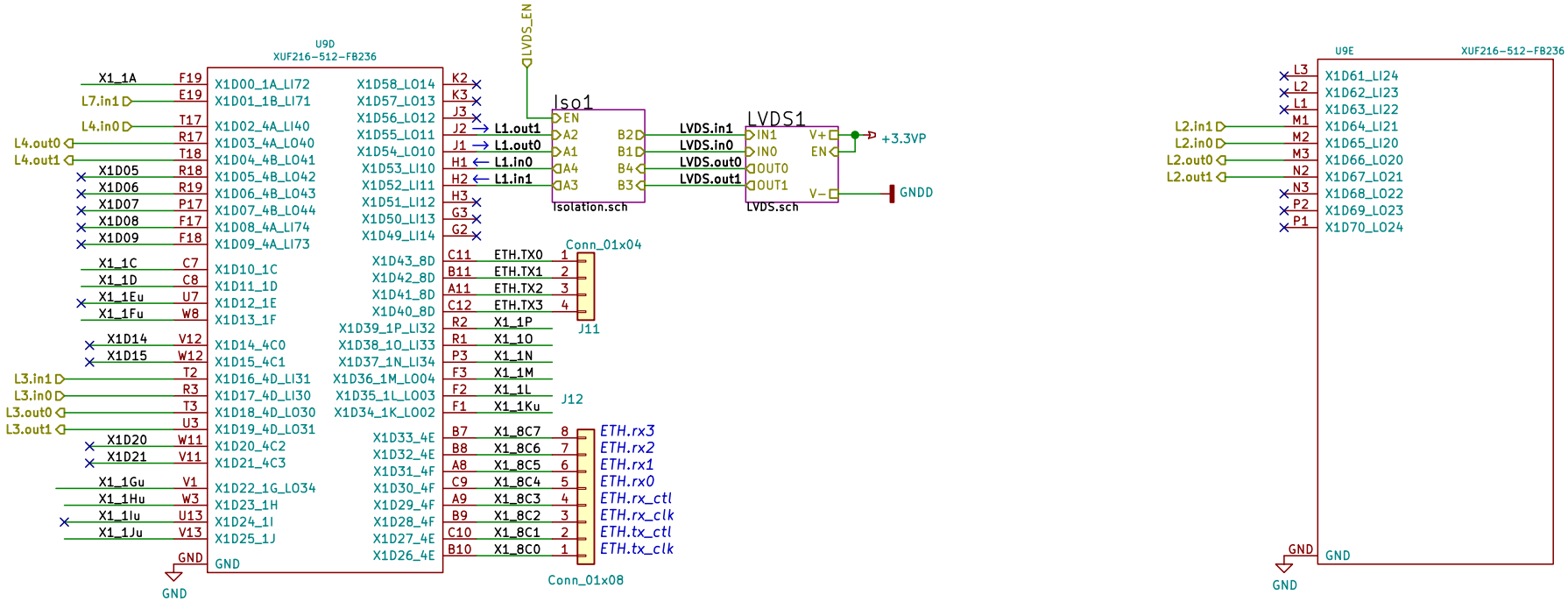
Open Source
openPnP

Sheet: /XMOS USB/JTAG/
File: XMOS_USB.sch

Title: XTAG & XMOS USB

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 5/16


J7
Mini-DIN-8
XTAG.TDO
XTAG.TDI
XTAG.TCK
XTAG.TRST
XTAG.TMS
XTAG.DEBUG
GND
+3V3
R26
47k
R27
47k
XTAGin / xSYS header
J6
Conn_02x10_MALE_FROM_XTAG
5V_XTAG
XTAG.MSEL
XTAG.in1
XTAG.in0
XTAG.out0
XTAG.out1
UART_RX
UART_TX
TMS
TCK
33R
RN9
Y2 A2
Y1 A1
NC7WZ17
U11
TRST
Pin 5,7,9,13,15 must be connected for xCORE-200.
Pin 11 for multi-PCB debug events.
XTAG does not power any device.
TDI to pin 5 of the xSYS header
TMS to pin 7 of the xSYS header
TCK to pin 9 of the xSYS header
DEBUG_N to pin 11 of the xSYS header
TDO to pin 13 of the xSYS header
Stdout can be directed to
JTAG, XLink or UART.
JTAG disruptes realtime
execution.
The UART interface
executes at a rate of 2MB/s
XMOS_TDI
TDI
R28
33R
NC7SZ157
U12
XMOS.TDO
TDO_CHAINED
CHAINED_SELECT
TDO_LAST
TDO from last XMOS chip in chain
XTAGout
J8
Conn_02x10_FEMALE_toNext
A connected header or mini DIN will ground this net
R29
47k
TDO from XMOS chip on this PCB
XMOS_TDO
Buffered TMS
Buffered TCK
Buffered TCK
Global RST
XMOS.TMS
XMOS.TCK
XMOS.RST
MSEL
TDO
TMS
TCK
DEBUG
TDI
RST
XL.out1
XL.out0
XL.in0
XL.in1
All one-way data flow wires has
inverted direction in FEMALE connector
to mate with MALE
J9
Mini-DIN-8
XMOS.TDO
TDO_CHAINED
XMOS.TCK
XMOS.RST
XMOS.TMS
DEBUG
CHAINED_SELECT
Open Source
openPnP
Sheet: /XTAG/
File: XTAG.sch
Title: XTAG / xSYS
Size: A4
Date: 2019-01-01
Rev: BETA
KiCad E.D.A. kicad (5.0.2)-1
Id: 6/16

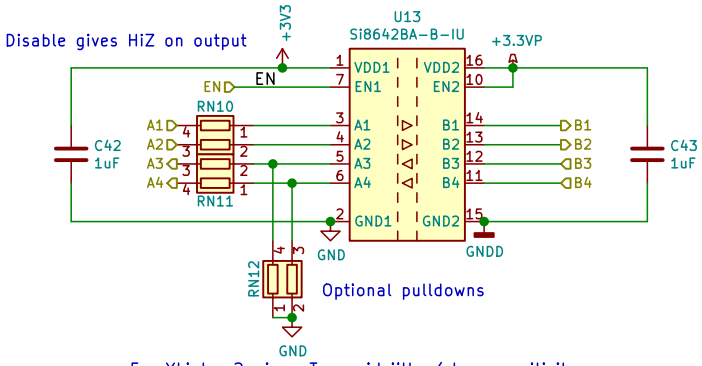


Open Source
openPnP

Sheet: /Tile1/
File: Tile1.sch

Title: XMOS Tile1

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 7/16



For XLinks-2 wire: To avoid jitter/skew sensitivity,
only one transition per clock cycle can happen within the pair.

Open Source
openPnP

Sheet: /Tile1/Iso1/
File: Isolation.sch

Title: Isolation

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 8/16

RJ45 PINOUT:

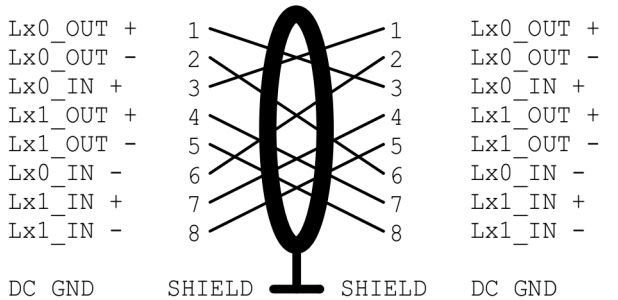
1/2 Lx0_OUT +/-

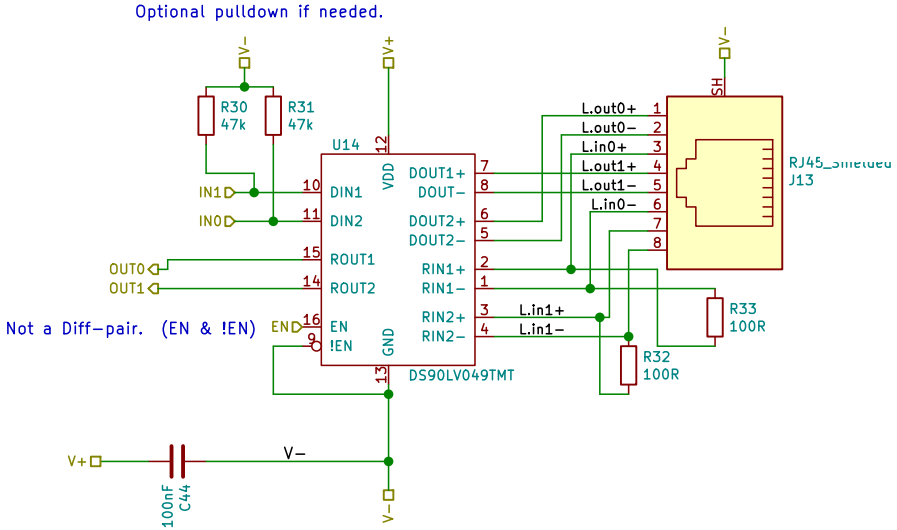
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /Tile1/LVDS1/
File: LVDS.sch

Title: LVDS <-> Xlinks

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 9/16

RJ45 PINOUT:

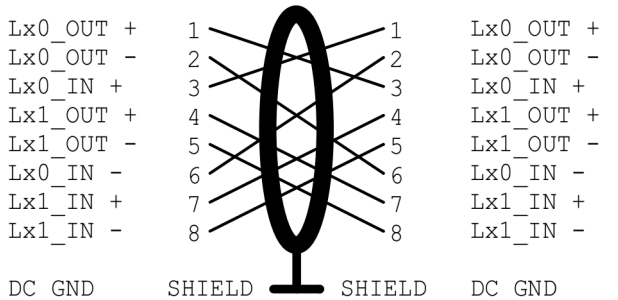
1/2 Lx0_OUT +/-

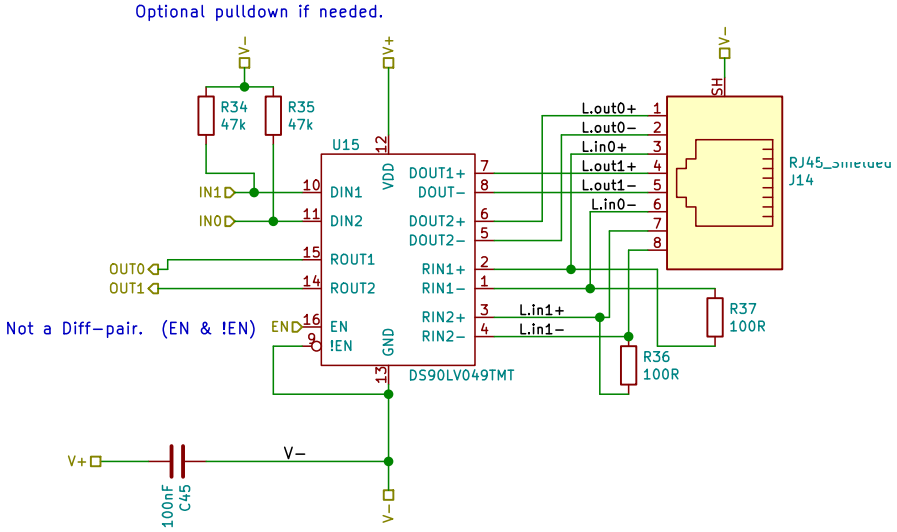
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

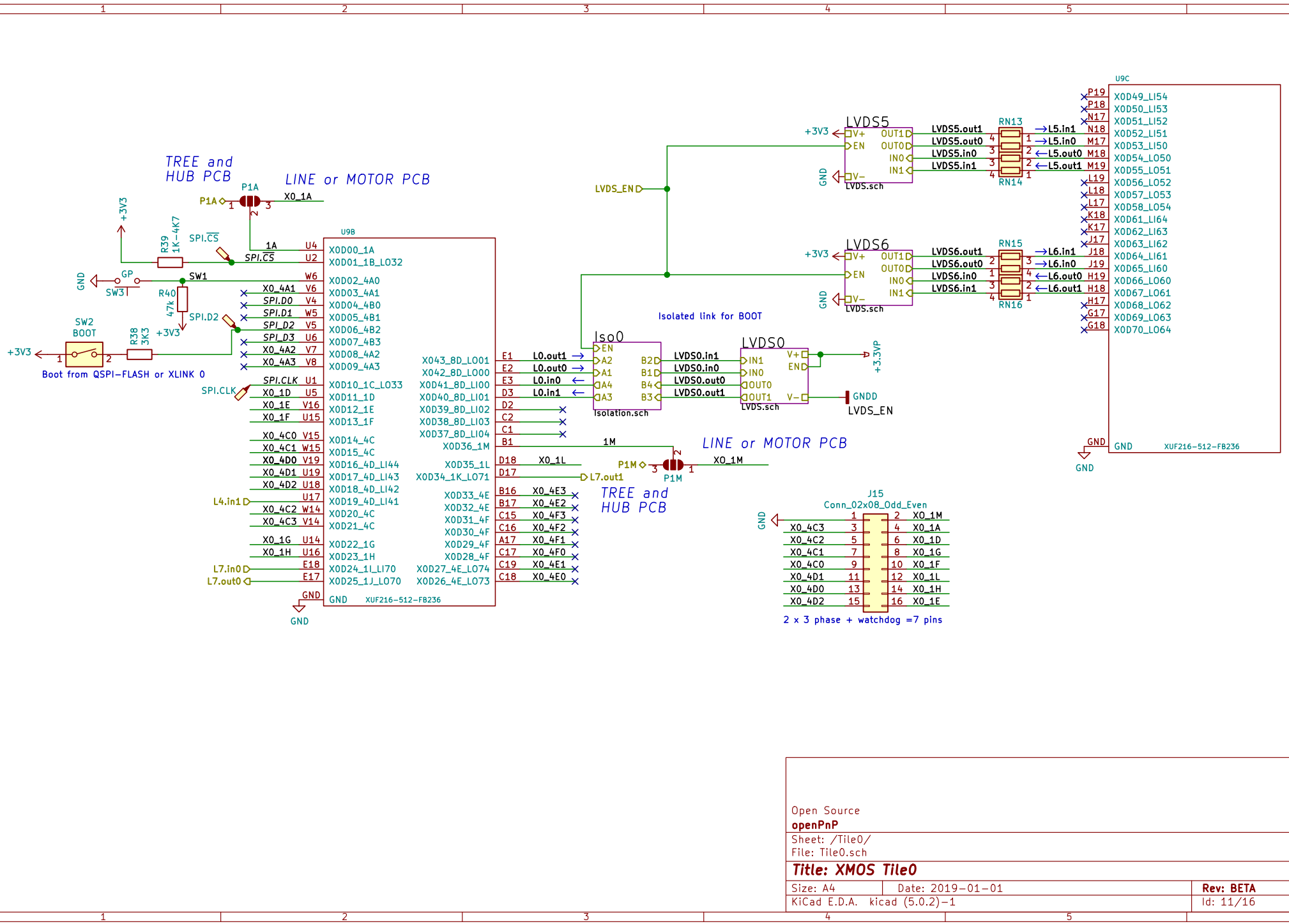
This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /LVDS4/
File: LVDS.sch

Title: LVDS <-> Xlinks

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 10/16


TREE and HUB PCB
LINE or MOTOR PCB
P1A
X0_1A
+3V3
R39 1K-4K7
SPI.CS
U9B
X0D00_1A
X0D01_1B_LO32
GND
GP
SW1
SW3
R40 47k
SPI.D2
SW2 BOOT
R38 3K3
Boot from QSPI-FLASH or XLINK 0
SPI.CLK
X0_4A1 V6
SPI.D0 V4
SPI.D1 W5
SPI_D2 V5
SPI_D3 U6
X0_4A2 V7
X0_4A3 V8
X0_1D U5
X0_1E V16
X0_1F U15
X0_4C0 V15
X0_4C1 W15
X0_4D0 V19
X0_4D1 U19
X0_4D2 U18
L4.in1
X0_4C2 W14
X0_4C3 V14
X0_1G U14
X0_1H U16
L7.in0
L7.out0
X0D02_4A0
X0D03_4A1
X0D04_4B0
X0D05_4B1
X0D06_4B2
X0D07_4B3
X0D08_4A2
X0D09_4A3
X0D10_1C_LO33
X0D11_1D
X0D12_1E
X0D13_1F
X0D14_4C
X0D15_4C
X0D16_4D_LI44
X0D17_4D_LI43
X0D18_4D_LI42
X0D19_4D_LI41
X0D20_4C
X0D21_4C
X0D22_1G
X0D23_1H
X0D24_1I_LI70
X0D25_1J_LO70
X0D43_8D_LO01
X0D42_8D_LO00
X0D41_8D_LI00
X0D40_8D_LI01
X0D39_8D_LI02
X0D38_8D_LI03
X0D37_8D_LI04
X0D36_1M
X0D35_1L
X0D34_1K_LO71
X0D33_4E
X0D32_4E
X0D31_4F
X0D30_4F
X0D29_4F
X0D28_4F
X0D27_4E_LO74
X0D26_4E_LO73
XUF216-512-FB236
LVDS_EN
Iso0
E1 LO.out1
E2 LO.out0
E3 LO.in0
D3 LO.in1
B2 LVDS0.in1
B1 LVDS0.in0
B4 LVDS0.out0
B3 LVDS0.out1
Isolation.sch
LVDS0
LVDS.sch
+3.3VP
GNDD
Isolated link for BOOT
1M
D18 X0_1L
D17 L7.out1
P1M
X0_1M
B16 X0_4E3
B17 X0_4E2
C15 X0_4F3
C16 X0_4F2
A17 X0_4F1
C17 X0_4F0
C19 X0_4E1
C18 X0_4E0
LVDS5
LVDS5.out1
LVDS5.out0
LVDS5.in0
LVDS5.in1
RN13
RN14
L5.in1
L5.in0
L5.out0
L5.out1
LVDS6
LVDS6.out1
LVDS6.out0
LVDS6.in0
LVDS6.in1
RN15
RN16
L6.in1
L6.in0
L6.out0
L6.out1
U9C
P19 X0D49_LI54
P18 X0D50_LI53
N17 X0D51_LI52
N18 X0D52_LI51
M17 X0D53_LI50
M18 X0D54_LO50
M19 X0D55_LO51
L19 X0D56_LO52
L18 X0D57_LO53
L17 X0D58_LO54
K18 X0D61_LI64
K17 X0D62_LI63
J17 X0D63_LI62
J18 X0D64_LI61
J19 X0D65_LI60
H19 X0D66_LO60
H18 X0D67_LO61
H17 X0D68_LO62
G17 X0D69_LO63
G18 X0D70_LO64
J15
Conn_02x08_Odd_Even
2 x 3 phase + watchdog =7 pins
Open Source
openPnP
Sheet: /Tile0/
File: Tile0.sch
Title: XMOS Tile0
Size: A4
Date: 2019-01-01
Rev: BETA
KiCad E.D.A. kicad (5.0.2)-1
Id: 11/16

RJ45 PINOUT:

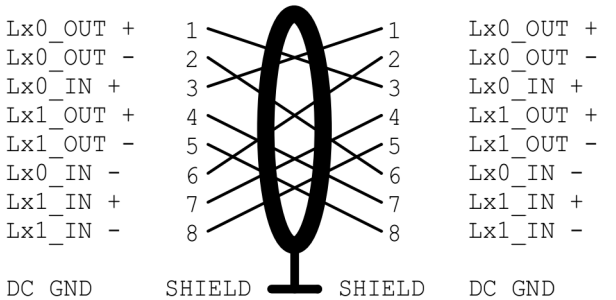
1/2 Lx0_OUT +/-

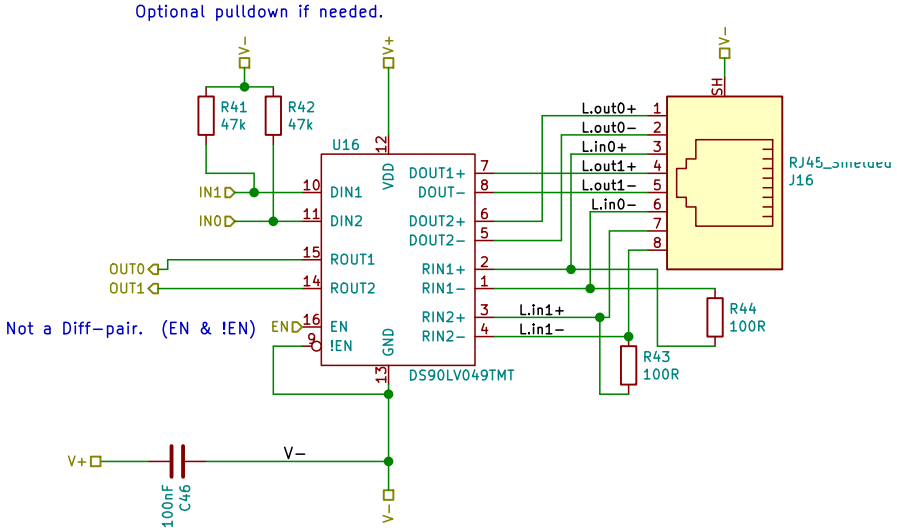
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /Tile0/LVDS6/
File: LVDS.sch

Title: LVDS <-> Xlinks

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 12/16

RJ45 PINOUT:

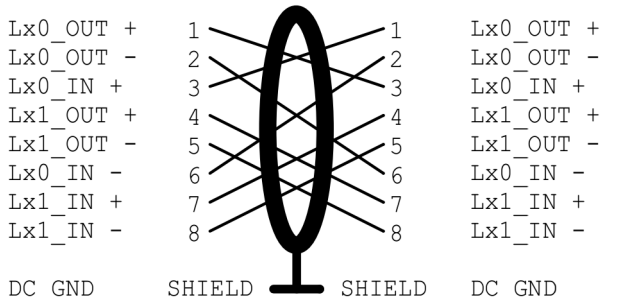
1/2 Lx0_OUT +/-

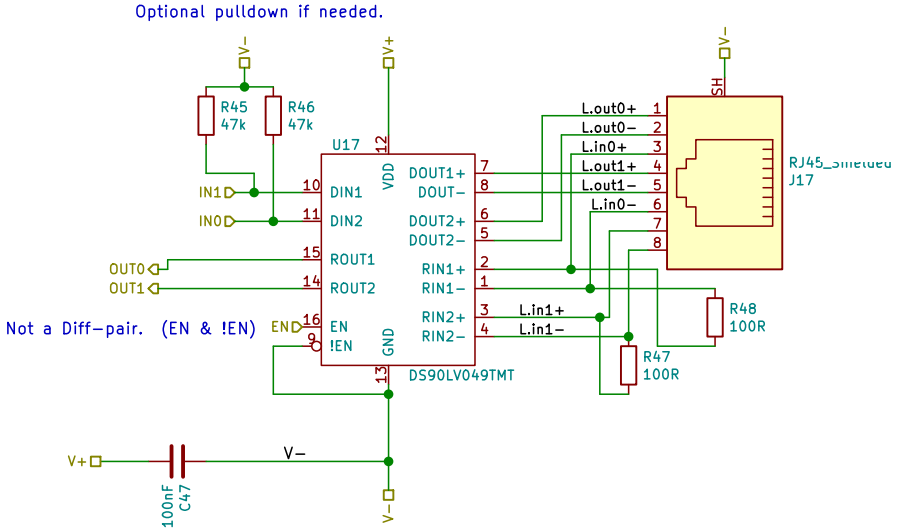
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /Tile0/LVDS5/
File: LVDS.sch

Title: LVDS <-> Xlinks

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 13/16

RJ45 PINOUT:

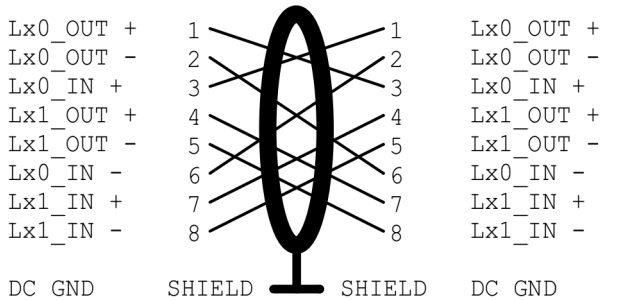
1/2 Lx0_OUT +/-

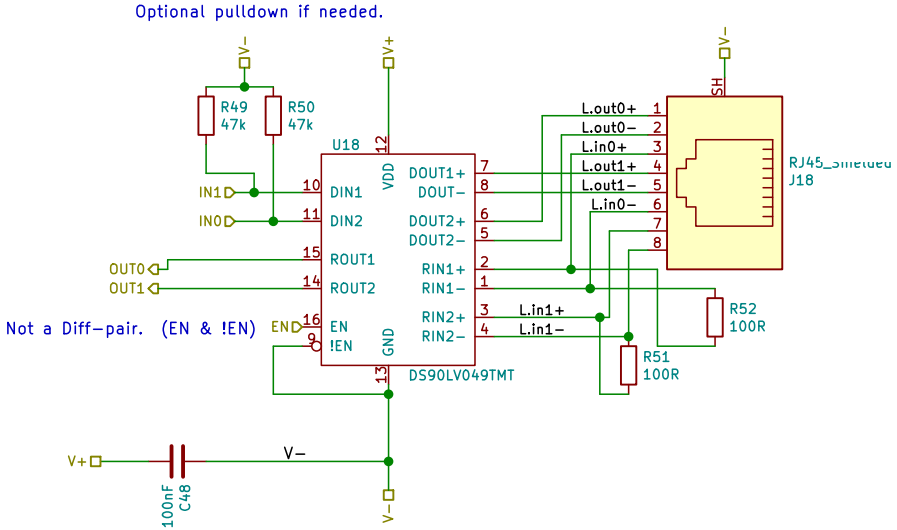
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

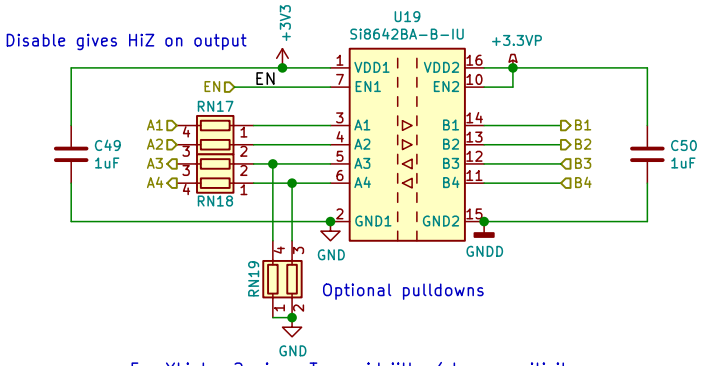
This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

Open Source
openPnP

Sheet: /Tile0/LVDS0/
File: LVDS.sch

Title: LVDS <-> Xlinks

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 14/16



For XLinks-2 wire: To avoid jitter/skew sensitivity,
only one transition per clock cycle can happen within the pair.

Open Source
openPnP

Sheet: /Tile0/Iso0/
File: Isolation.sch

Title: Isolation

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 15/16

RJ45 PINOUT:

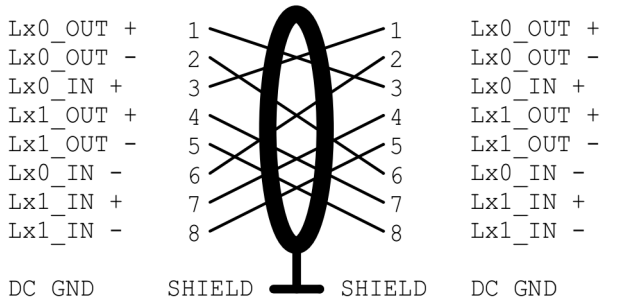
1/2 Lx0_OUT +/-

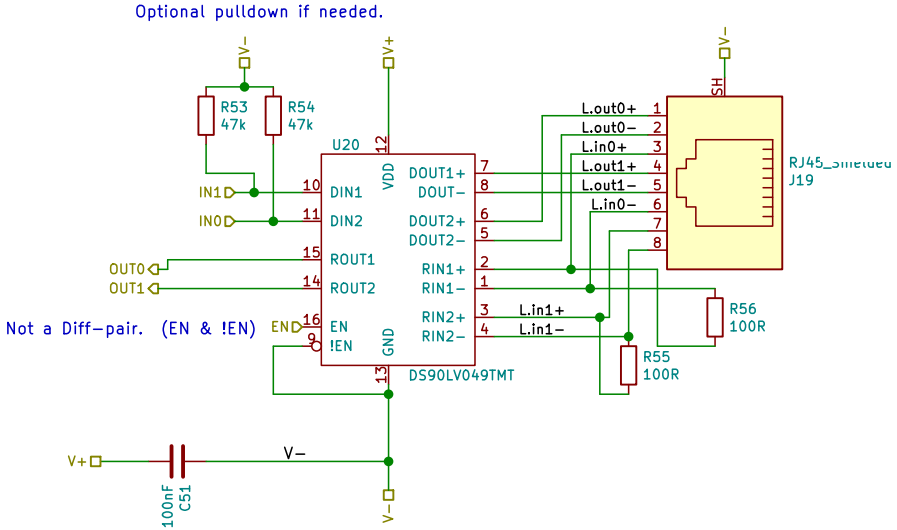
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





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Open Source
openPnP

Sheet: /LVDS3/
File: LVDS.sch

Title: LVDS <-> Xlinks

Size: A4	Date: 2019-01-01	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 16/16