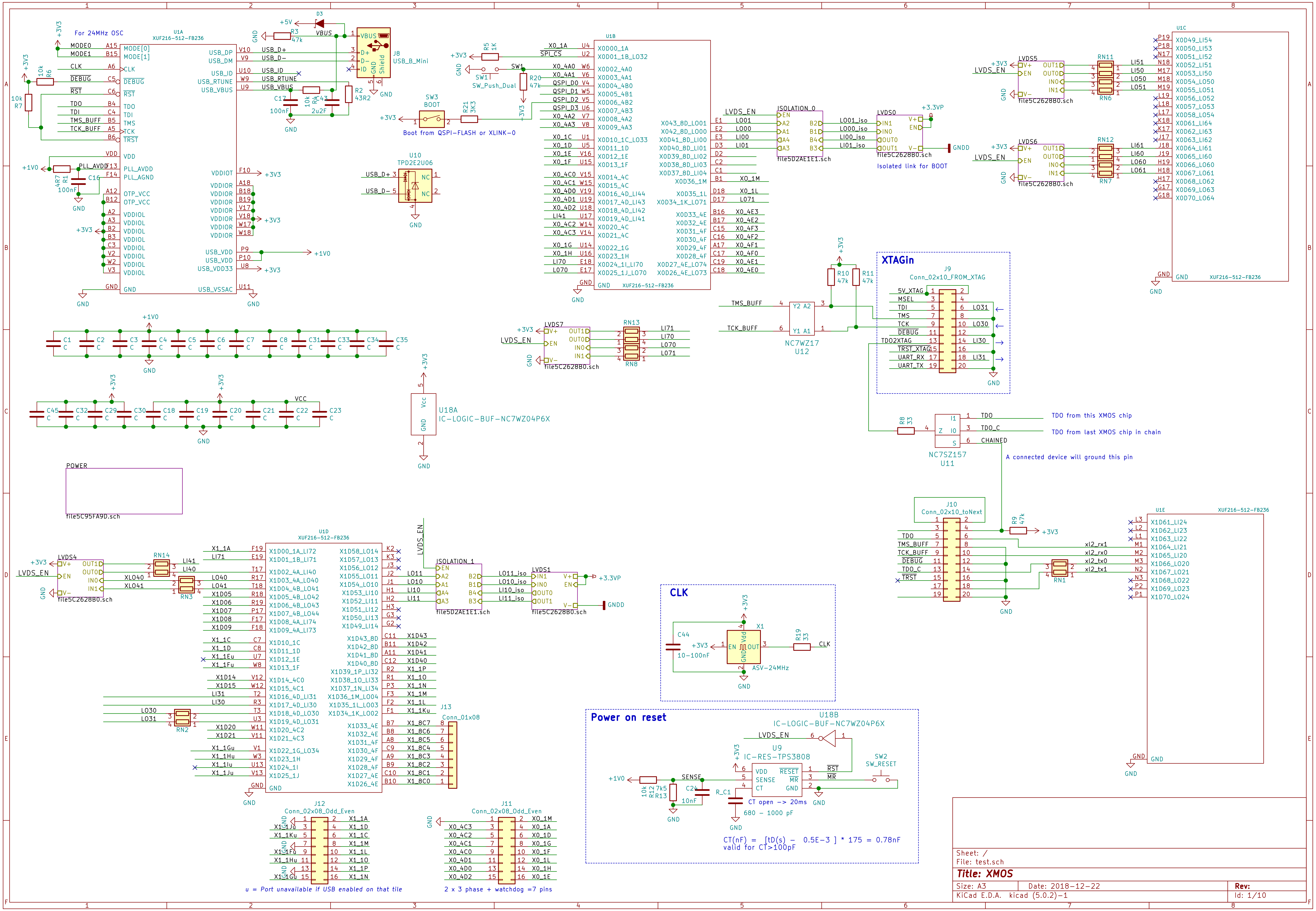


For 24MHz OSC
XUF216-512-FB236
USB_B_Mini
Boot from QSPI-FLASH or XLINK-0
Isolated link for BOOT
XTAGin
Conn_02x10_FROM_XTAG
TDO from this XMOS chip
TDO from last XMOS chip in chain
A connected device will ground this pin
NC7WZ17
NC7SZ157
IC-LOGIC-BUF-NC7WZ04P6X
POWER
file5C95FA9D.sh
Conn_02x10_toNext
CLK
ASV-24MHz
10-100nF
Power on reset
IC-RES-TPS3808
SW_RESET
CT open -> 20ms
680 - 1000 pF
CT(nF) = [tD(s) - 0.5E-3] * 175 = 0.78nF
valid for CT>100pF
Conn_02x08_Odd_Even
u = Port unavailable if USB enabled on that tile
2 x 3 phase + watchdog =7 pins
Conn_01x08
Sheet: /
File: test.sch
Title: XMOS
Size: A3
Date: 2018-12-22
Rev:
KiCad E.D.A. kicad (5.0.2)-1
Id: 1/10

RJ45 PINOUT:

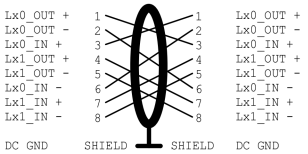
1/2 Lx0_OUT +/-

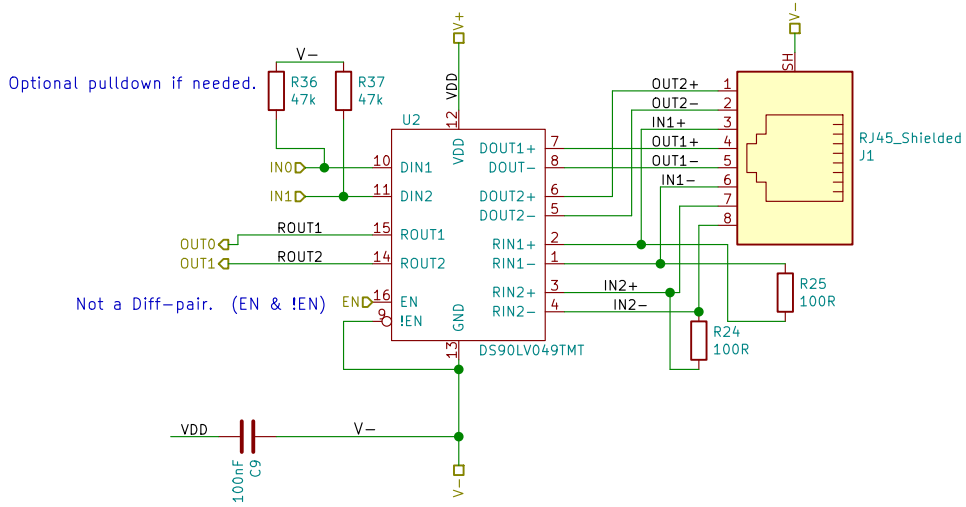
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
XLink input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

Sheet: /LVDS0/
File: file5C2628B0.sch

Title:

Size: A4 | Date: | **Rev:**

KiCad E.D.A. kicad (5.0.2)−1 | Id: 2/10

RJ45 PINOUT:

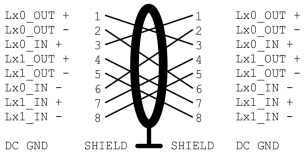
1/2 Lx0_OUT +/-

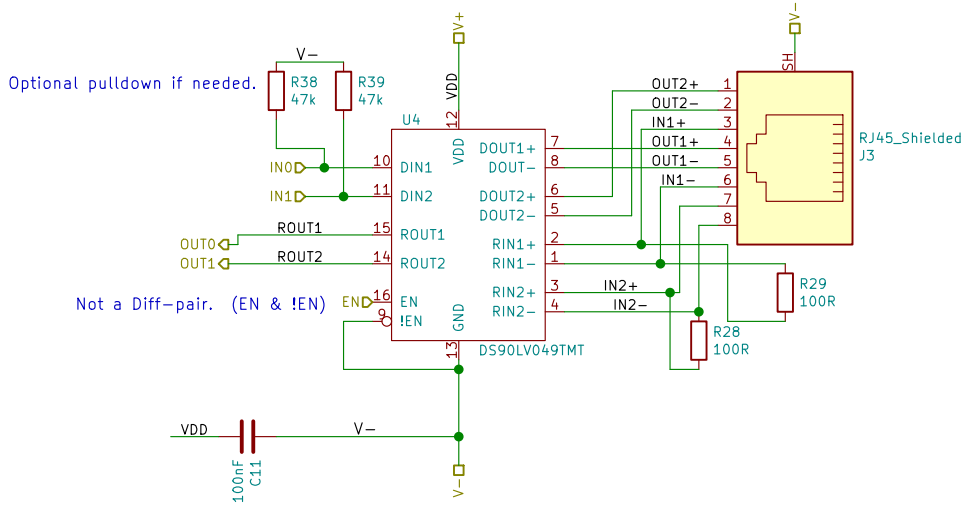
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
XLink input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

Sheet: /LVDS4/
File: file5C2628B0.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.0.2)−1		Id: 3/10

RJ45 PINOUT:

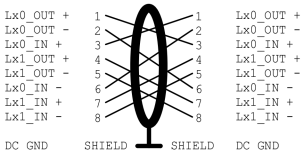
1/2 Lx0_OUT +/-

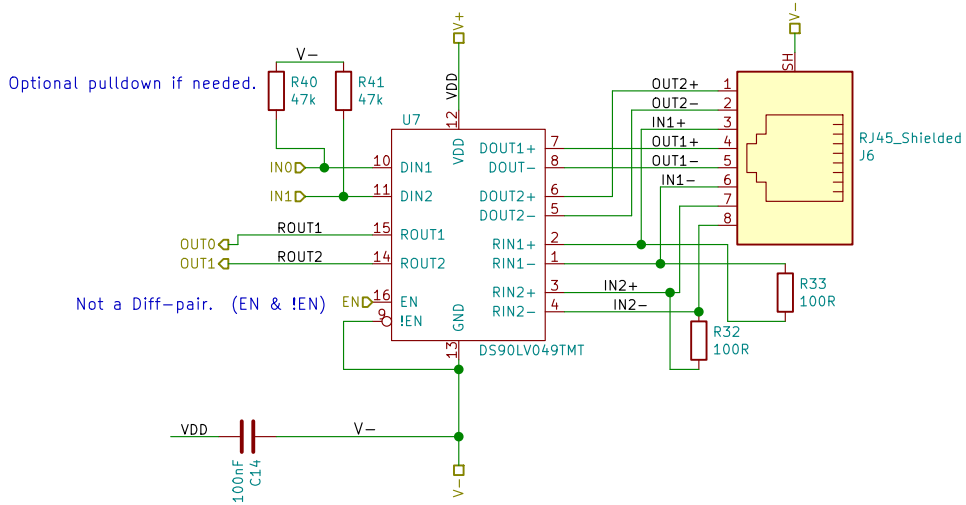
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
XLink input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

Sheet: /LVDS6/
File: file5C2628B0.sch

Title:

Size: A4 | Date: | **Rev:**

KiCad E.D.A. kicad (5.0.2)−1 | Id: 4/10

RJ45 PINOUT:

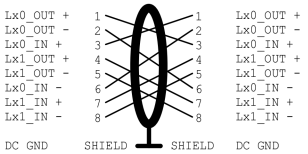
1/2 Lx0_OUT +/-

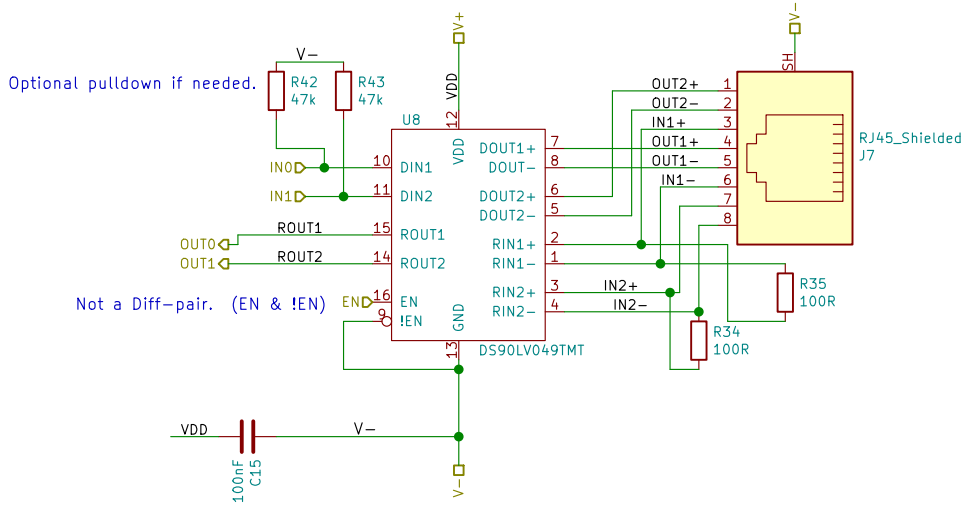
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

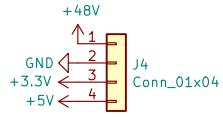
CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE

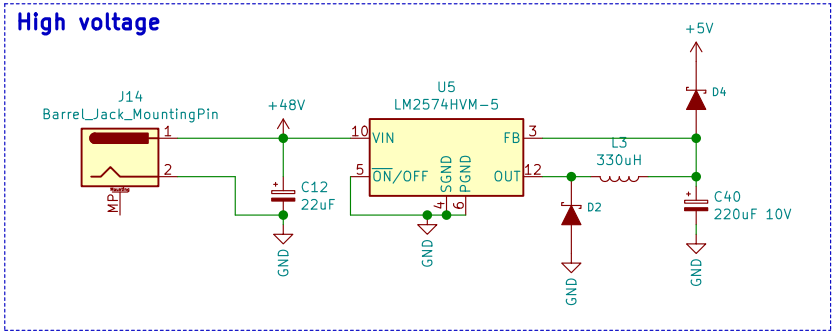


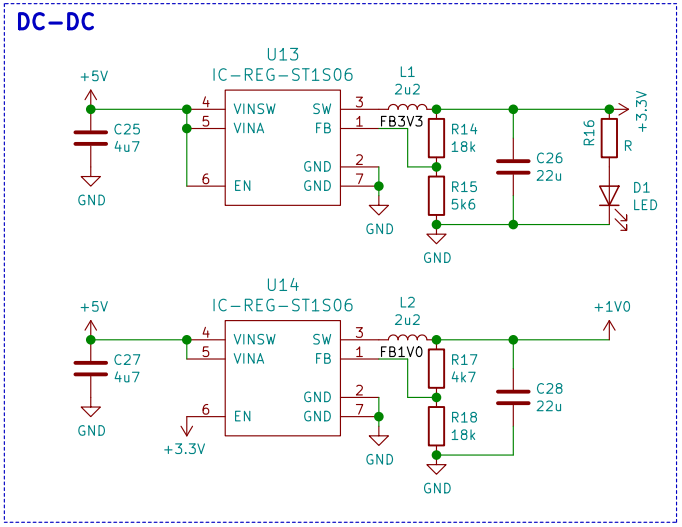


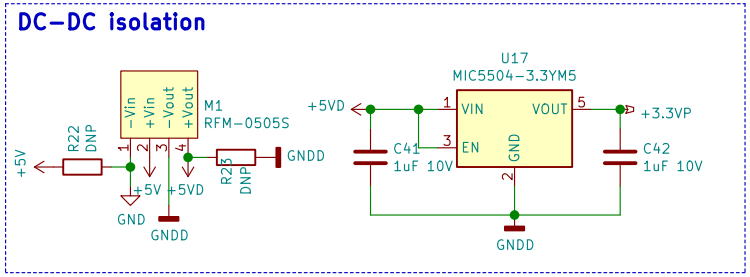
Unconnected LVDS input gives HI out on TTL side.
XLink input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

Sheet: /LVDS7/		
File: file5C2628B0.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.0.2)−1		Id: 5/10

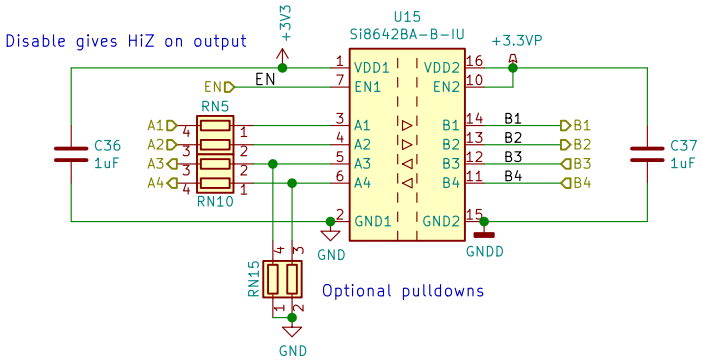






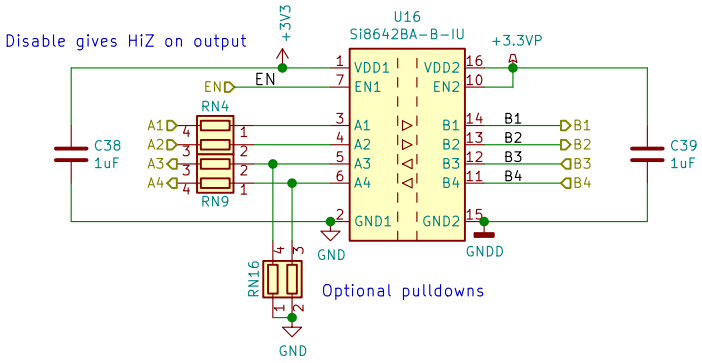


Sheet: /POWER/ File: file5C95FA9D.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.0.2)-1		Id: 6/10



On XLinks-2 wire, only one transition per clock cycle can happen within the pair, to avoid jitter/skew sensitivity.

Sheet: /ISOLATION_0/		
File: file5D2AE1E1.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.0.2)-1		Id: 7/10



On XLinks-2 wire, only one transition per clock cycle can happen within the pair, to avoid jitter/skew sensitivity.

Sheet: /ISOLATION_1/ File: file5D2AE1E1.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.0.2)-1		Id: 8/10

RJ45 PINOUT:

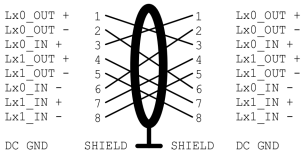
1/2 Lx0_OUT +/-

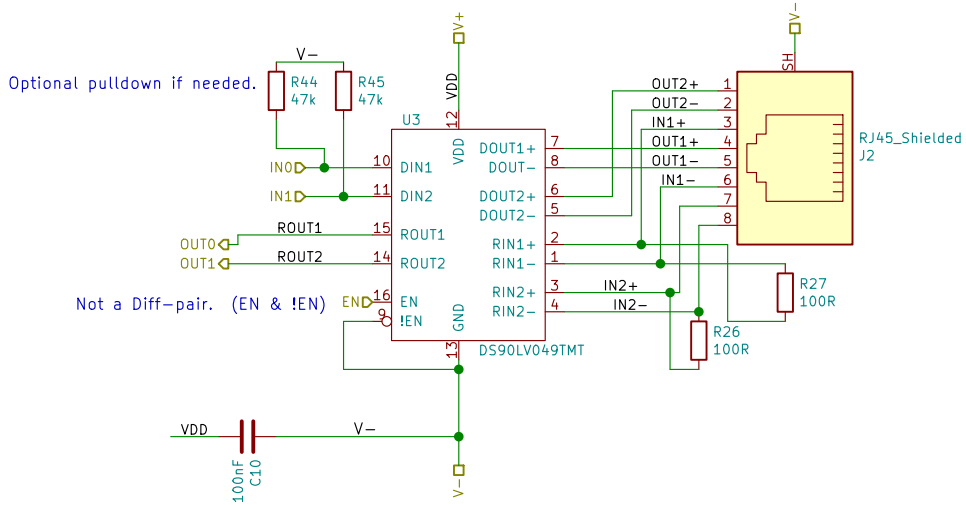
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

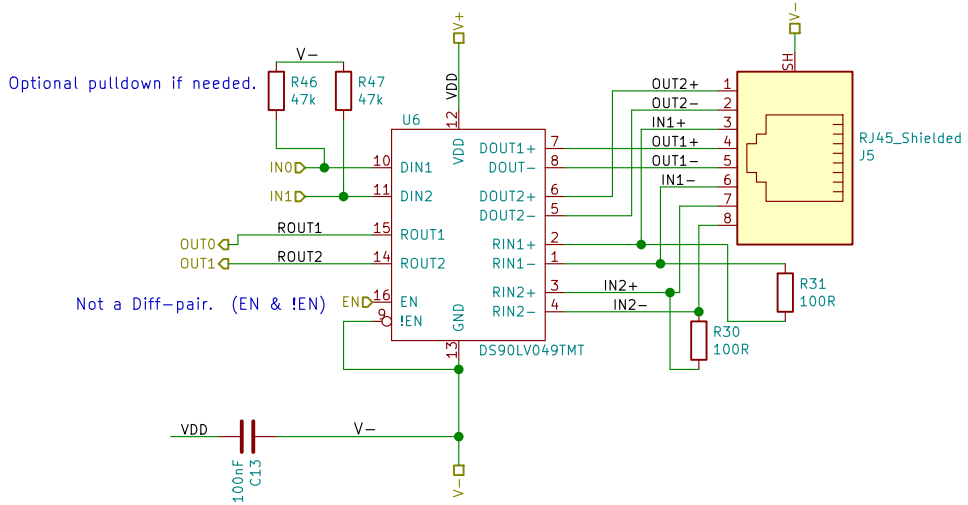
CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
XLink input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

Sheet: /LVDS1/ File: file5C2628B0.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.0.2)−1		Id: 9/10

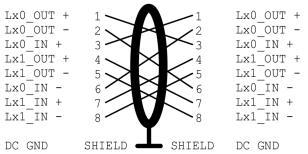


Unconnected LVDS input gives HI out on TTL side.
XLink input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE



Sheet: /LVDS5/
File: file5C2628B0.sch

Title:

Size: A4 | Date: | **Rev:**
KiCad E.D.A. kicad (5.0.2)−1 | Id: 10/10