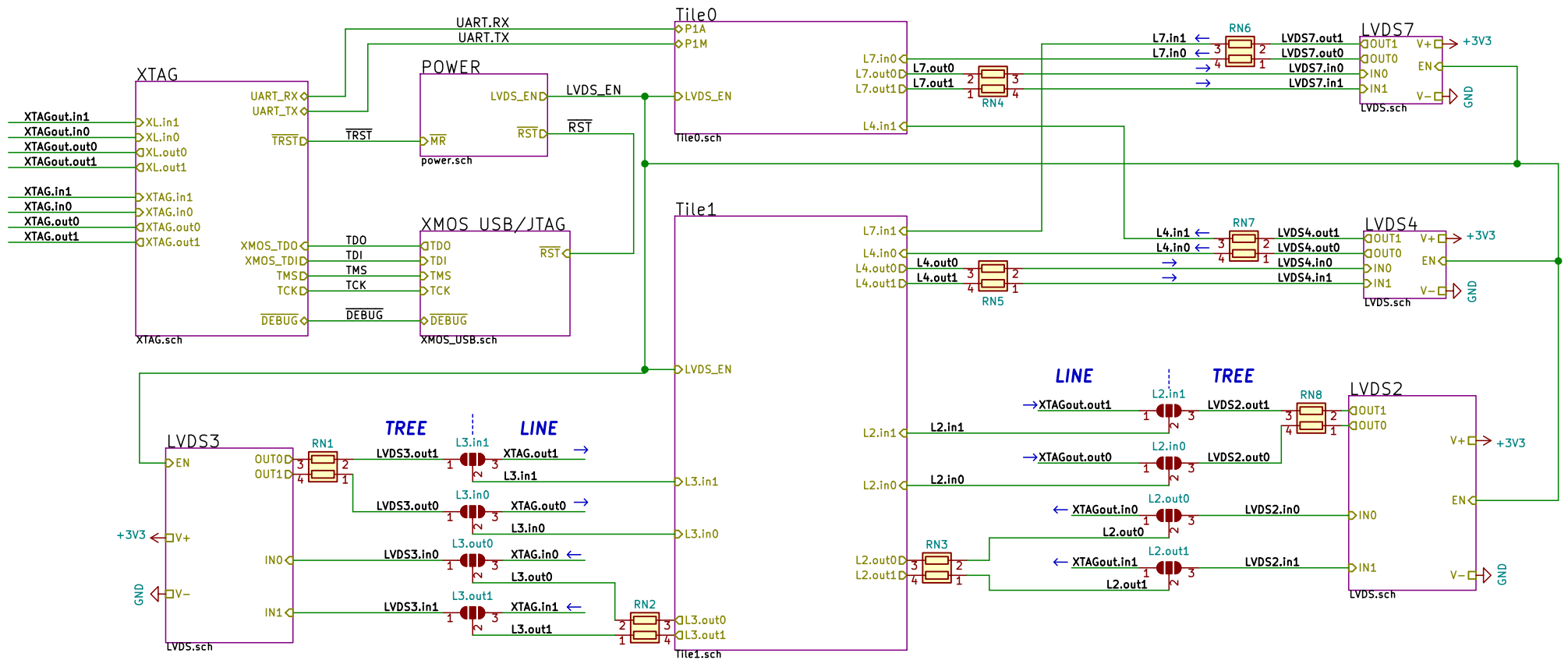


**Board can be configured for
Line or Tree/Star network.**



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Sheet: /
File: XMOS_XUF216_FB236.sch

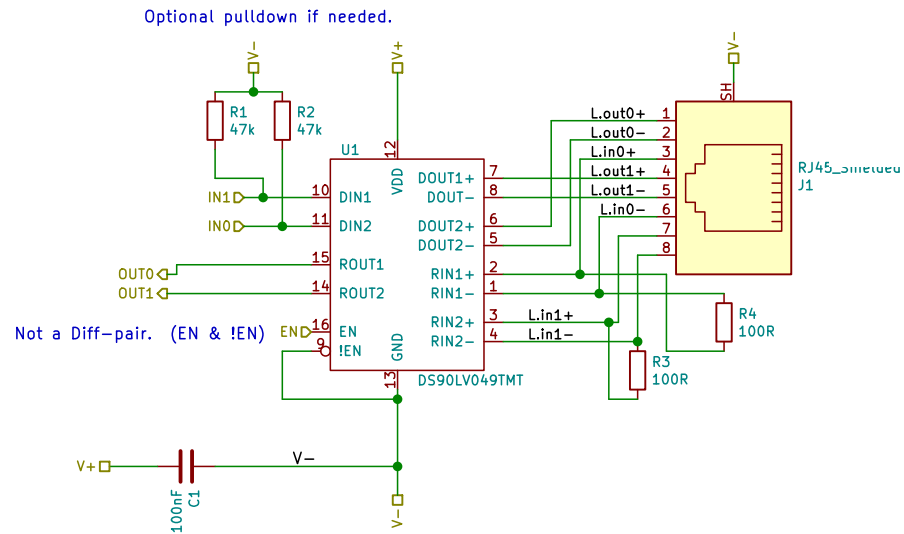
Title: XMOS top level

Size: A4 Date: 2019-01-03

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Rev: BETA

Id: 1/16



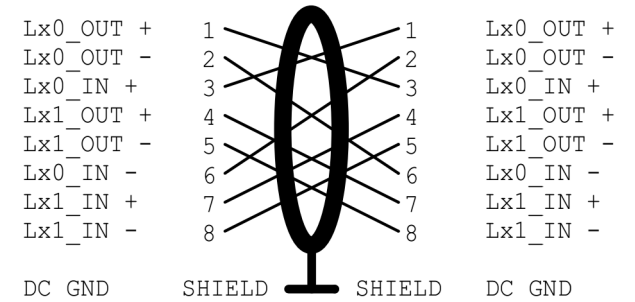
Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMO pins has internal pullup.
Transceiver needs to be in HiZ during XMO reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

RJ45 PINOUT:

1/2 Lx0_OUT +/-
3/6 Lx0_IN +/-
4/5 Lx1_OUT +/-
7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE



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openPnP

Sheet: /LVDS7/
File: LVDS.sch

Title: LVDS <--> Xlinks

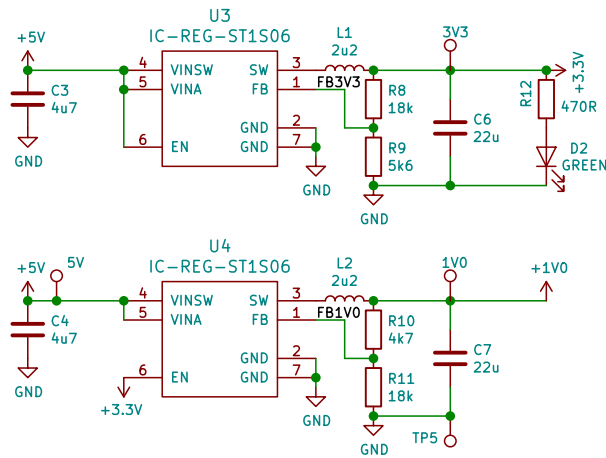
Size: A4 Date: 2019-01-03
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Rev: BETA
Id: 2/16

Cards can be power by USB or by the barrel jack 8-48V.
Alternative "+48V" can come from a connected daughter card.
Both USB and +48V should not be connected on the same PCB.
USB ground should be isolated from power ground for PC safety.

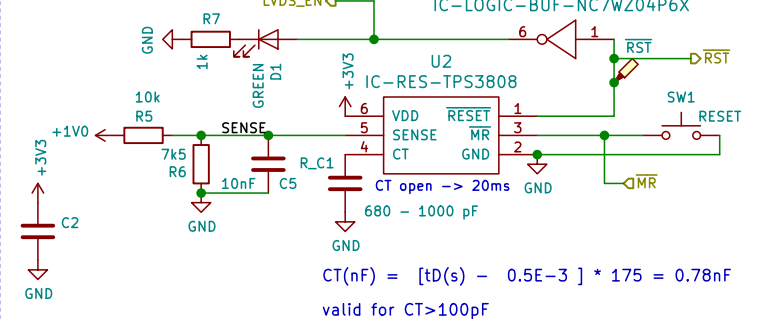
Power ports are Global in the schematics.

DC-DC



VDDIO/OTP_VCC and VDD can ramp up independently.
In order to reduce stresses on the device, it is preferable to make them ramp up in a short time frame of each other,
no more than 50 ms apart.
RST_N and TRST_N should be kept low until all power supplies are stable and within tolerances of their final voltage.
If your design is powered by VBUS, then RST_N should go high within 10 ms of attaching to VBUS in order to ensure that USB timings are met.
RST_N should be at least 1 ms after VDDIO good to enable the built-in flash to settle

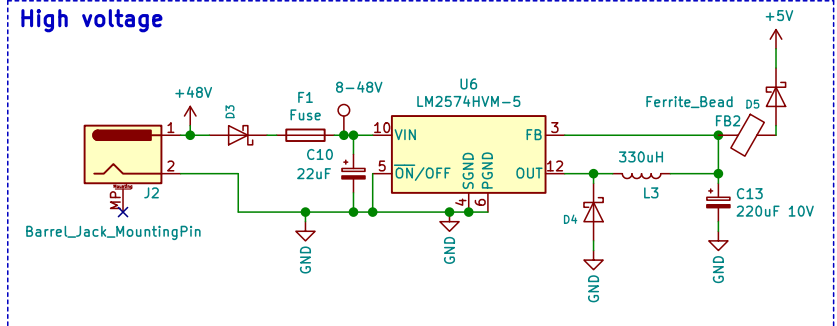
Power on reset



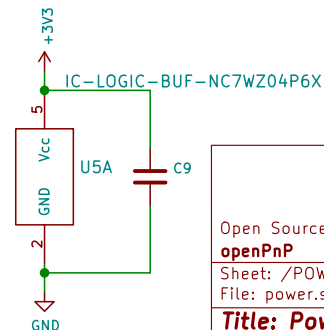
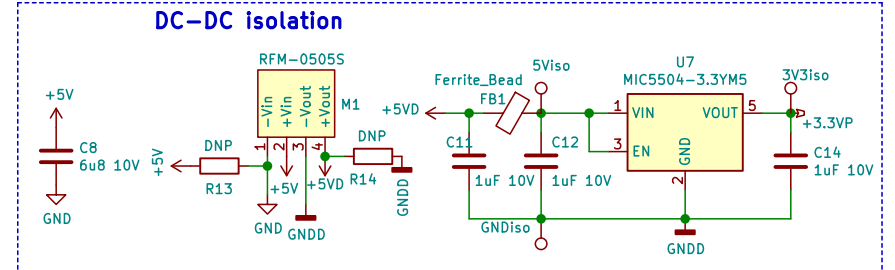
$$CT(nF) = [tD(s) - 0.5E-3] * 175 = 0.78nF$$

valid for CT>100pF

High voltage



DC-DC isolation



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Sheet: /POWER/
File: power.sch

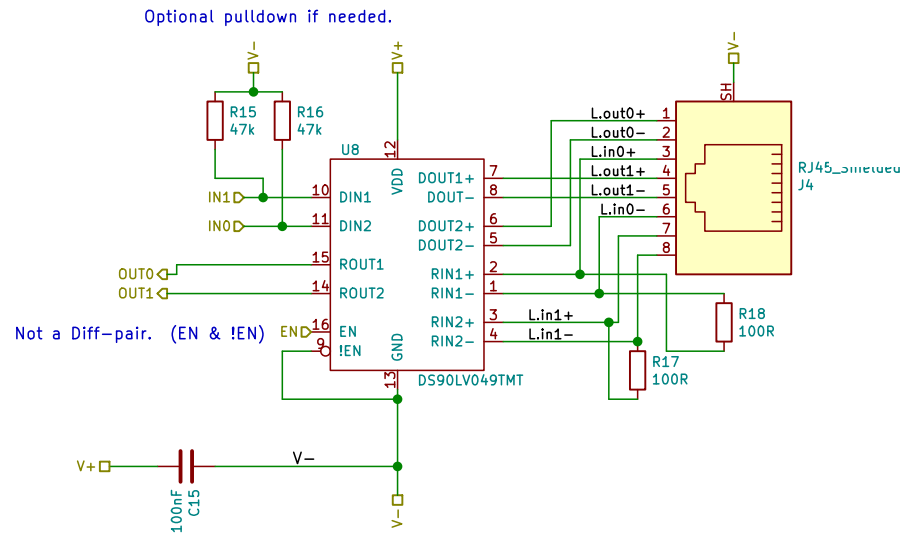
Title: Power

Size: A4 Date: 2019-01-03

KiCad E.D.A. kicad (5.0.2)-1

Rev: BETA

Id: 3/16



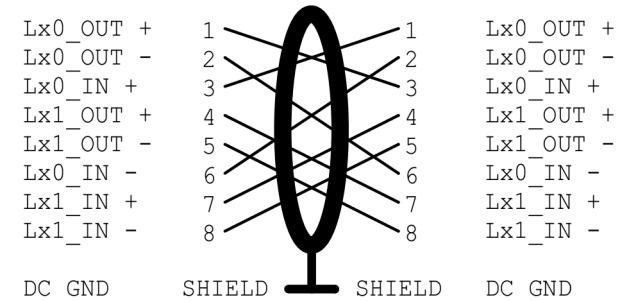
Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMO pins has internal pullup.
Transceiver needs to be in HiZ during XMO reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

RJ45 PINOUT:

1/2 Lx0_OUT +/-
3/6 Lx0_IN +/-
4/5 Lx1_OUT +/-
7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE



Open Source
openPnP

Sheet: /LVDS2/
File: LVDS.sch

Title: LVDS <--> Xlinks

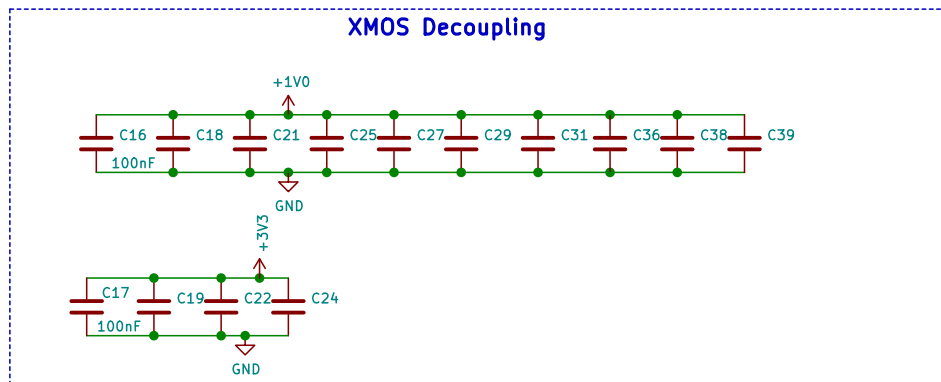
Size: A4 Date: 2019-01-03

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Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD	Tile DC supply voltage	0.95	1.00	1.05	V	
VDDIOL	I/O supply voltage	3.135	3.30	3.465	V	
VDDIOR	I/O supply voltage	3.135	3.30	3.465	V	
VDDIOT 3v3	I/O supply voltage	3.135	3.30	3.465	V	
VDDIOT 2v5	I/O supply voltage	2.375	2.50	2.625	V	
USB_VDD	USB tile DC supply voltage	0.95	1.00	1.05	V	
VDD33	Peripheral supply	3.135	3.30	3.465	V	
PLL_AVDD	PLL analog supply	0.95	1.00	1.05	V	



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Sheet: /XMOS USB/JTAG/
File: XMOS_USB.sch

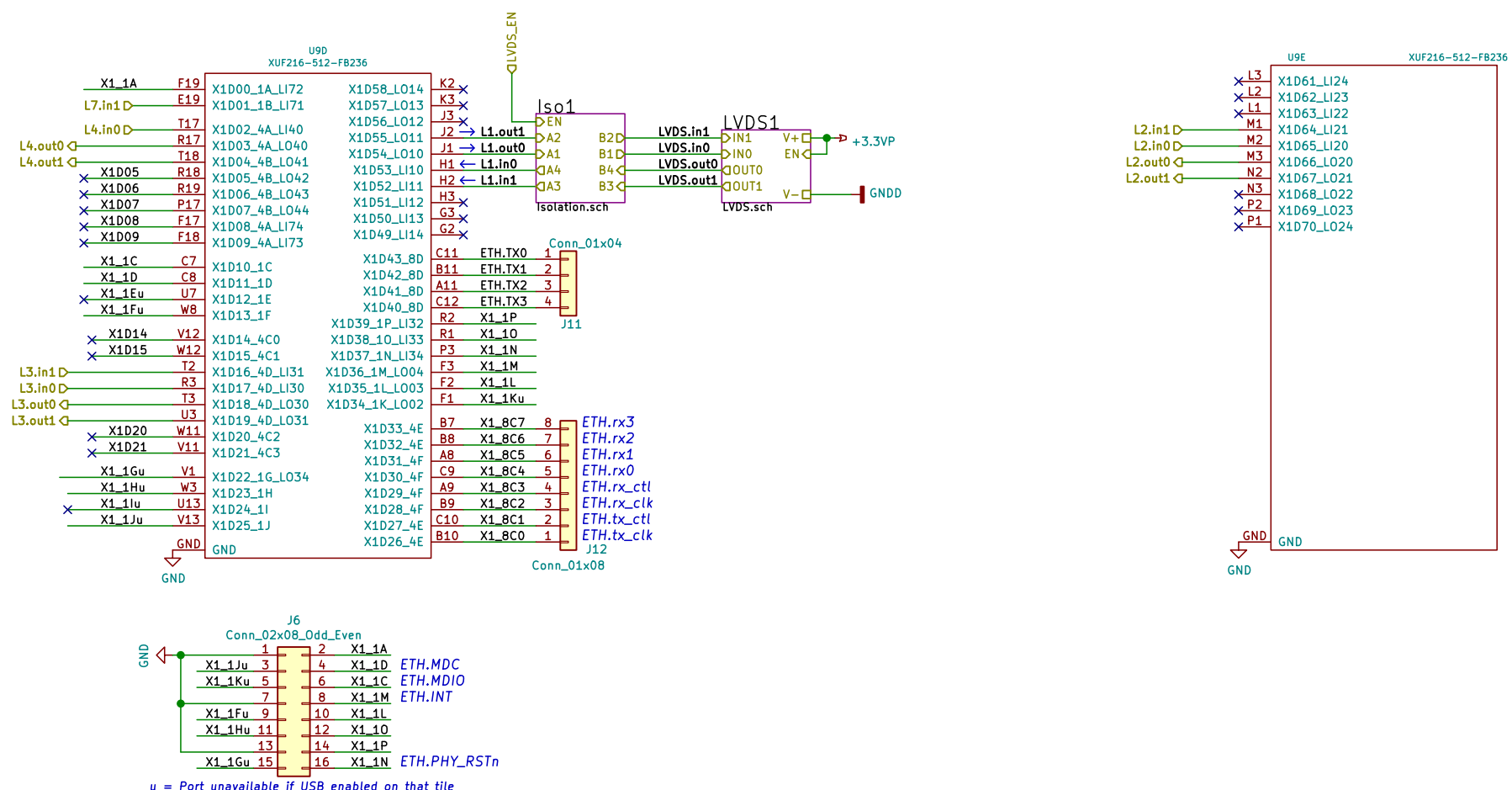
Title: XTAG & XMOS USB

Size: A4 Date: 2019-01-03

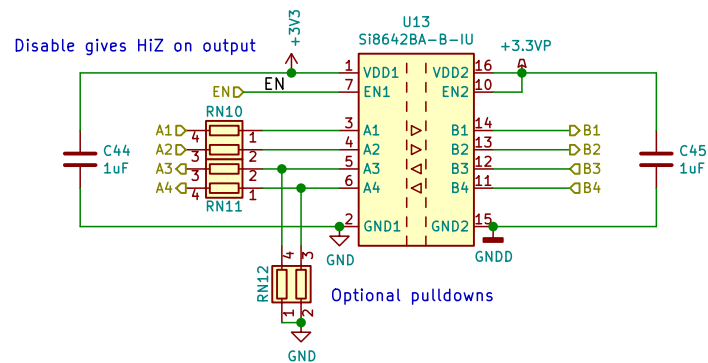
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Rev: BETA

Id: 5/16



u = Port unavailable if USB enabled on that tile



Disable gives HiZ on output

For XLinks-2 wire: To avoid jitter/skew sensitivity,
only one transition per clock cycle can happen within the pair.

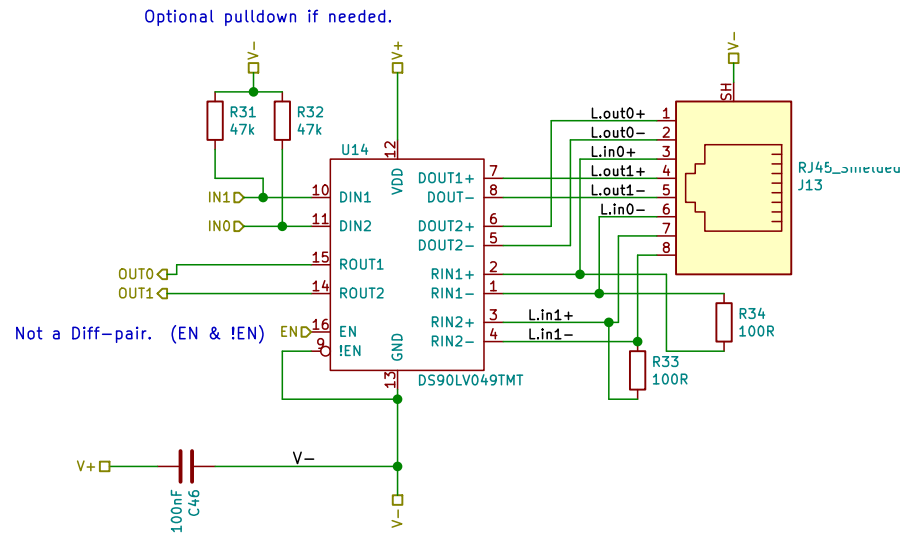
Open Source
openPnP

Sheet: /Tile1/Iso1/
File: Isolation.sch

Title: Isolation

Size: A4 Date: 2019-01-03
KiCad E.D.A. kicad (5.0.2)-1

Rev: BETA
Id: 8/16



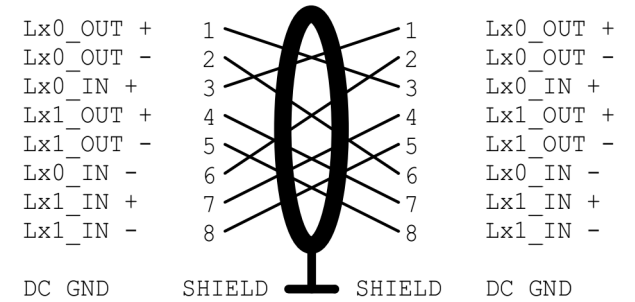
Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMO pins has internal pullup.
Transceiver needs to be in HiZ during XMO reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

RJ45 PINOUT:

1/2 Lx0_OUT +/-
3/6 Lx0_IN +/-
4/5 Lx1_OUT +/-
7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE



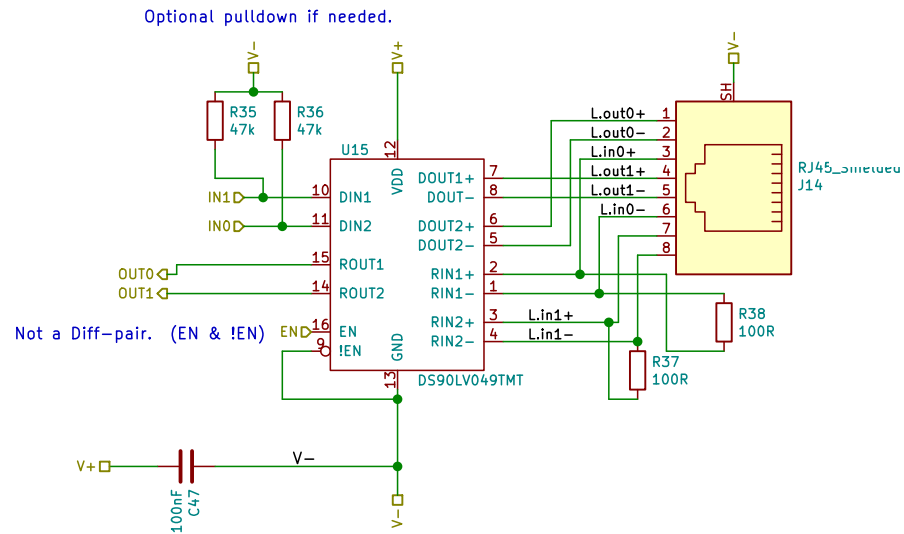
Open Source
openPnP

Sheet: /Tile1/LVDS1/
File: LVDS.sch

Title: LVDS <--> Xlinks

Size: A4 Date: 2019-01-03
KiCad E.D.A. kicad (5.0.2)-1

Rev: BETA
Id: 9/16



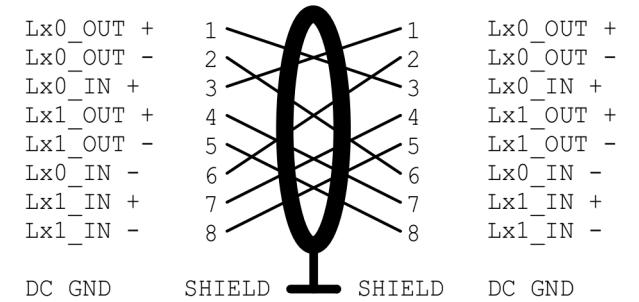
Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMO pins has internal pullup.
Transceiver needs to be in HiZ during XMO reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

RJ45 PINOUT:

1/2 Lx0_OUT +/-
3/6 Lx0_IN +/-
4/5 Lx1_OUT +/-
7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE



Open Source
openPnP

Sheet: /LVDS4/
File: LVDS.sch

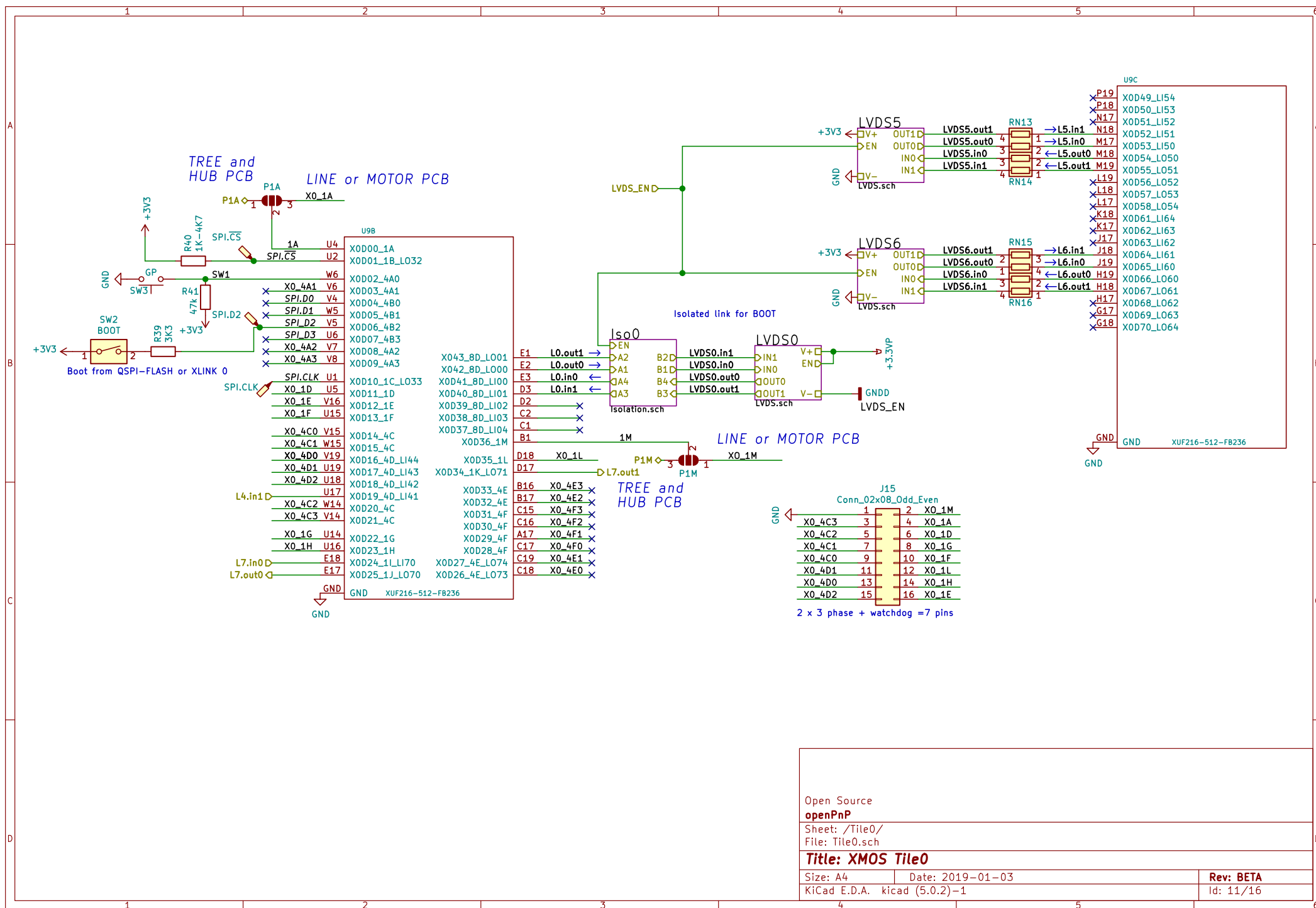
Title: LVDS <--> Xlinks

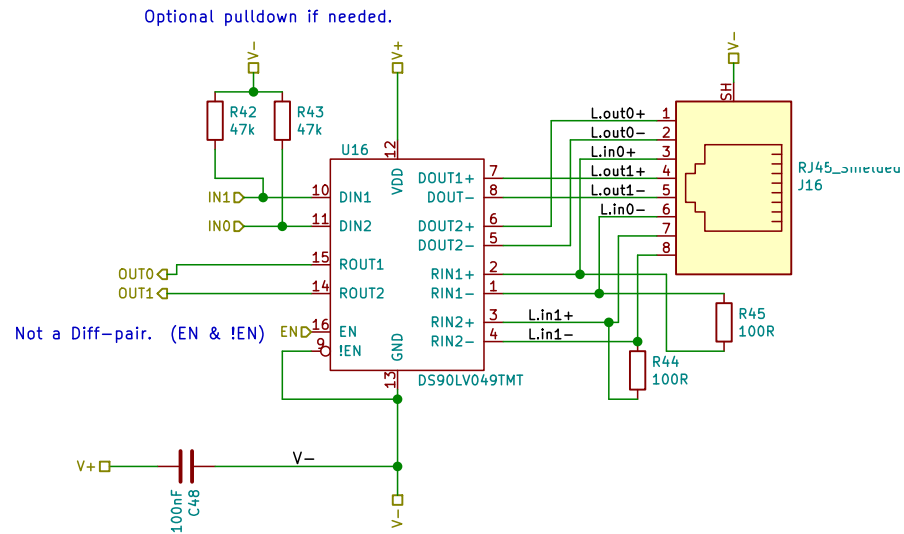
Size: A4 Date: 2019-01-03

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Rev: BETA

Id: 10/16





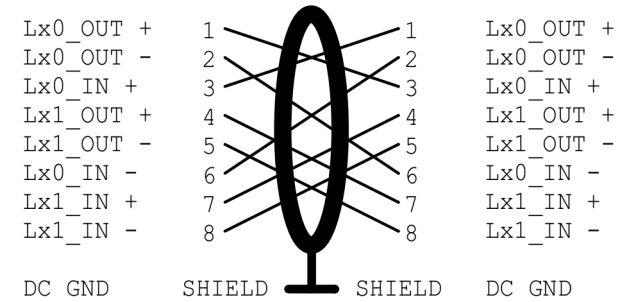
Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMO pins has internal pulldown.
Transciever needs to be in HiZ during XMO reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

RJ45 PINOUT:

1/2 Lx0_OUT +/-
3/6 Lx0_IN +/-
4/5 Lx1_OUT +/-
7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE



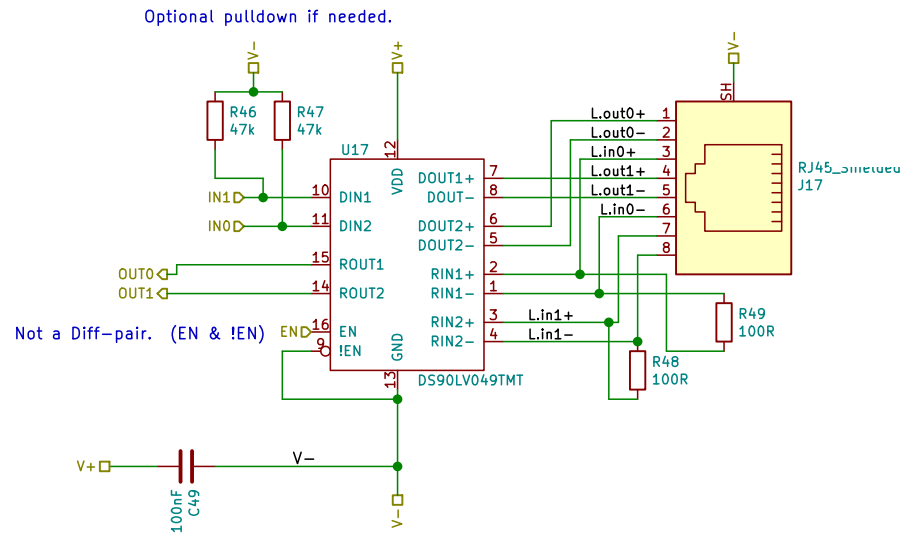
Open Source
openPnP

Sheet: /Tile0/LVDS6/
File: LVDS.sch

Title: LVDS <--> Xlinks

Size: A4 Date: 2019-01-03
KiCad E.D.A. kicad (5.0.2)-1

Rev: BETA
Id: 12/16



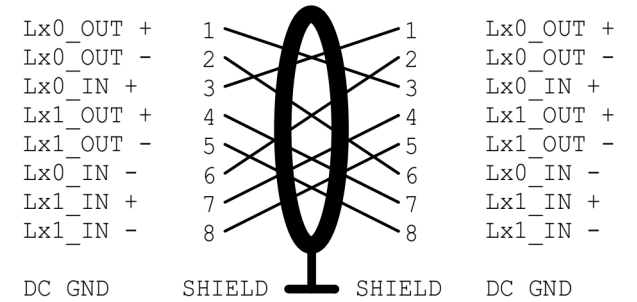
Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMO pins has internal pullup.
Transceiver needs to be in HiZ during XMO reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

RJ45 PINOUT:

1/2 Lx0_OUT +/-
3/6 Lx0_IN +/-
4/5 Lx1_OUT +/-
7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE



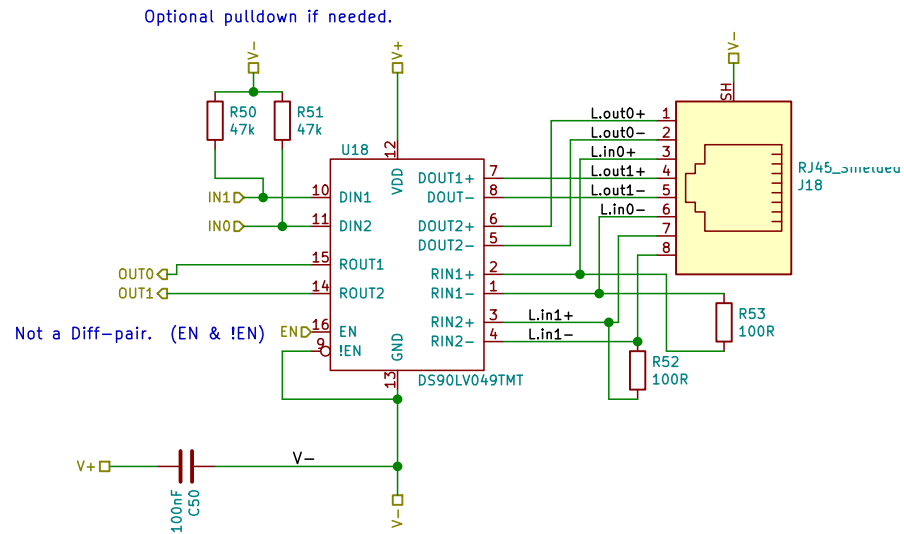
Open Source
openPnP

Sheet: /Tile0/LVDS5/
File: LVDS.sch

Title: LVDS <--> Xlinks

Size: A4 Date: 2019-01-03
KiCad E.D.A. kicad (5.0.2)-1

Rev: BETA
Id: 13/16



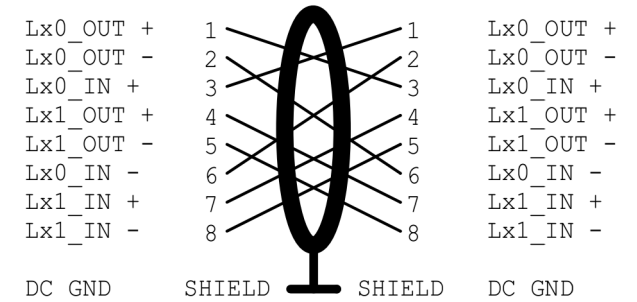
Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
X MOS pins has internal pulldown.
Transciever needs to be in HiZ during X MOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

RJ45 PINOUT:

1/2 Lx0_OUT +/-
3/6 Lx0_IN +/-
4/5 Lx1_OUT +/-
7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE



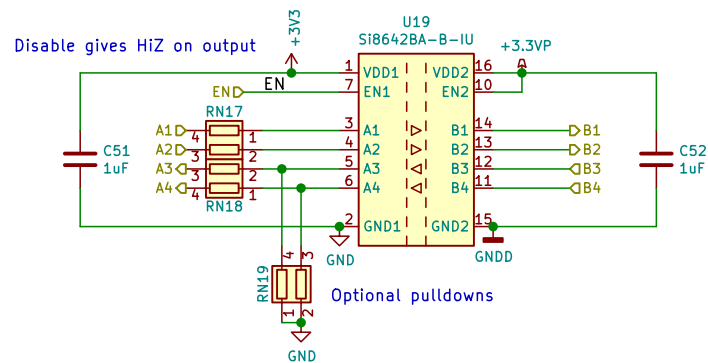
Open Source
openPnP

Sheet: /Tile0/LVDS0/
File: LVDS.sch

Title: LVDS <--> Xlinks

Size: A4 Date: 2019-01-03
KiCad E.D.A. kicad (5.0.2)-1

Rev: BETA
Id: 14/16



For XLinks-2 wire: To avoid jitter/skew sensitivity,
only one transition per clock cycle can happen within the pair.

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Sheet: /Tile0/Iso0/
File: Isolation.sch

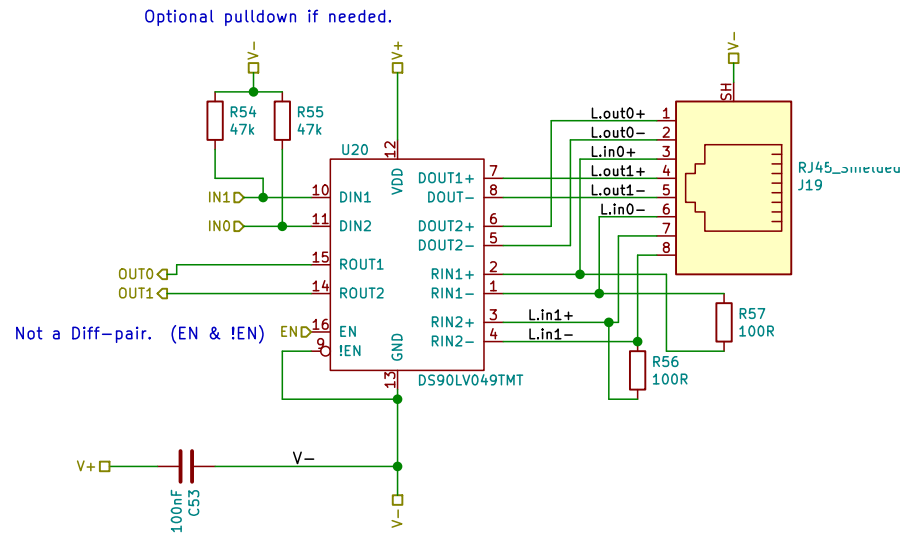
Title: Isolation

Size: A4 Date: 2019-01-03

KiCad E.D.A. kicad (5.0.2)-1

Rev: BETA

Id: 15/16



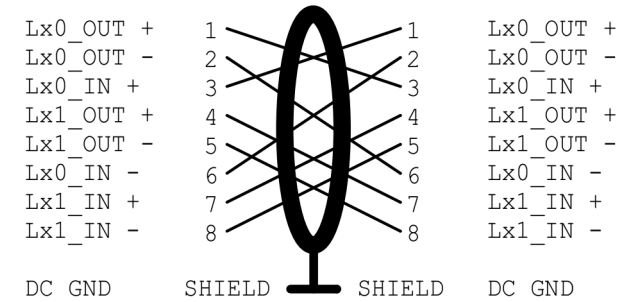
Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
X MOS pins has internal pulldown.
Transceiver needs to be in HiZ during X MOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

RJ45 PINOUT:

1/2 Lx0_OUT +/-
3/6 Lx0_IN +/-
4/5 Lx1_OUT +/-
7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE



Open Source
openPnP

Sheet: /LVDS3/
File: LVDS.sch

Title: LVDS <--> Xlinks

Size: A4 Date: 2019-01-03

KiCad E.D.A. kicad (5.0.2)-1

Rev: BETA

Id: 16/16