For 24MHz OSC

U1.A
XUF216-512-FB236

MODE0 A15
MODE1 B15
CLK A6
DEBUG C5
RST C6
TDO B4
TDI C4
TMS_BUFF B5
TCK_BUFF A5
B6
VDD
PLL_AVDD F13
PLL_AGND F14
OTP_VCC A12
OTP_VCC B12
VDDIOL A2
VDDIOL A3
VDDIOL B2
VDDIOL B3
VDDIOL C3
VDDIOL V2
VDDIOL W2
VDDIOL V3
GND

MODE[0]
MODE[1]
CLK
DEBUG
RST
TDO
TDI
TMS
TCK
TRST
VDD
PLL_AVDD
PLL_AGND
OTP_VCC
VDDIOL
GND

USB_DP V10
USB_DM V9
USB_ID U10
USB_RTUNE W9
USB_VBUS U9
VDDIOT F10
VDDIOR A18
VDDIOR B18
VDDIOR B19
VDDIOR V17
VDDIOR V18
VDDIOR W17
VDDIOR W18
USB_VDD P9
USB_VDD P10
USB_VDD33 U8
USB_VSSAC U11

USB_DP
USB_DM
USB_ID
USB_RTUNE
USB_VBUS
VDDIOT
VDDIOR
USB_VDD
USB_VDD33
USB_VSSAC

USB_D+
USB_D-
USB_ID
USB_VBUS

D3
VBUS
J8
USB_B_Mini
VBUS
D+
D-
ID
GND
Shield
R3 47k
R2 43R2
C17 100nF
C44 10k
C43 2u2F

SW3
BOOT
R21 3K3
Boot from QSPI-FLASH or XLINK-0

R5 1K
SW1
SW_Push_Dual
R20 47k

U10
TPD2E2U06
USB_D+
USB_D-
NC
NC

U1.B

X0_1A U4
SPI_CS U2
X0_4A0 W6
X0_4A1 V6
QSPI_D0 V4
QSPI_D1 W5
QSPI_D2 V5
QSPI_D3 U6
X0_4A2 V7
X0_4A3 V8
X0_1C U1
X0_1D U5
X0_1E V16
X0_1F U15
X0_4C0 V15
X0_4C1 W15
X0_4D0 V19
X0_4D1 U19
X0_4D2 U18
LI41 U17
X0_4C2 W14
X0_4C3 V14
X0_1G U14
X0_1H U16
LI70 E18
LO70 E17

X0D00_1A
X0D01_1B_LO32
X0D02_4A0
X0D03_4A1
X0D04_4B0
X0D05_4B1
X0D06_4B2
X0D07_4B3
X0D08_4A2
X0D09_4A3
X0D10_1C_LO33
X0D11_1D
X0D12_1E
X0D13_1F
X0D14_4C
X0D15_4C
X0D16_4D_LI44
X0D17_4D_LI43
X0D18_4D_LI42
X0D19_4D_LI41
X0D20_4C
X0D21_4C
X0D22_1G
X0D23_1H
X0D24_1I_LI70
X0D25_1J_LO70
GND

X043_8D_LO01
X042_8D_LO00
X0D41_8D_LI00
X0D40_8D_LI01
X0D39_8D_LI02
X0D38_8D_LI03
X0D37_8D_LI04
X0D36_1M
X0D35_1L
X0D34_1K_LO71
X0D33_4E
X0D32_4E
X0D31_4F
X0D30_4F
X0D29_4F
X0D28_4F
X0D27_4E_LO74
X0D26_4E_LO73

E1 LO01
E2 LO00
E3 LI00
D3 LI01
D2
C2
C1
B1 X0_1M
D18 X0_1L
D17 LO71
B16 X0_4E3
B17 X0_4E2
C15 X0_4F3
C16 X0_4F2
A17 X0_4F1
C17 X0_4F0
C19 X0_4E1
C18 X0_4E0

LVDS_EN
ISOLATION_0
EN
A2
A1
A4
A3
B2
B1
B4
B3
file5D2AE1E1.sch
LO01_iso
LO00_iso
LI00_iso
LI01_iso
LVDS0
IN1
IN0
OUT0
OUT1
V+
EN
V-
file5C2628B0.sch
+3.3VP
GNDD
Isolated link for BOOT

U1.C

XOD49_LI54
XOD50_LI53
XOD51_LI52
XOD52_LI51
XOD53_LI50
XOD54_LO50
XOD55_LO51
XOD56_LO52
XOD57_LO53
XOD58_LO54
XOD61_LI64
XOD62_LI63
XOD63_LI62
XOD64_LI61
XOD65_LI60
XOD66_LO60
XOD67_LO61
XOD68_LO62
XOD69_LO63
XOD70_LO64

LVDS5
LVDS6
RN11
RN12
RN6
RN7
LI51 N18
LI50 M17
LO50 M18
LO51 M19
LI61 J18
LI60 J19
LO60 H19
LO61 H18
file5C2628B0.sch

Pin 5,7,9,13,15 must be connected for xCORE-200.
Pin 11 for multi-PCB debug events.
XTAG does not power any device.

XTAGin
J9
Conn_02x10_FROM_XTAG
5V_XTAG 1
MSEL 3
TDI 5
TMS 7
TCK 9
DEBUG_XTAG 11
TDO2XTAG 13
TRST_XTAG 15
UART_RX 17
UART_TX 19
LO31
LO30
LI30
LI31

R10 47k
R11 47k
TMS_BUFF
TCK_BUFF
Y2 A2
Y1 A1
NC7WZ17
U12
JP1
SolderJumper_2_Bridged
DEBUG

C1 C2 C3 C4 C5 C6 C7 C8 C31 C33 C34 C35
C45 C32 C29 C30 C18 C19 C20 C21 C22 C23
C

U18.A
IC-LOGIC-BUF-NC7WZ04P6X

LVDS7
RN13
LI71
LI70
LO70
L071
RN8

R8 33
TDO
TDO_C
CHAINED
NC7SZ157
U11
TDO from this XMOS chip
TDO from last XMOS chip in chain
A connected device will ground this pin

J10
Conn_02x10_toNext
TDO 5
TMS_BUFF 7
TCK_BUFF 9
DEBUG 11
TDO_C 13
RST 15

R9 47k

U1.E
XUF216-512-FB236
X1D61_LI24
X1D62_LI23
X1D63_LI22
X1D64_LI21
X1D65_LI20
X1D66_LO20
X1D67_LO21
X1D68_LO22
X1D69_LO23
X1D70_LO24
xl2_rx1 M1
xl2_rx0 M2
xl2_tx0 M3
xl2_tx1 N2
RN1

POWER
file5C95FA9D.sch

U1.D
XUF216-512-FB236
X1D00_1A_LI72
X1D01_1B_LI71
X1D02_4A_LI40
X1D03_4A_LO40
X1D04_4B_LO41
X1D05_4B_LO42
X1D06_4B_LO43
X1D07_4B_LO44
X1D08_4A_LI74
X1D09_4A_LI73
X1D10_1C
X1D11_1D
X1D12_1E
X1D13_1F
X1D14_4C0
X1D15_4C1
X1D16_4D_LI31
X1D17_4D_LI30
X1D18_4D_LO30
X1D19_4D_LO31
X1D20_4C2
X1D21_4C3
X1D22_1G_LO34
X1D23_1H
X1D24_1I
X1D25_1J
GND

X1D58_LO14
X1D57_LO13
X1D56_LO12
X1D55_LO11
X1D54_LO10
X1D53_LI10
X1D52_LI11
X1D51_LI12
X1D50_LI13
X1D49_LI14
X1D43_8D
X1D42_8D
X1D41_8D
X1D40_8D
X1D39_1P_LI32
X1D38_1O_LI33
X1D37_1N_LI34
X1D36_1M_LO04
X1D35_1L_LO03
X1D34_1K_LO02
X1D33_4E
X1D32_4E
X1D31_4F
X1D30_4F
X1D29_4F
X1D28_4F
X1D27_4E
X1D26_4E

X1_1A F19
LI71 E19
LO40 T17
LO41 T18
X1D05 R18
X1D06 R19
X1D07 P17
X1D08 F17
X1D09 F18
X1_1C C7
X1_1D C8
X1_1Eu U7
X1_1Fu W8
X1D14 V12
X1D15 W12
LI31 T2
LI30 R3
X1D20 W11
X1D21 V11
X1_1Gu V1
X1_1Hu W3
X1_1Iu U13
X1_1Ju V13

K2 X1D43
B11 X1D42
A11 X1D41
C12 X1D40
R2 X1_1P
R1 X1_1O
P3 X1_1N
F3 X1_1M
F2 X1_1L
F1 X1_1Ku
B7 X1_8C7 8
B8 X1_8C6 7
A8 X1_8C5 6
C9 X1_8C4 5
A9 X1_8C3 4
B9 X1_8C2 3
C10 X1_8C1 2
B10 X1_8C0 1

LVDS_EN
ISOLATION_1
LO11
LO10
LI10
LI11
file5D2AE1E1.sch
LO11_iso
LO10_iso
LI10_iso
LI11_iso
LVDS1
file5C2628B0.sch
+3.3VP
GNDD

RN14
RN3
RN2
LI41
LI40
LO40
LO41
XLO40
XLO41
LO30
LO31

J13
Conn_01x08

J12
Conn_02x08_Odd_Even
X1_1Ju 3
X1_1Ku 5
X1_1Fu 9
X1_1Hu 11
X1_1Gu 15
X1_1A 2
X1_1D 4
X1_1C 6
X1_1M 8
X1_1L 10
X1_1O 12
X1_1P 14
X1_1N 16
u = Port unavailable if USB enabled on that tile

J11
Conn_02x08_Odd_Even
X0_4C3 3
X0_4C2 5
X0_4C1 7
X0_4C0 9
X0_4D1 11
X0_4D0 13
X0_4D2 15
X0_1M 2
X0_1A 4
X0_1D 6
X0_1G 8
X0_1F 10
X0_1L 12
X0_1H 14
X0_1E 16
2 x 3 phase + watchdog =7 pins

CLK
C44 10-100nF
X1
ASV-24MHz
R19 33
CLK

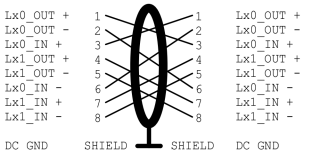
Power on reset
U18.B
IC-LOGIC-BUF-NC7WZ04P6X
R48 1k
LED D5
LVDS_EN
U9
IC-RES-TPS3808
VDD
SENSE
CT
RESET
MR
GND
RST
TRST_XTAG
SW2
SW_RESET
R12 10k
R13 7k5
C24 10nF
R_C1
CT open -> 20ms
680 - 1000 pF
CT(nF) = [tD(s) - 0.5E-3] * 175 = 0.78nF
valid for CT>100pF

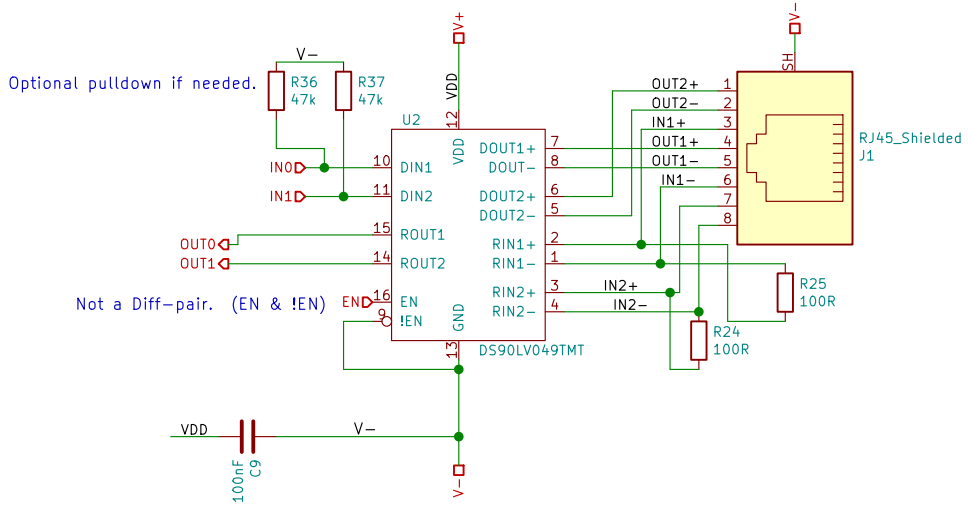
openPnP
Sheet: /
File: test.sch
Title: XMOS top level
Size: A3
Date: 2018-12-30
Rev: BETA
KiCad E.D.A. kicad (5.0.2)-1
Id: 1/10

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

openPnP		
Sheet: /LVDS0/		
File: file5C2628B0.sch		
Title: LVDS <-> Xlinks		
Size: A4	Date: 2018-12-30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 2/10

RJ45 PINOUT:

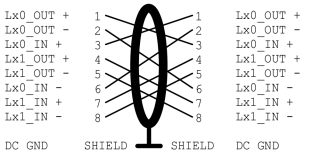
1/2 Lx0_OUT +/-

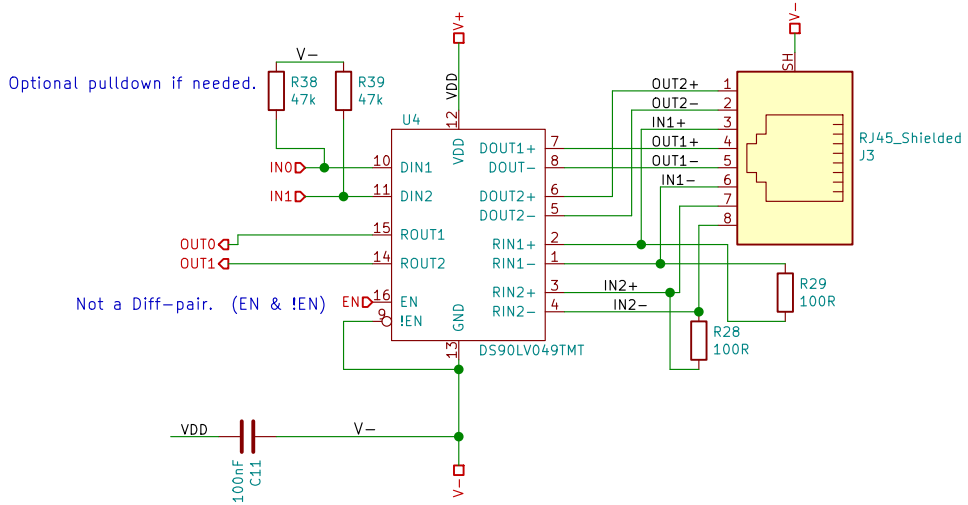
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

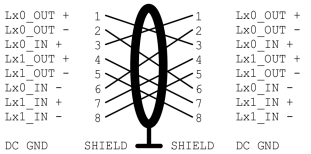
This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

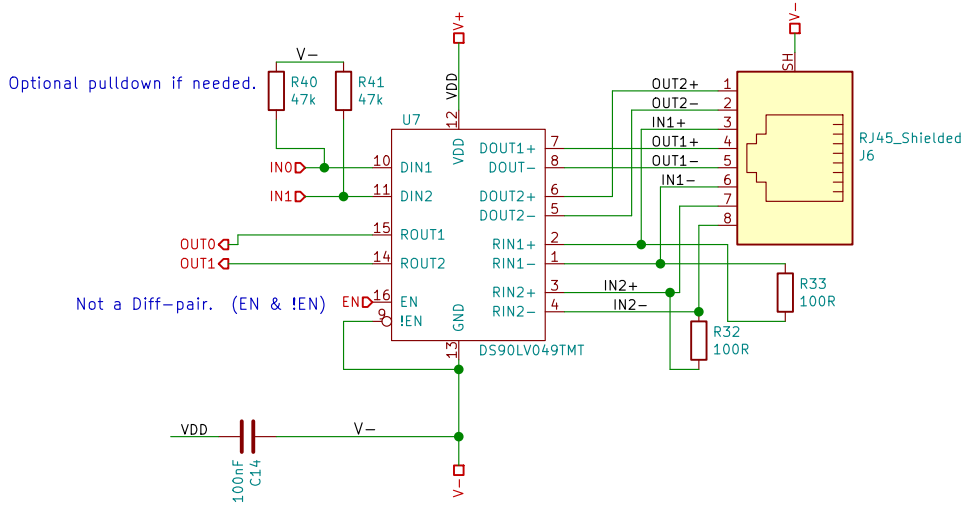
openPnP		
Sheet: /LVDS4/		
File: file5C2628B0.sch		
Title: LVDS <−> Xlinks		
Size: A4	Date: 2018−12−30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 3/10

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

openPnP		
Sheet: /LVDS6/		
File: file5C2628B0.sch		
Title: LVDS <−> Xlinks		
Size: A4	Date: 2018−12−30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 4/10

RJ45 PINOUT:

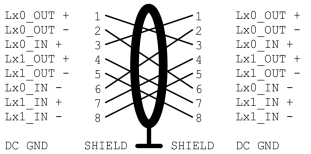
1/2 Lx0_OUT +/-

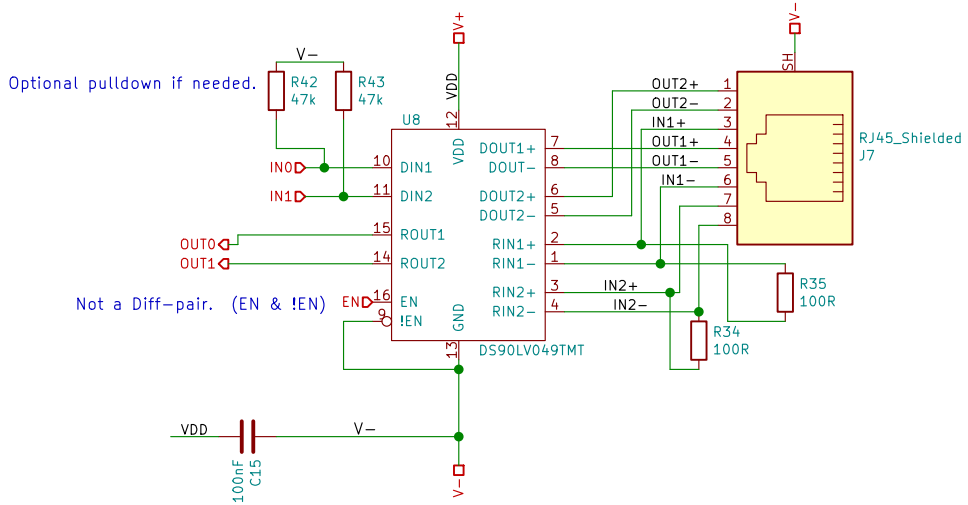
3/6 Lx0_IN +/-

4/5 Lx1_OUT +/-

7/8 Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





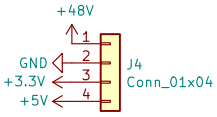
Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

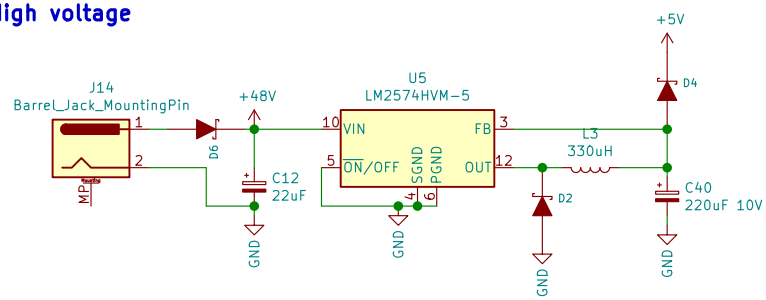
openPnP		
Sheet: /LVDS7/		
File: file5C2628B0.sch		
Title: LVDS <−> Xlinks		
Size: A4	Date: 2018−12−30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)−1		Id: 5/10

Cards can be power by USB or by the barrel jack 8–48V.
Alternative "+48V" can come from a connected daugther card.
Both USB and +48V should not be connected on the same PCB.
USB ground should be isolated from power ground for PC safety.

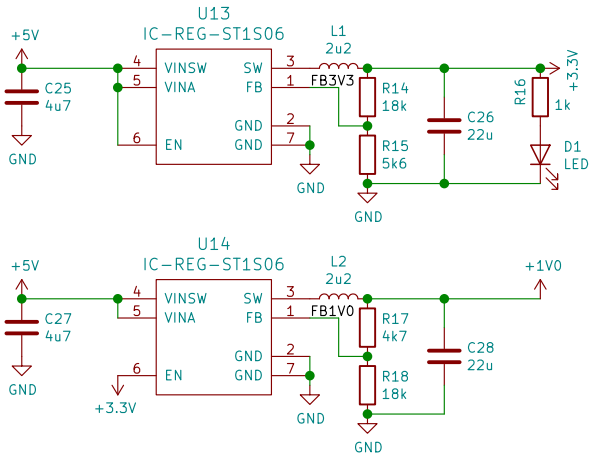
Power ports are Global in the schematics.



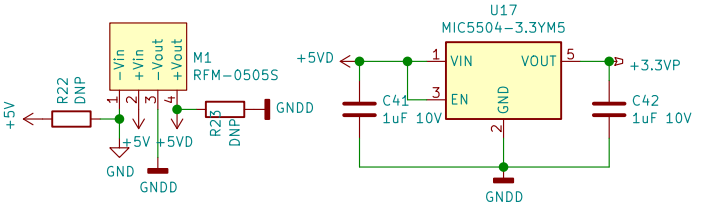
High voltage



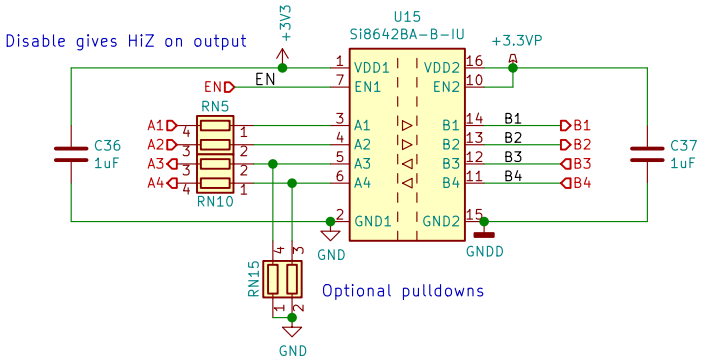
DC–DC



DC–DC isolation

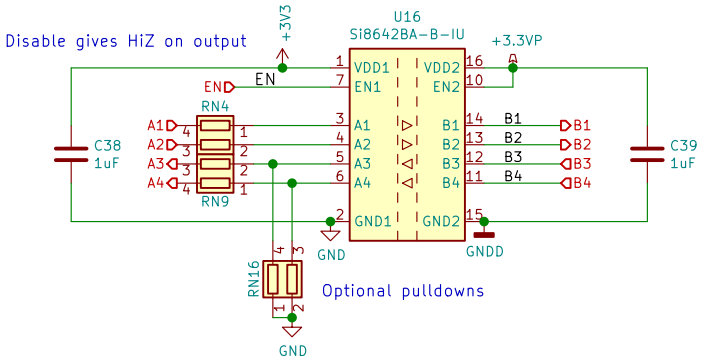


openPnP		
Sheet: /POWER/		
File: file5C95FA9D.sch		
Title: Power		
Size: A4	Date: 2018–12–30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)–1		Id: 6/10



On XLinks-2 wire, only one transition per clock cycle can happen within the pair, to avoid jitter/skew sensitivity.

openPnP		
Sheet: /ISOLATION_0/		
File: file5D2AE1E1.sch		
Title: Isolation		
Size: A4	Date: 2018-12-30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 7/10



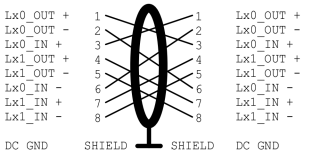
On XLinks-2 wire, only one transition per clock cycle can happen within the pair, to avoid jitter/skew sensitivity.

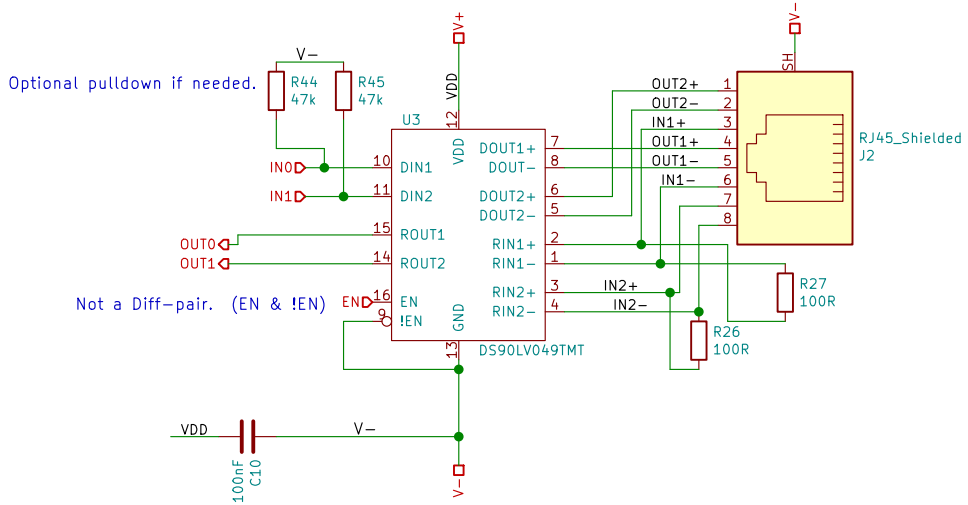
openPnP		
Sheet: /ISOLATION_1/		
File: file5D2AE1E1.sch		
Title: Isolation		
Size: A4	Date: 2018-12-30	**Rev: BETA**
KiCad E.D.A. kicad (5.0.2)-1		Id: 8/10

RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

openPnP

Sheet: /LVDS1/
File: file5C2628B0.sch

Title: LVDS <−> Xlinks

Size: A4	Date: 2018−12−30	**Rev: BETA**
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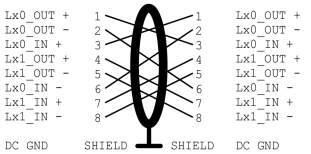
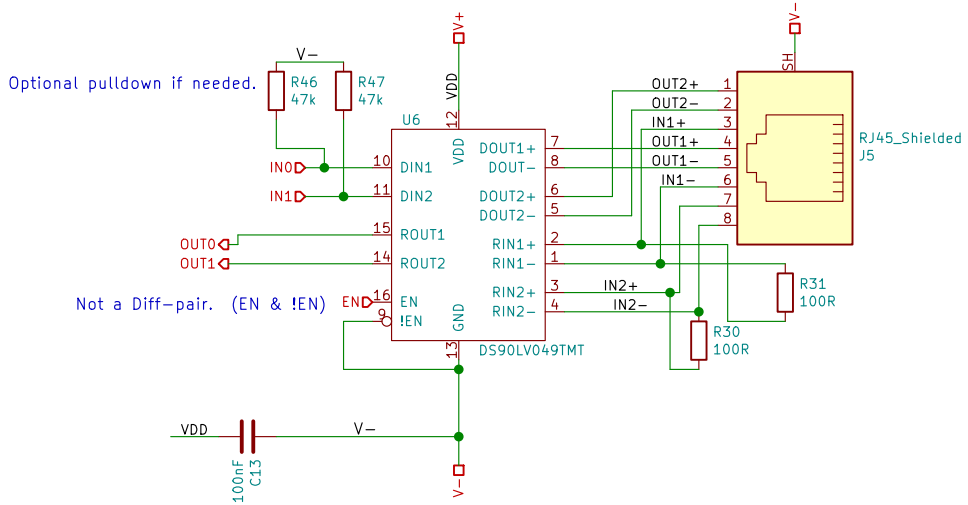
RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE





Unconnected LVDS input gives HI out on TTL side.
Active XLinks input should be LO during reset.
XMOS pins has internal pulldown.
Transciever needs to be in HiZ during XMOS reset.

This should give hardware support for hotswap with unconnected active XLinks, with bootloader in Flash.

openPnP		
Sheet: /LVDS5/		
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