COE3DQ5 – Lab #4 Report

Group 14

Mengjia Li (400011362)
Nicole Wu (400089778)
lim14@mcmaster.ca
wuz78@mcmaster.ca

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a. Changing the original BIST state machine to burst R/W mode

In order to change the SRAM self-test to burst mode, the state between S_WRITE_CYCLE and S_DELAY_1 & S_DELAY_2 is switched. The read mode is turned on 2 clock cycles before the read cycle. Within S_WRITE_CYCLE and S_READ_CYCLE a compare logic is written to check whether *BIST_address* has reached *3FFFE/3FFFF* to decide getting to delay state. Correspondingly, *BIST_expected_data* is not assigned to address in combinational logic but incremented by 1 within the state machine to make sure the alignment with *BIST_read_data*.

b. R/W of SRAM addresses is separated into even and odd

A flag *BIST_flag* is used to indicate if the next write/read cycle is even or odd. The identification operation is added in S_IDLE state, where an if statement is utilized to check whether *BIST_flag* is 0 or 1. When it is 0, *BIST_address* and *BIST_expected_data i*s assigned with 0; when it is 1, they are assigned with 1 instead and the increment/decrement will be by 2 rather than 1. At the state when one session of operation is about to finish (S_DELAY_3), *BIST_flag* is inverted.

c. Write is in increasing order, read is in decreasing order

To achieve writing to addresses in increasing order, when the state is in S_IDLE, both *BIST_expected_data* and *BIST_address* are initialized to 0. Similarly, in S_WRITE_CYCLE both two signals are incremented by 2. On the other hand, to reach the fact that reading the address in decreasing order, when writing operation is finished and state enters S_DELAY_1 *BIST_address* and *BIST_expected_data* are assigned with (*3FFFE & FFFE*) or (*3FFFF & FFFF*). When reading them, a subtraction by 2 is performed instead.