PHY 338k Lab Report 2

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1 Lab 4: Diode Circuits

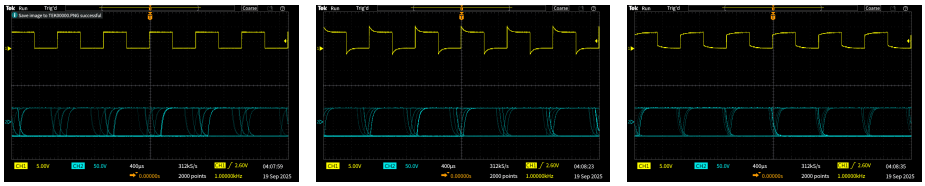
1.1 Oscilloscope probe

1.1.1 Compensation capacitor

To obtain accurate waveform measurements, we must ensure the oscilloscope probe is properly compensated so that its RC time constant matches the oscilloscope input. We connected the probe to the scope's Probe Comp terminal and adjusted the small screw near the probe connector while observing the waveform. Figure 1 shows the three compensation states.

1. When **under-compensated**, the square wave has rounded edges because the probe capacitance is too small, limiting high-frequency response.
2. When **over-compensated**, the waveform overshoots at transitions since the probe capacitance is too large, which over-emphasizes higher frequency components.
3. When **properly compensated**, the waveform displays flat tops and sharp corners, indicating a balanced frequency response.

These changes occur because a square wave contains many harmonics, so any mismatch between the probe and scope capacitances would cause unequal attenuation of those harmonics and distort the waveform. Thus, proper adjustment ensures that the measured signal accurately represents the true voltage at the circuit node.



(a) Properly Compensated (b) Over-compensated (c) Under-compensated

Figure 1: Oscilloscope traces for different probe compensation settings. Proper compensation yields flat tops and clean edges, whereas incorrect compensation leads to overshoot or rounding.

1.1.2 Reduction of oscilloscope load on a signal with a 10x probe

We used two configurations to explore the effects of oscilloscope loading in this section. Circuit A used a direct BNC connection from the function generator to CH2 and Circuit B used a 10x probe connection to CH2. In both cases, we connected CH1 to the generator output as a reference.

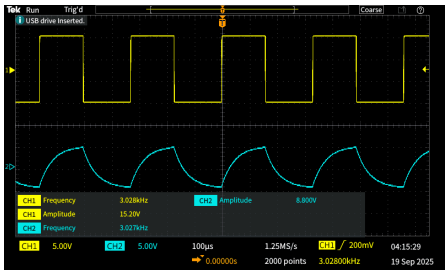
At low frequencies, both configurations produced similar waveforms. As we increased the frequency, the we observed reduced amplitude and distortion in Circuit A's scope display due to the oscilloscope's finite input impedance and capacitance. At $f = 3.0\text{kHz}$, we measured an amplitude ratio of:

$$\frac{V_{\text{CH2}}}{V_{\text{CH1}}} = \frac{8.8\text{V}}{15.2\text{V}} = 0.58. \tag{1}$$

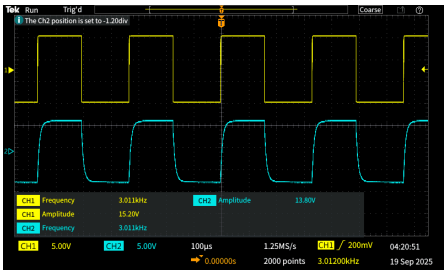
When we added the 10x probe, the measured CH2 amplitude increased to 13.8V, giving an amplitude ratio of:

$$\frac{V_{\text{CH2}}}{V_{\text{CH1}}} = \frac{13.8\text{V}}{15.2\text{V}} = 0.91. \tag{2}$$

Furthermore, the waveform closely matched CH1 with negligible phase shift. Our results agree well with the theoretical predictions from Homework 2, where the 10x probe's higher input impedance and reduced capacitance were expected to minimize loading.



(a) Direct scope connection (Circuit A): significant distortion and reduced amplitude.



(b) 10x probe connection (Circuit B): restored amplitude and cleaner waveform.

Figure 2: Scope displays showing the effect of oscilloscope loading with and without a 10x probe at 3.0 kHz.

Thus, we confirm the 10x probe minimizes loading by preserving both amplitude and waveform integrity, making it essential for accurate measurements in high-impedance or high-frequency circuits.

1.2 Diode circuits

1.2.1 Multimeter diode test

Using the diode test mode on the digital multimeter, we measured to the forward voltage of the 1N4007 diode to be 0.562V and the reverse voltage to be 3.122V. The forward reading indicates a typical silicon diode drop of approximately 0.6V, whereas the reverse reading reflects the multimeter's open-circuit voltage, indicating that negligible current flows when the diode is reverse-biased. Our measurements validate that the 1N4007 conducts in the forward direction and effectively blocks current in the reverse direction, so we confirm our device functions as expected.

1.2.2 Half-wave rectifier

We constructed a half-wave rectifier using a 1N4007 diode and a 4V amplitude, and a 1.021kHz input sine wave. The measured waveforms for V_{in} and V_{out} (CH2) are shown in Figure 3.

At 1.02kHz, V_{in} ranged from 3.9V to -4.5V, while V_{out} varied from 29.6V to -0.80V. The apparent voltage amplification is due to probe scaling rather than actual circuit gain. Qualitatively, the output waveform displays the expected half-wave rectifier behavior where current flows only during the positive half-cycles when the diode is forward-biased and is blocked during the negative half-cycles.

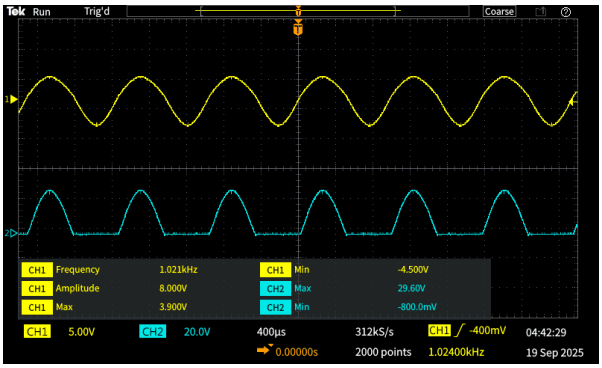


Figure 3: Input (CH1) and output (CH2) waveforms for the half-wave rectifier at 1kHz.

The maximum output voltage $V_{2(\max)}$ occurs when the diode conducts on the positive half-cycle. It's slightly lower than the input peak because of the diode's forward voltage drop ($V_{\text{drop}} \approx 0.7\text{V}$), so $V_{2(\max)} \approx V_{\text{in, peak}} - V_{\text{drop}} \approx 3.2\text{V}$. Our measured value differs due to the oscilloscope scaling factor. The minimum output voltage $V_{2(\min)}$ occurs where the diode is reverse-biased since the current is blocked, ideally producing 0V across the load.

Thus, our observed waveform confirms the expected behavior of a half-wave rectifier where positive cycles exhibit conduction and negative cycles exhibit suppression, yielding a pulsating DC output.

1.2.3 Diode clamp

We tested a diode clamp circuit using a 10V amplitude and 1kHz sine wave. Our goal with this circuit was to shift the input waveform upward and fix its negative peaks near +5V to produce a pulsing DC output. The input (V_{in}) and output (V_{out}) waveforms are displayed in Figure 4.

At 1.079kHz, the V_{in} ranged from 12.5V to -10.3V, while V_{out} ranged from 58.0V to -104.0V as displayed on the oscilloscope. The apparent voltage difference is due to probe scaling rather than actual gain. We observed a flattened peaks instead of the expected uniform shift in the output waveform, which suggests that our circuit behaved more like a diode clipper than a true clamp.

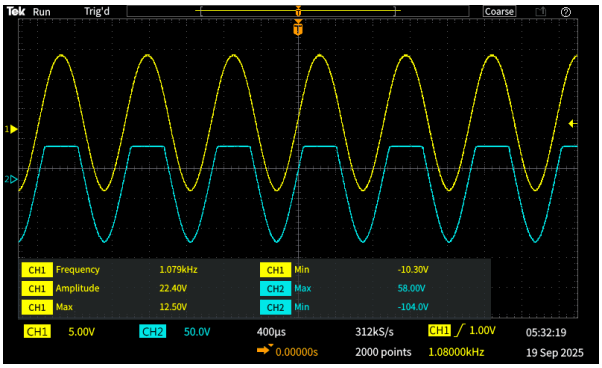


Figure 4: Input (CH1) and output (CH2) waveforms for the diode clamp circuit at 1kHz.

In theory, a diode clamp would shift the DC reference of an AC waveform without altering its shape. During the negative half-cycle, the diode conducts and charges the capacitor to the input's peak value. When the signal swings positive, the diode becomes reverse-biased, and the stored charge acts as a DC offset that raises the entire waveform and clamps its minimum voltage near +5V.

In our experiment, the clipping behavior we observed suggests that the capacitor did not charge properly or that the bias connection was incorrect. As a result, the diode limited the voltage supply rather than shifting the waveform baseline. Despite this possible mistake, our data still shows the diode's rectifying action and voltage-limiting effect, which is consistent with partial conduction near the +5V bias.

1.2.4 Zener diode IV curve

Finally, we measured the current vs. reverse voltage for the 1N4736 Zener diode with the TTi EL302R power supply in reverse-bias configuration. Our measurements are shown in Table 1, and the corresponding IV-curve is plotted in Figure 5.

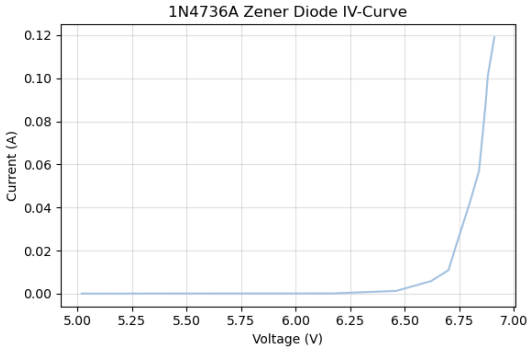


Figure 5: IV plot for the 1N4736A Zener diode.

Voltage (V)	Current (mA)
5.02	0.022
6.17	0.097
6.46	1.25
6.62	5.80
6.70	10.9
6.73	20.7
6.80	43.0
6.84	57.0
6.87	88.0
6.88	101.0
6.91	119.0

Table 1: Measured reverse current as a function of voltage for the 1N4736A Zener diode. Most data points were taken near the breakdown region (6.5-9.6V), where the current rises from 1mA to 120mA while the voltage remains nearly constant.

At low reverse voltages (below approximately 6.3V), we observed only small leakage current in the µA range. Once we reached the reverse voltage $V_{\text{reverse}} \approx$ 6.6V, the current increased rapidly for small changes in voltage. Between 50mA and 100mA, the voltage remained nearly constant around 6.8V, which confirms the zener diode's voltage regulation behavior. Thus, we confirm that the diode maintains a stable output voltage despite significant changes in current, a property that is useful for voltage reference and regulation circuits.

2 Lab 5: Bipolar Junction Transistors

2.1 Multimeter Measurements

2.1.1 Measurements using diode test function

We used the diode test mode of a digital multimeter to investigate the junction behavior of three bipolar junction transistors: the 2N3904, 2N2222, and 2N3906. For each device, we measured the voltage drops between the emitter, base, and collector terminals in both polarities to simulate diode junctions as shown in the equivalent circuit model.

The table below summarizes our measured voltage drops:

Measurement	2N3904 (NPN)	2N2222 (NPN)	2N3906 (PNP)
$V_{E\to B}$ (E more +)	3.190 V	3.189 V	0.705 V
$V_{B\to E}$ (B more +)	0.717 V	0.671 V	3.189 V
$V_{C\to B}$ (C more +)	3.189 V	3.189 V	0.696 V
$V_{B\to C}$ (B more +)	0.714 V	0.656 V	3.189 V

Table 2: Diode voltage drops measured with DMM for three BJT types.

For the NPN transistors (2N3904 and 2N2222), the base-emitter and base-collector junctions behave like forward-biased diodes when the base is more positive, with typical voltage drops around 0.6 to 0.7 V. When we reversed the polarity, the measured voltages are much higher, which is consistent with reverse-biased junctions.

For the PNP transistor (2N3906), we observed the opposite behavior. The emitter-base and collector-base junctions conducted when the emitter or collector was more positive than the base, with forward voltage drops around 0.7 V.

Our results are consistent with the expected behavior of BJTs and allow us to distinguish between the NPN and PNP types based on polarity and voltage drop direction.

2.1.2 Measurements using transistor h_{FE} measurement

Next, we measured the DC current gain h_{FE} of each transistor using the DMM's transistor gain function. The results are shown in the table below:

Transistor	h_{FE}
2N3904	297
2N2222	208
2N3906	305

Table 3: Measured current gain h_{FE} for each transistor.

2.2 Basic transistor circuit

2.2.1 I_c vs. V_{CE} at fixed V_{in}

We investigated the behavior of a 2N2222 NPN BJT by measuring the collector-emitter voltage V_{CE} for a fixed V_{in} shown in Figure 6. The curve shows a rapid increase in I_C at low V_{CE}, followed by a plateau region where I_C remains approximately constant despite further increases in V_{CE}. The flat region corresponds to the active mode of the transistor where it behaves like a current source.

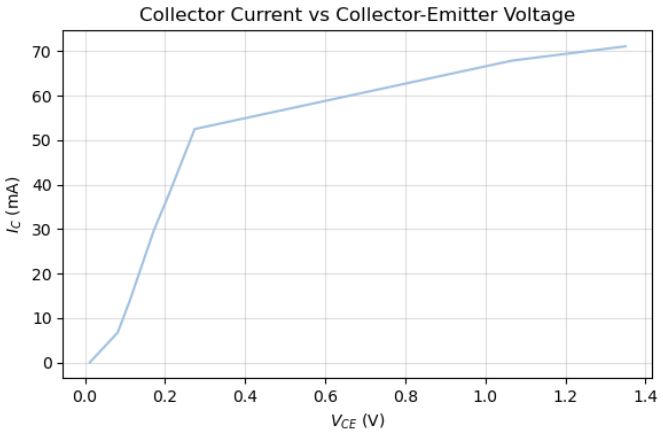


Figure 6: Plot of I_C vs. V_{CE} for fixed V_{in}.

We also computed the current gain $h_{FE} = I_C/I_B$ and plotted it against V_{CE} in Figure 7. The gain increases fairly quickly at low V_{CE}, then stabilizes in the active region as expected. Across our measured points, h_{FE} stabilized around 120-160, suggesting the transistor was operating in the forward-active region.

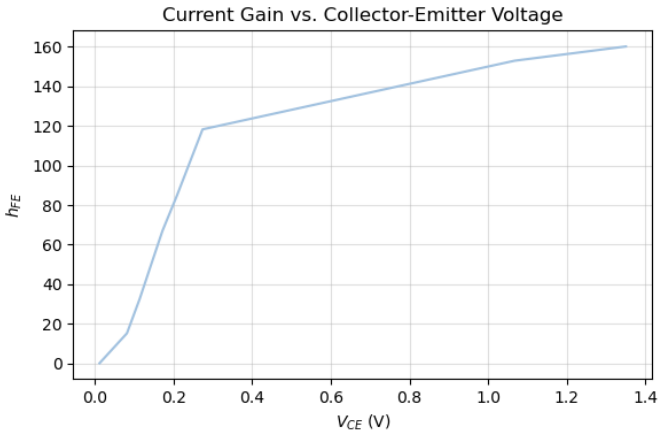


Figure 7: Plot of h_{FE} vs. V_{CE}.

The measured gain compares reasonably well with the values listed in the 2N2222A specifications sheet. Typical h_{FE} values at $I_C = 10$mA and $V_{CE} = 10$V range from 100 to 300, with a maximum of 325 for lower collector currents. Our measured value using the DMM in the previous section was 208, which also falls within the specified range, though it is slightly lower than what we observed under circuit bias conditions.

The saturation collector-emitter voltage $V_{CE(\text{sat})}$ is the voltage at which $h_{FE} = 10$. Based on our data, this occured around $V_{CE} \approx 0.02$V, which is where $I_C \approx 5$mA and $I_B \approx 0.5$mA, giving us $h_{FE} \approx 10$. This agrees with the typical datasheet value of $V_{CE(\text{sat})} = 0.3$V at $I_C = 150$mA and $I_B = 15$mA. Given our lower collector current value, it is expected that our saturation voltage would be lower than the datasheet's high-current test condition.

Overall, our measurements confirm the expected operating characteristics of the 2N2222A and are consistent with both the theory of BJT operation and the manufacturer specifications.

2.2.2 I_C vs. V_{BE} at fixed V_{CC}

To investigate the exponential relationship between base-emitter voltage V_{BE} and collector current I_C, we set $V_{CC} = 5.0$V and varied the input voltage to sweep I_C over a range from about 0.1mA to 100mA. We recorded both I_C and V_{BE} for each setting.

We plotted V_{BE} against I_C with I_C on a logarithmic scale, as seen in Figure 8. According to the Ebers-Moll relation:

$$I_C = I_S e^{V_{BE}/V_T}, \tag{3}$$

taking the natural logarithm of both sides gives us:

$$\ln(I_C) = \frac{V_{BE}}{V_T} + \ln(I_S). \tag{4}$$

This relation predicts that a plot of V_{BE} vs. $\ln(I_C)$ should yield a straight line, assuming I_S and V_T are constant.

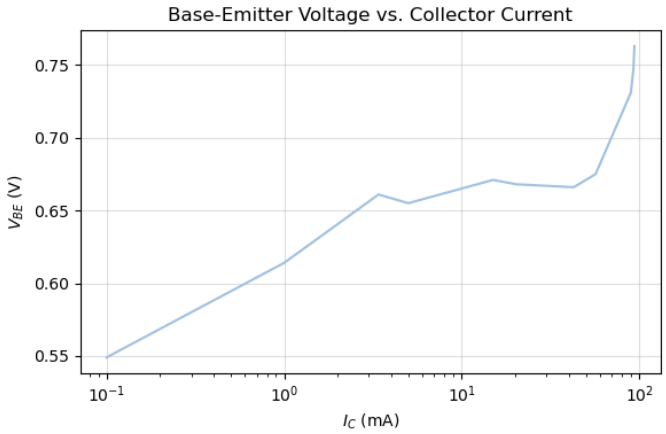


Figure 8: Plot of V_{BE} vs. I_C (log scale) at fixed $V_{CC} = 5.0\,\text{V}$.

As seen in the figure, the curve follows a roughly linear trend over the central range of I_C values, which supports the exponential dependence predicted by the Ebers-Moll model. At higher values of I_C, the curve deviates from the semilog relationship likely due to the effects of base-emitter series resistance, which are which are not accounted for in the ideal Ebers-Moll model. These factors cause an excess voltage drop across the base and emitter terminals, which would increase the measured V_{BE} beyond the ideal exponential prediction. Thermal effects may also have contributed slightly by altering junction properties under high power dissipation.

Overall, the measured relationship between V_{BE} and I_C follows the expected exponential behavior described by the Ebers-Moll model, especially across the lowto mid range of collector currents. The trend we observed is also consistent with the base-emitter characteristic shown in Figure 4 of the 2N2222A datasheet, which validates both our measurement procedure and the theoretical model. Thus, we can confirm that the 2N2222A exhibits typical BJT exopnential behavior in the active region.

2.3 Biasing a transistor

We built the biasing circuit using a 2N3904 NPN transistor with resistor values shown in Table 4. The voltage measurements at the collector, base, and emitter

are given in Table 5.

Component	Calculated Value	Actual Value Used
R_1	$185\,\mathrm{k\Omega}$	$185\,\mathrm{k\Omega}$
R_2	$15\,\mathrm{k\Omega}$	$13.8\,\mathrm{k\Omega}$
R_C	$10\,\mathrm{k\Omega}$	$9.93\,\mathrm{k\Omega}$
R_E	$1\,\mathrm{k\Omega}$	$1.08\,\mathrm{k\Omega}$

Table 4: Calculated and actual resistor values used in the biasing circuit.

Node	Measured Voltage
V_C	$57.3\,\mathrm{mV}$
V_B	$0.625\,\mathrm{V}$
V_E	$34.0\,\mathrm{mV}$

Table 5: Measured voltages at transistor terminals.

The base-emitter voltage $V_{BE} = V_B - V_E \approx 0.591\mathrm{V}$ is within the expected range for forward bias. However, the collector voltage $V_C = 57.3\mathrm{mV}$ is much lower than expected, suggesting that the transistor is operating in saturation rather than in the forward-active region. To shift it into the active region (typically V_C between 8 to 12V), we could modify the circuit by increasing R_C to reduce collector current or increasing R_2 to decrease the base current and base bias voltage.

2.4 Common emitter AC amplifier

Finally, we built a common emitter amplifier circuit and measured the input and output sine waves across a specified range of frequencies. Figure 9 shows an example oscilloscope trace where the output signal is inverted and amplified relative to the input, as expected for this setup.

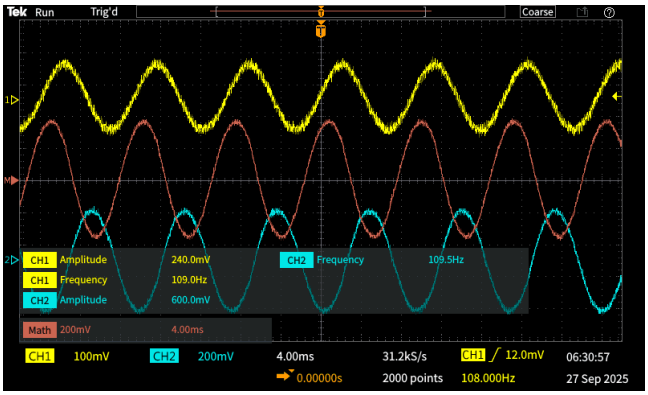


Figure 9: Oscilloscope trace of input (CH1) and output (CH2) sine waves at 109.0 Hz.

To analyze frequency-dependent behavior, we calculated the voltage gain in dB across input frequencies from 100Hz to 500kHz. We computed the gain as:

$$\text{Voltage Gain (dB)} = 20 \log_{10} \left(\frac{V_{\text{out}}}{V_{\text{in}}} \right). \tag{5}$$

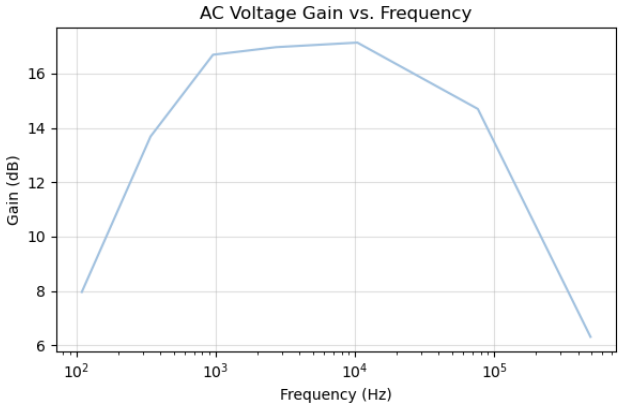


Figure 10: AC voltage gain vs. frequency for the common emitter amplifier.

The voltage gain is low at low frequencies due the high-pass filtering effect of the coupling and emitter bypass capacitors. In the mid-frequency range, the gain plateaus at its maximum (approximately 17 dB), which is where the amplifier behaves linearly. At higher frequencies, the gain drops off, likely due to parasistic capacitiances within the transistor and wiring, which introduce low-pass filtering. This aligns with typical band-pass behavior for a common emitter amplifier.

3 Lab 6: Field Effect Transistors

3.1 JFET Properties

In this section, we explored the characteristics of of the J112 n-channel JFET and examined how the drain current responds to changes in the gate-source voltage. We measured I_D across a range of positive and negative V_{GS} values and used our results to identify the transistor's parameters as well as compare its behavior to the J112 datasheet.

We plotted I_D vs. V_{GS} for the J112 n-channel JFET shown below. The drain current decreases as V_{GS} becomes more negative and approaches zero near $V_{GS} \approx -5.0\,\text{V}$, indicating a cutoff voltage of $V_{GS(\text{off})} = -5.0\,\text{V}$.

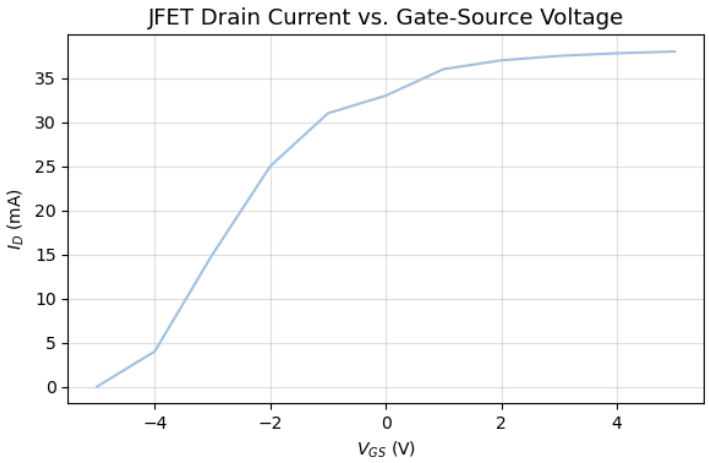


Figure 11: Plot of I_D vs. V_{GS} for the J112 n-channel JFET.

To determine the increment in gate voltage $V_{GS} - V_{GS(\text{off})}$ required to obtain a drain current of 10 mA, we used the Shockley equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2. \tag{6}$$

Using our measured values $I_{DSS} \approx 38\,\text{mA}$ and $V_{GS(\text{off})} \approx -5.0\,\text{V}$, we set $I_D = 10\,\text{mA}$ and solved for V_{GS}. Our result was $V_{GS} \approx -2.44\,\text{V}$, which corresponds to an increment of:

$$V_{GS} - V_{GS(\text{off})} = (-2.44) - (-5.0) = 2.56\,\text{V}. \tag{7}$$

Thus, an increase of approximately 2.56 V from the cutoff voltage is required for the drain current to reach 10mA.

Next, we plotted g_m vs. V_{GS} for the J112 n-channel JFET using the equation:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}. \tag{8}$$

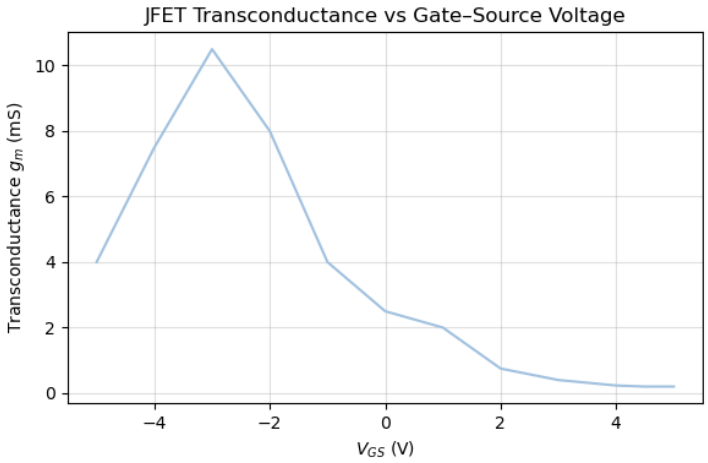


Figure 12: Plot of g_m vs. V_{GS} for the J112 n-channel JFET.

The transconductance increases as the gate-source voltage becomes less negative, reaching a maximum of a little over 10mS around $V_{GS} \approx -2.5$V, and then decreases toward zero for positive gate voltages. Our result was within the same order of typical maximum transconductances for the JFET, and the curve aligned with the general expected behavior.

3.2 N-channel MOSFET properties

3.2.1 Drain current vs. Gate-source voltage

In this section, observed characteristics of the 2N7000 n-channel MOSFET by measuring the drain current I_D as a function of the gate-source voltage V_{GS} from 0V to approximately 6V while keeping the drain supply voltage fixed at 10V with a 50Ω series resistor to limit current. Figure 13 shows the transistor's threshold and saturation behavior.

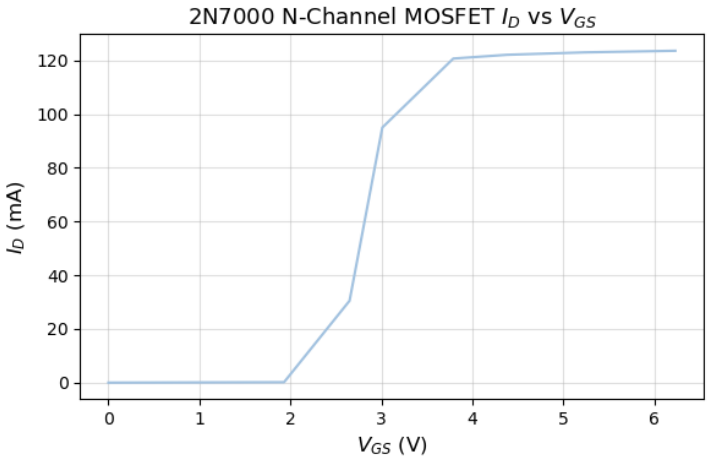


Figure 13: Plot of I_D vs. V_{GS} for the 2N7000 n-channel MOSFET.

From the curve above, we observed that the drain current remains near zero until V_{GS} exceeds the threshold voltage at $V_{GS,th} \approx 2$V, after which it increases rapidly and saturates around 120mA for $V_{GS} > 3.5$V.

From our observed data, the drain current of $I_D \approx 100$mA occurred at approximately $V_{GS} = 3.1$V, which makes the increment in gate voltage:

$$\Delta V = V_{GS} - V_{GS,th} = 3.1 - 2.0 = 1.1\text{V}. \tag{9}$$

At $V_{GS} = 5.23$V, the measured drain current was approximately 123mA. With a 10V supply and a 50Ω resistor in series with the drain, we calculated the drain-source voltage V_{DS} as:

$$V_{DS} = V_{DD} - I_D R_D = 10 - (0.123\text{A})(50\Omega) = 3.85\text{V}. \tag{10}$$

Thus, the corresponding on-resistance of the MOSFET is:

$$R_{DS(\text{on})} = \frac{V_{DS}}{I_D} = \frac{3.85}{0.123} \approx 31.3\Omega. \tag{11}$$

We also calculated the transconductance $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$. The resulting plot in Figure 14 shows that g_m rises sharply near the threshold region and peaks around $V_{GS} \approx 3$V at a maximum of about 130mS, and then decreases as the MOSFET enters the saturation region. This behavior agrees with the expected characteristics of the 2N7000.

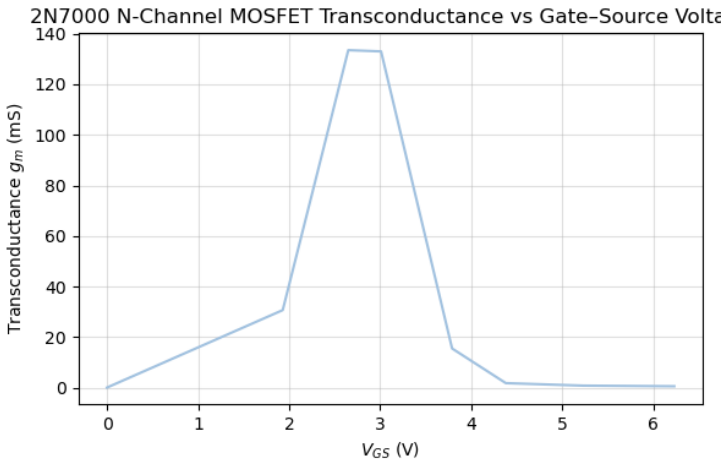


Figure 14: Plot of g_m vs. V_{GS} for the 2N7000 n-channel MOSFET.

3.2.2 Drain current vs. Drain-source voltage

In this section, we measured drain current I_D as a function of the drain-source voltage V_{DS} for the 2N7000 n-channel MOSFET while keeping the gate-source voltage fixed at $V_{GS} = 5$V. The resulting plot in Figure 15 shows the expected MOSFET behavior. The drain current increases approximately linearly for V_{DS} in the ohmic region, then levels off into saturation around $I_D \approx 120$mA for $V_{DS} > 2$V.

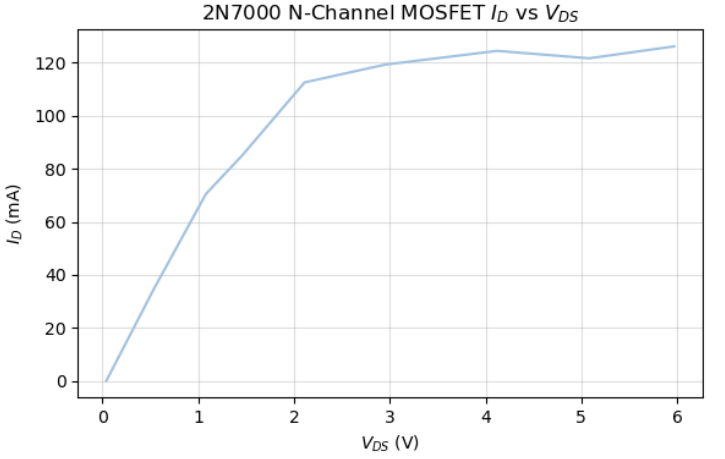


Figure 15: Plot of I_D vs. V_{DS} for the 2N7000 n-channel MOSFET at $V_{GS} = 5$V.

To estimate the MOSFET's channel resistance in the linear (ohmic) region, we selected two data points from the I_D vs. V_{DS} curve where the transistor operates below saturation. Using Ohm's law:

$$R = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1.08 - 0.53}{(70.5 - 34.2) \times 10^{-3}} \approx \frac{0.55}{0.0363} \approx 15.2\Omega. \tag{12}$$

This calculated resistance represents the MOSFET's on-state channel resistance $R_{DS(\text{on})}$ at $V_{GS} = 5\,\text{V}$. While this is somewhat higher than the typical $R_{DS(\text{on})}$ values listed in the datasheet for similar V_{GS} and I_D conditions, the discrepancy can be attributed to measurement conditions, contact resistance, and the fact that our operating current was below the device's rated maximum.

3.3 Power MOSFET switching of a load

Finally, we built the circuit from Fig. VI-3(a) to observe how a power MOSFET controls current through a resistive load, which in this case is a lamp. With the MOSFET turned on, we recorded the following measurements:

1. Lamp current: $I_{\text{lamp}} = 1.192\text{A}$
2. Voltage across lamp: $V_{\text{lamp}} = 4.37\text{V}$
3. Voltage across MOSFET (drain-to-source): $V_{DS} = 0.90\text{V}$

To calculate the on-state resistance of the MOSFET, we used Ohm's law:

$$R_{DS(\text{on})} = \frac{V_{DS}}{I_{\text{lamp}}} = \frac{0.90}{1.192} \approx 0.755\Omega \tag{13}$$

According to the datasheet, the typical value of $R_{DS(\text{on})}$ is 0.54Ω at $V_{GS} = 5\text{V}$ and $I_D = 3.4\,\text{A}$, with a maximum specified value of 0.76Ω. Our measured resistance of 0.755Ω is slightly above the typical value but within the expected range considering differences in test current and measurement conditions.

The power dissipated in the lamp was:

$$P_{\text{lamp}} = I_{\text{lamp}} \cdot V_{\text{lamp}} = (1.192)(4.37) \approx 5.21\text{W}, \tag{14}$$

whereas the power dissipated in the MOSFET was:

$$P_{\text{MOSFET}} = I_{\text{lamp}} \cdot V_{DS} = (1.192)(0.90) \approx 1.07\text{W}. \tag{15}$$

The total power delivered to the circuit was:

$$P_{\text{total}} = P_{\text{lamp}} + P_{\text{MOSFET}} = 5.21 + 1.07 = 6.28\text{W}. \tag{16}$$

Thus, the fraction of power dissipated in the MOSFET was:

$$\frac{P_{\text{MOSFET}}}{P_{\text{total}}} = \frac{1.07}{6.28} \approx 17.0\%. \tag{17}$$

When we disconnected the gate from the supply, the lamp remained lit briefly before gradually dimming. This occurred because the MOSFET's gate capacitance retained charge, temporarily keeping the transistor in conduction. As the gate voltage slowly discharged through leakage paths, the MOSFET eventually turned off and the lamp faded.