B. Procedure

1. Multimeter measurements

a) Measurements using diode test function

(a) (b)

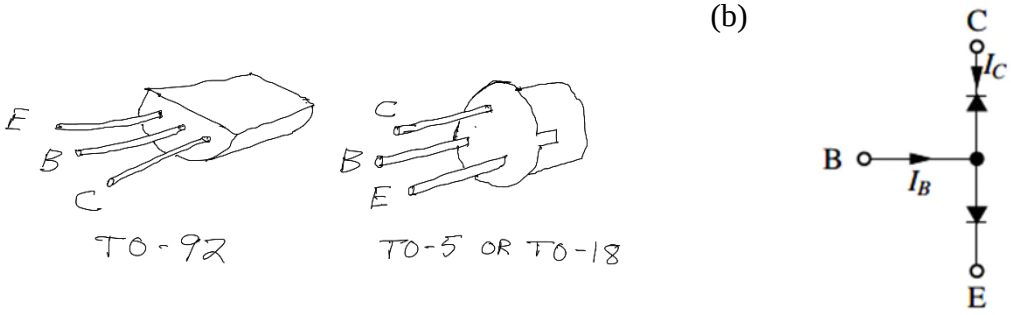

Figure V-1. (a) Pin-out of common bipolar transistor packages (b) Equivalent circuit for two-terminal connections to an NPN transistor

Bring the following to your bench: one each of the 2N3904, 2N2222, and 2N3906 transistors, a DMM, and the connectors needed to connect a transistor to your DMM. Figure V-1(a) shows the pin-outs of the transistor packages.

From the perspective of your multimeter, a connection to E and B (or C and B) can be understood from the equivalent circuit diagram of Figure V-1(b): in both cases you're connecting your multimeter to a diode. For each of your three transistors use the diode test setting of your DMM to measure

(i) the voltage drop from E to B with E more positive than B

(ii) the voltage drop from B to E with B more positive than E

(iii) the voltage drop from C to B with C more positive than B

(iv) the voltage drop from B to C with B more positive than C.

For your report: report the four measured voltage drops for each transistor. Do the values you observed match what you'd expect based on the equivalent circuit of Figure V-1(b)? Can you tell from these measurements whether a given transistor is an NPN or a PNP?

b) Measurements using transistor h_{FE} measurement function.

The BK Precision Model 388B DMM has a transistor h_{FE} measurement function. This function applies $V_{CE} = 3.2\text{V}$ to the transistor, regulates the base current to $I_B = 10\ \mu\text{A},$ and displays the measured current gain $h_{FE} = \dfrac{I_C}{I_B}$ for this condition.

To use this function, you set the dial to either NPN or PNP, depending on which type of transistor you have, and insert the transistor legs into the correct sockets labelled E, B, and C.

Use the DMM to measure h_{FE} for all three transistors. (The sockets seem to be designed to contact thicker leads than we have, so you may need to press your transistor down or a little to the side to get it to connect to the DMM properly.)

For your report: give the values of h_{FE} that you measured.

Note: if you didn't observe normal diode behavior between E and B and between C and B, or if you didn't find a value of h_{FE} in the range from 100 to 300, your transistor may be bad. In that case ask your TA to check that you've made the measurement correctly. If he also finds that the transistor is bad, throw it away and get another one.

2. Basic transistor circuit

a) I_C *vs.* V_{CE} at fixed V_{in}

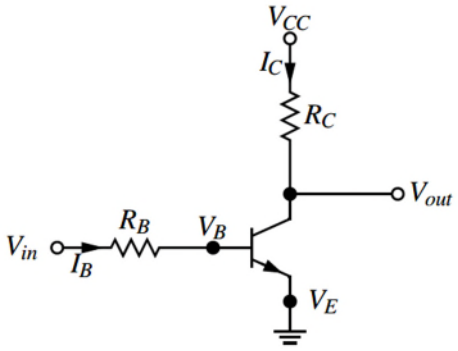

Figure V-2. Basic transistor circuit

Using your 2N2222 transistor, set up the circuit shown in Figure V-2. Use one of the TTi EL302R supplies to generate V_{CC}, and use the positive variable supply on your prototyping board to generate V_{in}. (In terms of the DC voltages and currents, this is a common emitter configuration since the grounds of both supplies are connected to the emitter.) Choose $R_B = 10\ \text{k}\Omega$ and a value of V_{in} such that the base current $I_B \approx 0.5$ mA. (Remember that the voltage drop across R_B is $V_{in} - V_{BE}$, and that with an 0.5 mA base current you can expect that $I_c = \beta I_B \sim 100$ mA and $V_{BE} \approx 0.8$ V (from the 2N2222 spec sheet). Use $R_C = 50\ \Omega$ and set $V_{CC} = +5$ V. You'll be dissipating up to 0.5 Watts in the $50\ \Omega$ resistor. For this reason, choose one of the green resistors that have "PAC 01" written on them for your $50\ \Omega$ resistor. These have a power handling capability of 1 W, so you won't burn them out. The $50\ \Omega$ resistor will limit I_C to be no more than 100 mA, which is safe for the transistor. So, you don't need to worry about setting a safe current limit on your EL302R power supply. Just adjust the current setpoint to be somewhere above 100 mA. Before installing the resistors, check their exact resistance with a multimeter so you can use those values later.

Turn the power supplies on, and measure the voltages across R_B and R_C. From this find the currents I_B and I_C. You should have $I_B \approx 0.5$ mA and $I_C \sim 100$ mA. If you don't, correct the

problem before continuing. For the rest of this part, don't change V_{in}. You will then have a very nearly constant I_B for the rest of this part, independent of the setting of V_{CC}. (Q: why is that?)

Using your multimeter, take a set of measurements of I_C and V_{CE} for a set of different values of V_{CC} ranging from 0 V to 5 V. Take more data points where I_C changes rapidly and less points where it doesn't.

For your report: Make a plot of I_C *vs.* V_{CE} and another plot of h_{FE} *vs.* V_{CE}. How constant is h_{FE}? How do the values you measure for h_{FE} compare to what is on the spec sheet, and also to what you measured with the DMM? The *saturation collector-to-emitter voltage* $V_{CE(sat)}$ is defined as the value of V_{CE} at which the value of $h_{FE} = 10$. What is the value of $V_{CE(sat)}$ for your transistor? How does that compare to what is on the spec sheet?

b) I_C *vs.* V_{BE} at fixed V_{CC}

Set $V_{CC} = 5.0$ V and leave it there for the rest of this part. Take a series of measurements of I_C and V_{BE} for different values of V_{in}. (It will be easiest to measure I_C through measurements of the voltage across R_C, unless you can come up with a second DMM.) Your goal is to make a plot with I_C plotted on a log scale, so take measurements with values of I_C roughly evenly spaced on a log scale. You should be able to cover a range for I_C from about 0.1 mA to 100 mA.

For your report: Make a plot of V_{BE} *vs.* I_C with V_{BE} plotted on a linear scale and I_C plotted on a log scale. According to the *Ebers-Moll* relation the relation between I_C and V_{BE} is $I_C \approx I_S e^{\frac{V_{BE}}{V_T}}$, where I_S and V_T are constants. If this were correct, it follows that a plot of V_{BE} *vs.* $\log(I_C)$ should be a straight line. How close does your data come to following an Ebers-Moll relation? Also, how does your result compare to the similar curve given on the transistor spec sheet?

3. Biasing a transistor

In this part we will work through the biasing of an NPN transistor in a common emitter amplifier. Biasing means that we position the DC voltages and currents on the transistor so that it operates in its active region, *i.e.* is not close to being saturated or in cutoff. The DC conditions that achieve this goal are referred to as the *quiescent* conditions.

Built the circuit shown in Figure I-1 using a 2N3904 npn transistor. It will serve as the beginning of your first common emitter amplifier.

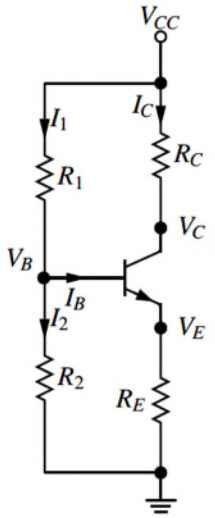

Figure V-3. Biased transistor circuit with no input or output

Helpful hint: The circuits we will make from now on get rather complicated. You definitely want to avoid the "rat's nest" type of circuit. To make good progress, it will help you to make an organized circuit layout that "looks like" the circuit diagram. This will make it easier to find errors in the circuit wiring and to make measurements on the circuit.

Use +20 V for V_{CC}. You want the quiescent current, meaning the current into the collector with no input into the base, to be about 1 mA. Keep in mind that since $I_B \ll I_C$ and $I_B + I_C = I_E$, you can make the approximation $I_C \approx I_E$. You also want the DC component of V_C to be half way in between V_{CC} and ground. This will give the largest possible symmetric swing of the output at V_C once you start adding AC voltages to the DC voltages. Use Ohm's law, the desired voltage drop across R_C and the desired quiescent current to determine the value of R_C.

R_E serves as a way to stabilize any temperature drift in the diode drop V_{BE}. It is necessary to choose $R_E \ll R_C$ so that R_E doesn't significantly affect the total series resistance $R_C + R_E$ (and therefore the quiescent current of 1 mA). About a factor of 10 is good enough for our purposes, meaning you should choose $R_E = R_C / 10$.[1] This will make the voltage drop across R_E to be about 1 V. Since $V_E = 1\,\text{V}$ and $V_C = 10\ \text{V}$, the total quiescent voltage drop across the transistor will be $V_{CE} = 9\ \text{V}$.

[1] Note this part of the biasing problem is different than the one in HW3. In HW 3 problem 3, one goal is to get a AC voltage gain of –25, and the value of R_E is constrained by that requirement. Here, we will be using a circuit in which R_E determines only the biasing and not the AC voltage gain. So here, the value of R_E is *not* constrained by a requirement on AC voltage gain.

R_1 and R_2 serve as a voltage divider to "bias" the base to a constant DC voltage that puts the circuit at the desired quiescent operating point. You don't need much current through the divider to do this, but it is best if the current is large compared to the base current. Since the base current is $1\text{ mA} / h_{FE} \sim 1\text{ mA}/200 \sim 5\ \mu\text{A}$, a current through the divider of about $I_C / 10 = 0.1\text{ mA}$ would work well. You want the base voltage V_B to be 1 diode drop higher than the V_E for the quiescent conditions. From the Ebers-Moll model and the 2N3904 data sheet, this drop is about 0.55 V, so you want $V_B \approx 1.55$ V.

Using this desired $V_B \approx 1.55$ V, $V_{CC} = 20$ V, and the condition that the current through the voltage divider is about 0.1 mA, determine the values of R_1 and R_2.

A few things to notice:

- Your calculated value for R_2 is much less than R_1, so it doesn't significantly affect the total series resistance $(R_1 + R_2)$ of the voltage divider.
- The input impedance looking into the base of the transistor is approximately βR_E. Since this is significantly large than R_2, the voltage divider feeds only a small fraction of its current into the base, so it is relatively "stiff".

Once you've computed your values for R_C, R_E, R_1, and R_2, set everything up and turn on V_{CC}. Measure V_C, V_B, and V_E. If you find the V_C is not in the range from 8 V to 12 V, make adjustments to your voltage divider as need to get V_C into that range.

For your report: Give your values for R_C, R_E, R_1, and R_2. Report your voltage measurements for V_C, V_B, and V_E.

4. Common emitter AC amplifier

Now build the circuit shown in Figure V-4 by adding onto your circuit from the previous part. This is your common emitter AC amplifier. You can use either an electrolytic or a film capacitor for the 1 μF capacitor (film is a little better), but if you use an electrolytic capacitor, take care to insert it into your circuit with the correct polarity. You can damage the capacitor if you put it in backwards.

Normally the AC gain of the common-emitter amplifier is $A_V = \dfrac{R_C}{r_{tr} + R_E}$, where $r_{tr} \approx \dfrac{0.026\text{ V}}{I_E}$ is the transistor *transresistance.* It is a resistance that appears in series with the emitter. However in this case we have a large capacitor in parallel with R_E. One key idea of this circuit is that R_E is a part of the DC network that biases the transistor, but it does not affect the AC gain of the circuit for frequencies ω such that the capacitor reactance $\dfrac{1}{\omega C}$ is negligible. That is because the

capacitor effectively becomes an AC short circuit to ground. In that limit the AC gain of the amplifier should (in theory) be $A_V \approx \frac{R_C}{r_{tr}}$.

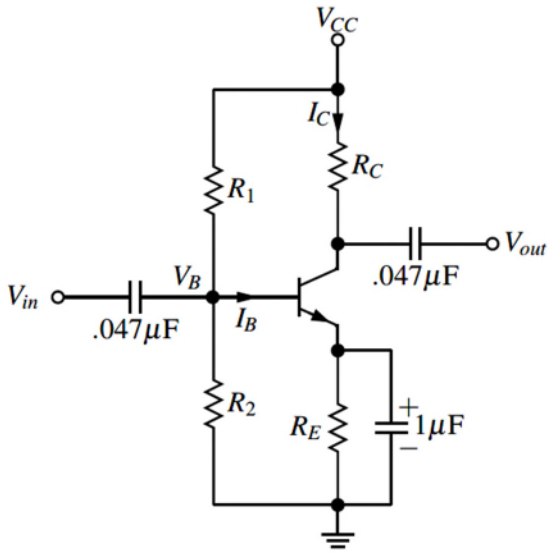

Figure V-4. AC coupled common-emitter amplifer.

Set V_{in} to be a sine wave and observe the output voltage V_{out} on an oscilloscope. Set the amplitude of V_{in} to be very small so that you don't have any clipping of the output sine wave. (The 20 dB attenuation button on the signal generator may help with this, and if necessary you can get a further input voltage reduction with an approximate 10x voltage divider made from a 500 Ohm and 50 Ohm resistor just before V_{in}.) Measure the AC voltage gain of this circuit as a function of frequency from about 100 Hz to about 500 kHz.

For your report: include an oscilloscope trace showing an example of the input and output sine waves. Include a plot of the AC voltage gain *vs.* frequency. Explain as much as you can about the frequency-dependent gain. In particular, discuss the role of the capacitors in setting this gain.

5. 2N2222A specifications

2N2222A

Small Signal Switching Transistor

NPN Silicon

Features

- MIL−PRF−19500/255 Qualified
- Available as JAN, JANTX, and JANTXV

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	50	Vdc
Collector−Base Voltage	V_{CBO}	75	Vdc
Emitter−Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	800	mAdc
Total Device Dissipation @ T_A = 25°C	P_T	500	mW
Total Device Dissipation @ T_C = 25°C	P_T	1.0	W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	325	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	150	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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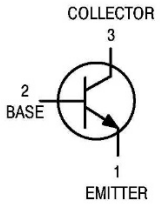

TO−18
CASE 206AA
STYLE 1

ORDERING INFORMATION

Device	Package	Shipping
JAN2N2222A	TO−18	Bulk
JANTX2N2222A		
JANTXV2N2222A		

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (I_C = 10 mAdc)	$V_{(BR)CEO}$	50	−	Vdc
Collector−Base Cutoff Current (V_{CB} = 75 Vdc) (V_{CB} = 60 Vdc)	I_{CBO}	− −	10 10	μAdc nAdc
Emitter−Base Cutoff Current (V_{EB} = 6.0 Vdc) (V_{EB} = 4.0 Vdc)	I_{EBO}	− −	10 10	μAdc nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 Vdc)	I_{CES}	−	50	nAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain (I_C = 0.1 mAdc, V_{CE} = 10 Vdc) (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (I_C = 500 mAdc, V_{CE} = 10 Vdc)	h_{FE}	50 75 100 100 30	− 325 − 300 −	−
Collector−Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	− −	0.3 1.0	Vdc
Base−Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{BE(sat)}$	0.6 −	1.2 2.0	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Magnitude of Small−Signal Current Gain (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	$\|h_{fe}\|$	2.5	−	−
Small−Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{fe}	50	−	−
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, 100 kHz ≤ f ≤ 1.0 MHz)	C_{ibo}	−	25	pF
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0,100 kHz ≤ f ≤ 1.0 MHz)	C_{obo}	−	8.0	pF
SWITCHING (SATURATED) CHARACTERISTICS				
Turn−On Time (Reference Figure in MIL−PRF−19500/255)	t_{on}	−	35	ns
Turn−Off Time (Reference Figure in MIL−PRF−19500/255)	t_{off}	−	300	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

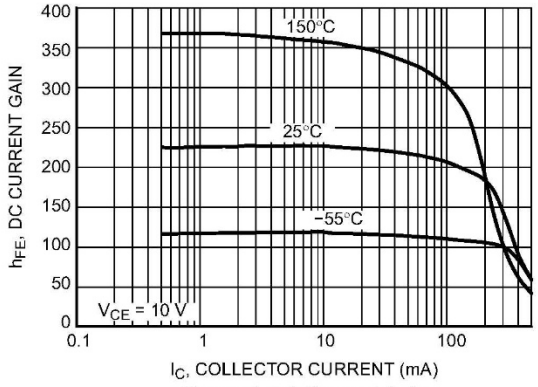

Figure 1. DC Current Gain

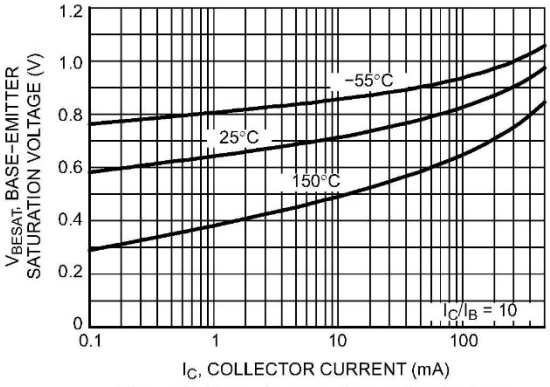

Figure 2. Base−Emitter Saturation Voltage

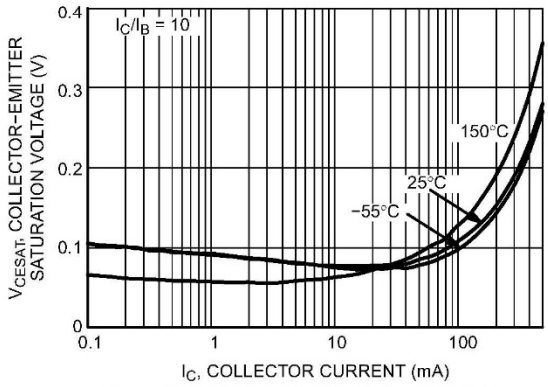

Figure 3. Collector−Emitter Saturation Voltage

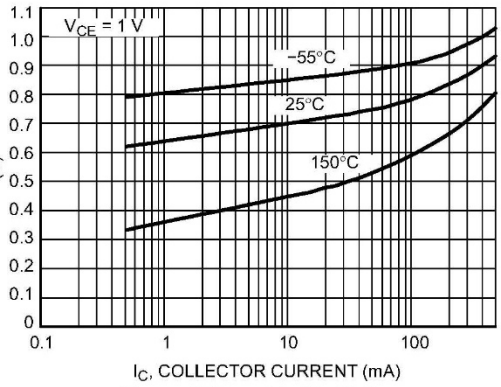

Figure 4. Base−Emitter Voltage

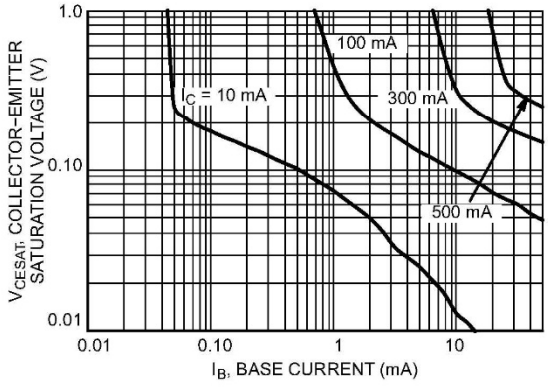

Figure 5. Collector Saturation Region

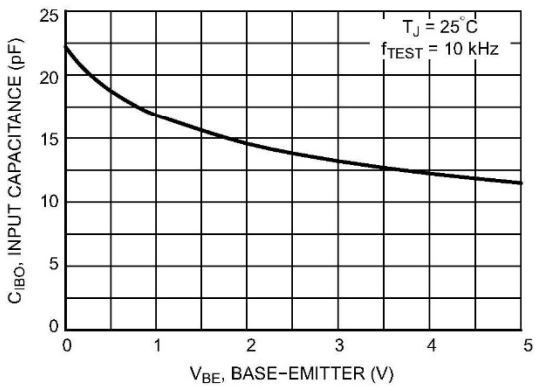

Figure 6. Input Capacitance