VII. Lab 7: Operational Amplifiers I

A. Introduction

In this lab you will study (i) the open-loop behavior of an op-amp, (ii) an inverting amplifier, and (iii) a summing amplifier.

1. Op amp rules

When used with negative feedback, an op-amp comes close to an ideal op-amp that obeys the following rules

I. The output attempts to adjust itself so that the voltage difference between the two input pins goes to zero.

II. The inputs draw no current.

To reiterate, rule I applies only if the circuit has negative feedback. If it has no feedback or positive feedback, rule I does not apply.

2. Op-amps in the lab

A "jelly-bean" op-amp is one that is widely used, relatively inexpensive (less than $1 each) and has specs that are good enough for basic applications.

We have the following "jelly-bean" op-amps in the lab:

1. LM741. This is a bipolar transistor op-amp. It was the most widely used op-amp for decades after its introduction in 1968. Today, it is rarely used in new designs. However it still has decent specs and works fine for many applications. It's nearly always used with ±15 V supply voltages.

2. TL071. This is an op-amp with JFET input transistors. As a result its inputs draw much less current than the LM741. It is also about 5 times faster than the LM741. It can be operated with supply voltages ranging from ±2.25 V to ±20 V.

3. LF411. This is a JFET input op-amp that is similar to the TL071. It has somewhat lower noise than the TL071 and is not quite as fast. It can be operated with supply voltages ranging from ±3.5 V to ±18 V.

4. LM358. This is a bipolar transistor op-amp, and also a "single-supply" op amp. This means that the input and output voltage cans swing to the negative supply voltage. This allows the op-amp to be used with its negative supply at ground, even with small input signals that are close to ground. With the above op-amps that wouldn't work because the input voltage can't be within about 1 or 2 volts of the negative supply. But the LM358 can do that, so it can be powered with a single supply providing the voltage V_{CC+}. This positive supply can be operated at voltages from +3 V to + 30 V. The LM358 can also be operated on a dual supply with voltages up to ±15 V. The LM358 is also a "dual" op-amp, *i.e.* the package contains two separate op-amps.

We'll mainly use the LF411 for our measurements because it is a very typical op-amp for dual supply operation that has quite good specs. The specifications for the LF411 are given at the end of this chapter.

In addition we have the following special purpose op-amps in the lab:

5. OPA227. This is a high-end precision op amp with very low input offset voltage and noise. It is a bipolar transistor op amp. It can be operated with supply voltages ranging from ±2.5 V to ±18 V.

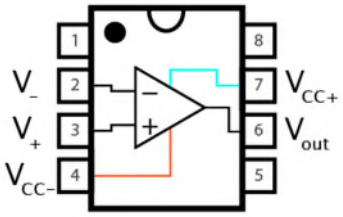
6. LTC1150. This is a zero-drift "chopper" op amp. It is a CMOS op-amp which excels at DC applications requiring very low input offset voltage and drift.

7. MCP602. This is a low-voltage, low-power, single supply CMOS op-amp. This combination of low power, low voltage, and single supply operation make it very suitable for battery-powered circuits. The voltage difference between the positive and negative supply pin must be between 2.7 and 6.0 V. It is the only op-amp in the lab that *cannot* be operated on ±15 V supply. It is also a "dual" op-amp, *i.e.* the package contains two separate op-amps.

Please don't use these special-purpose op-amps until directed to do so. The OPA227 and the LTC1150 cost $4.18 and $8.62, respectively, and they won't show a different behavior for the first set of experiments. The MCP602 is not expensive but it can't be operated with the same dual supply voltages as the others.

3. Op-amp pin-out and use in breadboard.

(a)



(b)

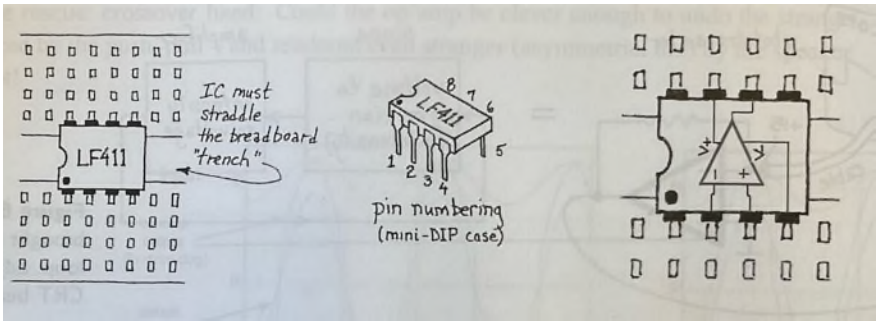


Figure VII-1. (a) Pin-out for an LM741 or LF411 op-amp in a DIP8 package. This image shows the top view of the IC. (b) Placement of a DIP8 package op-amp in a breadboard. Image is borrowed from "Learning the art of electronics," by T. C. Hayes.

All of our op-amps come in a so-called "DIP8" package. The pin-outs for the LM741 and LF411 are shown in Figure VII-1(a). This shows the IC from the top. You determine where to start counting pin 1 by referring either to the dot or the half-circle cutout on the IC. In the figure, V_{CC+} denotes the positive power supply pin and V_{CC-} denotes the negative power supply pin. Pin 1 and

pin 5 are “offset null” connections that can be used to adjust the input offset voltage of the op-amp, but we won’t be using these connections today. Pin 8 is not connected to anything.

Most single op-amps in a DIP8 package have this same pin-out, although you should refer to the spec sheet to be sure. Of course dual op-amps like the LM358 have a completely different pin-out.

To use the op-amp in a breadboard, you position it so that it *straddles the gap* in the breadboard as shown in Figure VII-1(b). Once the IC is inserted in this way, you can connect to pin1 using any of the four sockets lined up with pin 1, and similarly for the other pins.

4. Power supply decoupling.

Any circuit that has a high-gain element such as an op-amp is vulnerable to “parasitic oscillations.” This happens when the “parasitic” capacitances or inductances of parallel wires or loops of wire cause phase shifts that turn negative feedback into positive feedback. This typically occurs at high frequency ~ hundreds of kHz to tens of MHz ~ and often appears as a “fuzz” on your signals. In a severe case it can cause your op-amp circuit to oscillate between its supply voltages. This is particularly a problem with breadboard circuits due to the use of relatively long wires without any nearby ground plane.

One step that can really help to prevent these oscillations is *power supply decoupling*. To do this, you insert a 10 to 100 nF capacitor between each voltage supply pin and ground at a point that is close to the op-amp, as shown in Figure VII-2. This effectively puts an AC short circuit between the power supply pins and ground, which removes the parasitic capacitances and inductance of the power supply wires from the circuit. Most experienced electronic designers do this as a routine practice. If you don’t do this and see evidence of parasitic oscillations, try it and see if the oscillations go away.

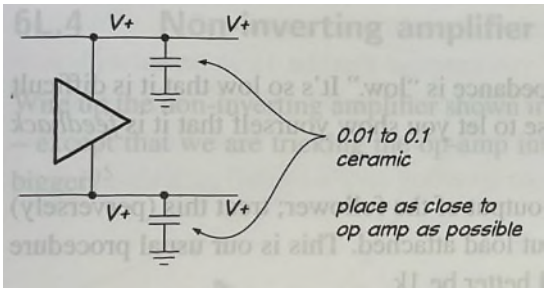


Figure VII-2. Decoupling of power supply from op-amp circuit. Without taking this step, you may find that your circuit generates some “fuzz.” Image is borrowed from “Learning the art of electronics”, by T. C. Hayes.

B. Procedure

1. Open-loop op-amp, comparator

Build the circuit shown in Figure VII-3(a). Use +15 V for V_{CC+} and -15 V for V_{CC-}. You can get these voltages from your breadboard +V and –V power supplies. Just make sure to adjust the voltage to the correct ± 15 V using the adjustment knobs or screws before hooking up the op-amp. (It is generally good practice to (i) adjust your supply voltages, (ii) turn the supplies off,

(iii) construct your circuit with the supplies off making sure you have the wiring correct, and then (iv) turn the supplies on.)

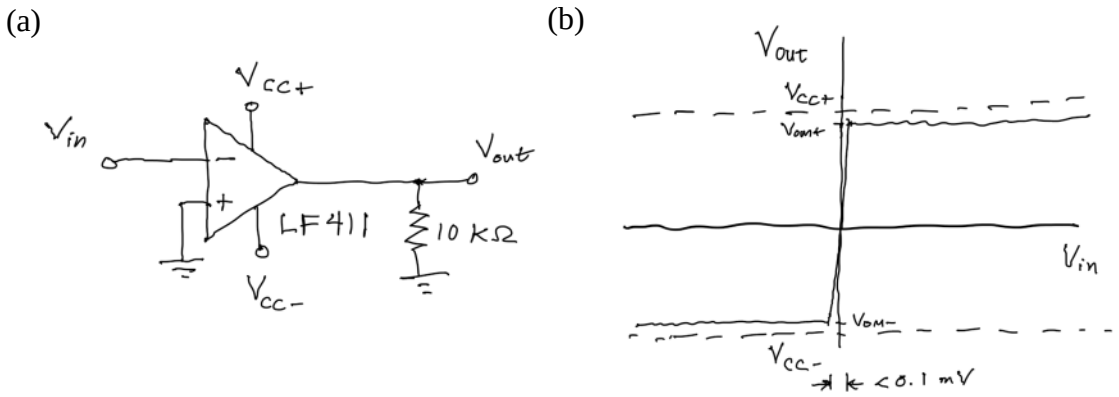


Figure VII-3. (a) Open-loop op-amp circuit (b) Expected V_{out} *vs.* V_{in} for the open-loop circuit.

Connect a function generator to V_{in} and also display V_{in} on an oscilloscope. Connect V_{out} to the other channel of the oscilloscope. Adjust V_{in} to be a small-amplitude, low frequency sine wave with no offset. An amplitude of a few hundred mV would be suitable. Observe what you get for $V_{out}(t)$ and $V_{in}(t)$.

You should find that your circuit functions as a *comparator*. A comparator is a circuit that outputs a high voltage (here near V_{CC+}) when $V_+ > V_-$ and outputs a low voltage (here near V_{CC-}) when $V_+ < V_-$, where V_+ and V_- are the voltages on the + and – input pins, respectively. Observe the output for a range of frequencies to see what happens.

For your report: Include a representative copy of the oscilloscope display of $V_{out}(t)$ and $V_{in}(t)$. Explain why the linear gain region of the op-amp (sloped region near $V_{in} = 0$) does not play any role in this circuit. Measure the maximum output voltage V_{0M+} and the minimum output voltage V_{0M-}. These measure the output voltage range that the op-amp can do. Are these the same as the supply voltages, or different than the supply voltages? Compare what you get to the maximum voltage swing shown on the spec sheet.

You should find that the output voltage is visibly different from a perfect square wave because it takes a finite time for the voltage to rise or fall. This will be especially obvious for frequencies above 100 kHz. Measure this rise and fall time.

The effect you're seeing is a consequence of the finite *slew rate* of the op amp. This is the fastest rate at which its output voltage can change. It is more precisely defined as the rate at which the voltage changes with a *square wave input with an amplitude of 1 Volt or more*. So, switch your input function to a square wave with 1 Volt amplitude. Measure the slew rate (slope of the rise or fall of the output waveform) in units of Volts per microsecond in this condition. How does your result compare to what is shown on the spec sheet?

Comment: although an op-amp can function as a comparator, it's best not to use it for that purpose. You should use a comparator IC instead. These are circuits that are optimized for the comparator function and have fast switching times.

2. Inverting amplifier

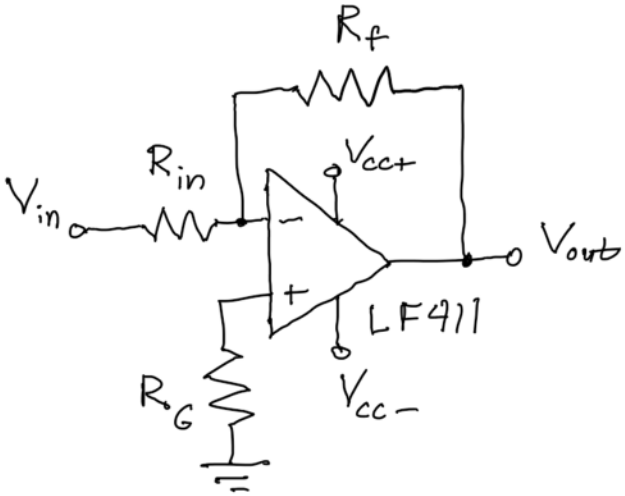


Figure VII-4. Inverting amplifier

Build the inverting amplifier circuit shown in Figure VII-4. The voltage gain of this circuit is $G = \frac{-R_f}{R_{in}}$. Start with resistors that give you a gain of 10. A good range for the resistance values of R_f and R_{in} is between about 5 kΩ and 500 kΩ. The value of R_G doesn't matter very much. Something like 1 kΩ is fine for that.

Hook a function generator up to the input set for a sine wave with no offset. Again display $V_{out}(t)$ and $V_{in}(t)$ on the oscilloscope, and set the scope to measure the frequency of the waveform and the amplitude of $V_{out}(t)$ and $V_{in}(t)$. *Measure the gain of the amplifier as a function of the sine wave frequency f.* Cover the range of *f* from 1 Hz to 1 MHz, with about 2-3 points per decade of *f*.

Repeat the last step with a gain of 100.

For your report: plot the gain vs. *f* for both resistance ratios together on the same log-log plot. After you make this plot, extrapolate from these curves (by hand using a ruler if you like) to get a rough estimate of the open-loop gain as a function of frequency.

Use the two rules for an op-amp given above to explain/derive how the gain is produced for the inverting amplifier.

3. Summing amplifier

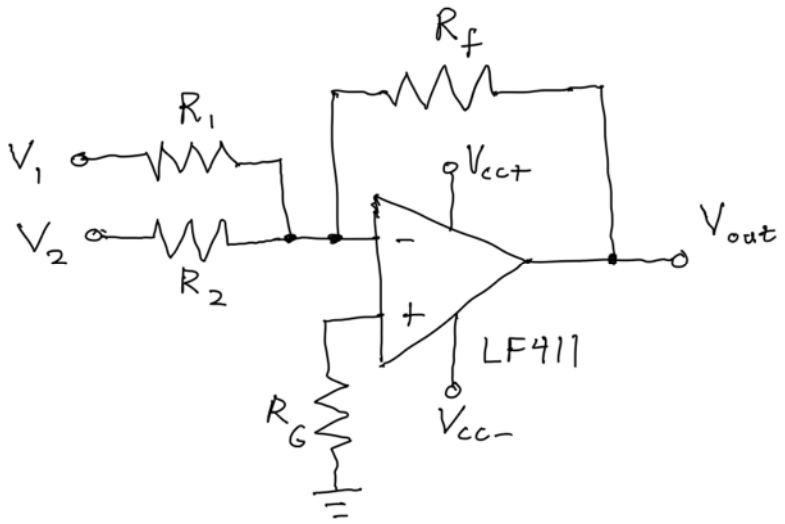


Figure VII-5. Summing amplifier.

Build the summing amplifier circuit shown in Figure VII-5. In addition to your power supplies for V_{CC+} and V_{CC-}, you will need two more DC power supplies for V_1 and V_2. You can use the TTi, BK precision, and/or the Extech power supplies for these latter two.

First, use $V_1 = V_2 = +5$ V and $R_1 = R_2 = R_f = 10$ kΩ and measure V_{out} using your multimeter. To see what the circuit does, change the input voltages and observe the output. Then, using the input voltages equal, try different values for some of the resistances (including R_f) and look at the output. Use however many combinations that you need to determine what the circuit does.

For your report: Report each voltage and resistor combination that you used along with the corresponding output voltage for each. Use what you observed to determine an equation relating the input and output voltages to the three resistor values. Generalize this equation for *N* inputs.

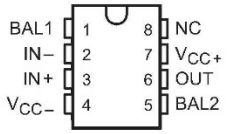
Op Amp Specifications

LF411
JFET-INPUT OPERATIONAL AMPLIFIER

SLOS011C – MARCH 1987 – REVISED OCTOBER 1997

- **Low Input Bias Current, 50 pA Typ**
- **Low Input Noise Current, 0.01 pA/√Hz Typ**
- **Low Supply Current, 2 mA Typ**
- **High Input impedance, 10^{12} Ω Typ**
- **Low Total Harmonic Distortion**
- **Low 1/f Noise Corner, 50 Hz Typ**
- **Package Options Include Plastic Small-Outline (D) and Standard (P) DIPs**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

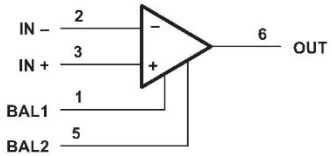
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a maximum input offset voltage drift. It requires low supply current, yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF411 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF411C is characterized for operation from 0°C to 70°C. The LF411I is characterized for operation from –40°C to 85°C.

symbol



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	2 mV	LF411CD	LF411CP
–40°C to 85°C	2 mV	LF411ID	LF411IP

The D packages are available taped and reeled. Add the suffix R to the device type (i.e., LF411CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} . . . . . 18 V
Supply voltage, V_{CC-} . . . . . –18 V
Differential input voltage, V_{ID} . . . . . +30 V
Input voltage, V_I (see Note 1) . . . . . +15 V
Duration of output short circuit . . . . . Unlimited
Continuous total power dissipation . . . . . 500 mW
Package thermal impedance, θ_{JA} (see Note 2): D package 1975C/W
P package 1045C/W
Storage temperature range, T_{stg} . . . . . –655C to 1505C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds 2605C

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	C SUFFIX		I SUFFIX		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC+}	3.5	18	3.5	18	V
Supply voltage, V_{CC-}	–3.5	–18	–3.5	–18	V
Operating free-air temperature, T_A	0	70	–40	–85	5C

electrical characteristics over operating free-air temperature range, V_{CC+} = +15 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A		MIN	TYP	MAX	UNIT
			LF411C	LF411I				
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ	255C	255C		0.8	2	mV
α_{VIO}	Average temperature coeffi-cient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ				10	20†	µV/5C
I_{IO}	Input offset current‡	V_{IC} = 0	255C	255C		25	100	pA
			705C	855C			2	nA
I_{IB}	Input bias current‡	V_{IC} = 0	255C	255C		50	200	pA
			705C	855C			4	nA
V_{ICR}	Common-mode input voltage range				+11	–11.5 to 14.5		V
V_{OM}	Maximum peak output-voltage swing	R_L = 10 kΩ			+12	+13.5		V
A_{VD}	Large-signal differential voltage	V_O = +10 V, R_L = 2 kΩ	255C	255C	25	200		V/mV
			05C to 705C	–405C to 855C	15	200		
r_i	Input resistance	T_J = 255C				10^{12}		Ω
CMR R	Common-mode rejection ratio	R_S 3 10 kΩ			70	100		dB
k_{SVR}	Supply-voltage rejection ratio	See Note 3			70	100		dB
I_{CC}	Supply current					2	3.4	mA

† At least 90% of the devices meet this limit for α_{VIO}.
‡ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperatures as possible.
NOTE 3: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

operating characteristics, V_{CC+} = +15 V, T_A = 255C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/µs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz