Computer Organization 2023 Lab 4

Finished part:

I finished/updated all the modules including ALU_Ctrol.v, Decoder.v, Reg_file.v, and Simple_Single_CPU.v. Moreover, I passed all the testcases given by the TAs.

```
============================================
(A) basic score:          75 / 75
============================================
   Congratulation. You pass  TA's pattern
============================================
```

Problems you met and solutions:

The only problem I met was connecting the CPU in the Simple_Single_CPU.v. I thought I could reuse some wires (ex: wireA = wireA && wireB), but it turns out to be a greedy move and cost me a few hours of debugging. After noticing my mistake, the problem was easily resolved.

If you create additional module, please give a short explanation here:

I do not have any additional module. However, in this homework’s testbench, there are “`include” on top of the code while the previous homework did not. Moreover, it does not contain ALU_1bit.v and Full_Adder.v and my program needs these 2, so please be aware.