Curriculum Vitae

Personal Details

Name	YANG Yuze	Birth Date	September 1, 1995
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Education Background

09/2014-06/2018 **Nanjing Tech University**
Degree: Bachelor of Science in Applied Physics

09/2018-09/2019 **Hongkong University of Science and Technology**
Degree: Master of IC Design Engineering

Academic Projects

10/2016-5/2017 **Measurement of Bridge Deformation Using Resistance Strain Gauges | University Student Innovation Project**

- Built bridge circuits and programmed to control SCM with the knowledge of circuit analysis

09/2017 Calibration and Imaging of Computed Tomography System Parameters | Mathematical Modeling Contest

- Worked as a paper writer in the team, participated in group discussion, and summarized modelling ideas

03/2017-07/2017

Exciplex OLEDs Based on ICT Materials | Extracurricular Experiment

- Tested the spectral properties of organic fluorescent materials in different environments with the spectrometer, the laser emitter and the vacuum coating machine, aiming at extending the usage and selection scope of the TADF material and give an outline for choosing transporting materials when optimizing the TADF device.

Working Experience

04/2017-06/2017 **Intern | Schneider Electric (China) Co., Ltd**

- Set up the test configuration according to the test plan, conducted required tests cases, and delivered defined documents.

01/2018-07/2018 Intern | The ivip Group of the Electrical Engineering Department of Tsinghua University

- Responsible to the chip's test method, design the test plan based on the requirement.

  Doing research on DVS (Dynamic Version Sensor), combining the DVS with Image recognition algorithm.

9/2019-2022/3 **Engineer | HongKong Applied Science and Technology Research Institution**

- Responsible for part of SAR ADC circuit design, and ran basic simulation on Cadence virtuoso to check ADC performance. Highly brought up the ADC resulotion to 9.8 bits.
- Designed a test plan for taped out ADC and design ADC test board by using Altium Designer.Finished ADC chip validation and draft testing report.

- Responsible for BGR trimming circuit for a 16bits sigma-delta ADC, and built testbench for integrated circuit simulation.Debugged some modulation error to increase dynamic performance.

3/2022-Present **Senior Engineer | HongKong Applied Science and Technology Research Institution**

- Implement digital IC design for speed bridge of ethernet adaptor circuits. It can adapt high speed IO (XGMII) comunication with low speed host interface.
- Implement digital IC design for USB3.0 speed bridge circuits design.

Publication

03/2020 MSP-MFCC: Energy-Efficient MFCC Feature Extraction Method With Mixed-Signal Processing Architecture for Wearable Speech Recognition DOI: 10.1109/ACCESS.2020.2979799

In this paper,we propose a Mixed-Signal Processing (MSP) architecture to efficiently extract Mel-Frequency Cepstrum Coefficients (MFCC) features. Based on measured results show the energy consumption of MSP-MFCC is 0.72 μJ /frame, and the processing speed is up to 45.79 μs /frame. MSP-MFCC achieves 95% energy saving and about 6.4× speedup than state of the art.

Honors and Awards

05/2014 The Third Class Scholarship of School of Mathematical Sciences, Nanjing Tech University

10/2017 The Second Award of The 13th Nanjing Tech University Undergraduate science and Technology Forum.

11/2017 The First Award of The Jiangsu Province Innovation Competition of Physical Experiment of College Students

Skills

Languages English (Fluent): TOEFL 90 (R28, L24, S18, W20), Mandarin (Native Speaker)

Software Visual C++(Advanced), Matlab (Intermediate), Verilog(Advanced)

Programming C(Advanced)