林亦波

助理教授 ◇ 设计自动化与计算系统系 ◇ 集成电路学院 ◇ 北京大学

yibolin@pku.edu.cn ◇ www.yibolin.com

研究方向

面向超大规模集成电路设计自动化的建模和优化、深度学习及其应用、异构计算

教育经历

德克萨斯大学奥斯汀分校 2013 年 8 月 – 2018 年 5 月

博士学位, 电子与计算机工程系

指导老师: David Z. Pan

博士毕业论文: Bridging Design and Manufacturing Gap through Machine Learning and Machine-Generated Layout

上海交通大学 2009 年 9 月 – 2013 年 6 月

学士学位, 微电子学院

工作经历

北京大学 (Peking University) 2019 年 7 月至今

助理教授

集成电路学院设计自动化与计算系统系 (自 2021 年 11 月)

信息科学技术学院高能效计算与应用中心

德克萨斯大学奥斯汀分校 (University of Texas at Austin) 2018 年 6 月 – 2019 年 6 月

博士后

授课经历

主讲	集成电路工程算法	研究生课程, 2023-2024 年
主讲	设计自动化与计算系统	研究生课程, 2022-2024 年
主讲	芯片设计自动化与智能优化	本科生课程, 2021-2024 年
主讲	计算概论 B	本科生课程, 2020-2022 年

奖项及荣誉

最佳论文提名	ASPDAC	2025 年
最佳论文提名	ICCAD	2024 年
最佳论文 & 荣誉提名论文	ISEDA	2024 年
青年科技奖 (Early Career Award, 每年仅 1 位)	中国计算机学会集成电路专委	2023 年
首届最佳审稿人奖	ICCAD	2023 年
最佳论文 (4/205)	DATE	2023 年
最佳论文 (4/249)	DATE	2022 年
最佳论文提名	ICCAD	2022 年
最佳论文 (2/3495, 4 年)	TCAD	2021 年

最佳论文	ISPD	2020 年
最佳论文提名	ASPDAC	2020 年
最佳论文 (1/201) & 提名 (5/201)	DAC	2019 年
最佳论文提名	ISPD	2019 年
首届最佳论文	Integration, the VLSI Journal	2018 年
Franco Cerrina Memorial 最佳学生论文	SPIE	2016 年
A. Richard Newton Young Student Fellow	DAC	2014 年

学术服务

执行委员会成员

- 大会共同主席, ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD), 2025 年
- 程序共同主席, ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD), 2024 年
- 圆桌论坛主席, IEEE International Symposium of Electronics Design Automation (ISEDA), 2023 年–2024 年
- 财务主席, ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2021 年–2023 年

期刊编辑

- 副编辑，ACM Transaction on Design Automation of Electronic Systems (TODAES), 2024 年至今
- 副编辑，Elsevier Integration, the VLSI Journal (Integration), 2024 年至今
- 客座编辑，ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2024 年
- 客座编辑，ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2022 年

赛题主席

- 赛题主席，集成电路 EDA 设计精英挑战赛，2021 年–2023 年

技术程序委员会成员

- ACM/IEEE Design Automation Conference (DAC): 2020
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD): 2018 – 2021, 2023
- Design, Automation and Test in Europe Conference (DATE): 2025
- IEEE International Conference on Computer Design (ICCD): 2019
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC): 2021 – 2022
- ACM International Symposium on Physical Design (ISPD): 2020, 2025
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD): 2021
- ACM Great Lakes Symposium on VLSI (GLVLSI): 2024
- Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI): 2021
- IEEE Electron Devices Technology and Manufacturing Conference (EDTM): 2021

- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS): 2022.

期刊审稿人

- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Computers (TC)
- ACM Transaction on Design Automation of Electronic Systems (TODAES)
- SPIE Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)
- Elsevier, Integration, the VLSI Journal (Integration)

其他志愿服务

- ACM SIGDA 网站管理负责人，2021 年至今

10 篇代表性论文

按时间倒序排列。标 * 表示通讯作者。

1. Yifan Chen, Zaiwen Wen, Yun Liang and **Yibo Lin***, "Stronger Mixed-Size Placement Backbone Considering Second-Order Information", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct 29-31, 2023.
2. Haoyi Zhang, Xiaohan Gao, Haoyang Luo, Jiahao Song, Xiyuan Tang, Junhua Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, "SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Apr 17-19, 2023. (**Best Paper Award**)
3. Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin***, "Multi-Electrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity, Clock Feasibility, and Timing Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sep, 2023.
4. Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "Accelerating Static Timing Analysis using CPU-GPU Heterogeneous Parallelism", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2023.
5. Qipan Wang, Xiaohan Gao, **Yibo Lin***, Runsheng Wang and Ru Huang, "DeePEB: A Neural Partial Differential Equation Solver for Post Exposure Baking Simulation in Lithography", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 01-03, 2022. (**Best Paper Nomination**)
6. Zizheng Guo and **Yibo Lin***, "Differentiable-Timing-Driven Global Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.
7. Siting Liu, Peiyu Liao, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, "FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022. (**Best Paper Award**)
8. Zizheng Guo, Jing Mai and **Yibo Lin***, "Ultrafast CPU/GPU Kernels for Density Accumulation in Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

9. Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Large Designs", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

10. **Yibo Lin***, Zixuan Jiang, Jiaqi Gu, Wuxi Li, Shounak Dhar, Haoxing Ren, Brucek Khailany and David Z. Pan, "DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Apr, 2021. (**Best Paper Award**)

发明专利列表

[P18] 吴恒, 卢浩然, 江循, 孙嘉诚, 王润声, **林亦波**, 黄如, "半导体结构的制备方法、半导体结构、器件及设备", 中国专利, CN2024101785421, Feb 09, 2024. (submitted)

[P17] **林亦波**, 郭资政, 张作栋, 江循, 王润声, 黄如, "电路门级逻辑仿真方法、装置、计算机设备和存储介质", 中国专利, CN2023112735027, Jan 09, 2024. (submitted)

[P16] 余备, 廖培宇, **林亦波**, "一种基于 MoreauEnvelope 近似线长模型的大规模解析布局方法", 中国专利, CN2023111300780, Nov 28, 2023. (submitted)

[P15] 王润声, 张作栋, **林亦波**, 黄如, "一种基于解析模型的晶体管老化应力计算方法", 中国专利, CN202310843291X, Oct 13, 2023. (submitted)

[P14] **林亦波**, 高笑涵, 张昊懿, 王润声, 黄如, "一种多驱动能力的集成电路标准单元版图迁移的方法", 中国专利, CN2023101249631, Mar 28, 2023.

[P13] **林亦波**, 王启盼, 王润声, 黄如, "一种集成电路微带线传输线自动化分析设计方法", 中国专利, CN2023100496576, Mar 17, 2023.

[P12] **林亦波**, 郭资政, 谷丰, "一种 GPU 加速构建最小直角斯坦纳树的芯片布线方法", 中国专利, CN2022112858018, Jan 03, 2023. (submitted)

[P11] **林亦波**, 高笑涵, 张昊懿, 王润声, 黄如, "可处理电学和几何约束的模拟电路布线自动化方法及系统", 中国专利, CN2022114229951, Dec 20, 2022.

[P10] 郭资政, **林亦波**, 黄琮蔚, "一种集成电路静态时序分析中的路径分析方法", 中国专利, CN2021103772507, Oct 18, 2022. (submitted)

[P9] **林亦波**, 郭资政, "一种可微分时序驱动的芯片布局优化方法", 中国专利, CN2022107930171, Aug 05, 2022.

[P8] **林亦波**, 张昊懿, 高笑涵, 王润声, 黄如, "一种用于模拟电路版图布线的交互式编辑方法及工具", 中国专利, CN2022100363194, May 17, 2022.

[P7] **林亦波**, 麦景, "基于多电场模型的时钟驱动 FPGA 芯片全局布局方法", 中国专利, CN2022102058942, Apr 12, 2022.

[P6] **林亦波**, 张作栋, 郭资政, 王润声, 黄如, "一种老化及涨落感知的动态时序分析方法", 中国专利, CN2021115414669, Apr 5, 2022. (submitted)

[P5] **林亦波**, 张作栋, 郭资政, 王润声, 黄如, "一种基于事件传播的动态时序分析方法", 中国专利, CN2021109930951, Dec 24, 2021.

[P4] **林亦波**, 郭资政, 黄琮蔚, "一种 GPU 加速计算的集成电路无悲观路径分析方法", 中国专利, CN2021110703249, Dec 24, 2021.

[P3] 麦景, 郭资政, **林亦波**, "一种集成电路设计中器件密度分布的计算方法", 中国专利, CN2021105506486, Aug 27, 2021.

[P2] 高笑涵, **林亦波**, 刘鸣杰, 潘志刚, "一种交互式模拟电路版图编辑方法及系统", 中国专利, CN2021101747163, Jun 18, 2021.

[P1] 郭资政, 黄琮蔚, **林亦波**, "一种 GPU 加速计算的集成电路静态时序分析方法", 中国专利, CN2020111436325, Jan 22, 2021.

著作及论文列表

书籍章节

[B3] **Yibo Lin**, Zizheng Guo and Jing Mai, "Deep Learning Framework for Placement", Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)

[B2] Haoyu Yang, **Yibo Lin** and Bei Yu, "Machine Learning for Mask Synthesis and Verification", Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)

会议及期刊论文 (标 * 表示通讯作者)

论文成果包括: DAC (23 篇), ICCAD (16 篇), IEEE TCAD (27 篇), DATE (14 篇), ...

[J176] Siting Liu, Ziyi Wang, Fangzhou Liu, **Yibo Lin**, Bei Yu* and Martin Wong, "Sign-off Timing Considerations via Concurrent Routing Topology Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J175] Yuxiang Zhao, Zhuomin Chai, Xun Jiang, **Yibo Lin***, Runsheng Wang and Ru Huang, "PDNNet: PDN-Aware GNN-CNN Heterogeneous Network for Dynamic IR Drop Prediction", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J174] Zhenkun Lin, Genggeng Liu*, Xing Huang, **Yibo Lin**, Jixin Zhang, Wenhao Liu and Ting-Chi Wang, "A Unified Deep Reinforcement Learning Approach for Constructing Rectilinear and Octilinear Steiner Minimum Tree", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J173] Bingyang Liu, Haoyi Zhang, Xiaohan Gao, Zichen Kong, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, "LayoutCopilot: An LLM-powered Multi-agent Collaborative Framework for Interactive Analog Layout Design", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[C172] Tianxiang Zhu, Qipan Wang, **Yibo Lin***, Runsheng Wang and Ru Huang, "MORE-Stress: Model Order Reduction based Efficient Numerical Algorithm for Thermal Stress Simulation of TSV Arrays in 2.5D/3D IC", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025. (accepted)

[C171] Xizhe Shi, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "Handling Latch Loops in Timing Analysis with Improved Complexity and Divergent Loop Detection", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025. (accepted)

[C170] Haikang Diao, Haoyi Zhang, Jiahao Song, Haoyang Luo, **Yibo Lin**, Runsheng Wang, Yuan Wang and Xiyuan Tang*, "SEGA-DCIM: Design Space Exploration-Guided Automatic Digital CIM Compiler with Multiple Precision Support", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025. (accepted)

[C169] Che Chang, Boyang Zhang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yi-Hua Chung, Wan-Luan Lee, Zizheng Guo, **Yibo Lin** and Tsung-Wei Huang*, "PathGen: An Efficient Parallel Critical Path Generation Algorithm", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan, 2025. (**Best Paper Nomination**)

[C168] Boyang Zhang, Che Chang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yang Sui, Chih-Chun Chang, Yi-Hua Chung, Wan Luan Lee, Zizheng Guo, **Yibo Lin** and Tsung-Wei Huang*, "iTAP: An Incremental Task Graph Partitioner for Task-parallel Static Timing Analysis", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan, 2025.

[C167] Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "Analyzing Timing in Shorter Time: A Journey through Heterogeneous Parallelism for Static Timing Analysis", IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Zhuhai, China, Oct 22-25, 2024. (**Invited paper**)

[C166] Qipan Wang, Xueqing Li, Tianyu Jia, **Yibo Lin***, Runsheng Wang and Ru Huang, "AT-Place2.5D: Analytical Thermal-Aware Chiplet Placement Framework for Large-Scale 2.5D-IC", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[C165] Chunyuan Zhao, Zizheng Guo, Rui Wang, Zaiwen Wen, Yun Liang and **Yibo Lin***, "HeLEM-GR: Heterogeneous Global Routing with Linearized Exponential Multiplier Method", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[C164] Zizheng Guo, Zuodong Zhang, Wuxi Li, Tsung-Wei Huang, Xizhe Shi, Yufan Du, **Yibo Lin***, Runsheng Wang and Ru Huang, "HeteroExcept: A CPU-GPU Heterogeneous Algorithm to Accelerate Exception-aware Static Timing Analysis", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[C163] Xiaohan Gao, Haoyi Zhang, Bingyang Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, "Joint Placement Optimization for Hierarchical Analog/Mixed-Signal Circuits", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[C162] Yufan Du, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "Fusion of Global Placement and Gate Sizing with Differentiable Optimization", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (**Best Paper Nomination**)

[C161] Tianxiang Zhu, Qipan Wang, **Yibo Lin***, Runsheng Wang and Ru Huang, "FaStTherm: Fast and Stable Full-Chip Transient Thermal Predictor Considering Nonlinear Effects", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[C160] Jing Mai, Zuodong Zhang, **Yibo Lin***, Runsheng Wang and Ru Huang, "MORPH: More Robust ASIC Placement for Hybrid Region Constraint Management", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[J159] Tsung-Yi Ho, Sadaf Khan, Jinwei Liu, Yi Liu, Zhengyuan Shi, Ziyi Wang, Qiang Xu*,

Evangeline F.Y. Young, Bei Yu, Ziyang Zheng, Binwu Zhu, Keren Zhu, Yiqi Che, Yun Liang, **Yibo Lin**, Guojie Luo, Guangyu Sun, Runsheng Wang, Xinming Wei, Chenhao Xue, Haoyi Zhang, Zuodong Zhang, Yuxiang Zhao, Sunan Zou, Lei Chen, Yu Huang, Min Li, Dimitrios Tsaras, Mingxuan Yuan, Hui-Ling Zhen, Zhufei Chu, Wenji Fang, Xingquan Li and Zhiyao Xie, "Large Circuit Models: Opportunities and Challenges", Science China Information Sciences, Sep, 2024.

[J158] Yuxuan Zhao, Peiyu Liao, Siting Liu, Jiaxi Jiang, **Yibo Lin** and Bei Yu*, "Analytical Heterogeneous Die-to-Die 3D Placement With Macros", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Aug, 2024. (accepted)

[J157] Xun Jiang, Jiarui Wang, Jing Mai, Zhixiong Di and **Yibo Lin***, "A Robust FPGA Router With Optimization of High-Fanout Nets and Intra-CLB Connections", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Aug, 2024. (accepted)

[C156] Jiarui Wang, Xun Jiang and **Yibo Lin***, "Top-Level Routing for Multiply-Instantiated Blocks with Topology Hashing", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C155] Yufan Du, Zizheng Guo, Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, "PowPrediCT: Cross-Stage Power Prediction with Circuit-Transformation-Aware Learning", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C154] Haoyi Zhang, Jiahao Song, Xiaohan Gao, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, "EasyACIM: An End-to-End Automated Analog CIM with Synthesizable Architecture and Agile Design Space Exploration", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C153] Zichen Kong, Xiyuan Tang*, Wei Shi, Yiheng Du, **Yibo Lin** and Yuan Wang, "PVTSizing: A TuRBO-RL-Based Batch-Sampling Optimization Framework for PVT-Robust Analog Circuit Synthesis", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C152] Yuan Pu, Fangzhou Liu, Yu Zhang, Zhuolun He, Kai-Yuan Chao, **Yibo Lin** and Bei Yu*, "Lesyn: Placement-aware Logic Resynthesis for Non-Integer Multiple-Cell-Height Designs", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C151] Wan Luan Lee, Dian-Lun Lin, Tsung-Wei Huang*, Shui Jiang, Tsung-Yi Ho, **Yibo Lin** and Bei Yu, "G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C150] Chenhao Xue, Chen Zhang, Xun Jiang, Gao Zhutianya, **Yibo Lin** and Guangyu Sun*, "Oltron: Algorithm-Hardware Co-design for Outlier-Aware Quantization of LLMs with Inter-/Intra-Layer Adaptation", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C149] Haoran Lu, Yandong Ge, Xun Jiang, Jiacheng Sun, Wanyue Peng, Rui Guo, Ming Li, **Yibo Lin**, Runsheng Wang, Heng Wu* and Ru Huang, "First Experimental Demonstration of Self-Aligned Flip FET (FFET): A Breakthrough Stacked Transistor Technology with 2.5T Design, Dual-Side Active and Interconnects", IEEE Symposium on VLSI Technology and Circuits (VLSI), Honolulu, HI, Jun 16-20, 2024.

[J148] Peiyu Liao, Yuxuan Zhao, Dawei Guo, **Yibo Lin** and Bei Yu*, "Analytical Die-to-Die 3D Placement With Bistratal Wirelength Model and GPU Acceleration", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2024.

[C147] Xiaohan Gao, Haoyi Zhang, Zhu Pan, **Yibo Lin***, Runsheng Wang and Ru Huang, "Migrating Standard Cells for Multiple Drive Strengths by Routing Imitation", IEEE/ACM International Symposium of EDA (ISEDA), Xi'an, China, May 10-13, 2024.

[C146] Qipan Wang, Tianxiang Zhu, **Yibo Lin***, Runsheng Wang and Ru Huang, "ATSim3D: Towards Accurate Thermal Simulator for Heterogeneous 3D IC Systems Considering Nonlinear Leakage and Conductivity", IEEE/ACM International Symposium of EDA (ISEDA), Xi'an, China, May 10-13, 2024. (**Honorable Mention Paper Award**)

[C145] Jing Mai, Jiarui Wang, Yifan Chen, Zizheng Guo, Xun Jiang, Yun Liang and **Yibo Lin***, "OpenPARF 3.0: Robust Multi-Electrostatics Based FPGA Macro Placement Considering Cascaded Macros Groups and Fence Regions", IEEE/ACM International Symposium of EDA (ISEDA), Xi'an, China, May 10-13, 2024. (**Best Paper Award**)

[C144] Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, "CircuitNet 2.0: An Advanced Dataset for Promoting Machine Learning Innovations in Realistic Chip Design Environment", International Conference on Learning Representations (ICLR), Vienna, Austria, May 7-11, 2024.

[J143] Yufei Chen, Zizheng Guo, Runsheng Wang, Ru Huang, **Yibo Lin** and Cheng Zhuo, "Dynamic Supply Noise Aware Timing Analysis With JIT Machine Learning Integration", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May, 2024. (accepted)

[C142] Zizheng Guo, Tsung-Wei Huang, Zhou Jin, Cheng Zhuo, **Yibo Lin***, Runsheng Wang and Ru Huang, "Heterogeneous Static Timing Analysis with Advanced Delay Calculator", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.

[C141] Haoyi Zhang, Xiaohan Gao, Zilong Shen, Jiahao Song, Xiaoxu Cheng, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, "SAGERoute 2.0: Hierarchical Analog and Mixed Signal Routing Considering Versatile Routing Scenarios", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.

[C140] Yuan Pu, Tinghuan Chen, Zhuolun He, Chen Bai, Haisheng Zheng, **Yibo Lin** and Bei Yu*, "IncreMacro: Incremental Macro Placement Refinement", ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024. (**Best Paper Nomination**)

[C139] Yu Zhang, Yuan Pu, Fangzhou Liu, Peiyu Liao, Kaiyuan Chao, Keren Zhu, **Yibo Lin** and Bei Yu*, "Multi-Electrostatics Based Placement for Non-Integer Multiple-Height Cells", ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.

[C138] Siting Liu, Jiaxi Jiang, Zhuolun He, Ziyi Wang, **Yibo Lin** and Bei Yu*, "Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs", ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.

[J137] Zhixiong Di*, Runzhe Tao, Jing Mai, Lin Chen and **Yibo Lin**, "LEAPS: Topological-Layout-Adaptable Multi-Die FPGA Placement for Super Long Line Minimization", IEEE Transactions on Circuits and Systems I, Mar, 2024.

[J136] Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin***, "Multielectrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity, Clock Feasibility, and Timing Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Feb, 2024.

[C135] Cheng-Hsiang Chiu, Zhicheng Xiong, Zizheng Guo, Tsung-Wei Huang* and **Yibo Lin**, "An Efficient Task-parallel Pipeline Programming Framework", International Conference on High-Performance Computing in Asia-Pacific Region (HPC Asia), Nagoya, Japan, Jan, 2024.

[J134] Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "Accelerating Static Timing Analysis using CPU-GPU Heterogeneous Parallelism", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2023.

[J133] Zhuomin Chai, Yuxiang Zhao, Wei Liu*, **Yibo Lin***, Runsheng Wang and Ru Huang, "CircuitNet: An Open-Source Dataset for Machine Learning in VLSI CAD Applications with Improved Domain-Specific Evaluation Metric and Learning Strategies", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2023.

[J132] Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin***, "OpenPARF: 基于深度学习工具包的大规模异构 FPGA 开源布局布线框架", 电子与信息学报, 2023.

[J131] Zuodong Zhang, Zizheng Guo, **Yibo Lin***, Meng Li*, Runsheng Wang and Ru Huang, "AVATAR: An Aging- and Variation-Aware Dynamic Timing Analyzer for Error-Efficient Computing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Nov, 2023.

[J130] Guannan Guo, Tsung-Wei Huang*, **Yibo Lin**, Zizheng Guo, Sushma Yellapragada and Martin Wong, "A GPU-accelerated Framework for Path-based Timing Analysis", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Nov, 2023.

[C129] Yifan Chen, Zaiwen Wen, Yun Liang and **Yibo Lin***, "Stronger Mixed-Size Placement Backbone Considering Second-Order Information", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct 29-31, 2023.

[J128] Peiyu Liao, Dawei Guo, Zizheng Guo, Siting Liu, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, "DREAMPlace 4.0: Timing-driven Placement with Momentum-based Net Weighting and Lagrangian-based Refinement", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2023.

[J127] Xiaohan Gao, Haoyi Zhang, Siyuan Ye, Mingjie Liu, David Z. Pan, Linxiao Shen, Runsheng Wang, **Yibo Lin*** and Ru Huang, "Post-Layout Simulation Driven Analog Circuit Sizing", SCIENCE CHINA Information Sciences, Oct, 2023.

[C126] Jing Mai, Jiaru Wang, Zhixiong Di, Guojie Luo, Yun Liang and **Yibo Lin***, "OpenPARF: An Open-Source Placement and Routing Framework for Large-Scale Heterogeneous FPGAs with Deep Learning Toolkit", International Conference on ASIC (ASICON), Nanjing, China, Oct, 2023. (**Invited paper**)

[C125] Xun Jiang, Zizheng Guo, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, "Accelerating Routability and Timing Optimization with Open-Source AI4EDA Dataset CircuitNet and Heterogeneous Platforms", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct, 2023. (**Invited paper**)

[C124] Kexing Zhou, Yun Liang*, **Yibo Lin**, Runsheng Wang and Ru Huang, "Khronos: Fusing Memory Access for Improved Hardware RTL Simulation", IEEE/ACM International Symposium on Microarchitecture (MICRO), Toronto, Canada, Oct, 2023.

[J123] Binwu Zhu, Xinyun Zhang, **Yibo Lin**, Bei Yu and Martin Wong, "DRC-SG 2.0: Efficient Design Rule Checking Script Generation via Key Information Extraction", ACM Transactions on Design Automation of Electronic Systems (TODAES), Sep, 2023.

[C122] Zizheng Guo, Zuodong Zhang, Xun Jiang, Wuxi Li, **Yibo Lin***, Runsheng Wang and Ru Huang, "General-Purpose Gate-Level Simulation with Partition-Agnostic Parallelism", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C121] Qipan Wang, Ping Liu, Ligguo Jiang, Mingjie Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, "MTL-Designer: An Integrated Flow for Analysis and Synthesis of Microstrip Transmission Line", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C120] Peiyu Liao, Hongduo Liu, **Yibo Lin***, Bei Yu* and Martin Wong, "On a Moreau Envelope Wirelength Model for Analytical Global Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C119] Siting Liu, Ziyi Wang, Fangzhou Liu, **Yibo Lin**, Bei Yu and Martin Wong*, "Concurrent Sign-off Timing Optimization via Deep Steiner Points Refinement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C118] Su Zheng, Lancheng Zou, Siting Liu, **Yibo Lin**, Bei Yu and Martin Wong*, "Mitigating Distribution Shift for Congestion Optimization in Global Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C117] Yu Zhang, Yifan Chen, Zhonglin Xie, Hong Xu, Zaiwen Wen, **Yibo Lin*** and Bei Yu*, "LRSDP: Low-Rank SDP for Triple Patterning Lithography Layout Decomposition", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[J116] Siting Liu, Yuan Pu, Peiyu Liao, Hongzhong Wu, Rui Zhang, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, "FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2023.

[C115] Yuxiang Zhao, Zhuomin Chai, **Yibo Lin***, Runsheng Wang and Ru Huang, "HybridNet: Dual-Branch Fusion of Geometrical and Topological Views for VLSI Congestion Prediction", IEEE/ACM International Symposium of EDA (ISEDA), Nanjing, China, May 8-11, 2023.

[C114] Haoyi Zhang, Xiaohan Gao, **Yibo Lin***, Runsheng Wang and Ru Huang, "Multi-Scenario Analog and Mixed-Signal Circuit Routing with Agile Human Interaction", IEEE/ACM International Symposium of EDA (ISEDA), Nanjing, China, May 8-11, 2023.

[C113] Haoyi Zhang, Xiaohan Gao, Haoyang Luo, Jiahao Song, Xiyuan Tang, Junhua Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, "SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Apr 17-19, 2023. (**Best Paper Award**)

[C112] Zuodong Zhang, Meng Li*, **Yibo Lin**, Runsheng Wang and Ru Huang, "READ: Reliability-Enhanced Accelerator Dataflow Optimization using Critical Input Pattern Reduction", IEEE/ACM

Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Apr 17-19, 2023.

[J111] Xiaohan Gao, Haoyi Zhang, Mingjie Liu, Linxiao Shen, David Z. Pan, **Yibo Lin***, Runsheng Wang and Ru Huang, "Interactive Analog Layout Editing with Instant Placement and Routing Legalization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Mar, 2023.

[J110] **Yibo Lin**, Avi Ziv and Haoxing Ren, "Introduction to the Special Issue on Machine Learning for CAD/EDA", ACM Transactions on Design Automation of Electronic Systems (TODAES), Mar, 2023.

[J109] Xinfa Zhang, Zuodong Zhang, **Yibo Lin***, Zhigang Ji*, Runsheng Wang and Ru Huang, "Efficient Aging-Aware Standard Cell Library Characterization Based on Sensitivity Analysis", IEEE Transactions on Circuits and Systems II: Express Briefs, Feb, 2023.

[C108] Yifan Chen, Jing Mai, Xiaohan Gao, Muhan Zhang and **Yibo Lin***, "MacroRank: Ranking Macro Placement Solutions Leveraging Translation Equivariancy", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 16-19, 2023.

[C107] Jiarui Wang, Jing Mai, Zhixiong Di and **Yibo Lin***, "A Robust FPGA Router with Concurrent Intra-CLB Rerouting", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 16-19, 2023.

[J106] Junchi Yan*, Xianglong Lyu, Ruoyu Cheng and **Yibo Lin**, "Towards Machine Learning for Placement and Routing in Chip Design: a Methodological Overview", arXiv preprint, 2022.

[J105] Wei Li, Jialu Xia, Yuzhe Ma, Jialu Li, **Yibo Lin** and Bei Yu*, "Adaptive Layout Decomposition with Graph Embedding Neural Networks", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Nov, 2022.

[C104] Zizheng Guo, Feng Gu and **Yibo Lin***, "GPU-Accelerated Rectilinear Steiner Tree Generation", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 01-03, 2022.

[C103] Qipan Wang, Xiaohan Gao, **Yibo Lin***, Runsheng Wang and Ru Huang, "DeePEB: A Neural Partial Differential Equation Solver for Post Exposure Baking Simulation in Lithography", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 01-03, 2022. (**Best Paper Nomination**)

[C102] **Yibo Lin***, Xiaohan Gao, Haoyi Zhang, Runsheng Wang and Ru Huang, "Intelligent and Interactive Analog Layout Design Automation", IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Nanjing, China, Oct 25-28, 2022. (**Invited paper**)

[J101] Zizheng Guo, Mingwei Yang, Tsung-Wei Huang and **Yibo Lin***, "A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Large Designs", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2022.

[J100] Martin Rapp, Hussam Amrouch, **Yibo Lin**, Bei Yu, David Z. Pan, Marilyn Wolf and Jörg Henkel*, "MLCAD: A Survey of Research in Machine Learning for CAD", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2022. (**Invited Keynote paper**)

[C99] Binwu Zhu, Xinyun Zhang, **Yibo Lin**, Bei Yu* and Martin Wong, "Efficient Design Rule Checking Script Generation via Key Information Extraction", ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), Snowbird, Utah, Sep 12-13, 2022.

[J98] **Yibo Lin**, Tong Qu, Zongqing Lu, Yajuan Su* and Yayi Wei*, "Asynchronous Reinforcement Learning Framework and Knowledge Transfer for Net Order Exploration in Detailed Routing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sep, 2022.

[J97] Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Wei Liu, Runsheng Wang and Ru Huang, "CircuitNet: An Open-Source Dataset for Machine Learning Applications in Electronic Design Automation (EDA)", SCIENCE CHINA Information Sciences, Sep, 2022.

[C96] Jing Mai, Yibai Meng, Zhixiong Di and **Yibo Lin***, "Multi-Electrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity and Clock Feasibility", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

[C95] Zizheng Guo and **Yibo Lin***, "Differentiable-Timing-Driven Global Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

[C94] Zizheng Guo, Mingjie Liu, Jiaqi Gu, Shuhan Zhang, David Z. Pan and **Yibo Lin***, "A Timing Engine Inspired Graph Neural Network Model for Pre-Routing Slack Prediction", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

[C93] Zuodong Zhang, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "AVATAR: An Aging- and Variation-Aware Dynamic Timing Analyzer for Application-based DVAFS", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

[C92] Bowen Wang, Guibao Shen, Dong Li, Jianye Hao, Wulong Liu, Yu Huang, Hongzhong Wu, **Yibo Lin**, Guangyong Chen and Pheng Ann Heng, "LHNN: Lattice Hypergraph Neural Network for VLSI Congestion Prediction", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

[J91] Tsung-Wei Huang*, Dian-Lun Lin, Chun-Xun Lin and **Yibo Lin**, "Taskflow: A Lightweight Parallel and Heterogeneous Task Graph Computing System", IEEE Transactions on Parallel and Distributed Systems (TPDS), Jun, 2022.

[C90] Zuodong Zhang, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "EventTimer: Fast and Accurate Event-Based Dynamic Timing Analysis", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022.

[C89] Siting Liu, Peiyu Liao, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, "FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022. (**Best Paper Award**)

[C88] Peiyu Liao, Siting Liu, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, "DREAMPlace 4.0: Timing-driven Global Placement with Momentum-based Net Weighting", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022.

[C87] Haoyu Yang, Kit Fung, Yuxuan Zhao, **Yibo Lin** and Bei Yu*, "Mixed-Cell-Height Legalization on CPU-GPU Heterogeneous Systems", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022.

[C86] Xun Jiang, **Yibo Lin** and Zhongfeng Wang*, "FPGA-Accelerated Maze Routing Kernel for VLSI Designs", IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), Virtual Conference, Jan 17-20, 2022.

[C85] Kexing Zhou, Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "Efficient Critical Paths Search Algorithm using Mergeable Heap", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Virtual Conference, Jan 17-20, 2022.

[J84] Yibai Meng, Wuxi Li, **Yibo Lin*** and David Z. Pan, "elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jan, 2022.

[C83] Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Large Designs", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

[C82] Guannan Guo, Tsung-Wei Huang*, **Yibo Lin** and Martin Wong, "GPU-accelerated Path-based Timing Analysis", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

[C81] Zizheng Guo, Jing Mai and **Yibo Lin***, "Ultrafast CPU/GPU Kernels for Density Accumulation in Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

[C80] Xiaohan Gao, Mingjie Liu, David Z. Pan and **Yibo Lin***, "Interactive Analog Layout Editing with Instant Placement Legalization", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

[J79] **Yibo Lin***, "模拟电路版图自动化与智能设计", 中国计算机学会通讯, Dec, 2021.

[J78] Wei Li, Yuzhe Ma, Qi Sun, Zhang Lu, **Yibo Lin**, Iris Hui-Ru Jiang, Bei Yu* and David Z. Pan, "OpenMPL: An Open Source Layout Decomposer", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Nov, 2021.

[C77] Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "HeteroCPPR: Accelerating Common Path Pessimism Removal with Heterogeneous CPU-GPU Parallelism", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Virtual Conference, Nov 01-04, 2021.

[C76] Guannan Guo, Tsung-Wei Huang*, **Yibo Lin** and Martin Wong, "GPU-accelerated Critical Path Generation with Path Constraints", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Virtual Conference, Nov 01-04, 2021.

[C75] Tong Qu, **Yibo Lin**, Tianyang Gai, Xiaojing Su, Shuhan Wang, Bojie Ma, Yajuan Su* and Yayi Wei*, "Litho-Aware Redundant Local-Loop Insertion Framework With Convolutional Neural Network", Proceedings of SPIE, San Jose, CA, Sep 27, 2021.

[J74] Tsung-Wei Huang*, **Yibo Lin**, Chun-Xun Lin, Guannan Guo and Martin Wong, "Cpp-Taskflow: A General-purpose Parallel Task Programming System at Scale", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Aug, 2021.

[J73] **Yibo Lin***, Zixuan Jiang, Jiaqi Gu, Wuxi Li, Shounak Dhar, Haoxing Ren, Brucek Khailany and David Z. Pan, "DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Apr, 2021. (**Best Paper Award**)

[J72] Junzhe Cai, Changhao Yan*, Yudong Tao, **Yibo Lin**, Sheng-Guo Wang, David Z. Pan and Xuan Zeng, "A Novel and Unified Full-chip CMP Model Aware Dummy Fill Insertion Framework with SQP-Based Optimization Method", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Mar, 2021.

[J71] Mohamed Baker Alawieh, **Yibo Lin**, Zaiwei Zhang, Meng Li, Qixing Huang and David Z. Pan*, "GAN-SRAF: Sub-Resolution Assist Feature Generation using Generative Adversarial Networks", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Feb, 2021.

[J70] **Yibo Lin***, Xiaohan Gao, Tinghuan Chen and Bei Yu*, "机器学习辅助数字集成电路后端设计方法", 微纳电子与智能制造, Feb, 2021.

[J69] Cheng Zhuo*, Zizheng Guo, Xiao Dong, Qing He and **Yibo Lin**, "先进工艺下的数字签核", 微纳电子与智能制造, Feb, 2021.

[C68] Tong Qu, **Yibo Lin**, Zongqing Lu, Yajuan Su* and Yayi Wei*, "Asynchronous Reinforcement Learning Framework for Net Order Exploration in Detailed Routing", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Virtual Conference, Feb 01-05, 2021.

[C67] Siting Liu, Qi Sun, Peiyu Liao, **Yibo Lin** and Bei Yu*, "Global Placement with Deep Learning-Enabled Explicit Routability Optimization", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Virtual Conference, Feb 01-05, 2021.

[C66] Hongjia Li, Mengshu Sun, Tianyun Zhang, Olivia Chen, Nobuyuki Yoshikawa, Bei Yu, Yanzhi Wang* and **Yibo Lin**, "Towards AQFP-Capable Physical Design Automation", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Virtual Conference, Feb 01-05, 2021.

[C65] Xiaohan Gao, Chenhui Deng, Mingjie Liu, Zhiru Zhang, David Z. Pan and **Yibo Lin***, "Layout Symmetry Annotation for Analog Circuits with Graph Neural Networks", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 18-21, 2021.

[C64] **Yibo Lin***, "Deep Learning for Mask Synthesis and Verification: A Survey", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 18-21, 2021. (**Invited paper**)

[J63] **Yibo Lin***, Wuxi Li, Jiaqi Gu, Haoxing Ren, Brucek Khailany and David Z. Pan, "ABCD-Place: Accelerated Batch-based Concurrent Detailed Placement on Multi-threaded CPUs and GPUs", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2020.

[C62] Jiaqi Gu, Zixuan Jiang, **Yibo Lin** and David Z. Pan*, "DREAMPlace 3.0: Multi-Electrostatics Based Robust VLSI Placement with Region Constraints", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov 2-5, 2020.

[C61] Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "GPU-Accelerated Static Timing Analysis", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov 2-5, 2020.

[C60] **Yibo Lin***, "GPU Acceleration in VLSI Back-end Design: Overview and Case Studies", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov 2-5, 2020. (**Invited tutorial**)

[C59] Wei Ye, Mohamed Baker Alawieh, Yuki Watanabe, Shigeki Nojima, **Yibo Lin** and David Z. Pan*, "TEMPO: Fast Mask Topography Effect Modeling with Deep Learning", ACM International Symposium on Physical Design (ISPD), Taipei, Taiwan, Sep 20-23, 2020. (**Best Paper Award**)

[J58] Jing Chen, Mohamed Baker Alawieh, **Yibo Lin**, Maolin Zhang, Jun Zhang, Yufeng Guo* and David Z. Pan, "Automatic Selection of Structure Parameters of Silicon on Insulator Lateral Power Device Using Bayesian Optimization", IEEE Electron Device Letters (EDL), Sep, 2020.

[C57] Wei Li, Jialu Xia, Yuzhe Ma, Jialu Li, **Yibo Lin** and Bei Yu*, "Adaptive Layout Decomposition with Graph Embedding Neural Networks", ACM/IEEE Design Automation Conference (DAC), San Francisco, Jul 19-23, 2020.

[J56] Ying Chen, **Yibo Lin**, Rui Chen, Lisong Dong, Ruixuan Wu, Tianyang Gai, Le Ma, Yajuan Su* and Yayi Wei*, "EUV Multilayer Defect Characterization via Cycle-Consistent Learning", Optics Express, Jun, 2020.

[C55] **Yibo Lin***, David Z. Pan, Haoxing Ren and Brucek Khailany, "DREAMPlace 2.0: Open-Source GPU-Accelerated Global and Detailed Placement for Large-Scale VLSI Designs", China Semiconductor Technology International Conference (CSTIC), Shanghai, China, Jun, 2020. (**Invited paper**)

[J54] Jing Chen, Mohamed Baker Alawieh, **Yibo Lin**, Maolin Zhang, Jun Zhang, Yufeng Guo* and David Z. Pan, "Powernet: SOI Lateral Power Device Breakdown Prediction With Deep Neural Networks", IEEE Access, Feb, 2020.

[J53] Ying Chen, **Yibo Lin**, Lisong Dong, Tianyang Gai, Rui Chen, Yajuan Su*, Yayi Wei* and David Z. Pan, "SoulNet: Ultrafast Optical Source Optimization Utilizing Generative Neural Networks for Advanced Lithography", Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), Nov, 2019.

========== 以下为博士及博士后期间发表内容 ==========

书籍章节

[B1] **Yibo Lin** and David Z. Pan, "Machine Learning in Physical Verification, Mask Synthesis, and Physical Design", Machine Learning in VLSI Computer-Aided Design, Springer, 2018, edited by Abe Elfedel, Duane Boning and Xin Li. (**Invited Book Chapter**)

会议及期刊论文 (标 * 表示通讯作者)

论文成果包括: DAC (7 篇), ICCAD (7 篇), IEEE TCAD (10 篇), DATE (1 篇), ...

[J52] Hao Chen, Mingjie Liu, Biying Xu, Keren Zhu, Xiyuan Tang, Shaolan Li, **Yibo Lin**, Nan Sun and David Z. Pan*, "MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII", IEEE Design & Test, Apr, 2021.

[C51] Rachel Selina Rajarathnam, **Yibo Lin**, Yier Jin and David Z. Pan*, "ReGDS: A Reverse Engineering Framework from GDSII to Gate-level Netlist", IEEE International Workshop on Hardware-Oriented Security and Trust (HOST), San Jose, CA, May 4, 2020.

[C50] Mingjie Liu, Wuxi Li, Keren Zhu, Biying Xu, **Yibo Lin**, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan*, "S3DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jan 13-16, 2020. (**Best Paper Nomination**)

[C49] Mohamed Baker Alawieh, Wuxi Li, **Yibo Lin**, Love Singhal, Mahesh Iyer and David Z. Pan*, "High-Definition Routing Congestion Prediction for Large-Scale FPGAs", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jan 13-16, 2020.

[C48] Wuxi Li, **Yibo Lin** and David Z. Pan*, "elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Westminster, CO, Nov 4-7, 2019.

[C47] Keren Zhu, Mingjie Liu, **Yibo Lin**, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan*, "GeniusRoute: A New Analog Routing Paradigm Using Generative Neural Network Guidance", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Westminster, CO, Nov 4-7, 2019.

[C46] Chengyue Gong, Zixuan Jiang, Dilin Wang, **Yibo Lin**, Qiang Liu and David Z. Pan*, "Mixed Precision Neural Architecture Search for Energy Efficient Deep Learning", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Westminster, CO, Nov 4-7, 2019.

[C45] Biying Xu, Keren Zhu, Mingjie Liu, **Yibo Lin**, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan*, "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Westminster, CO, Nov 4-7, 2019. (**Invited paper**)

[J44] **Yibo Lin**, Meng Li, Yuki Watanabe, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima and David Z. Pan*, "Data Efficient Lithography Modeling with Transfer Learning and Active Data Selection", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2019.

[C43] Wei Li, Yuzhe Ma, Qi Sun, **Yibo Lin**, Iris Hui-Ru Jiang, Bei Yu and David Z Pan, "OpenMPL: An Open Source Layout Decomposer", International Conference on ASIC (ASICON), Chongqing, China, Oct, 2019. (**Invited paper**)

[C42] **Yibo Lin**, Shounak Dhar, Wuxi Li, Haoxing Ren, Brucek Khailany and David Z. Pan*, "DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement", ACM/IEEE Design Automation Conference (DAC), Las Vegas, NV, Jun 2-6, 2019. (**Best Paper Award**)

[C41] Wei Ye, Mohamed Baker Alawieh, **Yibo Lin** and David Z. Pan*, "LithoGAN: End-to-End Lithography Modeling with Generative Adversarial Networks", ACM/IEEE Design Automation Conference (DAC), Las Vegas, NV, Jun 2-6, 2019. (**Best Paper Nomination**)

[C40] Biying Xu, **Yibo Lin**, Xiyuan Tang, Shaolan Li, Linxiao Shen, Nan Sun and David Z. Pan*, "WellGAN: Generative-Adversarial-Network-Guided Well Generation for Analog/Mixed-Signal Circuit Layout", ACM/IEEE Design Automation Conference (DAC), Las Vegas, NV, Jun 2-6, 2019.

[C39] Mohamed Baker Alawieh, **Yibo Lin**, Zaiwei Zhang, Meng Li, Qixing Huang and David Z. Pan*, "GAN-SRAF: Sub-Resolution Assist Feature Generation Using Conditional Generative Adversarial Networks", ACM/IEEE Design Automation Conference (DAC), Las Vegas, NV, Jun 2-6, 2019.

[C38] **Yibo Lin**, Zhao Song and Lin F. Yang*, "Towards a Theoretical Understanding of Hashing-Based Neural Nets", International Conference on Artificial Intelligence and Statistics (AIS-

TATS), Okinawa, Japan, Apr 16-18, 2019.

[C37] Biying Xu, Shaolan Li, Chak-Wa Pui, Derong Liu, Linxiao Shen, **Yibo Lin**, Nan Sun and David Z. Pan*, "Device Layer-Aware Analytical Placement for Analog Circuits", ACM International Symposium on Physical Design (ISPD), San Francisco, CA, Apr 14-17, 2019. (**Best Paper Nomination**)

[J36] Ying Chen, **Yibo Lin**, Tianyang Gai, Yajuan Su*, Yayi Wei* and David Z. Pan, "Semi-Supervised Hotspot Detection with Self-Paced Multi-Task Learning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Apr, 2019.

[C35] Wei Ye, Mohamed Baker Alawieh, Meng Li, **Yibo Lin** and David Z. Pan*, "Litho-GPA: Gaussian Process Assurance for Lithography Hotspot Detection", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Florence, Italy, Mar 25-29, 2019.

[J34] Jing Chen, **Yibo Lin**, Yufeng Guo, Maolin Zhang, Mohamed Baker Alawieh and David Z. Pan*, "Lithography Hotspot Detection Using a Double Inception Module Architecture", Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), Mar, 2019.

[C33] Ying Chen, **Yibo Lin**, Tianyang Gai, Yajuan Su*, Yayi Wei* and David Z. Pan, "Semi-Supervised Hotspot Detection with Self-Paced Multi-Task Learning", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 21-24, 2019.

[C32] Wei Ye, Mohamed Baker Alawieh, **Yibo Lin** and David Z. Pan*, "Tackling Signal Electromigration with Learning-Based Detection and Multistage Mitigation", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 21-24, 2019.

[C31] Wei Ye, **Yibo Lin**, Meng Li, Qiang Liu and David Z. Pan*, "LithoROC: Lithography Hotspot Detection with Explicit ROC Optimization", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 21-24, 2019. (**Invited paper**)

[C30] **Yibo Lin**, Mohamed Baker Alawieh, Wei Ye and David Z. Pan*, "Machine Learning for Yield Learning and Optimization", IEEE International Test Conference (ITC), Phoenix, Arizona, Oct, 2018. (**Invited paper**)

[J29] **Yibo Lin**, Bei Yu, Meng Li and David Z. Pan*, "Layout Synthesis for Topological Quantum Circuits with 1D and 2D Architectures", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Aug, 2018.

[J28] Meng Li, Bei Yu, **Yibo Lin**, Xiaoqing Xu, Wuxi Li and David Z Pan, "A practical split manufacturing framework for trojan prevention via simultaneous wire lifting and cell insertion", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2018.

[C27] Jiong Zhang, **Yibo Lin**, Zhao Song and Inderjit S Dhillon*, "Learning Long Term Dependencies via Fourier Recurrent Units", International Conference on Machine Learning (ICML), Stockholm, Sweden, Jun 10-15, 2018.

[J26] Xiaoqing Xu, **Yibo Lin**, Meng Li, Tetsuaki Matsunawa, Shigeki Nojima, Chikaaki Kodama, Toshiya Kotani and David Z. Pan*, "Subresolution Assist Feature Generation With Supervised Data Learning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2018.

[J25] **Yibo Lin**, Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu,

Zhuo Li, Charles J Alpert and David Z. Pan*, "MrDP: Multiple-row detailed placement of heterogeneous-sized cells for advanced nodes", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2018.

[J24] Wuxi Li, **Yibo Lin**, Meng Li, Shounak Dhar and David Z. Pan*, "UTPlaceF 2.0: A High-Performance Clock-Aware FPGA Placement Engine", ACM Transactions on Design Automation of Electronic Systems (TODAES), Jun, 2018.

[C23] **Yibo Lin**, Yuki Watanabe, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima, Meng Li and David Z. Pan*, "Data Efficient Lithography Modeling with Residual Neural Networks and Transfer Learning", ACM International Symposium on Physical Design (ISPD), Monterey, CA, Mar 25-28, 2018.

[C22] Meng Li, Bei Yu, **Yibo Lin**, Xiaoqing Xu, Wuxi Li and David Z. Pan*, "A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jeju, Korea, Jan 22-25, 2018.

[C21] Che-Lun Hsu, Shaofeng Guo, **Yibo Lin**, Xiaoqing Xu, Meng Li, Runsheng Wang, Ru Huang and David Z Pan, "Layout-dependent aging mitigation for critical path timing", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jeju, Korea, Jan 22-25, 2018.

[C20] **Yibo Lin**, Peter Debacker, Darko Trivkovic, Ryoung-han Kim, Praveen Raghavan and David Z. Pan*, "Patterning Aware Design Optimization of Selective Etching in N5 and Beyond", IEEE International Conference on Computer Design (ICCD), Boston, MA, Nov 5-8, 2017.

[C19] **Yibo Lin**, Xiaoqing Xu, Jiaojiao Ou and David Z Pan, "Machine learning for mask/wafer hotspot detection and mask synthesis", Photomask Technology, Oct 16, 2017. (**Invited paper**)

[J18] **Yibo Lin**, Bei Yu and David Z. Pan*, "High performance dummy fill insertion with coupling and uniformity constraints", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sep, 2017.

[C17] Wei Ye, **Yibo Lin**, Xiaoqing Xu, Wuxi Li, Yiwei Fu, Yongsheng Sun, Canhui Zhan and David Z. Pan*, "Placement Mitigation Techniques for Power Grid Electromigration", IEEE International Symposium on Low Power Electronics and Design (ISLPED), Taipei, Jul 24-26, 2017.

[J16] **Yibo Lin**, Bei Yu, Biying Xu and David Z. Pan*, "Triple patterning aware detailed placement toward zero cross-row middle-of-line conflict", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2017.

[J15] Xiaoqing Xu, **Yibo Lin**, Meng Li, Jiaojiao Ou, Brian Cline and David Z. Pan*, "Redundant local-Loop insertion for unidirectional routing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2017.

[C14] Xiaoqing Xu, **Yibo Lin**, Vinicius Livramento and David Z. Pan*, "Concurrent Pin Access Optimization for Unidirectional Routing", ACM/IEEE Design Automation Conference (DAC), Austin, TX, Jun 18-22, 2017.

[J13] **Yibo Lin**, Bei Yu, Yi Zou, Zhuo Li, Charles J Alpert and David Z. Pan*, "Stitch aware detailed placement for multiple e-beam lithography", Integration, the VLSI Journal, Jun,

2017. (**Best Paper Award**)

[J12] **Yibo Lin**, Xiaoqing Xu, Bei Yu, Ross Baldick and David Z. Pan*, "Triple/quadruple patterning layout decomposition via linear programming and iterative rounding", Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), Jun, 2017.

[C11] Jiaojiao Ou, Bei Yu, Xiaoqing Xu, Joydeep Mitra, **Yibo Lin** and David Z. Pan*, "DSAR: DSA aware routing with simultaneous DSA guiding pattern and double patterning assignment", ACM International Symposium on Physical Design (ISPD), Portland, OR, Mar 19-22, 2017.

[C10] **Yibo Lin**, Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J Alpert and David Z. Pan*, "MrDP: Multiple-row detailed placement of heterogeneous-sized cells for advanced nodes", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov 7-10, 2016.

[C9] Yudong Tao, Changhao Yan*, **Yibo Lin**, Sheng-Guo Wang, David Z. Pan and Xuan Zeng, "A novel unified dummy fill insertion framework with SQP-based optimization method", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov 7-10, 2016.

[C8] **Yibo Lin**, Bei Yu and David Z. Pan*, "Detailed placement in advanced technology nodes: a survey", IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Hangzhou, China, Oct 25-28, 2016. (**Invited paper**)

[J7] Bei Yu, Xiaoqing Xu, Subhendu Roy, **Yibo Lin**, Jiaojiao Ou and David Z. Pan*, "Design for manufacturability and reliability in extreme-scaling VLSI", Science China Information Sciences, May, 2016. (**Invited paper**)

[C6] **Yibo Lin**, Xiaoqing Xu, Bei Yu, Ross Baldick and David Z. Pan*, "Triple/quadruple patterning layout decomposition via novel linear programming and iterative rounding", Proceedings of SPIE, San Jose, CA, Feb 21-25, 2016. (**Best Student Paper Award**)

[C5] **Yibo Lin**, Bei Yu, Yi Zou, Zhuo Li, Charles J Alpert and David Z. Pan*, "Stitch aware detailed placement for multiple e-beam lithography", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Macau, China, Jan 25-28, 2016.

[C4] **Yibo Lin**, Bei Yu, Biying Xu and David Z. Pan*, "Triple patterning aware detailed placement toward zero cross-row middle-of-line conflict", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov 2-6, 2015.

[C3] **Yibo Lin**, Bei Yu and David Z. Pan*, "High performance dummy fill insertion with coupling and uniformity constraints", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 7-11, 2015.

[C2] David Z. Pan*, Lars Liebmann, Bei Yu, Xiaoqing Xu and **Yibo Lin**, "Pushing multiple patterning in sub-10nm: are we ready?", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 7-11, 2015. (**Invited Paper**)

[J1] Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, **Yibo Lin**, Zhuo Li, Charles Alpert and David Z. Pan*, "Methodology for standard cell compliance and detailed placement for triple patterning lithography", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May, 2015.