YIBO LIN

Assistant Professor ⋄ Department of Design Automation and Computing System
School of Integrated Circuits, 5 Yiheyuan Road, Beijing, China, 100871 ⋄ Peking University
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RESEARCH INTERESTS

Modeling and optimization in VLSI CAD, machine learning applications, and heterogeneous computing

EDUCATION

University of Texas at Austin, Texas, USA Aug. 2013 – May 2018
Ph.D., Department of Electrical and Computer Engineering
Advisor: David Z. Pan
Thesis: Bridging Design and Manufacturing Gap through Machine Learning and Machine-Generated Layout

Shanghai Jiao Tong University, Shanghai, China Sep. 2009 – Jun. 2013
B.S., Department of Microelectronics

EXPERIENCE

Peking University, Beijing, China Jul. 2019 – present
Assistant Professor
Department of Design Automation and Computing System,
School of Integrated Circuits (since Nov. 2021)
Center for Energy-efficient Computing and Applications (CECA),
School of Electronics Engineering and Computer Science

University of Texas at Austin, Texas, U.S. Jun. 2018 – Jun. 2019
Postdoc
Department of Electrical and Computer Engineering

TEACHING EXPERIENCE

Fundamental Algorithms for Engineering in Integrated Circuits		
Instructor	Graduate	2023–2024
Design Automation and Computing System		
Instructor	Graduate	2022–2024
Optimization and Machine Learning in VLSI Design Automation		
Instructor	Undergraduate	2021–2024
Introduction to Computing B		
Instructor	Undergraduate	2020–2022

AWARDS AND HONORS

Best Paper Award Nomination	ASPDAC	2025
Best Paper Award Nomination	ICCAD	2024
Best Paper Award & Honorable Mention	ISEDA	2024
Early Career Award (only one per year)	CCF Technical Committee in IC	2023
Inaugural Best Reviewer Award	ICCAD	2023
Best Paper Award (4/205)	DATE	2023
Best Paper Award (4/249)	DATE	2022
Best Paper Award Nomination	ICCAD	2022
Donald O. Pederson Best Paper Award (2/3495 in 4 years)	TCAD	2021
Best Paper Award	ISPD	2020
Best Paper Award Nomination	ASPDAC	2020
Best Paper Award (1/201) & Nomination (5/201)	DAC	2019
Best Paper Award Nomination	ISPD	2019
Inaugural Best Paper Award	Integration, the VLSI Journal	2018
Franco Cerrina Memorial Best Student Paper Award	SPIE	2016
A. Richard Newton Young Student Fellow	DAC	2014

PROFESSIONAL SERVICE

Executive Committee Member

- General co-chair, ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD) 2025
- Program co-chair, ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD) 2024
- Panel chair, IEEE International Symposium of Electronics Design Automation (ISEDA) 2023–2024
- Financial chair, ACM/IEEE Workshop on Machine Learning for CAD (MLCAD) 2021–2023

Journal Editor

- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024 – present
- Associate Editor, ACM Transaction on Design Automation of Electronic Systems (TODAES), 2024 – present
- Associate Editor, Elsevier Integration, the VLSI Journal (Integration), 2024 – present
- Guest Editor, ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2024
- Guest Editor, ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2022

Contest Chair

- Contest Problem Chair, Interated Circuits EDA Elite Challenge 2021 – 2023

Technical Program Committee Member

- ACM/IEEE Design Automation Conference (DAC): 2020
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD): 2018 – 2021, 2023

- Design, Automation and Test in Europe Conference (DATE): 2025
- IEEE International Conference on Computer Design (ICCD): 2019
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC): 2021 – 2022
- ACM International Symposium on Physical Design (ISPD): 2020, 2025
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD): 2021
- ACM Great Lakes Symposium on VLSI (GLVLSI): 2024
- Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI): 2021
- IEEE Electron Devices Technology and Manufacturing Conference (EDTM): 2021
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS): 2022.

Journal Reviewer

- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Computers (TC)
- ACM Transaction on Design Automation of Electronic Systems (TODAES)
- SPIE Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)
- Elsevier, Integration, the VLSI Journal (Integration)

Volunteer

- ACM SIGDA Website Administrator, 2021 – present

10 SELECTED PUBLICATIONS

Inverse chronological order. * denotes corresponding authors.

1. Yifan Chen, Zaiwen Wen, Yun Liang and **Yibo Lin***, "Stronger Mixed-Size Placement Backbone Considering Second-Order Information", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct 29-31, 2023.
2. Haoyi Zhang, Xiaohan Gao, Haoyang Luo, Jiahao Song, Xiyuan Tang, Junhua Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, "SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Apr 17-19, 2023. (**Best Paper Award**)
3. Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin***, "Multi-Electrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity, Clock Feasibility, and Timing Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sep, 2023.
4. Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "Accelerating Static Timing Analysis using CPU-GPU Heterogeneous Parallelism", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2023.
5. Qipan Wang, Xiaohan Gao, **Yibo Lin***, Runsheng Wang and Ru Huang, "DeePEB: A Neural Partial Differential Equation Solver for Post Exposure Baking Simulation in Lithography", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 01-03, 2022. (**Best Paper Nomination**)

6. Zizheng Guo and **Yibo Lin***, "Differentiable-Timing-Driven Global Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

7. Siting Liu, Peiyu Liao, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, "FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022. (**Best Paper Award**)

8. Zizheng Guo, Jing Mai and **Yibo Lin***, "Ultrafast CPU/GPU Kernels for Density Accumulation in Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

9. Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Large Designs", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

10. **Yibo Lin***, Zixuan Jiang, Jiaqi Gu, Wuxi Li, Shounak Dhar, Haoxing Ren, Brucek Khailany and David Z. Pan, "DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Apr, 2021. (**Best Paper Award**)

PUBLICATIONS

Book Chapters

[B3] **Yibo Lin**, Zizheng Guo and Jing Mai, "Deep Learning Framework for Placement", Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)

[B2] Haoyu Yang, **Yibo Lin** and Bei Yu, "Machine Learning for Mask Synthesis and Verification", Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)

Conference and Journal Papers (* denotes corresponding authors)

Summary: DAC (29), ICCAD (16), IEEE TCAD (27), DATE (15), etc.

[J189] Siting Liu, Ziyi Wang, Fangzhou Liu, **Yibo Lin**, Bei Yu* and Martin Wong, "Sign-off Timing Considerations via Concurrent Routing Topology Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J188] Yuxiang Zhao, Zhuomin Chai, Xun Jiang, **Yibo Lin***, Runsheng Wang and Ru Huang, "PDNNet: PDN-Aware GNN-CNN Heterogeneous Network for Dynamic IR Drop Prediction", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J187] Zhenkun Lin, Genggeng Liu*, Xing Huang, **Yibo Lin**, Jixin Zhang, Wenhao Liu and Ting-Chi Wang, "A Unified Deep Reinforcement Learning Approach for Constructing Rectilinear and Octilinear Steiner Minimum Tree", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J186] Bingyang Liu, Haoyi Zhang, Xiaohan Gao, Zichen Kong, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, "LayoutCopilot: An LLM-powered Multi-agent Collaborative Framework for Interactive Analog Layout Design", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J185] Rui Guo, Haoran Lu, Jiacheng Sun, Xun Jiang, Lining Zhangm, Ming Li, **Yibo Lin**, Runsheng Wang, Heng Wu* and Ru Huang, "Design Optimization of Flip FET Standard Cells With Dual-Sided Pins for Ultimate Scaling", IEEE Transactions on Electron Devices (TED), 2025. (accepted)

[C184] Lijie Zeng, Jiatai Sun, Xiao Wu, Dan Niu, Tianshi Wang, **Yibo Lin**, Zuochang Ye and Zhou Jin*, "G-SpNN: GPU-Accelerated Passivity Enforcement for S-Parameter Modeling with Neural Networks", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025. (accepted)

[C183] Ziyang Yu, Peng Xu, Zixiao Wang, Binwu Zhu, Qipan Wang, **Yibo Lin**, Runsheng Wang, Bei Yu* and Martin Wong, "SDM-PEB: Spatial-Depthwise Mamba for Enhanced Post-Exposure Bake Simulation", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025. (accepted)

[C182] Zizheng Guo, Yanqing Zhang, Runsheng Wang, **Yibo Lin** and Haoxing Ren, "GEM: GPU-Accelerated Emulator-Inspired RTL Simulation", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025. (accepted)

[C181] Xun Jiang, Haoran Lu, Yuxuan Zhao, Jiarui Wang, Zizheng Guo, Heng Wu, Bei Yu, Sung Kyu Lim, Runsheng Wang, Ru Huang and **Yibo Lin***, "A Systematic Approach for Multi-Objective Double-Side Clock Tree Synthesis", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025. (accepted)

[C180] Jiarui Wang, Yanjing Liu and **Yibo Lin***, "Synergistic Die-Level Router for Multi-FPGA System with Time-Division Multiplexing Optimization", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025. (accepted)

[C179] Yifan Chen, Jing Mai, Zuodong Zhang and **Yibo Lin***, "RUPlace: Optimizing Routability via Unified Placement and Routing Formulation", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025. (accepted)

[C178] Haoyi Zhang, Shizhao Sun, **Yibo Lin**, Runsheng Wang and Jiang Bian, "AnalogXpert: Automating Analog Topology Synthesis by Incorporating Circuit Design Expertise into Large Language Models", IEEE/ACM International Symposium of EDA (ISEDA), Hong Kong, May 9-12, 2025. (accepted)

[C177] Yufan Du, Zizheng Guo, Yang Hsu, Zhili Xiong, Seunggeun Kim, David Z. Pan, Runsheng Wang and **Yibo Lin***, "Addressing Continuity and Expressivity Limitations in Differentiable Physical Optimization: A Case Study in Gate Sizing", IEEE/ACM International Symposium of EDA (ISEDA), Hong Kong, May 9-12, 2025. (accepted)

[C176] Kairong Guo and **Yibo Lin***, "Multi-Row Standard Cell Layout Synthesis with Enhanced Scalability", IEEE/ACM International Symposium of EDA (ISEDA), Hong Kong, May 9-12, 2025. (accepted)

[C175] Qipan Wang, **Yibo Lin***, Runsheng Wang and Ru Huang, "ATSim3.5D: A Multiscale Thermal Simulator for 3.5D-IC Systems based on Nonlinear Multigrid Method", IEEE/ACM International Symposium of EDA (ISEDA), Hong Kong, May 9-12, 2025. (accepted)

[C174] Haoran Lu, Xun Jiang, Yanbang Chu, Ziqiao Xu, Rui Guo, Wanyue Peng, **Yibo Lin**, Runsheng Wang, Heng Wu* and Ru Huang, "A Tale of Two Sides of Wafer: Physical Implementation and Block-Level PPA on Flip FET with Dual-sided Signals", IEEE/ACM Proceedings

Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025. (accepted)

[C173] Tianxiang Zhu, Qipan Wang, **Yibo Lin***, Runsheng Wang and Ru Huang, "MORE-Stress: Model Order Reduction based Efficient Numerical Algorithm for Thermal Stress Simulation of TSV Arrays in 2.5D/3D IC", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025. (accepted)

[C172] Xizhe Shi, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "Handling Latch Loops in Timing Analysis with Improved Complexity and Divergent Loop Detection", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025. (accepted)

[C171] Haikang Diao, Haoyi Zhang, Jiahao Song, Haoyang Luo, **Yibo Lin**, Runsheng Wang, Yuan Wang and Xiyuan Tang*, "SEGA-DCIM: Design Space Exploration-Guided Automatic Digital CIM Compiler with Multiple Precision Support", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025. (accepted)

[C170] Jing Mai, Chunyuan Zhao, Zuodong Zhang, Zhixiong Di, **Yibo Lin***, Runsheng Wang and Ru Huang, "LEGALM: Efficient Legalization for Mixed-Cell-Height Circuits with Linearized Augmented Lagrangian Method", ACM International Symposium on Physical Design (ISPD), Austin, TX, Mar 16-19, 2025. (accepted)

[J169] Xun Jiang, Jiarui Wang, Jing Mai, Zhixiong Di and **Yibo Lin***, "A Robust FPGA Router With Optimization of High-Fanout Nets and Intra-CLB Connections", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Mar, 2025.

[J168] Yuxuan Zhao, Peiyu Liao, Siting Liu, Jiaxi Jiang, **Yibo Lin** and Bei Yu*, "Analytical Heterogeneous Die-to-Die 3D Placement With Macros", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Feb, 2025.

[C167] Che Chang, Boyang Zhang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yi-Hua Chung, Wan-Luan Lee, Zizheng Guo, **Yibo Lin** and Tsung-Wei Huang*, "PathGen: An Efficient Parallel Critical Path Generation Algorithm", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan, 2025. (**Best Paper Nomination**)

[C166] Boyang Zhang, Che Chang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yang Sui, Chih-Chun Chang, Yi-Hua Chung, Wan Luan Lee, Zizheng Guo, **Yibo Lin** and Tsung-Wei Huang*, "iTAP: An Incremental Task Graph Partitioner for Task-parallel Static Timing Analysis", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan, 2025.

[C165] Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "Analyzing Timing in Shorter Time: A Journey through Heterogeneous Parallelism for Static Timing Analysis", IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Zhuhai, China, Oct 22-25, 2024. (**Invited paper**)

[C164] Qipan Wang, Xueqing Li, Tianyu Jia, **Yibo Lin***, Runsheng Wang and Ru Huang, "AT-Place2.5D: Analytical Thermal-Aware Chiplet Placement Framework for Large-Scale 2.5D-IC", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[C163] Chunyuan Zhao, Zizheng Guo, Rui Wang, Zaiwen Wen, Yun Liang and **Yibo Lin***, "HeLEM-GR: Heterogeneous Global Routing with Linearized Exponential Multiplier Method", IEEE/ACM

International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[C162] Zizheng Guo, Zuodong Zhang, Wuxi Li, Tsung-Wei Huang, Xizhe Shi, Yufan Du, **Yibo Lin***, Runsheng Wang and Ru Huang, "HeteroExcept: A CPU-GPU Heterogeneous Algorithm to Accelerate Exception-aware Static Timing Analysis", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[C161] Xiaohan Gao, Haoyi Zhang, Bingyang Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, "Joint Placement Optimization for Hierarchical Analog/Mixed-Signal Circuits", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[C160] Yufan Du, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "Fusion of Global Placement and Gate Sizing with Differentiable Optimization", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (**Best Paper Nomination**)

[C159] Tianxiang Zhu, Qipan Wang, **Yibo Lin***, Runsheng Wang and Ru Huang, "FaStTherm: Fast and Stable Full-Chip Transient Thermal Predictor Considering Nonlinear Effects", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[C158] Jing Mai, Zuodong Zhang, **Yibo Lin***, Runsheng Wang and Ru Huang, "MORPH: More Robust ASIC Placement for Hybrid Region Constraint Management", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.

[J157] Tsung-Yi Ho, Sadaf Khan, Jinwei Liu, Yi Liu, Zhengyuan Shi, Ziyi Wang, Qiang Xu*, Evangeline F.Y. Young, Bei Yu, Ziyang Zheng, Binwu Zhu, Keren Zhu, Yiqi Che, Yun Liang, **Yibo Lin**, Guojie Luo, Guangyu Sun, Runsheng Wang, Xinming Wei, Chenhao Xue, Haoyi Zhang, Zuodong Zhang, Yuxiang Zhao, Sunan Zou, Lei Chen, Yu Huang, Min Li, Dimitrios Tsaras, Mingxuan Yuan, Hui-Ling Zhen, Zhufei Chu, Wenji Fang, Xingquan Li and Zhiyao Xie, "Large Circuit Models: Opportunities and Challenges", Science China Information Sciences, Sep, 2024.

[C156] Jiarui Wang, Xun Jiang and **Yibo Lin***, "Top-Level Routing for Multiply-Instantiated Blocks with Topology Hashing", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C155] Yufan Du, Zizheng Guo, Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, "PowPrediCT: Cross-Stage Power Prediction with Circuit-Transformation-Aware Learning", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C154] Haoyi Zhang, Jiahao Song, Xiaohan Gao, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, "EasyACIM: An End-to-End Automated Analog CIM with Synthesizable Architecture and Agile Design Space Exploration", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C153] Zichen Kong, Xiyuan Tang*, Wei Shi, Yiheng Du, **Yibo Lin** and Yuan Wang, "PVTSizing: A TuRBO-RL-Based Batch-Sampling Optimization Framework for PVT-Robust Analog Circuit Synthesis", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C152] Yuan Pu, Fangzhou Liu, Yu Zhang, Zhuolun He, Kai-Yuan Chao, **Yibo Lin** and Bei Yu*, "Lesyn: Placement-aware Logic Resynthesis for Non-Integer Multiple-Cell-Height Designs",

ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C151] Wan Luan Lee, Dian-Lun Lin, Tsung-Wei Huang*, Shui Jiang, Tsung-Yi Ho, **Yibo Lin** and Bei Yu, "G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C150] Chenhao Xue, Chen Zhang, Xun Jiang, Gao Zhutianya, **Yibo Lin** and Guangyu Sun*, "Oltron: Algorithm-Hardware Co-design for Outlier-Aware Quantization of LLMs with Inter-/Intra-Layer Adaptation", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C149] Haoran Lu, Yandong Ge, Xun Jiang, Jiacheng Sun, Wanyue Peng, Rui Guo, Ming Li, **Yibo Lin**, Runsheng Wang, Heng Wu* and Ru Huang, "First Experimental Demonstration of Self-Aligned Flip FET (FFET): A Breakthrough Stacked Transistor Technology with 2.5T Design, Dual-Side Active and Interconnects", IEEE Symposium on VLSI Technology and Circuits (VLSI), Honolulu, HI, Jun 16-20, 2024.

[J148] Peiyu Liao, Yuxuan Zhao, Dawei Guo, **Yibo Lin** and Bei Yu*, "Analytical Die-to-Die 3D Placement With Bistratal Wirelength Model and GPU Acceleration", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2024.

[C147] Xiaohan Gao, Haoyi Zhang, Zhu Pan, **Yibo Lin***, Runsheng Wang and Ru Huang, "Migrating Standard Cells for Multiple Drive Strengths by Routing Imitation", IEEE/ACM International Symposium of EDA (ISEDA), Xi'an, China, May 10-13, 2024.

[C146] Qipan Wang, Tianxiang Zhu, **Yibo Lin***, Runsheng Wang and Ru Huang, "ATSim3D: Towards Accurate Thermal Simulator for Heterogeneous 3D IC Systems Considering Nonlinear Leakage and Conductivity", IEEE/ACM International Symposium of EDA (ISEDA), Xi'an, China, May 10-13, 2024. (**Honorable Mention Paper Award**)

[C145] Jing Mai, Jiarui Wang, Yifan Chen, Zizheng Guo, Xun Jiang, Yun Liang and **Yibo Lin***, "OpenPARF 3.0: Robust Multi-Electrostatics Based FPGA Macro Placement Considering Cascaded Macros Groups and Fence Regions", IEEE/ACM International Symposium of EDA (ISEDA), Xi'an, China, May 10-13, 2024. (**Best Paper Award**)

[C144] Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, "CircuitNet 2.0: An Advanced Dataset for Promoting Machine Learning Innovations in Realistic Chip Design Environment", International Conference on Learning Representations (ICLR), Vienna, Austria, May 7-11, 2024.

[J143] Yufei Chen, Zizheng Guo, Runsheng Wang, Ru Huang, **Yibo Lin** and Cheng Zhuo, "Dynamic Supply Noise Aware Timing Analysis With JIT Machine Learning Integration", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May, 2024. (accepted)

[C142] Zizheng Guo, Tsung-Wei Huang, Zhou Jin, Cheng Zhuo, **Yibo Lin***, Runsheng Wang and Ru Huang, "Heterogeneous Static Timing Analysis with Advanced Delay Calculator", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.

[C141] Haoyi Zhang, Xiaohan Gao, Zilong Shen, Jiahao Song, Xiaoxu Cheng, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, "SAGERoute 2.0: Hierarchical Analog and Mixed

Signal Routing Considering Versatile Routing Scenarios", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.

[C140] Yuan Pu, Tinghuan Chen, Zhuolun He, Chen Bai, Haisheng Zheng, **Yibo Lin** and Bei Yu*, "IncreMacro: Incremental Macro Placement Refinement", ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024. (**Best Paper Nomination**)

[C139] Yu Zhang, Yuan Pu, Fangzhou Liu, Peiyu Liao, Kaiyuan Chao, Keren Zhu, **Yibo Lin** and Bei Yu*, "Multi-Electrostatics Based Placement for Non-Integer Multiple-Height Cells", ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.

[C138] Siting Liu, Jiaxi Jiang, Zhuolun He, Ziyi Wang, **Yibo Lin** and Bei Yu*, "Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs", ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.

[J137] Zhixiong Di*, Runzhe Tao, Jing Mai, Lin Chen and **Yibo Lin**, "LEAPS: Topological-Layout-Adaptable Multi-Die FPGA Placement for Super Long Line Minimization", IEEE Transactions on Circuits and Systems I, Mar, 2024.

[J136] Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin***, "Multielectrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity, Clock Feasibility, and Timing Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Feb, 2024.

[C135] Cheng-Hsiang Chiu, Zhicheng Xiong, Zizheng Guo, Tsung-Wei Huang* and **Yibo Lin**, "An Efficient Task-parallel Pipeline Programming Framework", International Conference on High-Performance Computing in Asia-Pacific Region (HPC Asia), Nagoya, Japan, Jan, 2024.

[J134] Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "Accelerating Static Timing Analysis using CPU-GPU Heterogeneous Parallelism", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2023.

[J133] Zhuomin Chai, Yuxiang Zhao, Wei Liu*, **Yibo Lin***, Runsheng Wang and Ru Huang, "CircuitNet: An Open-Source Dataset for Machine Learning in VLSI CAD Applications with Improved Domain-Specific Evaluation Metric and Learning Strategies", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2023.

[J132] Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin***, "OpenPARF: 基于深度学习工具包的大规模异构 FPGA 开源布局布线框架", 电子与信息学报, 2023.

[J131] Zuodong Zhang, Zizheng Guo, **Yibo Lin***, Meng Li*, Runsheng Wang and Ru Huang, "AVATAR: An Aging- and Variation-Aware Dynamic Timing Analyzer for Error-Efficient Computing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Nov, 2023.

[J130] Guannan Guo, Tsung-Wei Huang*, **Yibo Lin**, Zizheng Guo, Sushma Yellapragada and Martin Wong, "A GPU-accelerated Framework for Path-based Timing Analysis", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Nov, 2023.

[C129] Yifan Chen, Zaiwen Wen, Yun Liang and **Yibo Lin***, "Stronger Mixed-Size Placement Backbone Considering Second-Order Information", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct 29-31, 2023.

[J128] Peiyu Liao, Dawei Guo, Zizheng Guo, Siting Liu, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and

Bei Yu*, "DREAMPlace 4.0: Timing-driven Placement with Momentum-based Net Weighting and Lagrangian-based Refinement", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2023.

[J127] Xiaohan Gao, Haoyi Zhang, Siyuan Ye, Mingjie Liu, David Z. Pan, Linxiao Shen, Runsheng Wang, **Yibo Lin*** and Ru Huang, "Post-Layout Simulation Driven Analog Circuit Sizing", SCIENCE CHINA Information Sciences, Oct, 2023.

[C126] Jing Mai, Jiaru Wang, Zhixiong Di, Guojie Luo, Yun Liang and **Yibo Lin***, "OpenPARF: An Open-Source Placement and Routing Framework for Large-Scale Heterogeneous FPGAs with Deep Learning Toolkit", International Conference on ASIC (ASICON), Nanjing, China, Oct, 2023. (**Invited paper**)

[C125] Xun Jiang, Zizheng Guo, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, "Accelerating Routability and Timing Optimization with Open-Source AI4EDA Dataset CircuitNet and Heterogeneous Platforms", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct, 2023. (**Invited paper**)

[C124] Kexing Zhou, Yun Liang*, **Yibo Lin**, Runsheng Wang and Ru Huang, "Khronos: Fusing Memory Access for Improved Hardware RTL Simulation", IEEE/ACM International Symposium on Microarchitecture (MICRO), Toronto, Canada, Oct, 2023.

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