# 林亦波

长聘副教授 ◇ 设计自动化与计算系统系 ◇ 集成电路学院 ◇ 北京大学

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## 研究方向

面向超大规模集成电路设计自动化的建模和优化、深度学习及其应用、异构计算

## 教育经历

**德克萨斯大学奥斯汀分校**                                          2013 年 9 月 – 2018 年 5 月
博士学位, 电子与计算机工程系
指导老师: David Z. Pan
博士毕业论文: Bridging Design and Manufacturing Gap through Machine Learning and Machine-Generated Layout

**上海交通大学**                                                    2009 年 9 月 – 2013 年 7 月
学士学位，微电子学院

## 工作经历

**北京大学 (Peking University)**                                    2025 年 8 月至今
长聘副教授

**北京大学 (Peking University)**                                    2019 年 6 月 – 2025 年 7 月
助理教授
集成电路学院设计自动化与计算系统系 (自 2021 年 11 月)
信息科学技术学院高能效计算与应用中心

**德克萨斯大学奥斯汀分校 (University of Texas at Austin)**          2018 年 7 月 – 2019 年 6 月
博士后

## 授课经历

| | | |
|---|---|---|
| 主讲 | 集成电路工程算法 | 研究生课程, 2023-2025 年 |
| 主讲 | 设计自动化与计算系统 | 研究生课程, 2022-2024 年 |
| 主讲 | 芯片设计自动化与智能优化 | 本科生课程, 2021-2025 年 |
| 主讲 | 计算概论 B | 本科生课程, 2020-2022 年 |

## 奖项及荣誉

| | | |
|---|---|---|
| 最佳论文提名 | DAC | 2025 年 |
| 荣誉提名论文 (×2) | ISEDA | 2025 年 |
| 最佳论文提名 | ASPDAC | 2025 年 |
| 最佳论文提名 | ICCAD | 2024 年 |
| 最佳论文 & 荣誉提名论文 | ISEDA | 2024 年 |
| 集成电路青年科技奖 (每年仅 1 位) | 中国计算机学会容错计算专委 | 2023 年 |
| 首届最佳审稿人奖 | ICCAD | 2023 年 |

| 最佳论文 (4/205) | DATE | 2023 年 |
|---|---|---|
| 最佳论文 (4/249) | DATE | 2022 年 |
| 最佳论文提名 | ICCAD | 2022 年 |
| 最佳论文 (2/3495, 4 年) | TCAD | 2021 年 |
| 最佳论文 | ISPD | 2020 年 |
| 最佳论文提名 | ASPDAC | 2020 年 |
| 最佳论文 (1/201) & 提名 (5/201) | DAC | 2019 年 |
| 最佳论文提名 | ISPD | 2019 年 |
| 首届最佳论文 | Integration, the VLSI Journal | 2018 年 |
| Franco Cerrina Memorial 最佳学生论文 | SPIE | 2016 年 |
| A. Richard Newton Young Student Fellow | DAC | 2014 年 |

## 学术服务

### 执行委员会成员

- 大会共同主席, ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD), 2025 年

- 程序共同主席, ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD), 2024 年

- 圆桌论坛主席, IEEE International Symposium of Electronics Design Automation (ISEDA), 2023 年–2024 年

- 财务主席, ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2021 年–2023 年

### 期刊编委

- 副编辑, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024 年至今

- 副编辑, ACM Transaction on Design Automation of Electronic Systems (TODAES), 2024 年至今

- 副编辑, Elsevier Integration, the VLSI Journal (Integration), 2024 年至今

- 客座编辑, ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2024 年

- 客座编辑, ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2022 年

### 赛题主席

- 赛题主席, 集成电路 EDA 设计精英挑战赛, 2021 年–2023 年

### 技术程序委员会成员

- ACM/IEEE Design Automation Conference (DAC): 2020

- IEEE/ACM International Conference on Computer-Aided Design (ICCAD): 2018 – 2021, 2023

- Design, Automation and Test in Europe Conference (DATE): 2025

- IEEE International Conference on Computer Design (ICCD): 2019

- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC): 2021 – 2022

- ACM International Symposium on Physical Design (ISPD): 2020, 2025

- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD): 2021

- ACM Great Lakes Symposium on VLSI (GLVLSI): 2024

- Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI): 2021

- IEEE Electron Devices Technology and Manufacturing Conference (EDTM): 2021

- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS): 2022.

## 期刊审稿人

- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)

- IEEE Transactions on Computers (TC)

- ACM Transaction on Design Automation of Electronic Systems (TODAES)

- SPIE Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)

- Elsevier, Integration, the VLSI Journal (Integration)

## 其他志愿服务

- ACM SIGDA 网站管理负责人，2021 年至今

## 10 篇代表性论文

按时间倒序排列。标 * 表示通讯作者。

1. Yifan Chen, Zaiwen Wen, Yun Liang and **Yibo Lin**\*, "Stronger Mixed-Size Placement Backbone Considering Second-Order Information", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct 29-31, 2023.

2. Haoyi Zhang, Xiaohan Gao, Haoyang Luo, Jiahao Song, Xiyuan Tang, Junhua Liu, **Yibo Lin**\*, Runsheng Wang and Ru Huang, "SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Apr 17-19, 2023. (**Best Paper Award**)

3. Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin**\*, "Multi-Electrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity, Clock Feasibility, and Timing Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sep, 2023.

4. Zizheng Guo, Tsung-Wei Huang and **Yibo Lin**\*, "Accelerating Static Timing Analysis using CPU-GPU Heterogeneous Parallelism", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2023.

5. Qipan Wang, Xiaohan Gao, **Yibo Lin**\*, Runsheng Wang and Ru Huang, "DeePEB: A Neural Partial Differential Equation Solver for Post Exposure Baking Simulation in Lithography", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 01-03, 2022. (**Best Paper Nomination**)

6. Zizheng Guo and **Yibo Lin**\*, "Differentiable-Timing-Driven Global Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

7. Siting Liu, Peiyu Liao, Zhitang Chen, Wenlong Lv, **Yibo Lin**\* and Bei Yu\*, "FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022. (**Best Paper Award**)

8. Zizheng Guo, Jing Mai and **Yibo Lin**\*, "Ultrafast CPU/GPU Kernels for Density Accumulation in Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

9. Zizheng Guo, Tsung-Wei Huang and **Yibo Lin**\*, "A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Large Designs", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

10. **Yibo Lin**\*, Zixuan Jiang, Jiaqi Gu, Wuxi Li, Shounak Dhar, Haoxing Ren, Brucek Khailany and David Z. Pan, "DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Apr, 2021. (**Best Paper Award**)

## 发明专利列表

[P18] 吴恒, 卢浩然, 江徇, 孙嘉诚, 王润声, **林亦波**, 黄如, "半导体结构的制备方法、半导体结构、器件及设备", 中国专利, CN2024101785421, Feb 09, 2024. (submitted)

[P17] **林亦波**, 郭资政, 张作栋, 江徇, 王润声, 黄如, "电路门级逻辑仿真方法、装置、计算机设备和存储介质", 中国专利, CN2023112735027, Jan 09, 2024. (submitted)

[P16] 余备, 廖培宇, **林亦波**, "一种基于 MoreauEnvelope 近似线长模型的大规模解析布局方法", 中国专利, CN2023111300780, Nov 28, 2023. (submitted)

[P15] 王润声, 张作栋, **林亦波**, 黄如, "一种基于解析模型的晶体管老化应力计算方法", 中国专利, CN202310843291X, Oct 13, 2023. (submitted)

[P14] **林亦波**, 高笑涵, 张昊懿, 王润声, 黄如, "一种多驱动能力的集成电路标准单元版图迁移的方法", 中国专利, CN2023101249631, Mar 28, 2023.

[P13] **林亦波**, 王启盼, 王润声, 黄如, "一种集成电路微带线传输线自动化分析设计方法", 中国专利, CN2023100496576, Mar 17, 2023.

[P12] **林亦波**, 郭资政, 谷丰, "一种 GPU 加速构建最小直角斯坦纳树的芯片布线方法", 中国专利, CN2022112858018, Jan 03, 2023. (submitted)

[P11] **林亦波**, 高笑涵, 张昊懿, 王润声, 黄如, "可处理电学和几何约束的模拟电路布线自动化方法及系统", 中国专利, CN2022114229951, Dec 20, 2022.

[P10] 郭资政, **林亦波**, 黄琮蔚, "一种集成电路静态时序分析中的路径分析方法", 中国专利, CN2021103772507, Oct 18, 2022. (submitted)

[P9] **林亦波**, 郭资政, "一种可微分时序驱动的芯片布局优化方法", 中国专利, CN2022107930171, Aug 05, 2022.

[P8] **林亦波**, 张昊懿, 高笑涵, 王润声, 黄如, "一种用于模拟电路版图布线的交互式编辑方法及工具", 中国专利, CN2022100363194, May 17, 2022.

[P7] **林亦波**, 麦景, "基于多电场模型的时钟驱动 FPGA 芯片全局布局方法", 中国专利, CN2022102058942, Apr 12, 2022.

[P6] **林亦波**, 张作栋, 郭资政, 王润声, 黄如, "一种老化及涨落感知的动态时序分析方法", 中国专利, CN2021115414669, Apr 5, 2022. (submitted)

[P5] **林亦波**, 张作栋, 郭资政, 王润声, 黄如, "一种基于事件传播的动态时序分析方法", 中国专利, CN2021109930951, Dec 24, 2021.

[P4] **林亦波**, 郭资政, 黄琮蔚, "一种 GPU 加速计算的集成电路无悲观路径分析方法", 中国专利, CN2021110703249, Dec 24, 2021.

[P3] 麦景, 郭资政, **林亦波**, "一种集成电路设计中器件密度分布的计算方法", 中国专利, CN2021105506486, Aug 27, 2021.

[P2] 高笑涵, **林亦波**, 刘鸣杰, 潘志刚, "一种交互式模拟电路版图编辑方法及系统", 中国专利, CN2021101747163, Jun 18, 2021.

[P1] 郭资政, 黄琮蔚, **林亦波**, "一种 GPU 加速计算的集成电路静态时序分析方法", 中国专利, CN2020111436325, Jan 22, 2021.

## 著作及论文列表

### 书籍章节

[B3] **Yibo Lin**, Zizheng Guo and Jing Mai, "Deep Learning Framework for Placement", Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)

[B2] Haoyu Yang, **Yibo Lin** and Bei Yu, "Machine Learning for Mask Synthesis and Verification", Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)

### 会议及期刊论文 (标 * 表示通讯作者)

论文成果包括: DAC (29 篇), ICCAD (24 篇), IEEE TCAD (30 篇), DATE (15 篇), ...

[C209] Zizheng Guo, Haichuan Liu, Xizhe Shi, Shenglu Hua, Zuodong Zhang, Chunyuan Zhao, Runsheng Wang and **Yibo Lin**\*, "HeteroSTA: A CPU-GPU Heterogeneous Static Timing Analysis En- gine with Holistic Industrial Design Support", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Hong Kong, Jan, 2026. (accepted)

[C208] Xizhe Shi, Zizheng Guo, Zuodong Zhang, Yun Liang, Runsheng Wang\* and **Yibo Lin**\*, "HeteroLatch: A CPU-GPU Heterogeneous Latch-Aware Timing Analysis Engine", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Hong Kong, Jan, 2026. (accepted)

[C207] Kairong Guo, Haoran Lu, Rui Guo, Jiarui Wang, Chunyuan Zhao, Heng Wu, Runsheng Wang and **Yibo Lin**\*, "Standard Cell Layout Synthesis for Dual-Sided 3D-Stacked Transistors", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Hong Kong, Jan, 2026. (accepted)

[C206] Weijian Fan, Haoyi Zhang, Weibin Lin, Runsheng Wang and **Yibo Lin**\*, "MOSTAR: Multi-Stage Hierarchical Bayesian Optimization for Substructure-Aware High-Dimensional Analog Circuit Sizing", IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), Hong Kong, Jan, 2026. (accepted)

[C205] Chenhao Xue, Kezhi Li, Jiaxing Zhang, Yi Ren, Zhengyuan Shi, Chen Zhang, **Yibo Lin**, Lining Zhang, Qiang Xu and Guangyu Sun\*, "AC-Refiner: Efficient Arithmetic Circuit Op-

timization Using Conditional Diffusion Models", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Hong Kong, Jan, 2026. (accepted)

[J204] Siting Liu, Ziyi Wang, Fangzhou Liu, **Yibo Lin**, Bei Yu* and Martin Wong, "Sign-off Timing Considerations via Concurrent Routing Topology Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J203] Zhenkun Lin, Genggeng Liu*, Xing Huang, **Yibo Lin**, Jixin Zhang, Wenhao Liu and Ting-Chi Wang, "A Unified Deep Reinforcement Learning Approach for Constructing Rectilinear and Octilinear Steiner Minimum Tree", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J202] Bingyang Liu, Haoyi Zhang, Xiaohan Gao, Zichen Kong, Xiyuan Tang, **Yibo Lin**\*, Runsheng Wang and Ru Huang, "LayoutCopilot: An LLM-powered Multi-agent Collaborative Framework for Interactive Analog Layout Design", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J201] Jingchen Zhu, Chenhao Xue, Yiqi Chen, Zhao Wang, Chen Zhang, Yu Shen, Yifan Chen, Zekang Cheng, Yu Jiang, Tianqi Wang, **Yibo Lin**, Wei Hu, Bin Cui, Runsheng Wang, Yun Liang and Guangyu Sun*, "Theseus: Exploring Efficient Wafer-Scale Chip Design for Large Language Models", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J200] Yajuan Su, Zixi Liu, **Yibo Lin**, Xiaojing Su, Yuqin Wang, Xin Hong, Yujie Jiang, Pengyu Ren and Yayi Wei, "A Post-Routing Layout Optimization Framework for Lithography Process Window Enlargement", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[J199] Jing Mai, Chunyuan Zhao, Zuodong Zhang, Zhixiong Di, Runsheng Wang and **Yibo Lin**\*, "LEGALM 2.0: A Versatile Augmented Lagrangian Method-Based Methodology for Mixed-Cell-Height Legalization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)

[C198] Chunyuan Zhao, Jiarui Wang, Xun Jiang, Jincheng Lou and **Yibo Lin**\*, "GTA: GPU-Accelerated Track Assignment with Lightweight Lookup Table for Conflict Detection", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Munich, Germany, Oct, 2025. (**Best Paper Nomination**)

[C197] Yufan Du, Zizheng Guo, Runsheng Wang and **Yibo Lin**\*, "Differentiable Physical Optimization", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Munich, Germany, Oct, 2025.

[C196] Yuhao Ji, Yuntao Lu, Zuodong Zhang, Zizheng Guo, **Yibo Lin** and Bei Yu*, "DiffCCD: Differentiable Concurrent Clock and Data Optimization", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Munich, Germany, Oct, 2025.

[C195] Yuan Pu, Yuhao Ji, Siying Yu, Zuodong Zhang, Zizheng Guo, Zhuolun He, **Yibo Lin**, David Z. Pan and Bei Yu*, "GPU Acceleration for Versatile Buffer Insertion", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Munich, Germany, Oct, 2025.

[C194] Yi Ren, Baokang Peng, Chenhao Xue, Kairong Guo, Yukun Wang, Guoyao Cheng, **Yibo Lin**, Lining Zhang and Guangyu Sun*, "Orthrus: Dual-Loop Automated Framework for

System-Technology Co-Optimization", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Munich, Germany, Oct, 2025.

[C193] Haichuan Liu, Zizheng Guo, Runsheng Wang and **Yibo Lin**\*, "IncreGPUSTA: GPU-Accelerated Incremental Static Timing Analysis for Iterative Design Flows", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Munich, Germany, Oct, 2025.

[C192] Tianxiang Zhu, Qipan Wang, **Yibo Lin**\* and Runsheng Wang\*, "High-Resolution Full-Chip Thermal Resistance Extraction of BEOL Interconnects in 3-D ICs Considering Detailed Via Connectivity", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Munich, Germany, Oct, 2025.

[C191] Chenchen Zhao, Zhengyuan Shi, Xiangyu Wen, Chengjie Liu, Yi Liu, Yunhao Zhou, Yuxiang Zhao, Hefei Feng, Yinan Zhu, Waa Gwok-Wan, Xin Cheng, Weiyu Chen, Yongqi Fu, Chujie Chen, Chenhao Xue, Ying Wang, **Yibo Lin**, Jun Yang, Ning Xu, Xi Wang and Qiang Xu\*, "MMCircuitEval: A Comprehensive Multimodal Circuit-Focused Benchmark for Evaluating LLMs", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Munich, Germany, Oct, 2025.

[C190] Yuxiang Zhao, Zhuomin Chai, Xun Jiang, Qiang Xu, Runsheng Wang and **Yibo Lin**\*, "DeepLayout: Learning Neural Representations of Circuit Placement Layout", International Conference on Machine Learning (ICML), Vancouver, Canada, Jul 13-19, 2025.

[C189] Lijie Zeng, Jiatai Sun, Xiao Wu, Dan Niu, Tianshi Wang, **Yibo Lin**, Zuochang Ye and Zhou Jin\*, "G-SpNN: GPU-Accelerated Passivity Enforcement for S-Parameter Modeling with Neural Networks", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025.

[C188] Ziyang Yu, Peng Xu, Zixiao Wang, Binwu Zhu, Qipan Wang, **Yibo Lin**, Runsheng Wang, Bei Yu\* and Martin Wong, "SDM-PEB: Spatial-Depthwise Mamba for Enhanced Post-Exposure Bake Simulation", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025.

[C187] Zizheng Guo, Yanqing Zhang, Runsheng Wang, **Yibo Lin** and Haoxing Ren, "GEM: GPU-Accelerated Emulator-Inspired RTL Simulation", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025. (**Best Paper Nomination**)

[C186] Xun Jiang, Haoran Lu, Yuxuan Zhao, Jiarui Wang, Zizheng Guo, Heng Wu, Bei Yu, Sung Kyu Lim, Runsheng Wang, Ru Huang and **Yibo Lin**\*, "A Systematic Approach for Multi-Objective Double-Side Clock Tree Synthesis", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025.

[C185] Jiarui Wang, Yanjing Liu and **Yibo Lin**\*, "Synergistic Die-Level Router for Multi-FPGA System with Time-Division Multiplexing Optimization", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025.

[C184] Yifan Chen, Jing Mai, Zuodong Zhang and **Yibo Lin**\*, "RUPlace: Optimizing Routability via Unified Placement and Routing Formulation", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 22-25, 2025.

[J183] Yuxiang Zhao, Zhuomin Chai, Xun Jiang, **Yibo Lin**\*, Runsheng Wang and Ru Huang, "PDNNet: PDN-Aware GNN-CNN Heterogeneous Network for Dynamic IR Drop Prediction",

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2025.

[J182] Rui Guo, Haoran Lu, Jiacheng Sun, Xun Jiang, Lining Zhangm, Ming Li, **Yibo Lin**, Runsheng Wang, Heng Wu* and Ru Huang, "Design Optimization of Flip FET Standard Cells With Dual-Sided Pins for Ultimate Scaling", IEEE Transactions on Electron Devices (TED), Jun, 2025.

[C181] Haoyi Zhang, Shizhao Sun, **Yibo Lin**, Runsheng Wang and Jiang Bian, "AnalogXpert: Automating Analog Topology Synthesis by Incorporating Circuit Design Expertise into Large Language Models", IEEE/ACM International Symposium of EDA (ISEDA), Hong Kong, May 9-12, 2025.

[C180] Yufan Du, Zizheng Guo, Yang Hsu, Zhili Xiong, Seunggeun Kim, David Z. Pan, Runsheng Wang and **Yibo Lin**\*, "Addressing Continuity and Expressivity Limitations in Differentiable Physical Optimization: A Case Study in Gate Sizing", IEEE/ACM International Symposium of EDA (ISEDA), Hong Kong, May 9-12, 2025. (**Honorable Mention Paper Award**)

[C179] Kairong Guo and **Yibo Lin**\*, "Multi-Row Standard Cell Layout Synthesis with Enhanced Scalability", IEEE/ACM International Symposium of EDA (ISEDA), Hong Kong, May 9-12, 2025.

[C178] Qipan Wang, **Yibo Lin**\*, Runsheng Wang and Ru Huang, "ATSim3.5D: A Multiscale Thermal Simulator for 3.5D-IC Systems based on Nonlinear Multigrid Method", IEEE/ACM International Symposium of EDA (ISEDA), Hong Kong, May 9-12, 2025. (**Honorable Mention Paper Award**)

[C177] Chenhao Xue, Yi Ren, Jinwei Zhou, Kezhi Li, Chen Zhang, **Yibo Lin**, Lining Zhang, Qiang Xu and Guangyu Sun*, "DOMAC: Differentiable Optimization for High-Speed Multipliers and Multiply-Accumulators", IEEE/ACM International Symposium of EDA (ISEDA), Hong Kong, May 9-12, 2025.

[C176] Yi Ren, Chenhao Xue, Jiaxing Zhang, Chen Zhang, Qiang Xu, **Yibo Lin** and Guangyu Sun*, "DiffuSE: Cross-Layer Design Space Exploration of DNN Accelerator via Diffusion-Driven Optimization", IEEE/ACM International Symposium of EDA (ISEDA), Hong Kong, May 9-12, 2025.

[C175] Haoran Lu, Xun Jiang, Yanbang Chu, Ziqiao Xu, Rui Guo, Wanyue Peng, **Yibo Lin**, Runsheng Wang, Heng Wu* and Ru Huang, "A Tale of Two Sides of Wafer: Physical Implementation and Block-Level PPA on Flip FET with Dual-sided Signals", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025.

[C174] Tianxiang Zhu, Qipan Wang, **Yibo Lin**\*, Runsheng Wang and Ru Huang, "MORE-Stress: Model Order Reduction based Efficient Numerical Algorithm for Thermal Stress Simulation of TSV Arrays in 2.5D/3D IC", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025.

[C173] Xizhe Shi, Zizheng Guo, **Yibo Lin**\*, Runsheng Wang and Ru Huang, "Handling Latch Loops in Timing Analysis with Improved Complexity and Divergent Loop Detection", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025.

[C172] Haikang Diao, Haoyi Zhang, Jiahao Song, Haoyang Luo, **Yibo Lin**, Runsheng Wang, Yuan Wang and Xiyuan Tang*, "SEGA-DCIM: Design Space Exploration-Guided Automatic Digital

CIM Compiler with Multiple Precision Support", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025.

[C171] Jing Mai, Chunyuan Zhao, Zuodong Zhang, Zhixiong Di, **Yibo Lin**\*, Runsheng Wang and Ru Huang, "LEGALM: Efficient Legalization for Mixed-Cell-Height Circuits with Linearized Augmented Lagrangian Method", ACM International Symposium on Physical Design (ISPD), Austin, TX, Mar 16-19, 2025.

[J170] Xun Jiang, Jiarui Wang, Jing Mai, Zhixiong Di and **Yibo Lin**\*, "A Robust FPGA Router With Optimization of High-Fanout Nets and Intra-CLB Connections", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Mar, 2025.

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[J63] **Yibo Lin***, Wuxi Li, Jiaqi Gu, Haoxing Ren, Brucek Khailany and David Z. Pan, "ABCD-Place: Accelerated Batch-based Concurrent Detailed Placement on Multi-threaded CPUs and

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[C59] Wei Ye, Mohamed Baker Alawieh, Yuki Watanabe, Shigeki Nojima, **Yibo Lin** and David Z. Pan*, "TEMPO: Fast Mask Topography Effect Modeling with Deep Learning", ACM International Symposium on Physical Design (ISPD), Taipei, Taiwan, Sep 20-23, 2020. (**Best Paper Award**)

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=============== 以下为博士及博士后期间发表内容 ===============

书籍章节

[B1] **Yibo Lin** and David Z. Pan, "Machine Learning in Physical Verification, Mask Synthesis, and Physical Design", Machine Learning in VLSI Computer-Aided Design, Springer, 2018, edited by Abe Elfedel, Duane Boning and Xin Li. (**Invited Book Chapter**)

会议及期刊论文 (标 * 表示通讯作者)

论文成果包括: DAC (7 篇), ICCAD (7 篇), IEEE TCAD (10 篇), DATE (1 篇), ...

[J52] Hao Chen, Mingjie Liu, Biying Xu, Keren Zhu, Xiyuan Tang, Shaolan Li, **Yibo Lin**, Nan Sun and David Z. Pan*, "MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII", IEEE Design & Test, Apr, 2021.

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[C50] Mingjie Liu, Wuxi Li, Keren Zhu, Biying Xu, **Yibo Lin**, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan*, "S3DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jan 13-16, 2020. (**Best Paper Nomination**)

[C49] Mohamed Baker Alawieh, Wuxi Li, **Yibo Lin**, Love Singhal, Mahesh Iyer and David Z. Pan*, "High-Definition Routing Congestion Prediction for Large-Scale FPGAs", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jan 13-16, 2020.

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[J44] **Yibo Lin**, Meng Li, Yuki Watanabe, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima and David Z. Pan*, "Data Efficient Lithography Modeling with Transfer Learning and Active Data Selection", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2019.

[C43] Wei Li, Yuzhe Ma, Qi Sun, **Yibo Lin**, Iris Hui-Ru Jiang, Bei Yu and David Z Pan, "Open-MPL: An Open Source Layout Decomposer", International Conference on ASIC (ASICON), Chongqing, China, Oct, 2019. (**Invited paper**)

[C42] **Yibo Lin**, Shounak Dhar, Wuxi Li, Haoxing Ren, Brucek Khailany and David Z. Pan*, "DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement", ACM/IEEE Design Automation Conference (DAC), Las Vegas, NV, Jun 2-6, 2019. (**Best Paper Award**)

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[C40] Biying Xu, **Yibo Lin**, Xiyuan Tang, Shaolan Li, Linxiao Shen, Nan Sun and David Z. Pan*, "WellGAN: Generative-Adversarial-Network-Guided Well Generation for Analog/Mixed-Signal Circuit Layout", ACM/IEEE Design Automation Conference (DAC), Las Vegas, NV, Jun 2-6, 2019.

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[J28] Meng Li, Bei Yu, **Yibo Lin**, Xiaoqing Xu, Wuxi Li and David Z Pan, "A practical split manufacturing framework for trojan prevention via simultaneous wire lifting and cell insertion",

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[J18] **Yibo Lin**, Bei Yu and David Z. Pan\*, "High performance dummy fill insertion with coupling and uniformity constraints", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sep, 2017.

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[J13] **Yibo Lin**, Bei Yu, Yi Zou, Zhuo Li, Charles J Alpert and David Z. Pan*, "Stitch aware detailed placement for multiple e-beam lithography", Integration, the VLSI Journal, Jun, 2017. (**Best Paper Award**)

[J12] **Yibo Lin**, Xiaoqing Xu, Bei Yu, Ross Baldick and David Z. Pan*, "Triple/quadruple patterning layout decomposition via linear programming and iterative rounding", Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), Jun, 2017.

[C11] Jiaojiao Ou, Bei Yu, Xiaoqing Xu, Joydeep Mitra, **Yibo Lin** and David Z. Pan*, "DSAR: DSA aware routing with simultaneous DSA guiding pattern and double patterning assignment", ACM International Symposium on Physical Design (ISPD), Portland, OR, Mar 19-22, 2017.

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[C9] Yudong Tao, Changhao Yan*, **Yibo Lin**, Sheng-Guo Wang, David Z. Pan and Xuan Zeng, "A novel unified dummy fill insertion framework with SQP-based optimization method", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov 7-10, 2016.

[C8] **Yibo Lin**, Bei Yu and David Z. Pan*, "Detailed placement in advanced technology nodes: a survey", IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Hangzhou, China, Oct 25-28, 2016. (**Invited paper**)

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[C5] **Yibo Lin**, Bei Yu, Yi Zou, Zhuo Li, Charles J Alpert and David Z. Pan*, "Stitch aware detailed placement for multiple e-beam lithography", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Macau, China, Jan 25-28, 2016.

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[J1] Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, **Yibo Lin**, Zhuo Li, Charles Alpert and David Z. Pan*, "Methodology for standard cell compliance and detailed placement for triple patterning lithography", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May, 2015.