YIBO LIN

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RESEARCH INTERESTS

Physical design automation, placement and routing

EDUCATION			
University of Texas at Austin, TX, USA Ph.D. student, Department of Electrical and Computer Engineering (GPA 3.96/4.0) Advisor: David Z. Pan	Aug. 2013 – May 2018		
Shanghai Jiao Tong University, Shanghai, P.R.China B.S., Department of Microelectronics (GPA 91.17/100)	Sep. 2009 – Jun. 2013		
EXPERIENCE			
Peking University, Beijing, China Assistant Professor Center for Energy-efficient Computing and Applications (CECA) School of EECS	Jul. 2019 – present		
University of Texas at Austin, Texas, U.S. Postdoc ECE Department	Jun. 2018 – Jun. 2019		
Toshiba Memory Corporation, Yokohama, Japan Internship Memory lithography group	May 2017 - Aug. 2017		
IMEC, Leuven, Belgium Internship Design technology co-optimization for emerging lithography options	Sep. 2016 - Nov. 2016		
Chinese University of Hong Kong, China Summer Intern Quantum computing	Jun. 2016 – Aug. 2016		
Cadence Design System, TX, USA Summer Intern Routability driven detailed placement	May 2015 – Aug. 2015		
Oracle Inc., TX, USA Summer Intern Incremental timing driven detailed placement	May 2014 - Aug. 2014		

SELECTED PUBLICATIONS

- [1] Wei Li, Yuzhe Ma, Qi Sun, Zhang Lu, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu and David Z. Pan, "OpenMPL: An Open Source Layout Decomposer", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020. (accepted)
- [2] Yibo Lin, Wuxi Li, Jiaqi Gu, Haoxing Ren, Brucek Khailany and David Z. Pan, "ABCDPlace: Accelerated Batch-based Concurrent Detailed Placement on Multi-threaded CPUs and GPUs", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Feb, 2020. (accepted)

- [3] Yibo Lin, Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J Alpert and David Z. Pan, "MrDP: Multiple-row detailed placement of heterogeneous-sized cells for advanced nodes", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2018.
- [4] Yibo Lin, Bei Yu, Biying Xu and David Z. Pan, "Triple patterning aware detailed placement toward zero cross-row middle-of-line conflict", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2017.
- [5] Zizheng Guo, Tsung-Wei Huang and Yibo Lin, "GPU-Accelerated Static Timing Analysis", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov 2-5, 2020.

RELATED COURSES

• EE382M: VLSI I	Prof. Michael Orshansky
• EE382N: Computer Architecture	Prof. Aater Suleman
• EE382V: Optimization Issues in VLSI CAD	Prof. David Pan
• EE382M: VLSI II	Prof. Jacob Abraham
• EE380L: Engineer Programming Languages	Prof. Craig Chase
• EE382V: Nanometer Scale IC Design	Prof. Michael Orshansky
• EE382V: VLSI Physical Design Automation	Prof. David Pan
• EE381V: Advanced Algorithms	Prof. Evdokia Nikolova
• EE382V: Advanced Programming Tools	Prof. Aziz Adnan
• EE380N: Optimization in Engineering Systems	Prof. Ross Baldick
• CS383C: Numerical Analysis: Linear Algebra	Prof. Robert van de Geijn

SKILLS

Programming Languages

C/C++, Python, Verilog

Web Development

HTML5, JavaScript/jQuery

EDA Tools

Cadence Virtuoso, Synopsys Design Compiler, Synopsys IC Compiler

AWARDS AND HONORS

Best Paper Award	ISPD	2020
Best Paper Award Nomination	ASPDAC	2020
Best Paper Award $(\times 1)$ & Nomination $(\times 1)$	DAC	2019
Best Paper Award Nomination	ISPD	2019
Inaugural Best Paper Award	Integration, the VLSI Journal	2018
Graduate Continuing Fellowship	University of Texas at Austin	2017
Franco Cerrina Memorial Best Student Paper Award	SPIE	2016
A. Richard Newton Young Student Fellow	DAC	2014

SERVICES

TPC members: ICCAD 2018, ICCAD 2019, ICCD 2019, ISPD 2020, DAC 2020, ICCAD 2020