

林亦波

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研究方向

面向超大规模集成电路设计自动化的建模和优化、深度学习及其应用、异构计算

教育经历

德克萨斯大学奥斯汀分校	2013 年 8 月 – 2018 年 5 月
博士学位, 电子与计算机工程系	
指导老师: David Z. Pan	
博士毕业论文: Bridging Design and Manufacturing Gap through Machine Learning and Machine-Generated Layout	
上海交通大学	2009 年 9 月 – 2013 年 6 月
学士学位, 微电子学院	

工作经历

北京大学 (Peking University)	2019 年 7 月至今
助理教授	
集成电路学院设计自动化与计算系统系 (自 2021 年 11 月)	
信息科学技术学院高能计算与应用中心	
德克萨斯大学奥斯汀分校 (University of Texas at Austin)	2018 年 6 月 – 2019 年 6 月
博士后	

授课经历

主讲	集成电路工程算法	研究生课程, 2023-2024 年
主讲	设计自动化与计算系统	研究生课程, 2022-2024 年
主讲	芯片设计自动化与智能优化	本科生课程, 2021-2024 年
主讲	计算概论 B	本科生课程, 2020-2022 年

奖项及荣誉

最佳论文提名	ICCAD	2024 年
最佳论文 & 荣誉提名论文	ISEDA	2024 年
青年科技奖 (Early Career Award, 每年仅 1 位)	中国计算机学会集成电路专委	2023 年
首届最佳审稿人奖	ICCAD	2023 年
最佳论文 (4/205)	DATE	2023 年
最佳论文 (4/249)	DATE	2022 年
最佳论文提名	ICCAD	2022 年
最佳论文 (2/3495, 4 年)	TCAD	2021 年
最佳论文	ISPD	2020 年

最佳论文提名	ASPDAC	2020 年
最佳论文 (1/201) & 提名 (5/201)	DAC	2019 年
最佳论文提名	ISPD	2019 年
首届最佳论文	Integration, the VLSI Journal	2018 年
Franco Cerrina Memorial 最佳学生论文	SPIE	2016 年
A. Richard Newton Young Student Fellow	DAC	2014 年

学术服务

执行委员会成员

- 大会共同主席, ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD), 2025 年
- 程序共同主席, ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD), 2024 年
- 圆桌论坛主席, IEEE International Symposium of Electronics Design Automation (ISED), 2023 年–2024 年
- 财务主席, ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2021 年–2023 年

期刊编辑

- 副编辑, ACM Transaction on Design Automation of Electronic Systems (TODAES), 2024 年至今
- 副编辑, Elsevier Integration, the VLSI Journal (Integration), 2024 年至今
- 客座编辑, ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2024 年
- 客座编辑, ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2022 年

赛题主席

- 赛题主席, 集成电路 EDA 设计精英挑战赛, 2021 年–2023 年

技术程序委员会成员

- ACM/IEEE Design Automation Conference (DAC): 2020
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD): 2018 – 2021, 2023
- Design, Automation and Test in Europe Conference (DATE): 2025
- IEEE International Conference on Computer Design (ICCD): 2019
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC): 2021 – 2022
- ACM International Symposium on Physical Design (ISPD): 2020, 2025
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD): 2021
- ACM Great Lakes Symposium on VLSI (GLVLSI): 2024
- Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI): 2021
- IEEE Electron Devices Technology and Manufacturing Conference (EDTM): 2021
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS): 2022.

期刊审稿人

- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Computers (TC)
- ACM Transaction on Design Automation of Electronic Systems (TODAES)
- SPIE Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)
- Elsevier, Integration, the VLSI Journal (Integration)

其他志愿服务

- ACM SIGDA 网站管理负责人, 2021 年至今

10 篇代表性论文

按时间倒序排列。标 * 表示通讯作者。

1. Yifan Chen, Zaiwen Wen, Yun Liang and **Yibo Lin***, “[Stronger Mixed-Size Placement Backbone Considering Second-Order Information](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct 29-31, 2023.
2. Haoyi Zhang, Xiaohan Gao, Haoyang Luo, Jiahao Song, Xiyuan Tang, Junhua Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, “[SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Apr 17-19, 2023. (**Best Paper Award**)
3. Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin***, “[Multi-Electrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity, Clock Feasibility, and Timing Optimization](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sep, 2023.
4. Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, “[Accelerating Static Timing Analysis using CPU-GPU Heterogeneous Parallelism](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2023.
5. Qipan Wang, Xiaohan Gao, **Yibo Lin***, Runsheng Wang and Ru Huang, “[DeePEB: A Neural Partial Differential Equation Solver for Post Exposure Baking Simulation in Lithography](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 01-03, 2022. (**Best Paper Nomination**)
6. Zizheng Guo and **Yibo Lin***, “[Differentiable-Timing-Driven Global Placement](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.
7. Siting Liu, Peiyu Liao, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, “[FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022. (**Best Paper Award**)
8. Zizheng Guo, Jing Mai and **Yibo Lin***, “[Ultrafast CPU/GPU Kernels for Density Accumulation in Placement](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Dec 05-09, 2021.
9. Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, “[A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Large Designs](#)”, ACM/IEEE Design Automation

Conference (DAC), San Francisco, CA, Dec 05-09, 2021.

10. **Yibo Lin***, Zixuan Jiang, Jiaqi Gu, Wuxi Li, Shounak Dhar, Haoxing Ren, Brucek Khailany and David Z. Pan, “[DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Apr, 2021. (**Best Paper Award**)

发明专利列表

- [P18] 吴恒, 卢浩然, 江循, 孙嘉诚, 王润声, **林亦波**, 黄如, “半导体结构的制备方法、半导体结构、器件及设备”, 中国专利, CN2024101785421, Feb 09, 2024. (submitted)
- [P17] **林亦波**, 郭资政, 张作栋, 江循, 王润声, 黄如, “电路门级逻辑仿真方法、装置、计算机设备和存储介质”, 中国专利, CN2023112735027, Jan 09, 2024. (submitted)
- [P16] 余备, 廖培宇, **林亦波**, “一种基于 MoreauEnvelope 近似线长模型的大规模解析布局方法”, 中国专利, CN2023111300780, Nov 28, 2023. (submitted)
- [P15] 王润声, 张作栋, **林亦波**, 黄如, “一种基于解析模型的晶体管老化应力计算方法”, 中国专利, CN202310843291X, Oct 13, 2023. (submitted)
- [P14] **林亦波**, 高笑涵, 张昊懿, 王润声, 黄如, “一种多驱动能力的集成电路标准单元版图迁移的方法”, 中国专利, CN2023101249631, Mar 28, 2023.
- [P13] **林亦波**, 王启盼, 王润声, 黄如, “一种集成电路微带线传输线自动化分析设计方法”, 中国专利, CN2023100496576, Mar 17, 2023.
- [P12] **林亦波**, 郭资政, 谷丰, “一种 GPU 加速构建最小直角斯坦纳树的芯片布线方法”, 中国专利, CN2022112858018, Jan 03, 2023. (submitted)
- [P11] **林亦波**, 高笑涵, 张昊懿, 王润声, 黄如, “可处理电学和几何约束的模拟电路布线自动化方法及系统”, 中国专利, CN2022114229951, Dec 20, 2022.
- [P10] 郭资政, **林亦波**, 黄琮蔚, “一种集成电路静态时序分析中的路径分析方法”, 中国专利, CN2021103772507, Oct 18, 2022. (submitted)
- [P9] **林亦波**, 郭资政, “一种可微分时序驱动的芯片布局优化方法”, 中国专利, CN2022107930171, Aug 05, 2022.
- [P8] **林亦波**, 张昊懿, 高笑涵, 王润声, 黄如, “一种用于模拟电路版图布线的交互式编辑方法及工具”, 中国专利, CN2022100363194, May 17, 2022.
- [P7] **林亦波**, 麦景, “基于多电场模型的时钟驱动 FPGA 芯片全局布局方法”, 中国专利, CN2022102058942, Apr 12, 2022.
- [P6] **林亦波**, 张作栋, 郭资政, 王润声, 黄如, “一种老化及涨落感知的动态时序分析方法”, 中国专利, CN2021115414669, Apr 5, 2022. (submitted)
- [P5] **林亦波**, 张作栋, 郭资政, 王润声, 黄如, “一种基于事件传播的动态时序分析方法”, 中国专利, CN2021109930951, Dec 24, 2021.
- [P4] **林亦波**, 郭资政, 黄琮蔚, “一种 GPU 加速计算的集成电路无悲观路径分析方法”, 中国专利, CN2021110703249, Dec 24, 2021.
- [P3] 麦景, 郭资政, **林亦波**, “一种集成电路设计中器件密度分布的计算方法”, 中国专利, CN2021105506486, Aug 27, 2021.

- [P2] 高笑涵, **林亦波**, 刘鸣杰, 潘志刚, “一种交互式模拟电路版图编辑方法及系统”, 中国专利, CN2021101747163, Jun 18, 2021.
- [P1] 郭资政, 黄琮蔚, **林亦波**, “一种 GPU 加速计算的集成电路静态时序分析方法”, 中国专利, CN2020111436325, Jan 22, 2021.

著作及论文列表

书籍章节

- [B3] **Yibo Lin**, Zizheng Guo and Jing Mai, “[Deep Learning Framework for Placement](#)”, Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)
- [B2] Haoyu Yang, **Yibo Lin** and Bei Yu, “[Machine Learning for Mask Synthesis and Verification](#)”, Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)

会议及期刊论文 (标 * 表示通讯作者)

论文成果包括: DAC (23 篇), ICCAD (16 篇), IEEE TCAD (27 篇), DATE (14 篇), ...

- [J176] Siting Liu, Ziyi Wang, Fangzhou Liu, **Yibo Lin**, Bei Yu* and Martin Wong, “[Sign-off Timing Considerations via Concurrent Routing Topology Optimization](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)
- [J175] Yuxiang Zhao, Zhuomin Chai, Xun Jiang, **Yibo Lin***, Runsheng Wang and Ru Huang, “PDNNet: PDN-Aware GNN-CNN Heterogeneous Network for Dynamic IR Drop Prediction”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)
- [J174] Zhenkun Lin, Genggeng Liu*, Xing Huang, **Yibo Lin**, Jixin Zhang, Wenhao Liu and Ting-Chi Wang, “A Unified Deep Reinforcement Learning Approach for Constructing Rectilinear and Octilinear Steiner Minimum Tree”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)
- [J173] Bingyang Liu, Haoyi Zhang, Xiaohan Gao, Zichen Kong, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, “LayoutCopilot: An LLM-powered Multi-agent Collaborative Framework for Interactive Analog Layout Design”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025. (accepted)
- [C172] Tianxiang Zhu, Qipan Wang, **Yibo Lin***, Runsheng Wang and Ru Huang, “MORE-Stress: Model Order Reduction based Efficient Numerical Algorithm for Thermal Stress Simulation of TSV Arrays in 2.5D/3D IC”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025. (accepted)
- [C171] Xizhe Shi, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, “Handling Latch Loops in Timing Analysis with Improved Complexity and Divergent Loop Detection”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025. (accepted)
- [C170] Haikang Diao, Haoyi Zhang, Jiahao Song, Haoyang Luo, **Yibo Lin**, Runsheng Wang, Yuan Wang and Xiyuan Tang*, “SEGA-DCIM: Design Space Exploration-Guided Automatic Digital CIM Compiler with Multiple Precision Support”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Lyon, France, Mar 31, 2025. (accepted)

- [C169] Che Chang, Boyang Zhang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yi-Hua Chung, Wan-Luan Lee, Zizheng Guo, **Yibo Lin** and Tsung-Wei Huang*, “PathGen: An Efficient Parallel Critical Path Generation Algorithm”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan, 2025. (accepted)
- [C168] Boyang Zhang, Che Chang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yang Sui, Chih-Chun Chang, Yi-Hua Chung, Wan Luan Lee, Zizheng Guo, **Yibo Lin** and Tsung-Wei Huang*, “iTAP: An Incremental Task Graph Partitioner for Task-parallel Static Timing Analysis”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan, 2025. (accepted)
- [C167] Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, “Analyzing Timing in Shorter Time: A Journey through Heterogeneous Parallelism for Static Timing Analysis”, IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Zhuhai, China, Oct 22-25, 2024. (**Invited paper**)
- [C166] Qipan Wang, Xueqing Li, Tianyu Jia, **Yibo Lin***, Runsheng Wang and Ru Huang, “AT-Place2.5D: Analytical Thermal-Aware Chiplet Placement Framework for Large-Scale 2.5D-IC”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.
- [C165] Chunyuan Zhao, Zizheng Guo, Rui Wang, Zaiwen Wen, Yun Liang and **Yibo Lin***, “HeLEM-GR: Heterogeneous Global Routing with Linearized Exponential Multiplier Method”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.
- [C164] Zizheng Guo, Zuodong Zhang, Wuxi Li, Tsung-Wei Huang, Xizhe Shi, Yufan Du, **Yibo Lin***, Runsheng Wang and Ru Huang, “HeteroExcept: A CPU-GPU Heterogeneous Algorithm to Accelerate Exception-aware Static Timing Analysis”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.
- [C163] Xiaohan Gao, Haoyi Zhang, Bingyang Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, “Joint Placement Optimization for Hierarchical Analog/Mixed-Signal Circuits”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.
- [C162] Yufan Du, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, “Fusion of Global Placement and Gate Sizing with Differentiable Optimization”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (**Best Paper Nomination**)
- [C161] Tianxiang Zhu, Qipan Wang, **Yibo Lin***, Runsheng Wang and Ru Huang, “FaStTherm: Fast and Stable Full-Chip Transient Thermal Predictor Considering Nonlinear Effects”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.
- [C160] Jing Mai, Zuodong Zhang, **Yibo Lin***, Runsheng Wang and Ru Huang, “MORPH: More Robust ASIC Placement for Hybrid Region Constraint Management”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024.
- [J159] Tsung-Yi Ho, Sadaf Khan, Jinwei Liu, Yi Liu, Zhengyuan Shi, Ziyi Wang, Qiang Xu*, Evangeline F.Y. Young, Bei Yu, Ziyang Zheng, Binwu Zhu, Keren Zhu, Yiqi Che, Yun Liang, **Yibo Lin**, Guojie Luo, Guangyu Sun, Runsheng Wang, Xinming Wei, Chenhao Xue, Haoyi Zhang, Zuodong Zhang, Yuxiang Zhao, Sunan Zou, Lei Chen, Yu Huang, Min Li, Dimitrios Tsaras, Mingxuan Yuan, Hui-Ling Zhen, Zhufei Chu, Wenji Fang, Xingquan Li and Zhiyao Xie,

- “Large Circuit Models: Opportunities and Challenges”, Science China Information Sciences, Sep, 2024.
- [J158] Yuxuan Zhao, Peiyu Liao, Siting Liu, Jiayi Jiang, **Yibo Lin** and Bei Yu*, “[Analytical Heterogeneous Die-to-Die 3D Placement With Macros](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Aug, 2024. (accepted)
- [J157] Xun Jiang, Jiarui Wang, Jing Mai, Zhixiong Di and **Yibo Lin***, “[A Robust FPGA Router With Optimization of High-Fanout Nets and Intra-CLB Connections](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Aug, 2024. (accepted)
- [C156] Jiarui Wang, Xun Jiang and **Yibo Lin***, “[Top-Level Routing for Multiply-Instantiated Blocks with Topology Hashing](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C155] Yufan Du, Zizheng Guo, Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, “[PowPrediCT: Cross-Stage Power Prediction with Circuit-Transformation-Aware Learning](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C154] Haoyi Zhang, Jiahao Song, Xiaohan Gao, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, “[EasyACIM: An End-to-End Automated Analog CIM with Synthesizable Architecture and Agile Design Space Exploration](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C153] Zichen Kong, Xiyuan Tang*, Wei Shi, Yiheng Du, **Yibo Lin** and Yuan Wang, “[PVTsizing: A TuRBO-RL-Based Batch-Sampling Optimization Framework for PVT-Robust Analog Circuit Synthesis](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C152] Yuan Pu, Fangzhou Liu, Yu Zhang, Zhuolun He, Kai-Yuan Chao, **Yibo Lin** and Bei Yu*, “[Lesyn: Placement-aware Logic Resynthesis for Non-Integer Multiple-Cell-Height Designs](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C151] Wan Luan Lee, Dian-Lun Lin, Tsung-Wei Huang*, Shui Jiang, Tsung-Yi Ho, **Yibo Lin** and Bei Yu, “[G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C150] Chenhao Xue, Chen Zhang, Xun Jiang, Gao Zhutianya, **Yibo Lin** and Guangyu Sun*, “[Oltron: Algorithm-Hardware Co-design for Outlier-Aware Quantization of LLMs with Inter-/Intra-Layer Adaptation](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C149] Haoran Lu, Yandong Ge, Xun Jiang, Jiacheng Sun, Wanyue Peng, Rui Guo, Ming Li, **Yibo Lin**, Runsheng Wang, Heng Wu* and Ru Huang, “[First Experimental Demonstration of Self-Aligned Flip FET \(FFET\): A Breakthrough Stacked Transistor Technology with 2.5T Design, Dual-Side Active and Interconnects](#)”, IEEE Symposium on VLSI Technology and Circuits (VLSI), Honolulu, HI, Jun 16-20, 2024.
- [J148] Peiyu Liao, Yuxuan Zhao, Dawei Guo, **Yibo Lin** and Bei Yu*, “[Analytical Die-to-Die 3D Placement With Bistratal Wirelength Model and GPU Acceleration](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2024.

- [C147] Xiaohan Gao, Haoyi Zhang, Zhu Pan, **Yibo Lin***, Runsheng Wang and Ru Huang, “[Migrating Standard Cells for Multiple Drive Strengths by Routing Imitation](#)”, IEEE/ACM International Symposium of EDA (ISEDA), Xi’an, China, May 10-13, 2024.
- [C146] Qipan Wang, Tianxiang Zhu, **Yibo Lin***, Runsheng Wang and Ru Huang, “[ATSim3D: Towards Accurate Thermal Simulator for Heterogeneous 3D IC Systems Considering Nonlinear Leakage and Conductivity](#)”, IEEE/ACM International Symposium of EDA (ISEDA), Xi’an, China, May 10-13, 2024. (**Honorable Mention Paper Award**)
- [C145] Jing Mai, Jiarui Wang, Yifan Chen, Zizheng Guo, Xun Jiang, Yun Liang and **Yibo Lin***, “[OpenPARF 3.0: Robust Multi-Electrostatics Based FPGA Macro Placement Considering Cascaded Macros Groups and Fence Regions](#)”, IEEE/ACM International Symposium of EDA (ISEDA), Xi’an, China, May 10-13, 2024. (**Best Paper Award**)
- [C144] Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, “[CircuitNet 2.0: An Advanced Dataset for Promoting Machine Learning Innovations in Realistic Chip Design Environment](#)”, International Conference on Learning Representations (ICLR), Vienna, Austria, May 7-11, 2024.
- [J143] Yufei Chen, Zizheng Guo, Runsheng Wang, Ru Huang, **Yibo Lin** and Cheng Zhuo, “[Dynamic Supply Noise Aware Timing Analysis With JIT Machine Learning Integration](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May, 2024. (accepted)
- [C142] Zizheng Guo, Tsung-Wei Huang, Zhou Jin, Cheng Zhuo, **Yibo Lin***, Runsheng Wang and Ru Huang, “[Heterogeneous Static Timing Analysis with Advanced Delay Calculator](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.
- [C141] Haoyi Zhang, Xiaohan Gao, Zilong Shen, Jiahao Song, Xiaoxu Cheng, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, “[SAGERoute 2.0: Hierarchical Analog and Mixed Signal Routing Considering Versatile Routing Scenarios](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.
- [C140] Yuan Pu, Tinghuan Chen, Zhuolun He, Chen Bai, Haisheng Zheng, **Yibo Lin** and Bei Yu*, “[IncreMacro: Incremental Macro Placement Refinement](#)”, ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024. (**Best Paper Nomination**)
- [C139] Yu Zhang, Yuan Pu, Fangzhou Liu, Peiyu Liao, Kaiyuan Chao, Keren Zhu, **Yibo Lin** and Bei Yu*, “[Multi-Electrostatics Based Placement for Non-Integer Multiple-Height Cells](#)”, ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.
- [C138] Siting Liu, Jiayi Jiang, Zhuolun He, Ziyi Wang, **Yibo Lin** and Bei Yu*, “[Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs](#)”, ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.
- [J137] Zhixiong Di*, Runzhe Tao, Jing Mai, Lin Chen and **Yibo Lin**, “[LEAPS: Topological-Layout-Adaptable Multi-Die FPGA Placement for Super Long Line Minimization](#)”, IEEE Transactions on Circuits and Systems I, Mar, 2024.
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