

# YIBO LIN

Assistant Professor ◊ Department of Design Automation and Computing System  
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## RESEARCH INTERESTS

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Modeling and optimization in VLSI CAD, machine learning applications, and heterogeneous computing

## EDUCATION

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**University of Texas at Austin, TX, USA** *Aug. 2013 – May 2018*

Ph.D., Department of Electrical and Computer Engineering

Advisor: David Z. Pan

Thesis: “Bridging Design and Manufacturing Gap through Machine Learning and Machine-Generated Layout”

**Shanghai Jiao Tong University, Shanghai, P.R.China** *Sep. 2009 – Jun. 2013*

B.S., Department of Microelectronics

## EXPERIENCE

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**Peking University, Beijing, China** *Jul. 2019 – present*

Assistant Professor

Department of Design Automation and Computing System,

School of Integrated Circuits (since Nov. 2021)

Center for Energy-efficient Computing and Applications (CECA),

School of EECS

**University of Texas at Austin, Texas, U.S.** *Jun. 2018 – Jun. 2019*

Postdoc

ECE Department

## TEACHING EXPERIENCE

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Fundamental Algorithms for Engineering in Integrated Circuits

Instructor	Graduate	Spring 2023-2024
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Design Automation and Computing System

Instructor	Graduate	Fall 2022-2024
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Optimization and Machine Learning in VLSI Design Automation

Instructor	Undergraduate	Spring 2021-2022, Fall 2023-2024
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Introduction to Computing B

Instructor	Undergraduate	Fall 2020-2022
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## AWARDS AND HONORS

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Best Paper Award (x1) & Honorable Mention (x1)	ISEDA	2024
Early Career Award (only one per year)	CCF Technical Committee in IC	2023
Inaugural Best Reviewer Award	ICCAD	2023
Best Paper Award (4/205)	DATE	2023
Best Paper Award (4/249)	DATE	2022
Best Paper Award Nomination	ICCAD	2022
Donald O. Pederson Best Paper Award (2/3495 in 4 years)	TCAD	2021
Best Paper Award	ISPD	2020
Best Paper Award Nomination	ASPDAC	2020
Best Paper Award (1/201) & Nomination (5/201)	DAC	2019
Best Paper Award Nomination	ISPD	2019
Inaugural Best Paper Award	Integration, the VLSI Journal	2018
Graduate Continuing Fellowship	University of Texas at Austin	2017
Franco Cerrina Memorial Best Student Paper Award	SPIE	2016
A. Richard Newton Young Student Fellow	DAC	2014
National Scholarship	Shanghai Jiao Tong University	2012
Samsung Scholarship	Shanghai Jiao Tong University	2011
The Second Prize Scholarship	Shanghai Jiao Tong University	2010

## PROFESSIONAL SERVICE

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### TPC Member

- ACM/IEEE Design Automation Conference (DAC): 2020
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD): 2018, 2019, 2020, 2021, 2023
- IEEE International Conference on Computer Design (ICCD): 2019
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC): 2021, 2022
- ACM International Symposium on Physical Design (ISPD): 2020, 2024
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD): 2021
- ACM Great Lakes Symposium on VLSI (GLVLSI): 2024
- Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI): 2021
- IEEE Electron Devices Technology and Manufacturing Conference (EDTM): 2021
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS): 2022.

### Journal Reviewer

- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Computers (TC)
- ACM Transaction on Design Automation of Electronic Systems (TODAES)

- SPIE Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)
- Elsevier, Integration, the VLSI Journal (Integration)

### Journal Editor

- Guest Editor @ ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2022
- Guest Editor @ ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2024
- Associate Editor @ ACM Transaction on Design Automation of Electronic Systems (TODAES), 2024 – present
- Associate Editor @ Elsevier Integration, the VLSI Journal (Integration), 2024 – present

### EC Member

- Financial chair, ACM/IEEE Workshop on Machine Learning for CAD (MLCAD) 2021-2023
- Panel chair, IEEE International Symposium of Electronics Design Automation (ISED) 2023-2024
- Program co-chair, ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD) 2024
- General co-chair, ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD) 2025

## PUBLICATIONS

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### Book Chapters

- [B3] **Yibo Lin**, Zizheng Guo and Jing Mai, “[Deep Learning Framework for Placement](#)”, Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)
- [B2] Haoyu Yang, **Yibo Lin** and Bei Yu, “[Machine Learning for Mask Synthesis and Verification](#)”, Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)

### Conference and Journal Papers (\* denotes corresponding authors)

- [C166] Che Chang, Boyang Zhang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yi-Hua Chung, Wan-Luan Lee, Zizheng Guo, **Yibo Lin** and Tsung-Wei Huang\*, “PathGen: An Efficient Parallel Critical Path Generation Algorithm”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan, 2025. (accepted)
- [J165] Yuxuan Zhao, Peiyu Liao, Siting Liu, Jiayi Jiang, **Yibo Lin** and Bei Yu\*, “[Analytical Heterogeneous Die-to-Die 3D Placement With Macros](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024. (accepted)
- [J164] Xun Jiang, Jiarui Wang, Jing Mai, Zhixiong Di and **Yibo Lin**\*, “[A Robust FPGA Router With Optimization of High-Fanout Nets and Intra-CLB Connections](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024. (accepted)

- [C163] Zizheng Guo, **Yibo Lin\***, Runsheng Wang and Ru Huang, “Analyzing Timing in Shorter Time: A Journey through Heterogeneous Parallelism for Static Timing Analysis”, IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Zhuhai, China, Oct 22-25, 2024. (**Invited paper**)
- [C162] Qipan Wang, Xueqing Li, Tianyu Jia, **Yibo Lin\***, Runsheng Wang and Ru Huang, “AT-Place2.5D: Analytical Thermal-Aware Chiplet Placement Framework for Large-Scale 2.5D-IC”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)
- [C161] Chunyuan Zhao, Zizheng Guo, Rui Wang, Zaiwen Wen, Yun Liang and **Yibo Lin\***, “HeLEM-GR: Heterogeneous Global Routing with Linearized Exponential Multiplier Method”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)
- [C160] Zizheng Guo, Zuodong Zhang, Wuxi Li, Tsung-Wei Huang, Xizhe Shi, Yufan Du, **Yibo Lin\***, Runsheng Wang and Ru Huang, “HeteroExcept: A CPU-GPU Heterogeneous Algorithm to Accelerate Exception-aware Static Timing Analysis”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)
- [C159] Xiaohan Gao, Haoyi Zhang, Bingyan Liu, **Yibo Lin\***, Runsheng Wang and Ru Huang, “Joint Placement Optimization for Hierarchical Analog/Mixed-Signal Circuits”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)
- [C158] Yufan Du, Zizheng Guo, **Yibo Lin\***, Runsheng Wang and Ru Huang, “Fusion of Global Placement and Gate Sizing with Differentiable Optimization”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)
- [C157] Tianxiang Zhu, Qipan Wang, **Yibo Lin\***, Runsheng Wang and Ru Huang, “FaStTherm: Fast and Stable Full-Chip Transient Thermal Predictor Considering Nonlinear Effects”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)
- [C156] Jing Mai, Zuodong Zhang, **Yibo Lin\***, Runsheng Wang and Ru Huang, “MORPH: More Robust ASIC Placement for Hybrid Region Constraint Management”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)
- [J155] Tsung-Yi Ho, Sadaf Khan, Jinwei Liu, Yi Liu, Zhengyuan Shi, Ziyi Wang, Qiang Xu\*, Evangeline F.Y. Young, Bei Yu, Ziyang Zheng, Binwu Zhu, Keren Zhu, Yiqi Che, Yun Liang, **Yibo Lin**, Guojie Luo, Guangyu Sun, Runsheng Wang, Xinming Wei, Chenhao Xue, Haoyi Zhang, Zuodong Zhang, Yuxiang Zhao, Sunan Zou, Lei Chen, Yu Huang, Min Li, Dimitrios Tsaras, Mingxuan Yuan, Hui-Ling Zhen, Zhufei Chu, Wenji Fang, Xingquan Li and Zhiyao Xie, “[Large Circuit Models: Opportunities and Challenges](#)”, Science China Information Sciences, Sep, 2024.
- [C154] Jiarui Wang, Xun Jiang and **Yibo Lin\***, “Top-Level Routing for Multiply-Instantiated Blocks with Topology Hashing”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C153] Yufan Du, Zizheng Guo, Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin\***, Runsheng Wang and Ru Huang, “PowPrediCT: Cross-Stage Power Prediction with Circuit-Transformation-Aware Learning”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun

23-27, 2024.

- [C152] Haoyi Zhang, Jiahao Song, Xiaohan Gao, Xiyuan Tang, **Yibo Lin**<sup>\*</sup>, Runsheng Wang and Ru Huang, “EasyACIM: An End-to-End Automated Analog CIM with Synthesizable Architecture and Agile Design Space Exploration”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C151] Zichen Kong, Xiyuan Tang<sup>\*</sup>, Wei Shi, Yiheng Du, **Yibo Lin** and Yuan Wang, “PVT sizing: A TuRBO-RL-Based Batch-Sampling Optimization Framework for PVT-Robust Analog Circuit Synthesis”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C150] Yuan Pu, Fangzhou Liu, Yu Zhang, Zhuolun He, Kai-Yuan Chao, **Yibo Lin** and Bei Yu<sup>\*</sup>, “Lesyn: Placement-aware Logic Resynthesis for Non-Integer Multiple-Cell-Height Designs”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C149] Wan Luan Lee, Dian-Lun Lin, Tsung-Wei Huang<sup>\*</sup>, Shui Jiang, Tsung-Yi Ho, **Yibo Lin** and Bei Yu, “G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.
- [C148] Haoran Lu, Y Ge, ong, Xun Jiang, Jiacheng Sun, Wanyue Peng, Rui Guo, Ming Li, **Yibo Lin**, Runsheng Wang, Heng Wu<sup>\*</sup> and Ru Huang, “[First Experimental Demonstration of Self-Aligned Flip FET \(FFET\): A Breakthrough Stacked Transistor Technology with 2.5T Design, Dual-Side Active and Interconnects](#)”, IEEE Symposium on VLSI Technology and Circuits (VLSI), Honolulu, HI, Jun 16-20, 2024.
- [C147] Xiaohan Gao, Haoyi Zhang, Zhu Pan, **Yibo Lin**<sup>\*</sup>, Runsheng Wang and Ru Huang, “Migrating Standard Cells for Multiple Drive Strengths by Routing Imitation”, IEEE/ACM International Symposium of EDA (ISEDA), Xi’an, China, May 10-13, 2024.
- [C146] Qipan Wang, Tianxiang Zhu, **Yibo Lin**<sup>\*</sup>, Runsheng Wang and Ru Huang, “ATSim3D: Towards Accurate Thermal Simulator for Heterogeneous 3D IC Systems Considering Nonlinear Leakage and Conductivity”, IEEE/ACM International Symposium of EDA (ISEDA), Xi’an, China, May 10-13, 2024. (**Honorable Mention Paper Award**)
- [C145] Jing Mai, Jiarui Wang, Yifan Chen, Zizheng Guo, Xun Jiang, Yun Liang and **Yibo Lin**<sup>\*</sup>, “OpenPARF 3.0: Robust Multi-Electrostatics Based FPGA Macro Placement Considering Cascaded Macros Groups and Fence Regions”, IEEE/ACM International Symposium of EDA (ISEDA), Xi’an, China, May 10-13, 2024. (**Best Paper Award**)
- [C144] Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin**<sup>\*</sup>, Runsheng Wang and Ru Huang, “[CircuitNet 2.0: An Advanced Dataset for Promoting Machine Learning Innovations in Realistic Chip Design Environment](#)”, International Conference on Learning Representations (ICLR), Vienna, Austria, May 7-11, 2024.
- [C143] Zizheng Guo, Tsung-Wei Huang, Zhou Jin, Cheng Zhuo, **Yibo Lin**<sup>\*</sup>, Runsheng Wang and Ru Huang, “[Heterogeneous Static Timing Analysis with Advanced Delay Calculator](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.
- [C142] Haoyi Zhang, Xiaohan Gao, Zilong Shen, Jiahao Song, Xiaoxu Cheng, Xiyuan Tang, **Yibo**

- Lin\***, Runsheng Wang and Ru Huang, “[SAGERoute 2.0: Hierarchical Analog and Mixed Signal Routing Considering Versatile Routing Scenarios](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.
- [C141] Yuan Pu, Tinghuan Chen, Zhuolun He, Chen Bai, Haisheng Zheng, **Yibo Lin** and Bei Yu\*, “[IncreMacro: Incremental Macro Placement Refinement](#)”, ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024. (**Best Paper Nomination**)
- [C140] Yu Zhang, Yuan Pu, Fangzhou Liu, Peiyu Liao, Kaiyuan Chao, Keren Zhu, **Yibo Lin** and Bei Yu\*, “[Multi-Electrostatics Based Placement for Non-Integer Multiple-Height Cells](#)”, ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.
- [C139] Siting Liu, Jiayi Jiang, Zhuolun He, Ziyi Wang, **Yibo Lin** and Bei Yu\*, “[Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs](#)”, ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.
- [C138] Cheng-Hsiang Chiu, Zhicheng Xiong, Zizheng Guo, Tsung-Wei Huang\* and **Yibo Lin**, “[An Efficient Task-parallel Pipeline Programming Framework](#)”, International Conference on High-Performance Computing in Asia-Pacific Region (HPC Asia), Nagoya, Japan, Jan, 2024. (accepted)
- [J137] Peiyu Liao, Dawei Guo, Zizheng Guo, Siting Liu, Zhitang Chen, Wenlong Lv, **Yibo Lin\*** and Bei Yu\*, “[DREAMPlace 4.0: Timing-driven Placement with Momentum-based Net Weighting and Lagrangian-based Refinement](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- [J136] Zuodong Zhang, Zizheng Guo, **Yibo Lin\***, Runsheng Wang and Ru Huang, “[AVATAR: An Aging- and Variation-Aware Dynamic Timing Analyzer for Error-Efficient Computing](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- [J135] Binwu Zhu, Xinyun Zhang, **Yibo Lin**, Bei Yu and Martin Wong, “[DRC-SG 2.0: Efficient Design Rule Checking Script Generation via Key Information Extraction](#)”, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2023.
- [J134] Guannan Guo, Tsung-Wei Huang\*, **Yibo Lin**, Zizheng Guo, Sushma Yellapragada and Martin Wong, “[A GPU-accelerated Framework for Path-based Timing Analysis](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- [J133] Zhuomin Chai, Yuxiang Zhao, Wei Liu, **Yibo Lin\***, Runsheng Wang and Ru Huang, “[CircuitNet: An Open-Source Dataset for Machine Learning in VLSI CAD Applications with Improved Domain-Specific Evaluation Metric and Learning Strategies](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- [J132] Yufei Chen, Zizheng Guo, Runsheng Wang, Ru Huang, **Yibo Lin** and Cheng Zhuo, “[Dynamic Supply Noise Aware Timing Analysis With JIT Machine Learning Integration](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2023. (accepted)
- [J131] Zhixiong Di\*, Runzhe Tao, Jing Mai, Lin Chen and **Yibo Lin**, “[LEAPS: Topological-Layout-Adaptable Multi-Die FPGA Placement for Super Long Line Minimization](#)”, IEEE Transactions on Circuits and Systems I, Dec, 2023.

- [J130] Peiyu Liao, Yuxuan Zhao, Dawei Guo, **Yibo Lin** and Bei Yu\*, “[Analytical Die-to-Die 3D Placement With Bistratal Wirelength Model and GPU Acceleration](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2023.
- [C129] Yifan Chen, Zaiwen Wen, Yun Liang and **Yibo Lin\***, “[Stronger Mixed-Size Placement Backbone Considering Second-Order Information](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct 29-31, 2023.
- [J128] Xiaohan Gao, Haoyi Zhang, Siyuan Ye, Mingjie Liu, David Z. Pan, Linxiao Shen, Runsheng Wang, **Yibo Lin\*** and Ru Huang, “[Post-Layout Simulation Driven Analog Circuit Sizing](#)”, SCIENCE CHINA Information Sciences, Oct, 2023.
- [C127] Jing Mai, Jiaru Wang, Zhixiong Di, Guojie Luo, Yun Liang and **Yibo Lin\***, “[OpenPARF: An Open-Source Placement and Routing Framework for Large-Scale Heterogeneous FPGAs with Deep Learning Toolkit](#)”, International Conference on ASIC (ASICON), Nanjing, China, Oct, 2023. (**Invited paper**)
- [C126] Xun Jiang, Zizheng Guo, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin\***, Runsheng Wang and Ru Huang, “[Accelerating Routability and Timing Optimization with Open-Source AI4EDA Dataset CircuitNet and Heterogeneous Platforms](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct, 2023. (**Invited paper**)
- [C125] Kexing Zhou, Yun Liang\*, **Yibo Lin**, Runsheng Wang and Ru Huang, “[Khronos: Fusing Memory Access for Improved Hardware RTL Simulation](#)”, IEEE/ACM International Symposium on Microarchitecture (MICRO), Toronto, Canada, Oct, 2023.
- [J124] Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin\***, “[Multi-Electrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity, Clock Feasibility, and Timing Optimization](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sep, 2023.
- [C123] Zizheng Guo, Zuodong Zhang, Xun Jiang, Wuxi Li, **Yibo Lin\***, Runsheng Wang and Ru Huang, “General-Purpose Gate-Level Simulation with Partition-Agnostic Parallelism”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.
- [C122] Qipan Wang, Ping Liu, Ligguo Jiang, Mingjie Liu, **Yibo Lin\***, Runsheng Wang and Ru Huang, “MTL-Designer: An Integrated Flow for Analysis and Synthesis of Microstrip Transmission Line”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.
- [C121] Peiyu Liao, Hongduo Liu, **Yibo Lin\***, Bei Yu\* and Martin Wong, “On a Moreau Envelope Wirelength Model for Analytical Global Placement”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.
- [C120] Siting Liu, Ziyi Wang, Fangzhou Liu, **Yibo Lin**, Bei Yu and Martin Wong\*, “Concurrent Sign-off Timing Optimization via Deep Steiner Points Refinement”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.
- [C119] Su Zheng, Lancheng Zou, Siting Liu, **Yibo Lin**, Bei Yu and Martin Wong\*, “Mitigating Distribution Shift for Congestion Optimization in Global Placement”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.



- [C118] Yu Zhang, Yifan Chen, Zhonglin Xie, Hong Xu, Zaiwen Wen, **Yibo Lin\*** and Bei Yu\*, “LRSDP: Low-Rank SDP for Triple Patterning Lithography Layout Decomposition”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.
- [J117] Zizheng Guo, Tsung-Wei Huang and **Yibo Lin\***, “[Accelerating Static Timing Analysis using CPU-GPU Heterogeneous Parallelism](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2023.
- [C116] Yuxiang Zhao, Zhuomin Chai, **Yibo Lin\***, Runsheng Wang and Ru Huang, “[HybridNet: Dual-Branch Fusion of Geometrical and Topological Views for VLSI Congestion Prediction](#)”, IEEE/ACM International Symposium of EDA (ISEDA), Nanjing, China, May 8-11, 2023.
- [C115] Haoyi Zhang, Xiaohan Gao, **Yibo Lin\***, Runsheng Wang and Ru Huang, “[Multi-Scenario Analog and Mixed-Signal Circuit Routing with Agile Human Interaction](#)”, IEEE/ACM International Symposium of EDA (ISEDA), Nanjing, China, May 8-11, 2023.
- [C114] Haoyi Zhang, Xiaohan Gao, Haoyang Luo, Jiahao Song, Xiyuan Tang, Junhua Liu, **Yibo Lin\***, Runsheng Wang and Ru Huang, “[SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Apr 17-19, 2023. (**Best Paper Award**)
- [C113] Zuodong Zhang, Meng Li\*, **Yibo Lin**, Runsheng Wang and Ru Huang, “[READ: Reliability-Enhanced Accelerator Dataflow Optimization using Critical Input Pattern Reduction](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Apr 17-19, 2023.
- [J112] **Yibo Lin**, Avi Ziv and Haoxing Ren, “[Introduction to the Special Issue on Machine Learning for CAD/EDA](#)”, ACM Transactions on Design Automation of Electronic Systems (TODAES), Mar, 2023.
- [C111] Yifan Chen, Jing Mai, Xiaohan Gao, Muhan Zhang and **Yibo Lin\***, “[MacroRank: Ranking Macro Placement Solutions Leveraging Translation Equivariancy](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 16-19, 2023.
- [C110] Jiarui Wang, Jing Mai, Zhixiong Di and **Yibo Lin\***, “[A Robust FPGA Router with Concurrent Intra-CLB Rerouting](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 16-19, 2023.
- [J109] Junchi Yan\*, Xianglong Lyu, Ruoyu Cheng and **Yibo Lin**, “Towards Machine Learning for Placement and Routing in Chip Design: a Methodological Overview”, arXiv preprint, 2022.
- [C108] Zizheng Guo, Feng Gu and **Yibo Lin\***, “[GPU-Accelerated Rectilinear Steiner Tree Generation](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 01-03, 2022.
- [C107] Qipan Wang, Xiaohan Gao, **Yibo Lin\***, Runsheng Wang and Ru Huang, “[DeePEB: A Neural Partial Differential Equation Solver for Post Exposure Baking Simulation in Lithography](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 01-03, 2022. (**Best Paper Nomination**)



- [C106] **Yibo Lin\***, Xiaohan Gao, Haoyi Zhang, Runsheng Wang and Ru Huang, “[Intelligent and Interactive Analog Layout Design Automation](#)”, IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Nanjing, China, Oct 25-28, 2022. (**Invited paper**)
- [J105] Xinfa Zhang, Zuodong Zhang, **Yibo Lin\***, Zhigang Ji\*, Runsheng Wang and Ru Huang, “[Efficient Aging-Aware Standard Cell Library Characterization Based on Sensitivity Analysis](#)”, IEEE Transactions on Circuits and Systems II: Express Briefs, Oct, 2022.
- [J104] Siting Liu, Yuan Pu, Peiyu Liao, Hongzhong Wu, Rui Zhang, Zhitang Chen, Wenlong Lv, **Yibo Lin\*** and Bei Yu\*, “[FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2022.
- [C103] Binwu Zhu, Xinyun Zhang, **Yibo Lin**, Bei Yu\* and Martin Wong, “[Efficient Design Rule Checking Script Generation via Key Information Extraction](#)”, ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), Snowbird, Utah, Sep 12-13, 2022.
- [J102] Zhuomin Chai, Yuxiang Zhao, **Yibo Lin\***, Wei Liu, Runsheng Wang and Ru Huang, “[Circuit-Net: An Open-Source Dataset for Machine Learning Applications in Electronic Design Automation \(EDA\)](#)”, SCIENCE CHINA Information Sciences, Sep, 2022.
- [C101] Jing Mai, Yibai Meng, Zhixiong Di and **Yibo Lin\***, “[Multi-Electrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity and Clock Feasibility](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.
- [C100] Zizheng Guo and **Yibo Lin\***, “[Differentiable-Timing-Driven Global Placement](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.
- [C99] Zizheng Guo, Mingjie Liu, Jiaqi Gu, Shuhan Zhang, David Z. Pan and **Yibo Lin\***, “[A Timing Engine Inspired Graph Neural Network Model for Pre-Routing Slack Prediction](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.
- [C98] Zuodong Zhang, Zizheng Guo, **Yibo Lin\***, Runsheng Wang and Ru Huang, “[AVATAR: An Aging- and Variation-Aware Dynamic Timing Analyzer for Application-based DVAFS](#)”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.
- [C97] Bowen Wang, Guibao Shen, Dong Li, Jianye Hao, Wulong Liu, Yu Huang, Hongzhong Wu, **Yibo Lin**, Guangyong Chen and Pheng Ann Heng, “LHNN: Lattice Hypergraph Neural Network for VLSI Congestion Prediction”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.
- [J96] Xiaohan Gao, Haoyi Zhang, Mingjie Liu, Linxiao Shen, David Z. Pan, **Yibo Lin\***, Runsheng Wang and Ru Huang, “[Interactive Analog Layout Editing with Instant Placement and Routing Legalization](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2022.
- [C95] Zuodong Zhang, Zizheng Guo, **Yibo Lin\***, Runsheng Wang and Ru Huang, “[EventTimer: Fast and Accurate Event-Based Dynamic Timing Analysis](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022.

- [C94] Siting Liu, Peiyu Liao, Zhitang Chen, Wenlong Lv, **Yibo Lin\*** and Bei Yu\*, “[FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022. (**Best Paper Award**)
- [C93] Peiyu Liao, Siting Liu, Zhitang Chen, Wenlong Lv, **Yibo Lin\*** and Bei Yu\*, “[DREAMPlace 4.0: Timing-driven Global Placement with Momentum-based Net Weighting](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022.
- [C92] Haoyu Yang, Kit Fung, Yuxuan Zhao, **Yibo Lin** and Bei Yu\*, “[Mixed-Cell-Height Legalization on CPU-GPU Heterogeneous Systems](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022.
- [C91] Xun Jiang, **Yibo Lin** and Zhongfeng Wang\*, “[FPGA-Accelerated Maze Routing Kernel for VLSI Designs](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Virtual Conference, Jan 17-20, 2022.
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- [B1] **Yibo Lin** and David Z. Pan, “[Machine Learning in Physical Verification, Mask Synthesis, and Physical Design](#)”, Machine Learning in VLSI Computer-Aided Design, Springer, 2018, edited by Abe Elfedel, Duane Boning and Xin Li. (**Invited Book Chapter**)

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- [J52] Hao Chen, Mingjie Liu, Biying Xu, Keren Zhu, Xiyuan Tang, Shaolan Li, **Yibo Lin**, Nan Sun and David Z. Pan\*, “[MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII](#)”, IEEE Design & Test, Sep, 2020.
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- [C49] Mohamed Baker Alawieh, Wuxi Li, **Yibo Lin**, Love Singhal, Mahesh Iyer and David Z. Pan\*, “High-Definition Routing Congestion Prediction for Large-Scale FPGAs”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jan 13-16, 2020.
- [C48] Wuxi Li, **Yibo Lin** and David Z. Pan\*, “[elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Westminster, CO, Nov 4-7, 2019.
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- [J44] **Yibo Lin**, Meng Li, Yuki Watanabe, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima and David Z. Pan\*, “[Data Efficient Lithography Modeling with Transfer Learning and Active Data Selection](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2019.
- [C43] Wei Li, Yuzhe Ma, Qi Sun, **Yibo Lin**, Iris Hui-Ru Jiang, Bei Yu and David Z. Pan, “[OpenMPL: An Open Source Layout Decomposer](#)”, International Conference on ASIC (ASICON), Chongqing, China, Oct, 2019. (**Invited paper**)
- [C42] **Yibo Lin**, Shounak Dhar, Wuxi Li, Haoxing Ren, Brucek Khailany and David Z. Pan\*, “[DREAM-Place: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement](#)”, ACM/IEEE Design Automation Conference (DAC), Las Vegas, NV, Jun 2-6, 2019. (**Best Paper Award**)
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- [C40] Biying Xu, **Yibo Lin**, Xiyuan Tang, Shaolan Li, Linxiao Shen, Nan Sun and David Z. Pan\*, “[WellGAN: Generative-Adversarial-Network-Guided Well Generation for Analog/Mixed-Signal Circuit Layout](#)”, ACM/IEEE Design Automation Conference (DAC), Las Vegas, NV, Jun 2-6, 2019.
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- [C38] **Yibo Lin**, Zhao Song and Lin F. Yang\*, “[Towards a Theoretical Understanding of Hashing-Based Neural Nets](#)”, International Conference on Artificial Intelligence and Statistics (AISTATS), Okinawa, Japan, Apr 16-18, 2019.
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- [C30] **Yibo Lin**, Mohamed Baker Alawieh, Wei Ye and David Z. Pan\*, “[Machine Learning for Yield Learning and Optimization](#)”, IEEE International Test Conference (ITC), Phoenix, Arizona, Oct, 2018. (**Invited paper**)
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- [J28] Meng Li, Bei Yu, **Yibo Lin**, Xiaoqing Xu, Wuxi Li and David Z Pan, “[A practical split manufacturing framework for trojan prevention via simultaneous wire lifting and cell insertion](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2018.
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- [C21] Che-Lun Hsu, Shaofeng Guo, **Yibo Lin**, Xiaoqing Xu, Meng Li, Runsheng Wang, Ru Huang and David Z Pan, “[Layout-dependent aging mitigation for critical path timing](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jeju, Korea, Jan 22-25, 2018.
- [C20] **Yibo Lin**, Peter Debacker, Darko Trivkovic, Ryoung-han Kim, Praveen Raghavan and David Z. Pan\*, “[Patterning Aware Design Optimization of Selective Etching in N5 and Beyond](#)”, IEEE International Conference on Computer Design (ICCD), Boston, MA, Nov 5-8, 2017.
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