林亦波

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研究方向

面向超大规模集成电路设计自动化的建模和优化、深度学习及其应用、异构计算

教育经历

德克萨斯大学奥斯汀分校 *2013 年 8 月 – 2018 年 5 月*

博士学位, 电子与计算机工程系

指导老师: David Z. Pan

博士毕业论文: "Bridging Design and Manufacturing Gap through Machine Learning and Machine-Generated Layout"

上海交通大学 *2009 年 9 月 – 2013 年 6 月*

学士学位，微电子学院

工作经历

北京大学 (Peking University) *2019 年 7 月 – 现在*

助理教授

集成电路学院设计自动化与计算系统系 (自 2021 年 11 月)

信息科学技术学院高能效计算与应用中心

德克萨斯大学奥斯汀分校 (UT Austin) *2018 年 6 月 – 2019 年 6 月*

博后

授课经历

主讲	集成电路工程算法	研究生课, 2023-2024 年春
主讲	设计自动化与计算系统	研究生课, 2022-2024 年秋
主讲	芯片设计自动化与智能优化	本科生课, 2021-2022 年春, 2023-2024 年秋
主讲	计算概论 B	本科生课, 2020-2022 年秋

奖项及荣誉

最佳论文 (x1) & Honorable Mention (x1)	ISEDA	2024 年
Early Career Award (每年仅 1 位)	中国计算机协会集成电路专委	2023 年
首届最佳审稿人奖	ICCAD	2023 年
最佳论文 (4/205)	DATE	2023 年
最佳论文 (4/249)	DATE	2022 年
最佳论文提名	ICCAD	2022 年

最佳论文 (2/3495, 4 年总和)	TCAD	2021 年
最佳论文	ISPD	2020 年
最佳论文提名	ASPDAC	2020 年
最佳论文 (1/201) & 提名 (5/201)	DAC	2019 年
最佳论文提名	ISPD	2019 年
首届最佳论文	Integration, the VLSI Journal	2018 年
Graduate Continuing Fellowship	德克萨斯大学奥斯汀分校	2017 年
Franco Cerrina Memorial 最佳学生论文	SPIE	2016 年
A. Richard Newton Young Student Fellow	DAC	2014 年
国家奖学金	上海交通大学	2012 年
三星奖学金	上海交通大学	2011 年
二等奖学金	上海交通大学	2010 年

学术服务

技术程序委员会成员

- ACM/IEEE Design Automation Conference (DAC): 2020
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD): 2018, 2019, 2020, 2021
- IEEE International Conference on Computer Design (ICCD): 2019
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC): 2021, 2022
- ACM International Symposium on Physical Design (ISPD): 2020
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD): 2021
- ACM Great Lakes Symposium on VLSI (GLVLSI): 2024
- Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI): 2021
- IEEE Electron Devices Technology and Manufacturing Conference (EDTM): 2021
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS): 2022.

期刊审稿人

- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Computers (TC)
- ACM Transaction on Design Automation of Electronic Systems (TODAES)
- SPIE Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)
- Elsevier, Integration, the VLSI Journal (Integration)

期刊编辑

- Guest Editor @ ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2022
- Guest Editor @ ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2024

- Associate Editor @ ACM Transaction on Design Automation of Electronic Systems (TODAES), 2024 – 现在
- Associate Editor @ Elsevier Integration, the VLSI Journal (Integration), 2024 – 现在

执行委员会成员

- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD) 2021, financial chair
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD) 2022, financial chair
- IEEE International Symposium of Electronics Design Automation (ISEDA) 2023, panel chair
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD) 2023, financial chair
- IEEE International Symposium of Electronics Design Automation (ISEDA) 2024, panel chair
- ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD) 2024, program chair

出版物

书籍章节

[B3] **Yibo Lin**, Zizheng Guo and Jing Mai, "Deep Learning Framework for Placement", Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)

[B2] Haoyu Yang, **Yibo Lin** and Bei Yu, "Machine Learning for Mask Synthesis and Verification", Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)

会议及期刊论文 (标 * 表示通讯作者)

[C165] Che Chang, Boyang Zhang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yi-Hua Chung, Wan-Luan Lee, Zizheng Guo, **Yibo Lin** and Tsung-Wei Huang*, "PathGen: An Efficient Parallel Critical Path Generation Algorithm", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan, 2025. (accepted)

[J164] Yuxuan Zhao, Peiyu Liao, Siting Liu, Jiaxi Jiang, **Yibo Lin** and Bei Yu*, "Analytical Heterogeneous Die-to-Die 3D Placement With Macros", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024. (accepted)

[J163] Xun Jiang, Jiarui Wang, Jing Mai, Zhixiong Di and **Yibo Lin***, "A Robust FPGA Router With Optimization of High-Fanout Nets and Intra-CLB Connections", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024. (accepted)

[C162] Qipan Wang, Xueqing Li, Tianyu Jia, **Yibo Lin***, Runsheng Wang and Ru Huang, "AT-Place2.5D: Analytical Thermal-Aware Chiplet Placement Framework for Large-Scale 2.5D-IC", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)

[C161] Chunyuan Zhao, Zizheng Guo, Rui Wang, Zaiwen Wen, Yun Liang and **Yibo Lin***, "HeLEM-GR: Heterogeneous Global Routing with Linearized Exponential Multiplier Method", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)

[C160] Zizheng Guo, Zuodong Zhang, Wuxi Li, Tsung-Wei Huang, Xizhe Shi, Yufan Du, **Yibo Lin***, Runsheng Wang and Ru Huang, "HeteroExcept: A CPU-GPU Heterogeneous Algorithm to Accelerate Exception-aware Static Timing Analysis", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)

[C159] Xiaohan Gao, Haoyi Zhang, Bingyan Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, "Joint Placement Optimization for Hierarchical Analog/Mixed-Signal Circuits", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)

[C158] Yufan Du, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "Fusion of Global Placement and Gate Sizing with Differentiable Optimization", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)

[C157] Tianxiang Zhu, Qipan Wang, **Yibo Lin***, Runsheng Wang and Ru Huang, "FaStTherm: Fast and Stable Full-Chip Transient Thermal Predictor Considering Nonlinear Effects", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)

[C156] Jing Mai, Zuodong Zhang, **Yibo Lin***, Runsheng Wang and Ru Huang, "MORPH: More Robust ASIC Placement for Hybrid Region Constraint Management", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), New Jersey, Oct, 2024. (accepted)

[J155] Tsung-Yi Ho, Sadaf Khan, Jinwei Liu, Yi Liu, Zhengyuan Shi, Ziyi Wang, Qiang Xu*, Evangeline F.Y. Young, Bei Yu, Ziyang Zheng, Binwu Zhu, Keren Zhu, Yiqi Che, Yun Liang, **Yibo Lin**, Guojie Luo, Guangyu Sun, Runsheng Wang, Xinming Wei, Chenhao Xue, Haoyi Zhang, Zuodong Zhang, Yuxiang Zhao, Sunan Zou, Lei Chen, Yu Huang, Min Li, Dimitrios Tsaras, Mingxuan Yuan, Hui-Ling Zhen, Zhufei Chu, Wenji Fang, Xingquan Li and Zhiyao Xie, "Large Circuit Models: Opportunities and Challenges", Science China Information Sciences, Sep, 2024.

[C154] Jiarui Wang, Xun Jiang and **Yibo Lin***, "Top-Level Routing for Multiply-Instantiated Blocks with Topology Hashing", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C153] Yufan Du, Zizheng Guo, Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, "PowPrediCT: Cross-Stage Power Prediction with Circuit-Transformation-Aware Learning", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C152] Haoyi Zhang, Jiahao Song, Xiaohan Gao, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, "EasyACIM: An End-to-End Automated Analog CIM with Synthesizable Architecture and Agile Design Space Exploration", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C151] Zichen Kong, Xiyuan Tang*, Wei Shi, Yiheng Du, **Yibo Lin** and Yuan Wang, "PVTSizing: A TuRBO-RL-Based Batch-Sampling Optimization Framework for PVT-Robust Analog Circuit Synthesis", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C150] Yuan Pu, Fangzhou Liu, Yu Zhang, Zhuolun He, Kai-Yuan Chao, **Yibo Lin** and Bei Yu*, "Lesyn: Placement-aware Logic Resynthesis for Non-Integer Multiple-Cell-Height Designs", ACM/IEEE

Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C149] Wan Luan Lee, Dian-Lun Lin, Tsung-Wei Huang*, Shui Jiang, Tsung-Yi Ho, **Yibo Lin** and Bei Yu, "G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 23-27, 2024.

[C148] Haoran Lu, Y Ge, ong , Xun Jiang, Jiacheng Sun, Wanyue Peng, Rui Guo, Ming Li, **Yibo Lin**, Runsheng Wang, Heng Wu* and Ru Huang, "First Experimental Demonstration of Self-Aligned Flip FET (FFET): A Breakthrough Stacked Transistor Technology with 2.5T Design, Dual-Side Active and Interconnects", IEEE Symposium on VLSI Technology and Circuits (VLSI), Honolulu, HI, Jun 16-20, 2024.

[C147] Xiaohan Gao, Haoyi Zhang, Zhu Pan, **Yibo Lin***, Runsheng Wang and Ru Huang, "Migrating Standard Cells for Multiple Drive Strengths by Routing Imitation", IEEE/ACM International Symposium of EDA (ISEDA), Xi'an, China, May 10-13, 2024.

[C146] Qipan Wang, Tianxiang Zhu, **Yibo Lin***, Runsheng Wang and Ru Huang, "ATSim3D: Towards Accurate Thermal Simulator for Heterogeneous 3D IC Systems Considering Nonlinear Leakage and Conductivity", IEEE/ACM International Symposium of EDA (ISEDA), Xi'an, China, May 10-13, 2024. (**Honorable Mention**)

[C145] Jing Mai, Jiarui Wang, Yifan Chen, Zizheng Guo, Xun Jiang, Yun Liang and **Yibo Lin***, "OpenPARF 3.0: Robust Multi-Electrostatics Based FPGA Macro Placement Considering Cascaded Macros Groups and Fence Regions", IEEE/ACM International Symposium of EDA (ISEDA), Xi'an, China, May 10-13, 2024. (**Best Paper Award**)

[C144] Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, "CircuitNet 2.0: An Advanced Dataset for Promoting Machine Learning Innovations in Realistic Chip Design Environment", International Conference on Learning Representations (ICLR), Vienna, Austria, May 7-11, 2024.

[C143] Zizheng Guo, Tsung-Wei Huang, Zhou Jin, Cheng Zhuo, **Yibo Lin***, Runsheng Wang and Ru Huang, "Heterogeneous Static Timing Analysis with Advanced Delay Calculator", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.

[C142] Haoyi Zhang, Xiaohan Gao, Zilong Shen, Jiahao Song, Xiaoxu Cheng, Xiyuan Tang, **Yibo Lin***, Runsheng Wang and Ru Huang, "SAGERoute 2.0: Hierarchical Analog and Mixed Signal Routing Considering Versatile Routing Scenarios", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.

[C141] Yuan Pu, Tinghuan Chen, Zhuolun He, Chen Bai, Haisheng Zheng, **Yibo Lin** and Bei Yu*, "IncreMacro: Incremental Macro Placement Refinement", ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024. (**Best Paper Nomination**)

[C140] Yu Zhang, Yuan Pu, Fangzhou Liu, Peiyu Liao, Kaiyuan Chao, Keren Zhu, **Yibo Lin** and Bei Yu*, "Multi-Electrostatics Based Placement for Non-Integer Multiple-Height Cells", ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.

[C139] Siting Liu, Jiaxi Jiang, Zhuolun He, Ziyi Wang, **Yibo Lin** and Bei Yu*, "Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs", ACM International

Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.

[C138] Cheng-Hsiang Chiu, Zhicheng Xiong, Zizheng Guo, Tsung-Wei Huang* and **Yibo Lin**, "An Efficient Task-parallel Pipeline Programming Framework", International Conference on High-Performance Computing in Asia-Pacific Region (HPC Asia), Nagoya, Japan, Jan, 2024. (accepted)

[J137] Peiyu Liao, Dawei Guo, Zizheng Guo, Siting Liu, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, "DREAMPlace 4.0: Timing-driven Placement with Momentum-based Net Weighting and Lagrangian-based Refinement", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.

[J136] Zuodong Zhang, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "AVATAR: An Aging- and Variation-Aware Dynamic Timing Analyzer for Error-Efficient Computing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.

[J135] Binwu Zhu, Xinyun Zhang, **Yibo Lin**, Bei Yu and Martin Wong, "DRC-SG 2.0: Efficient Design Rule Checking Script Generation via Key Information Extraction", ACM Transactions on Design Automation of Electronic Systems (TODAES), 2023.

[J134] Guannan Guo, Tsung-Wei Huang*, **Yibo Lin**, Zizheng Guo, Sushma Yellapragada and Martin Wong, "A GPU-accelerated Framework for Path-based Timing Analysis", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.

[J133] Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "Accelerating Static Timing Analysis using CPU-GPU Heterogeneous Parallelism", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.

[J132] Zhuomin Chai, Yuxiang Zhao, Wei Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, "CircuitNet: An Open-Source Dataset for Machine Learning in VLSI CAD Applications with Improved Domain-Specific Evaluation Metric and Learning Strategies", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.

[J131] Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin***, "Multi-Electrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity, Clock Feasibility, and Timing Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.

[J130] Yufei Chen, Zizheng Guo, Runsheng Wang, Ru Huang, **Yibo Lin** and Cheng Zhuo, "Dynamic Supply Noise Aware Timing Analysis With JIT Machine Learning Integration", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2023. (accepted)

[J129] Zhixiong Di*, Runzhe Tao, Jing Mai, Lin Chen and **Yibo Lin**, "LEAPS: Topological-Layout-Adaptable Multi-Die FPGA Placement for Super Long Line Minimization", IEEE Transactions on Circuits and Systems I, Dec, 2023.

[J128] Peiyu Liao, Yuxuan Zhao, Dawei Guo, **Yibo Lin** and Bei Yu*, "Analytical Die-to-Die 3D Placement With Bistratal Wirelength Model and GPU Acceleration", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2023.

[J127] Xiaohan Gao, Haoyi Zhang, Siyuan Ye, Mingjie Liu, David Z. Pan, Linxiao Shen, Runsheng

Wang, **Yibo Lin*** and Ru Huang, "Post-Layout Simulation Driven Analog Circuit Sizing", SCIENCE CHINA Information Sciences, Oct, 2023.

[C126] Jing Mai, Jiaru Wang, Zhixiong Di, Guojie Luo, Yun Liang and **Yibo Lin***, "OpenPARF: An Open-Source Placement and Routing Framework for Large-Scale Heterogeneous FPGAs with Deep Learning Toolkit", International Conference on ASIC (ASICON), Nanjing, China, Oct, 2023. (**Invited paper**)

[C125] Yifan Chen, Zaiwen Wen, Yun Liang and **Yibo Lin***, "Stronger Mixed-Size Placement Backbone Considering Second-Order Information", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct, 2023.

[C124] Xun Jiang, Zizheng Guo, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Runsheng Wang and Ru Huang, "Accelerating Routability and Timing Optimization with Open-Source AI4EDA Dataset CircuitNet and Heterogeneous Platforms", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct, 2023. (**Invited paper**)

[C123] Kexing Zhou, Yun Liang*, **Yibo Lin**, Runsheng Wang and Ru Huang, "Khronos: Fusing Memory Access for Improved Hardware RTL Simulation", IEEE/ACM International Symposium on Microarchitecture (MICRO), Toronto, Canada, Oct, 2023.

[C122] Zizheng Guo, Zuodong Zhang, Xun Jiang, Wuxi Li, **Yibo Lin***, Runsheng Wang and Ru Huang, "General-Purpose Gate-Level Simulation with Partition-Agnostic Parallelism", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C121] Qipan Wang, Ping Liu, Ligguo Jiang, Mingjie Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, "MTL-Designer: An Integrated Flow for Analysis and Synthesis of Microstrip Transmission Line", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C120] Peiyu Liao, Hongduo Liu, **Yibo Lin***, Bei Yu* and Martin Wong, "On a Moreau Envelope Wirelength Model for Analytical Global Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C119] Siting Liu, Ziyi Wang, Fangzhou Liu, **Yibo Lin**, Bei Yu and Martin Wong*, "Concurrent Sign-off Timing Optimization via Deep Steiner Points Refinement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C118] Su Zheng, Lancheng Zou, Siting Liu, **Yibo Lin**, Bei Yu and Martin Wong*, "Mitigating Distribution Shift for Congestion Optimization in Global Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C117] Yu Zhang, Yifan Chen, Zhonglin Xie, Hong Xu, Zaiwen Wen, **Yibo Lin*** and Bei Yu*, "LRSDP: Low-Rank SDP for Triple Patterning Lithography Layout Decomposition", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.

[C116] Yuxiang Zhao, Zhuomin Chai, **Yibo Lin***, Runsheng Wang and Ru Huang, "HybridNet: Dual-Branch Fusion of Geometrical and Topological Views for VLSI Congestion Prediction", IEEE/ACM International Symposium of EDA (ISEDA), Nanjing, China, May 8-11, 2023.

[C115] Haoyi Zhang, Xiaohan Gao, **Yibo Lin***, Runsheng Wang and Ru Huang, "Multi-Scenario Analog and Mixed-Signal Circuit Routing with Agile Human Interaction", IEEE/ACM International

Symposium of EDA (ISEDA), Nanjing, China, May 8-11, 2023.

[C114] Haoyi Zhang, Xiaohan Gao, Haoyang Luo, Jiahao Song, Xiyuan Tang, Junhua Liu, **Yibo Lin***, Runsheng Wang and Ru Huang, "SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Apr 17-19, 2023. (**Best Paper Award**)

[C113] Zuodong Zhang, Meng Li*, **Yibo Lin**, Runsheng Wang and Ru Huang, "READ: Reliability-Enhanced Accelerator Dataflow Optimization using Critical Input Pattern Reduction", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Apr 17-19, 2023.

[J112] **Yibo Lin**, Avi Ziv and Haoxing Ren, "Introduction to the Special Issue on Machine Learning for CAD/EDA", ACM Transactions on Design Automation of Electronic Systems (TODAES), Mar, 2023.

[C111] Yifan Chen, Jing Mai, Xiaohan Gao, Muhan Zhang and **Yibo Lin***, "MacroRank: Ranking Macro Placement Solutions Leveraging Translation Equivariancy", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 16-19, 2023.

[C110] Jiarui Wang, Jing Mai, Zhixiong Di and **Yibo Lin***, "A Robust FPGA Router with Concurrent Intra-CLB Rerouting", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 16-19, 2023.

[J109] Junchi Yan*, Xianglong Lyu, Ruoyu Cheng and **Yibo Lin**, "Towards Machine Learning for Placement and Routing in Chip Design: a Methodological Overview", arXiv preprint, 2022.

[C108] Zizheng Guo, Feng Gu and **Yibo Lin***, "GPU-Accelerated Rectilinear Steiner Tree Generation", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 01-03, 2022.

[C107] Qipan Wang, Xiaohan Gao, **Yibo Lin***, Runsheng Wang and Ru Huang, "DeePEB: A Neural Partial Differential Equation Solver for Post Exposure Baking Simulation in Lithography", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 01-03, 2022. (**Best Paper Nomination**)

[C106] **Yibo Lin***, Xiaohan Gao, Haoyi Zhang, Runsheng Wang and Ru Huang, "Intelligent and Interactive Analog Layout Design Automation", IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Nanjing, China, Oct 25-28, 2022. (**Invited paper**)

[J105] Xinfa Zhang, Zuodong Zhang, **Yibo Lin***, Zhigang Ji*, Runsheng Wang and Ru Huang, "Efficient Aging-Aware Standard Cell Library Characterization Based on Sensitivity Analysis", IEEE Transactions on Circuits and Systems II: Express Briefs, Oct, 2022.

[J104] Siting Liu, Yuan Pu, Peiyu Liao, Hongzhong Wu, Rui Zhang, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, "FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2022.

[C103] Binwu Zhu, Xinyun Zhang, **Yibo Lin**, Bei Yu* and Martin Wong, "Efficient Design Rule Checking Script Generation via Key Information Extraction", ACM/IEEE Workshop on Machine

Learning for CAD (MLCAD), Snowbird, Utah, Sep 12-13, 2022.

[J102] Zhuomin Chai, Yuxiang Zhao, **Yibo Lin***, Wei Liu, Runsheng Wang and Ru Huang, "CircuitNet: An Open-Source Dataset for Machine Learning Applications in Electronic Design Automation (EDA)", SCIENCE CHINA Information Sciences, Sep, 2022.

[C101] Jing Mai, Yibai Meng, Zhixiong Di and **Yibo Lin***, "Multi-Electrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity and Clock Feasibility", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

[C100] Zizheng Guo and **Yibo Lin***, "Differentiable-Timing-Driven Global Placement", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

[C99] Zizheng Guo, Mingjie Liu, Jiaqi Gu, Shuhan Zhang, David Z. Pan and **Yibo Lin***, "A Timing Engine Inspired Graph Neural Network Model for Pre-Routing Slack Prediction", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

[C98] Zuodong Zhang, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "AVATAR: An Aging- and Variation-Aware Dynamic Timing Analyzer for Application-based DVAFS", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

[C97] Bowen Wang, Guibao Shen, Dong Li, Jianye Hao, Wulong Liu, Yu Huang, Hongzhong Wu, **Yibo Lin**, Guangyong Chen and Pheng Ann Heng, "LHNN: Lattice Hypergraph Neural Network for VLSI Congestion Prediction", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 10-14, 2022.

[J96] Xiaohan Gao, Haoyi Zhang, Mingjie Liu, Linxiao Shen, David Z. Pan, **Yibo Lin***, Runsheng Wang and Ru Huang, "Interactive Analog Layout Editing with Instant Placement and Routing Legalization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2022.

[C95] Zuodong Zhang, Zizheng Guo, **Yibo Lin***, Runsheng Wang and Ru Huang, "EventTimer: Fast and Accurate Event-Based Dynamic Timing Analysis", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022.

[C94] Siting Liu, Peiyu Liao, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, "FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022. (**Best Paper Award**)

[C93] Peiyu Liao, Siting Liu, Zhitang Chen, Wenlong Lv, **Yibo Lin*** and Bei Yu*, "DREAMPlace 4.0: Timing-driven Global Placement with Momentum-based Net Weighting", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022.

[C92] Haoyu Yang, Kit Fung, Yuxuan Zhao, **Yibo Lin** and Bei Yu*, "Mixed-Cell-Height Legalization on CPU-GPU Heterogeneous Systems", IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Antwerp, Belgium, Mar 14-23, 2022.

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[C90] Kexing Zhou, Zizheng Guo, Tsung-Wei Huang and **Yibo Lin***, "Efficient Critical Paths Search Algorithm using Mergeable Heap", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Virtual Conference, Jan 17-20, 2022.

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[C5] **Yibo Lin**, Bei Yu, Yi Zou, Zhuo Li, Charles J Alpert and David Z. Pan*, "Stitch aware detailed placement for multiple e-beam lithography", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Macau, China, Jan 25-28, 2016.

[C4] **Yibo Lin**, Bei Yu, Biying Xu and David Z. Pan*, "Triple patterning aware detailed placement toward zero cross-row middle-of-line conflict", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, Nov 2-6, 2015.

[C3] **Yibo Lin**, Bei Yu and David Z. Pan*, "High performance dummy fill insertion with coupling and uniformity constraints", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 7-11, 2015.

[C2] David Z. Pan*, Lars Liebmann, Bei Yu, Xiaoqing Xu and **Yibo Lin**, "Pushing multiple patterning in sub-10nm: are we ready?", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun 7-11, 2015. (**Invited Paper**)

[J1] Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, **Yibo Lin**, Zhuo Li, Charles Alpert and David Z. Pan*, "Methodology for standard cell compliance and detailed placement for triple patterning lithography", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May, 2015.

特邀报告

国际会议特邀报告

[T11] "Analyzing Timing in Shorter Time: A Journey through Heterogeneous Parallelism for Static Timing Analysis", in IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Zhuhai, China, Oct 22-25, 2024.

[T10] "Agile Analog IC Design: from Layout Automation to Circuit Synthesis", in IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Chengdu, China, Aug 28-30, 2024.

[T9] "Workshop Talk: Empowering Physical Design of VLSI Circuits with Deep Learning: from Modeling to Optimization", in International Symposium on Computer Architecture (ISCA), Buenos Aires, Argentina, Jun 29-Jul 3, 2024.

[T8] "Accelerating Routability and Timing Optimization with Open-Source AI4EDA Dataset CircuitNet and Heterogeneous Platforms", in ACM/IEEE International Conference on Computer-Aided Design (ICCAD), San Francisco, Oct 29-Nov 2, 2023.

[T7] "Tutorial: Deep Learning Enabled Timing Optimization in Physical Design", in ACM/IEEE Design Automation Conference (DAC), San Francisco, Jul 9-13, 2023.

[T6] "Timing Analysis and Optimization on Heterogeneous CPU-GPU Platforms", in International Workshop on Logic & Synthesis (IWLS), Virtual, Jul 18-21, 2022.

[T5] "DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement", in ACM/IEEE Design Automation WebiNar (DAWN), Virtual, Apr 11-12, 2022.

[T4] "DREAMPlace 3.X: Exploring Advanced Constraints and Multi-GPU Acceleration", in China Semiconductor Technology International Conference (CSTIC), Shanghai, China, Mar 14-15, 2021.

[T3] "Deep Learning for Mask Synthesis and Verification: A Survey", in IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 18-21, 2021.

[T2] "Tutorial: GPU Acceleration in VLSI Back-end Design: Overview and Case Studies", in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Virtual, Nov 2-5, 2020.

[T1] "DREAMPlace 2.0: Open-Source GPU-Accelerated Global and Detailed Placement for Large-Scale VLSI Designs", in China Semiconductor Technology International Conference (CSTIC), Shanghai, China, Jun 26, 2020.

国内会议特邀报告

[T12] " 深度学习赋能集成电路物理设计自动化：从建模到优化方法", 中国计算机大会（CNCC）, 横店, Oct 24-27, 2024.

[T11] "Agile Analog IC Design: from Layout Automation to Circuit Synthesis", 华为模拟设计自动化技术峰会, Aug 19, 2024.

[T10] "AI 赋能集成电路物理设计自动化：数据集，建模和优化方法", 全国超导薄膜和超导电子器件学术研讨会, 贵阳, Aug 13-17, 2024.

[T9] " 物理设计中的异构并行加速问题：从图理论到数值计算", 中国计算机协会芯片大会（CCF Chip）, 上海, Jul 19-21, 2024.

[T8] " 异构计算和人工智能加速物理设计与优化", 中国计算机协会集成电路设计与自动化学术会议（CCF-DAC）, 北京, Oct 13-16, 2023.

[T7] "A Timing Engine Inspired Graph Neural Network Model for Pre-Routing Slack Prediction", CCF Chip 芯片大会, 南京, Jul 29-31, 2022.

[T6] "Exploring AI-assisted Optimization Opportunities in Placement and Routing", 华为 Strategy and Technology Workshop (STW), 深圳, Oct 14-16, 2021.

[T5] "A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Static Timing Analysis", ChinaDA, 北京, Jul 10-11, 2021.

[T4] " 深度学习辅助布局布线优化", 中国计算机协会青年精英大会 (CCF-YEF), 沈阳, May 15, 2021.

[T3] "DREAMPlace 3.0: Multi-Electrostatics Based Robust VLSI Placement with Region Constraints", 东湖论坛, 武汉, Nov 28, 2020.

[T2] ” 先进工艺下 AI 辅助芯片后端设计与制造”, 中国计算机协会集成电路设计与自动化学术会议 (CCF-DAC), 线上, Aug 10-11, 2020.

[T1] ” 基于机器学习的集成电路后端设计及加速”, 华为海思与高校技术论坛, 北京, Nov 28, 2019.

国内外机构邀请报告

[T11] ”The Art of Formulation and Optimization in VLSI Placement for Diverse Design Scenarios”, Google DeepMind, Mountain View, California, Jul 29, 2024.

[T10] ”Deep Learning for Physical Design Automation of VLSI Circuits: Modeling, Optimization, and Datasets”, Synopsys, Armenia, Feb 5, 2024.

[T9] ”Deep Learning for Physical Design Automation of VLSI Circuits: Modeling, Optimization, and Datasets”, Georgia Institute of Technology, Atlanta, Georgia, Jul 3, 2024.

[T8] ”Accelerating Timing Closure of IC Design with Heterogeneous Computing and Machine Intelligence”, University of Wisconsin, Madison, Nov 3, 2023.

[T7] ”Accelerating Timing Closure of Integrated Circuits with Heterogeneous Computing and Machine Intelligence ”, Arizona State University, Oct 27, 2023.

[T6] ”Heterogenous Timing Analysis, Prediction, and Optimization of Integrated Circuits with Machine Intelligence ”, National University of Singapore, Aug 29, 2023.

[T5] ”Deep Learning for Backend Design Automation of VLSI Circuits: Modeling, Optimization, and Datasets”, Hong Kong University of Science and Technology, Apr 14, 2023.

[T4] ”Deep Learning for Physical Design Automation of VLSI Circuits: Modeling, Optimization, and Datasets”, Chinese University of Hong Kong, Mar 23, 2023.

[T3] ”Timing Analysis and Optimization on Heterogeneous CPU-GPU Platforms”, Synopsys, Armenia, Jan 30, 2023.

[T2] ”Accelerating VLSI Physical Design with Parallel and Heterogeneous Computing”, Synopsys, Armenia, Jan 24, 2022.

[T1] ”Machine Learning Based IC Backend Design and Acceleration”, Synopsys, Armenia, Apr 8, 2021.