High-Resolution Full-Chip Thermal Resistance Extraction of BEOL Interconnects in 3-D ICs Considering Detailed Via Connectivity

Tianxiang Zhu[1], Qipan Wang[1,2], Yibo Lin[1,3,4*], Runsheng Wang[1,3,4*],
[1]School of Integrated Circuits, [2]Academy for Advanced Interdisciplinary Studies, Peking University, Beijing,
[3]Institute of Electronic Design Automation, Peking University, Wuxi,
[4]Beijing Advanced Innovation Center for Integrated Circuits
{txzhu, qpwang, yibolin, r.wang}@pku.edu.cn

***Abstract*—With the rise of 3-D integration technology, the back-end-of-line (BEOL) interconnects start to play an important role in thermal analysis, as they inevitably occupy the main thermal dissipation path of the active devices in 3-D ICs. High-resolution full-chip thermal resistance extraction of BEOL interconnects is thus needed to obtain accurate temperatures of local hotspots, which renders rigorous numerical simulation based extraction methods unaffordable. Several analytical models have been proposed for efficient full-chip thermal resistance extraction of BEOL interconnects, but they are very inaccurate due to the inability to consider the detailed via connectivity. In this paper, we propose a novel analytical model based on the resistor network theory and the Woodbury formula. Our model takes the detailed via connectivity into consideration and achieves a 3.4× improvement in accuracy compared with the previous work, with negligible time overhead. Owing to the accuracy improvement in the extracted thermal resistances, we reduce the absolute percentage error of the maximum temperature predicted by further thermal analysis of a 3-D IC based on the extracted thermal resistances from 5.2% to 1.8%, compared with the previous work.**

I. Introduction

The transition of integrated circuits from 2-D to 3-D is becoming a general trend to meet the increasingly demanding performance, power, and area targets, which gives rise to increasingly severe thermal issues, mainly due to the enlargement of vertical thermal resistance and stacking of power sources [1]. Excessive on-chip temperatures will lead to performance degradation and reliability issues [2], while studies reveal that local hotspots are generally much hotter on finer scales [3], [4]. Thus, it is of the essence to perform high-resolution thermal analysis of 3-D ICs for design optimization and convergence [5]–[7].

Recently, a growing number of studies have put emphasis on the back-end-of-line (BEOL) interconnects during the thermal analysis of 3-D ICs [4], [8]–[11]. Besides that the detailed structures of BEOL interconnects are exposed at a higher resolution, the special stacking style of 3-D ICs is another main reason for the increasing significance of BEOL interconnects in thermal analysis. In the traditional 2-D flip chip package, the chips are placed facedown, with the BEOL adjoining the package substrate and the silicon substrate of the chip adjoining the heat spreader and heat sink. The main heat dissipation path (∼95% of total heat [3]) for the heat-generating front-end-of-line (FEOL) active devices punches through the silicon substrate and the thermal interface material, and does not include the BEOL part (Fig. 1(a)). However, in 3-D ICs, the heat generated in FEOL is bound to pass the BEOL, whether in face-to-face integration [12], [13] or in face-to-back integration [14], rendering the thermal resistance of BEOL interconnects unprecedentedly important (Fig. 1(b)(c)).

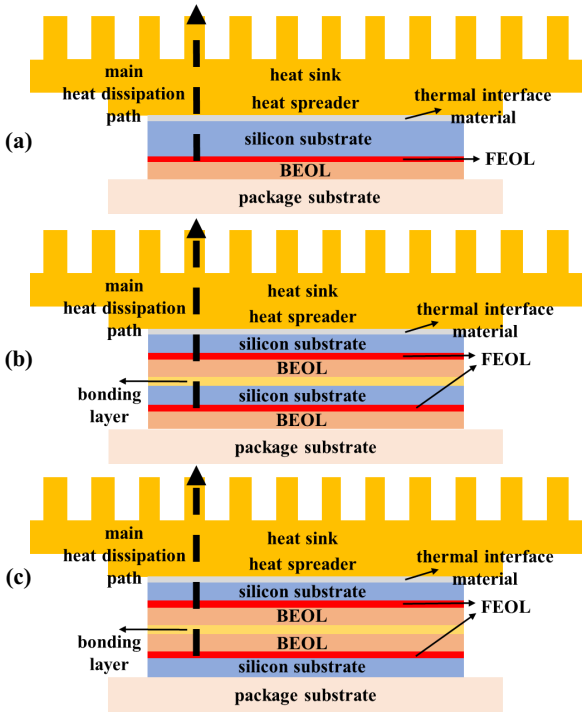

Fig. 1. Schematics of (a) 2-D IC with flip chip package, (b) 3-D IC with face-to-back integration, and (c) 3-D IC with face-to-face integration. The main heat dissipation path for the FEOL is bound to pass through the BEOL in the 3-D IC scenarios.

Although the thermal conductivity of metal interconnect is very high (several hundreds $\mathrm{W/m \cdot K}$), the low-k dielectric is a very poor conductor of heat (less than 1 $\mathrm{W/m \cdot K}$) [8], [15]. Thus, characterization experiments indicate that the typical equivalent thermal conductivity of BEOL stack is in the range of 0.1 $\mathrm{W/m \cdot K}$ to 10 $\mathrm{W/m \cdot K}$ (a rather low value compared with that of the silicon substrate, 140 $\mathrm{W/m \cdot K}$) [15]–[17]. In advanced packages such as hybrid bonding, BEOL contributes over 90% of the total inter-die thermal resistance [18]. These data imply that the actual values of thermal resistance of BEOL will have

*Corresponding authors.

a large impact on the results of thermal analysis for 3-D ICs. Moreover, extensive studies have shown that the values of BEOL thermal resistance vary in a wide range according to the specific metal line density, via density, and via connectivity, which makes setting a single equivalent thermal conductivity for the whole BEOL stack deviate from the real circumstances, especially in high-resolution scenarios [8], [15]–[17].

As there are a large number of metal lines in the BEOL, direct full-chip thermal simulation considering details of the BEOL is impossible. A common and natural detour is to divide the BEOL stack by a grid and then extract the thermal resistance of each patch of BEOL stack, which can be used for the subsequent full-chip thermal analysis [3], [4], [8], [19]. For high-resolution scenarios, extraction routines based on rigorous numerical simulation, such as finite element analysis, are extremely time-consuming, while the fact that the extraction procedure is likely to be performed multiple times until design convergence further deteriorates the situation.

To solve this issue, many methods have been proposed. Labun et al. [20] utilize the equivalence between thermal resistance and parasitic capacitance of BEOL interconnects to reduce the number of degrees of freedom in the system for numerical simulation. However, the efficiency improvement is not sufficient for high-resolution full-chip extraction. For the past decades, researchers have proposed various closed-form analytical models [21], [22]. The time cost of these methods is negligible compared with numerical simulation, but none of them is able to consider the detailed via connectivity, resulting in low accuracy. Recently, Chang et al. [8], [9] have improved the traditional analytical model and have proposed to use a correction factor to account for different via configurations. However, their method is not flexible enough and still suffers from low accuracy.

In this work, we propose a novel analytical model for high-resolution full-chip thermal resistance extraction of BEOL interconnects. Our model takes the detailed via connectivity into consideration and significantly improve the accuracy, with negligible time overhead. The main contributions of our work are as follows:

- We propose a novel closed-form analytical model for the thermal resistance of BEOL interconnects with the help of resistor network theory and the Woodbury formula, which takes the detailed via connectivity into consideration.
- We analyze the physical meaning of our analytical model, and provide useful instructions for the optimization of thermal resistance of BEOL interconnects.
- We test our model on a real design and perform thermal analysis of a 3-D IC with the extracted thermal resistances. Our model achieves a mean absolute percentage error of 7.2% in thermal resistance, which is 3.4× smaller than the previous work, with negligible time overhead. Applying the thermal resistances extracted by our model to further thermal analysis reduces the absolute percentage error of the maximum temperature from 5.2% to 1.8% compared with the previous work.

The rest of this paper is organized as follows. Section 2 provides a review of relevant works. Section 3 introduces the preliminaries of this work. Section 4 elaborates on the derivation and analysis of our model. Section 5 provides the experimental setup and results. Section 6 concludes this paper.

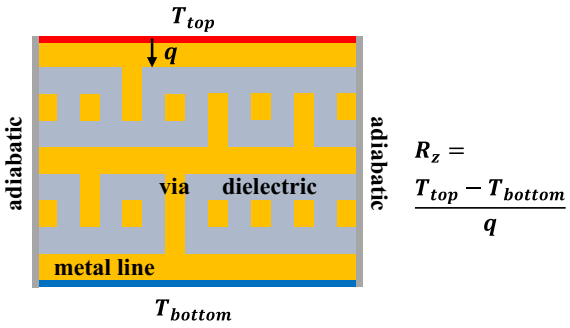

Fig. 2. Schematic of the extraction process of the (z-direction) thermal resistance of a BEOL stack through numerical simulation. The side surfaces are set to be adiabatic. The top and the bottom surfaces are applied with constant temperatures T_{top} and T_{bottom}, respectively. The total z-direction heat flow is then obtained through numerical simulation. After that, R_z can be calculated.

II. Related Works

A. Numerical simulation

Traditionally, thermal resistances of BEOL stacks are extracted through rigorous numerical simulations, such as finite element analysis [8], [19]. For example, during extraction of the z-direction thermal resistance of a small patch of BEOL stack, the side surfaces of the stack is set to be adiabatic, and the top and bottom surfaces are applied with constant temperatures T_{top} and T_{bottom}, respectively (Fig. 2). Through numerical simulation, the total z-direction heat flow q can be obtained and the thermal resistance R_z is calculated by:

$$R_z = \frac{T_{top} - T_{bottom}}{q}. \tag{1}$$

However, to perform high-resolution full-chip thermal resistance extraction, a large number of BEOL stacks have to be simulated during one extraction procedure, and the procedure is likely to be performed for multiple times during the whole design process, which makes the time cost completely unaffordable. For real chip designs and micron-scale resolutions, it will take days or even weeks to complete one extraction procedure. Thus, a fast extraction method is indispensable to fulfill the task.

There is a well-known equivalence between the thermal resistance of inter-layer dielectric (ILD) and inter-metal dielectric (IMD) in the BEOL stack, and the parasitic capacitance between metal lines, because their governing equations are of the same form [21]–[23]. As a result, the electrical parasitic netlist can be converted into a thermal resistor network, and the total thermal resistance of the BEOL stack can be obtained by simulation of the network [20]. This method reduces the number of degrees of freedom in the BEOL stack to be simulated, but still requires substantial time and is not suitable for high-resolution full-chip thermal resistance extraction. Moreover, numerical simulations cannot offer intuitions and direct guides to design optimization, because it does not provide an explicit relation between the input parameters and the results. The

above issues can be readily solved by closed-form analytical models with design parameters as their inputs.

B. Analytical models

Based on the idea of thermal-electrical equivalence mentioned above, many analytical models have been proposed for fast thermal resistance extraction of BEOL interconnects. Chiang et al. proposed the first analytical model based on simplification of the heat flow between metal lines, and further took the via effect into consideration [22], [24]. Xu et al. and Jiang et al. improved Chiang's model with a more realistic form using the analytical formulation of line-to-ground parasitic capacitance [21], [23]. They regarded the via and the dielectric part in the same layer as parallel resistors, and the contributions from different layers of the BEOL stack are then added in series.

However, none of these models is able to deal with detailed via connectivity, which is one of the main reasons for their low accuracy. Metal vias are important inter-layer high thermal conductance paths through the low thermal conductance dielectric, and previous studies reveal that the specific configuration of vias greatly influences the total thermal resistance of the BEOL stack [8], [15], [17]. For example, if two vias are connected to the same metal line segment in the current patch of BEOL stack, a via–line–via high thermal conductivity path is formed, resulting in low thermal resistance. Otherwise, heat must go through the inter-metal and inter-layer dielectric, resulting in high thermal resistance.

Recently, Chang et al. have thoroughly studied the thermal resistance of BEOL stack with different via connectivity patterns [8], [9]. They make small modifications to Xu's model and get accurate results on BEOL stacks with stacked and aligned vias in different layers. For BEOL stacks with staggered or random via connectivity, they propose to multiply the model's results by a pre-determined correlation factor (2 in their original work). Although their model partly takes the via connectivity into consideration, it is inflexible for using a fixed correlation factor, and is unable to deal with the abundant via connectivity patterns in real designs. An analytical model that explicitly brings the detailed via connectivity into its expression is in urgent need to perform efficient and accurate high-resolution full-chip thermal resistance extraction of BEOL interconnects.

C. Other works

Besides works that study the thermal resistance of BEOL interconnects, some other works focus on the thermal modeling of package-level interconnects, such as the redistribution layers (RDL), through silicon vias, and micro bumps [19], [25], [26]. The structures considered in most of these studies differ a lot from BEOL interconnects. The most relevant study is performed by Liu et al, where detailed metal patterns and via locations are considered during the extraction of thermal resistance of the RDL. However, they utilize the machine learning method to fulfill the task, which is limited by the training data and is not suitable for BEOL because patterns of BEOL are much more complex. Thus, we do not provide further discussions about these works.

III. Preliminaries

Our analytical model is also based on the thermal-electrical equivalence, so we first introduce the related theory in this section. After that, we introduce the detailed form of the widely used analytical model developed by Xu et al. and improved by Chang et al., which will serve as the baseline model in our work.

A. Thermal-Electrical Equivalence

In the scenario of BEOL interconnects, the thermal resistance of inter-metal and inter-layer dielectric is equivalent to the parasitic capacitance because their governing equations share the same form [21], [23]. The governing equation of parasitic capacitance is:

$$\nabla \cdot (\varepsilon_{diel} \nabla \phi) = 0\,, \tag{2}$$

where ε_{diel} is the permittivity, and ϕ is the electrical potential. The governing equation of thermal resistance of the dielectric is:

$$\nabla \cdot (k_{diel} \nabla T) = 0\,, \tag{3}$$

where k_{diel} is the thermal conductivity, and T is the temperature. The parasitic capacitance per unit length C can be expressed as:

$$C_{el,diel}/\varepsilon_{diel} = f(w,\, t_{wire},, t_{diel},, s)\,, \tag{4}$$

where w is the width of the metal line, t_{wire} is the thickness of the metal line, t_{diel} is the thickness of inter-layer dielectric, and s is the metal line spacing. The function f has been widely studied in previous works [27]–[29] on parasitic capacitance, and one of its specific forms can be found in [27], which is omitted here for brevity. Because the forms of Eq. 2 and Eq. 3 are similar to each other, the thermal resistance of the inter-metal dielectric per unit length $R_{th,diel}$ can be written as:

$$1/(k_{diel} R_{th,diel}) = f(w,\, t_{wire},\, t_{diel},\, s)\,. \tag{5}$$

Besides, for the metal lines and vias in the BEOL, the thermal resistance $R_{th,metal}$ is equivalent to the electrical parasitic resistance $R_{el,metal}$, that is:

$$R_{th,metal}/k_{metal} = R_{el,metal}/\rho_{metal}\,, \tag{6}$$

where ρ_{metal} is the metal electrical resistivity.

After discretizing the metal lines in a BEOL stack into small enough segments and converting the electrical parasitic capacitors and resistors into equivalent thermal resistors, a thermal resistor network can be developed. Temperatures are equivalent to voltages, and heat flows are equivalent to currents. The total thermal resistance (for example, z-direction) can be obtained by setting the voltages of nodes on the top surface to T_{top}, setting the voltages of nodes on the bottom surface to T_{bottom}, and performing simulation to obtain the total injected heat flow q. The thermal resistance of the BEOL stack can then be calculated by Eq. 1. Our goal is to avoid direct numerical simulation of this network and develop a closed-form analytical expression of the resistance between the top node and the bottom node under certain approximations.

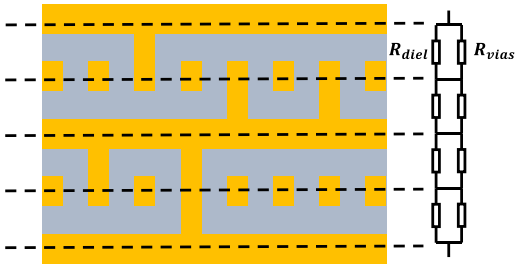

Fig. 3. Schematic of the baseline model. The dielectric part and the via part of each layer of vias in a BEOL stack are treated as parallel thermal resistors and then connected in series to get the total (z-direction) thermal resistance.

B. Introduction to the baseline model

The thermal resistance of a BEOL stack contains three orthogonal components: the x-direction one, the y-direction one, and the z-direction one. The x-direction and y-direction thermal resistances can be readily and accurately modeled using the rule of mixtures, and their impact on the thermal behavior of the chip is much weaker than the z-direction component [21]. For the z-direction component, the connectivity of vias plays an important role, so the circumstances are much more complex. Therefore, previous works mainly focus on the modeling of the z-direction component [8], [21], [24], and we follow this convention in our work. **Unless explicitly mentioned, "thermal resistance" refers to the z-direction one later in this paper**.

The baseline model treats the dielectric part and the via part of each layer of vias as parallel thermal resistors and then adds the resistance of each via layer in series (Fig. 3). The thermal resistance of the dielectric part of via layer l without the existence of vias, $R_{l,no-vias}$, can be derived from Eq. 5:

$$R_{l,no-vias} = \frac{w_l}{k_{diel} \times f(w_l,\, t_{l,wire},\, t_{l,diel},\, s_l) \times A_{l,wire}}\,, \tag{7}$$

where $A_{l,wire}$ is the total area of metal lines in layer l.

The thermal resistance of the via part of layer l, $R_{l,vias}$, derived in Xu's work is [21]:

$$R_{l,vias} = \frac{t_{l,diel} + t_{l,wire}}{k_{metal} \times A_{l,vias}}\,, \tag{8}$$

where $A_{l,vias}$ is the total area of vias in layer l. Chang et al. [8] improve this formula by considering the lateral heat conduction in the metal lines:

$$R_{l,vias} = \frac{t_{l,diel} + t_{l,wire} \times \ln(AR_l + 1)/AR_l}{k_{metal} \times A_{l,vias}}\,, \tag{9}$$

where $AR_l = t_{l,wire}/w_l$ is the aspect ratio of the metal lines.

The total thermal resistance (z-direction) of the BEOL stack can then be written as:

$$R_{sv} = \sum_{l=1}^{L} \frac{1}{1/\frac{A_{l,wire}}{(A_{l,wire}-A_{l,vias})} R_{l,no-vias} + 1/R_{l,vias}}\,, \tag{10}$$

where L is the number of via layers. Chang et al. propose that Eq. 9 is only suitable for scenarios where vias are stacked and aligned. For randomly connected vias, a predetermined correlation factor c should be multiplied by the expression:

$$R_r = c \times R_{sv}\,, \tag{11}$$

where c is obtained through simulations of prototypical BEOL stacks and is set to be 2 in their work.

IV. Derivation and Analysis of Our Model

As mentioned in Section III-B, we focus on the modeling of the z-direction component of the BEOL thermal resistance in this work. In this section, we first present the detailed derivation process of our closed-form analytical model based on the resistor network theory and the Woodbury formula. After that, we briefly analyze the implications of our model.

A. Derivation of our model

1) Splitting the BEOL stack into the via-free part and vias: As mentioned in Section III-A, a thermal resistor network $\mathcal{N}$ corresponding to the BEOL stack to be modeled can be developed according to the thermal-electrical equivalence. In $\mathcal{N}$, all of the nodes are on the metal lines, and each via is modeled as a thermal resistor. All of the nodes on the top surface are shorted to a single top node, and all of the nodes on the bottom surface are shorted to a single bottom node, because the top and the bottom surfaces are set to be isothermal during (z-direction) thermal resistance extraction. Our goal is to obtain the expression of the effective resistance between the top node and the bottom node of $\mathcal{N}$. Assume that the BEOL stack has L layers of vias, the number of vias in via layer l is n_l, the total area of metal lines of layer l is $A_{l,wire}$, and the total area of vias is $A_{l,vias}$.

Denote the thermal conductance (the inverse of thermal resistance) between node i, j by g_{ij}, and the Laplacian matrix of network $\mathcal{N}$ by L. The entries of L are [30]:

$$L_{ij} = \begin{cases} -g_{ij} & i \neq j\,, \\ \sum_j g_{ij} & i = j\,. \end{cases} \tag{12}$$

According to the theory of resistor network, the effective resistance R between the top and the bottom nodes is [31]:

$$R = (\boldsymbol{e}_{top} - \boldsymbol{e}_{bottom})^{\mathrm{T}} L^{-1} (\boldsymbol{e}_{top} - \boldsymbol{e}_{bottom})\,, \tag{13}$$

where $\boldsymbol{e}_{top}$ and $\boldsymbol{e}_{bottom}$ are the unit column vectors corresponding to the top node and the bottom node, respectively.

If there are no vias in the BEOL stack, the total thermal resistance is simply the summation of the $R_{l,no-vias}$ of each via layer, which is proven to be very accurate [8], [15]. Meanwhile, the number of vias in a BEOL stack is rather small, so the existence of vias can be treated as a low-rank modification to the Laplacian matrix of the same BEOL stack but without vias. We denote the resistor network of the via-free BEOL stack as $\mathcal{N}_{no-vias}$ and its Laplacian matrix as $L_{no-vias}$ (Fig. 4). Thus, L can be written as:

$$L = L_{no-vias} + \sum (\boldsymbol{e}_i - \boldsymbol{e}_j)(g_{l,via} - g_{l,diel})(\boldsymbol{e}_i - \boldsymbol{e}_j)^{\mathrm{T}}\,, \tag{14}$$

where $g_{l,via}$ is the thermal conductance of the via in layer l and $g_{l,diel}$ is the thermal conductance of the part of the dielectric occupied by the via. $\boldsymbol{e}_i$ and $\boldsymbol{e}_j$ are the unit

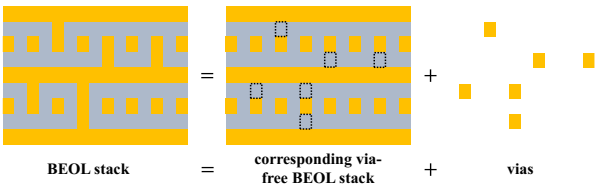

Fig. 4. Schematic of the core thought of our model. We treat the existence of vias in the BEOL stack as a low-rank modification to the Laplacian matrix of the corresponding via-free BEOL stack, which simplifies the problem and enables our model to explicitly include the detailed via connectivity through the Woodbury formula.

column vectors corresponding to node i and j, respectively. The summation is performed for all of the vias. Further, we denote $g_{via} - g_{diel}$ as $(1/\beta_l - 1)g_{l,diel}$, where $\beta_l = g_{l,diel}/g_{l,via} \ll 1$ because $k_{diel} \ll k_{metal}$.

The well-known Woodbury formula [32] can be used to calculate the inverse of a matrix in the form of Eq. 14:

$$(A+UCV)^{-1} = A^{-1} - A^{-1}U(C^{-1}+VA^{-1}U)VA^{-1}\,, \tag{15}$$

where A is an invertible matrix, and U, C, V are matrices with appropriate dimensions. By applying Eq. 15 to Eq. 14, we can get:

$$\begin{aligned} L^{-1} =& L_{no-vias}^{-1} - \\ & L_{no-vias}^{-1}U(G^{-1}+U^{\mathrm{T}}L_{no-vias}^{-1}U)U^{\mathrm{T}}L_{no-vias}^{-1}\,, \end{aligned} \tag{16}$$

where G is a diagonal matrix with $(1/\beta_l - 1)g_{l,diel}$ as its entries, and U is a matrix composed of column vectors $(\boldsymbol{e}_i - \boldsymbol{e}_j)$.

By substituting Eq. 16 into Eq. 13, the total thermal resistance can be expressed as:

$$\begin{aligned} R = \sum_{l=1}^{L} R_{l,no-vias} - (\boldsymbol{e}_{top}-\boldsymbol{e}_{bottom})^{\mathrm{T}}L_{no-vias}^{-1}U\times \\ (G^{-1}+U^{\mathrm{T}}L_{no-vias}^{-1}U)^{-1}\times U^{\mathrm{T}}L_{no-vias}^{-1}(\boldsymbol{e}_{top}-\boldsymbol{e}_{bottom})\,, \end{aligned} \tag{17}$$

The first term of Eq. 17 is well-defined in Eq. 7. There are three components in the second term, which will be simplified one by one.

2) Simplification of Eq. 17: According to the resistor network theory, considering a thermal resistor network with Laplacian matrix L, the physical meaning of $L^{-1}\boldsymbol{e}_i$ is the temperature distribution in the network with $+1$ heat flow injected into node i [31]. Thus, the physical meaning of $L_{no-vias}^{-1}(\boldsymbol{e}_{top}-\boldsymbol{e}_{bottom})$ is the temperature distribution in the via-free BEOL stack $\mathcal{N}_{no-vias}$ with $+1$ heat flow injected into the top node and -1 heat flow injected into the bottom node. Because matrix U is composed of column vectors $(\boldsymbol{e}_i - \boldsymbol{e}_j)$, where i and j are the nodes at the two ends of a via, a certain entry of the column vector $U^{\mathrm{T}}L_{no-vias}^{-1}(\boldsymbol{e}_{top}-\boldsymbol{e}_{bottom})$ in Eq. 17 can thus be interpreted as the temperature difference between two nodes in $\mathcal{N}_{no-vias}$ which are originally the ends of a certain via, when applying ± 1 heat flow to the top and the bottom nodes. Moreover, because Laplacian matrices are symmetric, the term $(\boldsymbol{e}_{top}-\boldsymbol{e}_{bottom})^{\mathrm{T}}L_{no-vias}^{-1}U$ is just the transpose of $U^{\mathrm{T}}L_{no-vias}^{-1}(\boldsymbol{e}_{top}-\boldsymbol{e}_{bottom})$.

To calculate the temperature differences between the via-related nodes mentioned above, we build several via-free prototypical BEOL stacks with metal line density ranging from 20%–80%, and apply constant temperatures to the top and the bottom surfaces. Through numerical simulation, we find that in via-free BEOL stacks, because there are no high conductance paths formed by vias through the inter-layer dielectric, the temperature distribution in each layer is rather uniform, with an in-plane variation of less than 1%. Thus, for the nodes of vias in layer l, the temperature difference can be approximated as $R_{l,no-vias}$. The term $U^{\mathrm{T}}L_{no-vias}^{-1}(\boldsymbol{e}_{top}-\boldsymbol{e}_{bottom})$ can then be expressed as:

$$\begin{aligned} & U^{\mathrm{T}}L_{no-vias}^{-1}(\boldsymbol{e}_{top}-\boldsymbol{e}_{bottom}) = \\ & (\underbrace{R_{1,no-vias},\cdots}_{n_1},\underbrace{R_{2,no-vias},\cdots}_{n_2},\cdots,\underbrace{R_{L,no-vias},\cdots}_{n_L})^{\mathrm{T}} \end{aligned} \tag{18}$$

Next we will simplify the term $G^{-1}+U^{\mathrm{T}}L_{no-vias}^{-1}U$. As G is a diagonal matrix with known entries, the only component that needs to be simplified is $U^{\mathrm{T}}L_{no-vias}^{-1}U$. Following the same thoughts mentioned above, the physical meaning of the m,n th entry of $U^{\mathrm{T}}L_{no-vias}^{-1}U$ can be interpreted as the temperature difference between nodes at the ends of via m, when applying ± 1 heat flow to the nodes at the ends of via n, all performed in $\mathcal{N}_{no-vias}$.

Now, extract $\mathrm{diag}(\underbrace{R_{1,no-vias},\cdots}_{n_1},\cdots,\underbrace{R_{L,no-vias},\cdots}_{n_L})$ from $(G^{-1}+U^{\mathrm{T}}L_{no-vias}^{-1}U)^{-1}$ in Eq. 17, and we can get:

$$\begin{aligned} R =& \sum_{l=1}^{L} R_{l,no-vias} - \\ & (\underbrace{R_{1,no-vias},\cdots}_{n_1},\cdots,\underbrace{R_{L,no-vias},\cdots}_{n_L})\Lambda^{-1}(\underbrace{1,\cdots,1}_{\sum n_l})^{\mathrm{T}}. \end{aligned} \tag{19}$$

The diagonal entries of Λ are:

$$\begin{aligned} \Lambda_{mm} &= \frac{\alpha_{mm}/g_{l,diel} + 1/(1/\beta_l - 1)g_{l,diel}}{R_{l,no-vias}} \\ &= \frac{\alpha_{mm}/g_{l,diel} + 1/(1/\beta_l - 1)g_{l,diel}}{\frac{A_{l,via}/n_l}{A_{l,wire}}\times g_{l,diel}} \\ &\approx \frac{n_l A_{l,wire}}{A_{l,via}} \times (\alpha_{mm}+\beta_l)\,, \end{aligned} \tag{20}$$

and the off-diagonal entries of Λ are:

$$\Lambda_{mn} = \frac{\alpha_{mm}/g_{l,diel}}{R_{l,no-vias}} \approx \frac{n_l A_{l,wire}}{A_{l,via}} \times \alpha_{mn}\,, \tag{21}$$

where α_{mn} is the part of the heat flow passing through the nodes at the ends of via m when applying ± 1 heat flow to the nodes at the ends of via n in $\mathcal{N}_{no-vias}$ (Fig. 5).

Because the thermal conductivity of the inter-layer and inter-metal dielectric is very low, heat conduction will be localized when applying heat flow to the nodes in $\mathcal{N}_{no-vias}$. Thus, we can reasonably assume that the diagonal entries of Λ are much larger than the off-diagonal entries of Λ, that is, $\alpha_{mm} \gg \alpha_{mn}$. By splitting Λ into the diagonal part D and the off-diagonal part E, we can get:

$$\Lambda^{-1} = (D+E)^{-1} \approx D^{-1} - D^{-1}ED^{-1}\,. \tag{22}$$

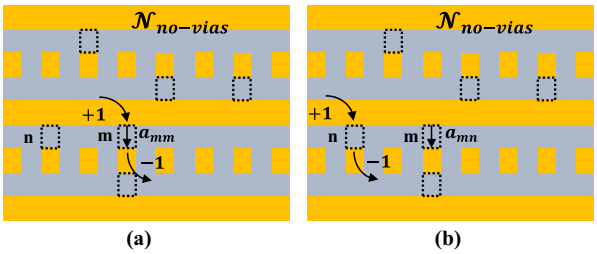

Fig. 5. The physical meaning of (a) α_{mm} and (b) α_{mn}. α_{mm} denotes the part of heat flow passing through the location of itself when applying ± 1 heat flow to the nodes of via m, and α_{mn} denotes the part of heat flow passing through the location of via m when applying ± 1 heat flow to the nodes of via n, both of which are considered in the via-free BEOL stack $\mathcal{N}_{no-vias}$.

Thus, the entries of Λ^{-1} are approximated as:

$$(\Lambda^{-1})_{mm} = \frac{A_{l,vias}}{n_l A_{l,wire}} \times \frac{1}{\alpha_{mm} + \beta_l}, \tag{23}$$
$$(\Lambda^{-1})_{mn} = \frac{A_{l,vias}}{n_l A_{l,wire}} \times \frac{\alpha_{mn}}{(\alpha_{mm} + \beta_l)(\alpha_{nn} + \beta_l)}.$$

By substituting Eq. 20, 21, and 22 into Eq. 19, we can obtain **the final expression of our analytical model** for the (z-direction) thermal resistance of BEOL stacks:

$$R = \sum_{l=1}^{L} R_{l,no-vias} \times (1 - \frac{A_{l,vias}}{A_{l,wire}} \varphi_l). \tag{24}$$

Here φ_l is a factor describing the modification introduced by vias in the via layer l on the via-free thermal resistance:

$$\varphi_l = \frac{1}{n_l} \sum_{m=1}^{n_l} \frac{1}{\alpha_{mm} + \beta_l} (1 - \sum_{n \in I(m)} \frac{\alpha_{mn}}{\alpha_{nn} + \beta_l}), \tag{25}$$

where $I(m)$ denotes the set of vias which can influence via m ($|\alpha_{mn}| > 0$). The physical meaning of this expression is very clear. Vias serve as the correlation to the via-free thermal resistance. α_{mm} denotes the ability of via m to influence the total heat conduction, and α_{mn}/α_{nn} denotes the influence of via n on via m.

B. Determination of the values of α_{mm} and α_{mn}

The final step is to determine the values of α_{mm} and α_{mn}. Because of the localization of heat conduction, the most accurate way to determine α_{mn} is through pattern matching, which is a commonly adopted method in parasitic extraction. However, in this work, we try to derive the analytical forms of α_{mn} to demonstrate a closed-form expression with some price of accuracy. The pattern matching method can be the topic of future work.

Through simulation of prototypical via-free BEOL stacks as mentioned before, we find that for via m in layer l, only vias which are in layer $l-1$, l, and $l+1$ and which are connected to the same metal lines can be considerably influenced by via m, so there is no need to go through all of the vias in the stack. Suppose that the area of the top metal lines connected to via m is $S_{m,top}$, while the area of the bottom metal lines connected to via m is $S_{m,bottom}$, and the area of via m itself is S_m. When applying ± 1 heat flow to the nodes at the ends of via m in the via-free BEOL stack, α_{mm} can be calculated as:

$$\alpha_{mm} = S_m \times (1/S_{m,top} + 1/S_{m,bottom}) \times \frac{g_{l,v}}{2(g_{l,h} + g_{l,v})}. \tag{26}$$

For via n that is connected to the same metal line as via m, denote its distance to m as d_{mn}. α_{mn} will decay exponentially with the distance between two vias [24], [33]. Because the interconnects are orthogonal in different adjacent metal line layers, via m and n can only share the top metal line or the bottom metal line. If they are in the same layer, there is $\alpha_{mn} > 0$:

$$\alpha_{mn} = S_m / S_{m,top\ (or\ m,bottom)} \times \frac{g_{l,v}}{2(g_{l,h} + g_{l,v})} \times e^{-d_{mn}/\zeta_l}. \tag{27}$$

Otherwise there is $\alpha_{mn} < 0$:

$$\alpha_{mn} = -S_m / S_{m,top\ (or\ m,bottom)} \times \frac{g_{l,v}}{2(g_{l,h} + g_{l,v})} \times e^{-d_{mn}/\zeta_l}. \tag{28}$$

In the above equations, g_v is the per unit length vertical line-to-line thermal conductance through dielectric, and g_h is the horizontal one. These values can be derived from the equivalence between thermal resistance and parasitic capacitance, and the specific forms can be found in [27]. ζ_l is the well-known feature length for thermal conduction along metal interconnects in BEOL [24], [33]:

$$\zeta_l = \sqrt{g_{l,wire}/(2g_{l,v} + 2g_{l,h})}, \tag{29}$$

where $g_{l,wire} = k_{metal} w_l t_{l,wire}$ is the per unit length thermal conductance of the metal line.

Up till now, all of the parameters in Eq. 24 can be determined by the design parameters and via connectivity of the BEOL stack. The implementation of our analytical model is shown in Algorithm 1. We use the techdef file from the PDK and the GDSII file of the design (split by a grid with the required resolution) as our input.

C. Analysis of our model

As the physical meaning of our model is straightforward and detailed via connectivity is considered, we can obtain several instructive implications from Eq. 24–29, which may be useful for the optimization of thermal resistances of the BEOL interconnects:

- The total thermal resistance of a BEOL stack monotonically decreases with the increase of the total area of vias, or via density.
- When two vias are in the same layer, $\alpha_{mn} > 0$. Thus, φ_l in Eq. 24 will decrease as the two vias get closer, and result in the increase of the total thermal resistance. Vias in the same layer have negative mutual effects on the thermal conduction abilities of each other.
- When two vias are not in the same layer, $\alpha_{mn} < 0$. Thus, φ_l in Eq. 24 will increase as the two vias get closer, and result in the decrease of the total thermal resistance. Vias in different layers have a positive effect on the thermal conduction abilities of each other.
- When a via is connected to a metal line with a larger area, α_{mm} in Eq. 25 will decrease as indicated by Eq. 26. Thus, the total thermal resistance will decrease. Increasing the number of vias connected to long metal

Algorithm 1 Implementation of our model

Input: tech.def and design.gds
Output: thermal resistances $R[N]$ of N BEOL stacks

obtain $t_{l,metal}$, $t_{l,diel}$, w_l, s_l, and L from tech.def
pre-calculate f, $g_{l,v}$, $g_{l,h}$, β_l and ζ_l
for all $i = 1, 2, \cdots, N$ **do**
  for all $l = 1, 2, \cdots, L$ **do**
    calculate $R_{l,no-vias}$ and store (Eq. 7)
    obtain the total number of vias n_l and store
    obtain $A_{l,wire}$ and $A_{l,vias}$ and store
    for all $m = 1, 2, \cdots, n_l$ **do**
      calculate α_{mm} and store (Eq. 26)
      find the connected vias in Layer l, $l-1$, and $l+1$ and store in $I(m)$
    end for
  end for
  $R[i] = 0$
  for all $l = 1, 2, \cdots, L$ **do**
    $\varphi_l = 0$
    for all $m = 1, 2, \cdots, n_l$ **do**
      $tmp = 0$
      for all $n \in I(m)$ **do**
        calculate α_{mn} (Eq. 27 & 28)
        $tmp = tmp + \alpha_{mn}/(\alpha_{nn} + \beta_l)$
      end for
      $\varphi_l = \varphi_l + 1/(\alpha_{mm} + \beta_l) \times (1 - tmp)$
    end for
    $\varphi_l = \varphi_l / n_l$
    $R[i] = R[i] + R_{l,no-vias} \times (1 - \frac{A_{l,vias}}{A_{l,wire}} \times \varphi_l)$
  end for
  store $R[i]$
end for

lines will help decrease the total thermal resistance, while increasing the number of vias connected to short metal lines will not, according to the second implication.

Most of these implications cannot be obtained through the baseline model introduced in Section III, because it does not take the detailed via connectivity into consideration.

V. Experimental Setup and Results

A. Experimental setup

To test the performance of our model on advanced technologies nodes, we adopt an ASAP7 based real design from [34]. The footprint of the design is $822\mu\text{m} \times 822\mu\text{m}$, and the resolution for extraction is set to be $5\mu\text{m} \times 5\mu\text{m}$, which results in $165 \times 165 = 27225$ BEOL stacks to be extracted. The metal layers used in the design range from M1 to M7, with via layers from V1 to V6. Dummy metal fill essential for realistic tape-outs is also added. The ASAP7 PDK does not provide the thickness of the layers, so we set the aspect ratio of the metal lines to be 2 and the dielectric layers to be the same thickness as the metal lines, which is reasonable in advanced technology nodes [8]. Besides, we set $k_{metal} = 300$ W/m · K [8] and $k_{diel} = 0.5$ W/m · K [15]. More accurate values can be obtained through characterization experiments of the materials, which is out of the scope of this work.

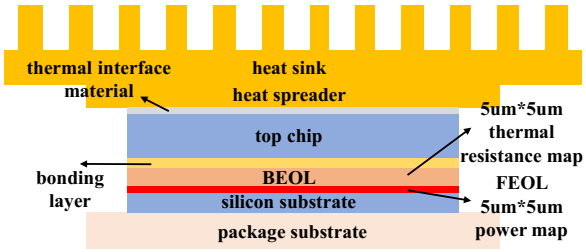

Fig. 6. Schematic of the 3-D IC used for further thermal analysis after thermal resistance extraction. The resolution of the thermal resistance and power maps of the bottom chip is $5\mu\text{m} \times 5\mu\text{m}$ (165×165).

In order to realize an automatic extraction flow from dividing the GDSII file to performing thermal resistance extraction using Python scripts, we adopt MTA [35] as the numerical simulator for ground truth data generation. MTA is an open-sourced finite element based rigorous thermal simulator that is specially optimized in mesh generation for cuboid domains, and has been validated against commercial software. We test several data points using MTA and Ansys Icepak [36]. The relative error of MTA against Icepak is within 1% and the difference in time cost is within 10%, which indicates that our customized flow can reflect the performance of commercial software. When implementing the baseline model, we find that the correlation factor $c = 2$ used in the original work is not suitable in our test case. For fair comparison, we randomly select 50 BEOL stacks and compare the thermal resistances extracted by the numerical simulator and the baseline model, and set a correlation factor $c = 1.5$ to make the average error small enough.

After the extraction of thermal resistances, we perform further thermal analysis to test the impact of the error of thermal resistance on the temperature results in 3-D IC scenarios. Because the original design is 2-D, we build a prototypical 3-D IC model following that in [37] by face-to-face integration with a virtual chip as shown in Fig. 6. The power map and thermal resistance map of the bottom chip are extracted from the design files with the same resolution, while the power and BEOL thermal resistance of the virtual top chip are set to be uniform. The z-direction thermal resistances of the BEOL stacks are extracted using the numerical simulator, the baseline model, and our proposed model, respectively. The x- and y-direction thermal resistances are calculated using the rule of mixtures [21], which produces a <5% error in thermal resistance compared with numerical simulation.

All of the experiments are performed on a Linux server with an AMD EPYC 7742 64-Core Processor. 48 threads are used for thermal resistance extraction for both numerical simulation and analytical modeling to accelerate the extraction process. The baseline model and our model are both implemented in Python, because the efficiency is already very high and there is no need to optimize the code.

B. Experimental results

1) Efficiency: The time cost of the whole extraction process is summarized in Table I. The time for dividing the GDSII file is not included because it is the same for different methods. The average time cost to extract the thermal resistance of one BEOL stack through numerical simulation is about 80 seconds using 1 single thread, which

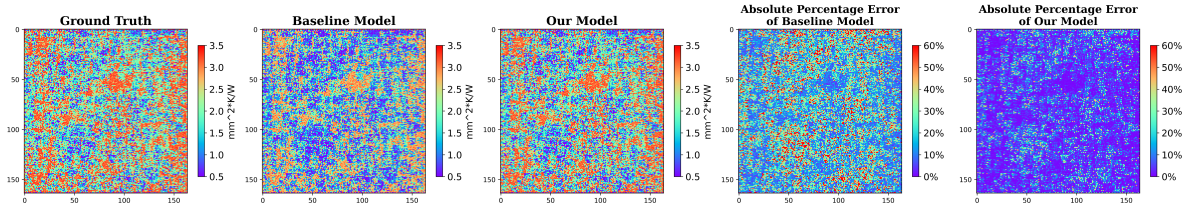

Fig. 7. Ground truth thermal resistance map extracted by numerical simulation, thermal resistance maps extracted by the baseline model and our model, and the absolute percentage error maps. Thermal resistances have been unified by the area of a single BEOL stack. The mean absolute percentage error of our model is 7.2%, while that of the baseline model is 24.5%, showing a 3.4× improvement in accuracy.

TABLE I
TIME COSTS OF DIFFERENT EXTRACTION METHODS.

	numerical simulation [8]	baseline model [8], [21]	our model
time cost	20 h 14 min	17 s	116 s

results in a total time of about 600 hours or 25 days for the whole extraction process. Parallel execution shortens the extraction process, but it still costs more than 20 hours. In contrast, the time costs of analytical methods are negligible compared with rigorous numerical simulation. Because our model takes the detailed via connectivity into consideration and requires iterations over the vias, its time cost increases compared with the baseline model. However, the time overhead does not change the order of magnitude of the time costs and can be neglected regarding the huge improvement over numerical simulation.

2) Accuracy: The detailed ground truth thermal resistance map extracted by numerical simulation, thermal resistance maps extracted by the baseline model and our model, together with the absolute percentage error maps ($\frac{|R_{simulation}-R_{model}|}{R_{simulation}} \times 100\%$) are shown in Fig. 7. Thermal resistances have been unified by the area of a single BEOL stack ($25\mu m^2$), so the unit is $\mathrm{mm}^2 \cdot \mathrm{K/W}$. The mean absolute percentage errors is 24.5% for the baseline model, and 7.2% for our model, showing a 3.4× improvement in accuracy. In high thermal resistance areas, the accuracy improvement of our model over the baseline model is relatively small, as the via densities are low in these areas, and the detailed via connectivity has less impact on the total thermal resistance. However, for BEOL stacks which have low thermal resistances, the improvement in accuracy is significant, because the via density is relatively high, and the detailed via connectivity plays an important role in the overall thermal conducting ability of the BEOL stack.

3) Impact on thermal analysis: We perform high-resolution (165×165) full-chip thermal analysis of the 3-D IC (Fig. 6) based on the thermal resistances extracted by numerical simulation, the baseline model, and our model. Moreover, we also calculate the average values of the thermal resistances extracted by numerical simulation for each 16×16 grid, obtain a thermal resistance map with 10×10 resolution, and perform thermal analysis based on the low-resolution thermal resistance value. The statistics of maximum temperatures are summarized in Table II. The absolute percentage errors in maximum temperatures obtained with the thermal resistances extracted by our model is 1.8%, while that of the baseline model is 5.2%. The predicted maximum temperature based on the baseline model is much lower than the ground truth one, which

TABLE II
STATISTICS OF MAXIMUM & MINIMUM TEMPERATURES OF THE BOTTOM CHIP BASED ON THERMAL RESISTANCES EXTRACTED BY DIFFERENT METHODS, TOGETHER WITH THE PERCENTAGE ERRORS (IN BRACKETS).

	numerical simulation [8]	baseline model [8], [21]	our model
maximum temperature	112.3 °C	106.5 °C (-5.2%)	114.3 °C (+1.8%)
minimum temperature	84.0 °C	85.6 °C (+1.9%)	85.4 °C (+1.7%)

may lead to an over-optimistic thermal design power. On the contrary, our model can help provide more faithful temperature predictions for 3-D ICs. The statistics of the minimum temperatures of the bottom chip are also listed, where our model also leads slightly in accuracy. Besides, the absolute percentage error in maximum temperatures of the low-resolution case is 6.7%, indicating the necessity for considering high-resolution distribution of BEOL thermal resistances during the thermal analysis of 3-D ICs.

VI. CONCLUSION

In this work, we propose a novel closed-form analytical model for the z-direction thermal resistance of BEOL interconnects based on the the theory of resistor network and the Woodbury formula. Our model takes the detailed via connectivity into consideration and reveals many implications which are overlooked by the previous model. Owing to the explicit consideration of via connectivity, our model achieves a 3.4× improvement in accuracy compared with the previous model, with negligible time overhead. This enables us to perform efficient and accurate high-resolution full-chip thermal resistance extraction of BEOL interconnects. Further thermal analysis of a 3-D IC based on the extracted thermal resistance maps shows that the absolute percentage error in maximum temperatures is only 1.8% for our model, while the previous model reaches an error of 5.2%, demonstrating the advantages of our model in high-resolution full-chip thermal analysis of 3-D ICs. In the future, we plan to further improve the accuracy of our model and apply it to more complex scenarios.

VII. ACKNOWLEDGMENT

This work was supported in part by the National Science Foundations of China (Grant No. 62125401), the 111 project (B18001), and the Beijing Outstanding Young Scientist Program (JWZQ20240101004).

REFERENCES

[1] V. Moroz, X. Xu, A. Svizhenko, X.-W. Lin, S. Popov, H. Sheng, and K. Larsen, "3dic system-technology co-optimization with a focus on the interplay of thermal, power, timing, and stress effects," in *2024*

IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits). IEEE, 2024, pp. 1–2.

[2] M. Pedram and S. Nazarian, "Thermal modeling, analysis, and management in vlsi circuits: Principles and methods," *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1487–1501, 2006.

[3] B. Vermeersch, S. Mishra, M. Brunion, O. Zografos, M. Lofrano, H. Oprins, J. Myers, Z. Tokei, and G. Hellings, "Multiscale thermal impact of bspdn: Soc hotspot challenges and partial mitigation," in *2024 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2024, pp. 1–4.

[4] T.-Y. Chen, K. Chuang, W. Hung, T.-S. Lin, and Y.-M. Chen, "Package-system thermal modeling and new material," in *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*. IEEE, 2024, pp. 1–2.

[5] Y. Chen, S. Mishra, J. Ryckaert, D. Biswas, and J. Myers, "Late breaking results: Thermal feasibility of backside integrated LDOs in 2.5d/3d system-in-package using nanosheet technology," in *2025 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, 2025.

[6] Q. Wang, T. Zhu, Y. Lin, R. Wang, and R. Huang, "Atsim3d: Towards accurate thermal simulator for heterogeneous 3d-ic systems considering nonlinear leakage and conductivity," in *2024 2nd International Symposium of Electronics Design Automation (ISEDA)*. IEEE, 2024, pp. 618–623.

[7] Q. Wang, T. Zhu, Y. Lin, R. Wang, and R. Huang, "Atsim3.5d: A multiscale thermal simulator for 3.5d-ic systems based on nonlinear multigrid method," in *2025 3rd International Symposium of Electronics Design Automation (ISEDA)*. IEEE, 2025.

[8] X. Chang, H. Oprins, B. Vermeersch, V. Cherman, M. Lofrano, S. Park, Z. Tokei, and I. De Wolf, "Experimentally validated thermal modeling prediction for beol and bspdn stacks," in *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)*. IEEE, 2024, pp. 498–505.

[9] X. Chang, H. Oprins, M. Lofrano, V. Cherman, B. Vermeersch, J. D. Fortuny, S. Park, Z. Tokei, and I. De Wolf, "Calibrated fast thermal calculation and experimental characterization of advanced beol stacks," in *2023 IEEE International Interconnect Technology Conference (IITC) and IEEE Materials for Advanced Metallization Conference (MAM)(IITC/MAM)*. IEEE, 2023, pp. 1–3.

[10] M. Lofrano, H. Oprins, V. Cherman, L. Witters, A. Jourdain, G. Van der Plas, and E. Beyne, "Block level and package level thermal assessment for back side power delivery network." in *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)*. IEEE, 2024, pp. 1036–1043.

[11] M. Lofrano, H. Oprins, X. Chang, B. Vermeersch, O. V. Pedreira, A. Lesniewska, V. Cherman, I. Ciofi, K. Croes, S. Park *et al.*, "Towards accurate temperature prediction in beol for reliability assessment," in *2023 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2023, pp. 1–7.

[12] D. Ingerly, S. Amin, L. Aryasomayajula, A. Balankutty, D. Borst, A. Chandra, K. Cheemalapati, C. Cook, R. Criss, K. Enamul *et al.*, "Foveros: 3d integration and the use of face-to-face chip stacking for logic devices," in *2019 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2019, pp. 19–6.

[13] S.-W. Kim, M. Detalle, L. Peng, P. Nolmans, N. Heylen, D. Velenis, A. Miller, G. Beyer, and E. Beyne, "Ultra-fine pitch 3d integration using face-to-face hybrid wafer bonding combined with a via-middle through-silicon-via process," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*. IEEE, 2016, pp. 1179–1185.

[14] J. J. S. Berru, S. Nicolas, N. Bresson, M. Assous, and S. Borel, "Demonstration of a wafer level face-to-back (f2b) fine pitch cu-cu hybrid bonding with high density tsv for 3d integration applications," in *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*. IEEE, 2023, pp. 97–102.

[15] E. Colgan, R. Polastre, J. Knickerbocker, J. Wakil, J. Gambino, and K. Tallman, "Measurement of back end of line thermal resistance for 3d chip stacks," in *29th IEEE Semiconductor Thermal Measurement and Management Symposium*. IEEE, 2013, pp. 23–28.

[16] J.-Y. Yan, S.-R. Jan, Y.-J. Peng, H. Lin, W. Wan, Y.-H. Huang, B. Hung, K.-T. Chan, M. Huang, M.-T. Yang *et al.*, "Thermal resistance modeling of back-end interconnect and intrinsic finfets, and transient simulation of inverters with capacitive loading effects," in *2016 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2016, pp. 35–6.

[17] E. Bury, B. Kaczer, S. Van Beek, and D. Lintern, "Experimental extraction of beol composite equivalent thermal conductivities for application in self-heating simulations," in *2018 48th European Solid-State Device Research Conference (ESSDERC)*. IEEE, 2018, pp. 186–189.

[18] V. Cherman, S. Van Huylenbroeck, M. Lofrano, X. Chang, H. Oprins, M. Gonzalez, G. Van der Plas, G. Beyer, K. Rebibis, and E. Beyne, "Thermal, mechanical and reliability assessment of hybrid bonded wafers, bonded at 2.5 μm pitch," in *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*. IEEE, 2020, pp. 548–553.

[19] J. Liu, Y. Li, D. Lu, S. Cao, and N. Sridhar, "Real-time evaluation of effective thermal conductivity profile for the redistribution layer (rdl)," in *2024 IEEE 26th Electronics Packaging Technology Conference (EPTC)*. IEEE, 2024, pp. 1187–1191.

[20] A. Labun and K. Jagjitkumar, "Rapid detailed temperature estimation for highly coupled ic interconnect," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 10, pp. 1840–1851, 2008.

[21] C. Xu, L. Jiang, S. K. Kolluri, B. J. Rubin, A. Deutsch, H. Smith, and K. Banerjee, "Fast 3-d thermal analysis of complex interconnect structures using electrical modeling and simulation methodologies," in *Proceedings of the 2009 International Conference on Computer-Aided Design*, 2009, pp. 658–665.

[22] T.-Y. Chiang, K. Banerjee, and K. C. Saraswat, "Analytical thermal model for multilevel vlsi interconnects incorporating via effect," *IEEE Electron Device Letters*, vol. 23, no. 1, pp. 31–33, 2002.

[23] L. Jiang, C. Xu, B. J. Rubin, A. J. Weger, A. Deutsch, H. Smith, A. Caron, and K. Banerjee, "A thermal simulation process based on electrical modeling for complex interconnect, packaging, and 3di structures," *IEEE transactions on advanced packaging*, vol. 33, no. 4, pp. 777–786, 2010.

[24] T.-Y. Chiang and K. C. Saraswat, "Closed-form analytical thermal model for accurate temperature estimation of multilevel ulsi interconnects," in *2003 Symposium on VLSI Circuits. Digest of Technical Papers (IEEE Cat. No. 03CH37408)*. IEEE, 2003, pp. 275–278.

[25] C. Wang, Q. Xu, C. Nie, H. Cao, J. Liu, D. Zhang, and Z. Li, "A multiscale anisotropic thermal model of chiplet heterogeneous integration system," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 32, no. 1, pp. 178–189, 2023.

[26] Y. Pi, N. Wang, J. Chen, M. Miao, Y. Jin, and W. Wang, "Anisotropic equivalent thermal conductivity model for efficient and accurate full-chip-scale numerical simulation of 3d stacked ic," *International journal of heat and mass transfer*, vol. 120, pp. 361–378, 2018.

[27] J.-H. Chern, J. Huang, L. Arledge, P.-C. Li, and P. Yang, "Multilevel metal capacitance models for cad design synthesis systems," *IEEE Electron Device Letters*, vol. 13, no. 1, pp. 32–34, 1992.

[28] U. Choudhury and A. Sangiovanni-Vincentelli, "Automatic generation of analytical models for interconnect capacitances," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 14, no. 4, pp. 470–480, 1995.

[29] S.-C. Wong, G.-Y. Lee, and D.-J. Ma, "Modeling of interconnect capacitance, delay, and crosstalk in vlsi," *IEEE Transactions on semiconductor manufacturing*, vol. 13, no. 1, pp. 108–111, 2000.

[30] F.-Y. Wu, "Theory of resistor networks: the two-point resistance," *Journal of Physics A: Mathematical and General*, vol. 37, no. 26, p. 6653, 2004.

[31] J. Rommes and W. H. Schilders, "Efficient methods for large resistor networks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, no. 1, pp. 28–39, 2009.

[32] W. W. Hager, "Updating the inverse of a matrix," *SIAM review*, vol. 31, no. 2, pp. 221–239, 1989.

[33] L. Chen, S. X.-D. Tan, Z. Sun, S. Peng, M. Tang, and J. Mao, "A fast semi-analytic approach for combined electromigration and thermomigration analysis for general multisegment interconnects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 2, pp. 350–363, 2020.

[34] M. Eslami, J. Knechtel, O. Sinanoglu, R. Karri, and S. Pagliarini, "Benchmarking advanced security closure of physical layouts: Ispd 2023 contest," in *Proceedings of the 2023 International Symposium on Physical Design*, 2023, pp. 256–264.

[35] S. Ladenheim, Y.-C. Chen, M. Mihajlović, and V. F. Pavlidis, "The mta: An advanced and versatile thermal simulator for integrated systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 12, pp. 3123–3136, 2018.

[36] "Ansys Icepak," https://www.ansys.com/products/electronics/ansys-icepak.

[37] Y. Shi, C. Gao, W. Ren, S. Xu, K. Xue, M. Yuan, C. Qian, and Z.-H. Zhou, "Open3dbench: Open-source benchmark for 3d-ic backend implementation and ppa evaluation," *arXiv preprint arXiv:2503.12946*, 2025.