

林亦波

助理教授 ◊ 设计自动化与计算系统系 ◊ 集成电路学院 ◊ 北京大学
yibolin@pku.edu.cn ◊ www.yibolin.com

研究方向

面向超大规模集成电路设计自动化的建模和优化、深度学习及其应用、异构计算

教育经历

- 德克萨斯大学奥斯汀分校

2013 年 8 月 – 2018 年 5 月

博士学位, 电子与计算机工程系

指导老师: David Z. Pan

博士毕业论文: “Bridging Design and Manufacturing Gap through Machine Learning and Machine-Generated Layout”
- 上海交通大学

2009 年 9 月 – 2013 年 6 月

学士学位, 微电子学院

工作经历

- 北京大学 (Peking University)

2019 年 7 月 – 现在

助理教授

集成电路学院设计自动化与计算系统系 (自 2021 年 11 月)

信息科学技术学院高能效计算与应用中心
- 德克萨斯大学奥斯汀分校 (UT Austin)

2018 年 6 月 – 2019 年 6 月

博后

授课经历

- | | | |
|----|--------------|--------------------|
| 主讲 | 设计自动化与计算系统导论 | 研究生课, 2022 年秋 |
| 主讲 | 芯片设计自动化与智能优化 | 本科生课, 2021-2022 年春 |
| 主讲 | 计算概论 B | 本科生课, 2020-2022 年秋 |

奖项及荣誉

- | | | |
|----------------------|--------|--------|
| 首届最佳审稿人奖 | ICCAD | 2023 年 |
| 最佳论文 (4/205) | DATE | 2023 年 |
| 最佳论文 (4/249) | DATE | 2022 年 |
| 最佳论文提名 | ICCAD | 2022 年 |
| 最佳论文 (2/3495, 4 年总和) | TCAD | 2021 年 |
| 最佳论文 | ISPD | 2020 年 |
| 最佳论文提名 | ASPDAC | 2020 年 |

最佳论文 (1/201) & 提名 (5/201)	DAC	2019 年
最佳论文提名	ISPD	2019 年
首届最佳论文	Integration, the VLSI Journal	2018 年
Graduate Continuing Fellowship	德克萨斯大学奥斯汀分校	2017 年
Franco Cerrina Memorial 最佳学生论文	SPIE	2016 年
A. Richard Newton Young Student Fellow	DAC	2014 年
国家奖学金	上海交通大学	2012 年
三星奖学金	上海交通大学	2011 年
二等奖学金	上海交通大学	2010 年

学术服务

技术程序委员会成员

- ACM/IEEE Design Automation Conference (DAC): 2020.
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD): 2018, 2019, 2020, 2021.
- IEEE International Conference on Computer Design (ICCD): 2019.
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC): 2021, 2022.
- ACM International Symposium on Physical Design (ISPD): 2020.
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD): 2021.
- ACM Great Lakes Symposium on VLSI (GLVLSI): 2024.
- Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI): 2021.
- IEEE Electron Devices Technology and Manufacturing Conference (EDTM): 2021.
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS): 2022.

期刊审稿人

- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD).
- IEEE Transactions on Computers (TC).
- ACM Transaction on Design Automation of Electronic Systems (TODAES).
- SPIE Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3).
- Elsevier, Integration, the VLSI Journal (Integration).

期刊编辑

- ACM Transaction on Design Automation of Electronic Systems (TODAES) Special Issue on MLCAD, 2022.

执行委员会成员

- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD) 2021, financial chair.

出版物

书籍章节

- [B3] **Yibo Lin**, Zizheng Guo and Jing Mai, “[Deep Learning Framework for Placement](#)”, Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)
- [B2] Haoyu Yang, **Yibo Lin** and Bei Yu, “[Machine Learning for Mask Synthesis and Verification](#)”, Machine Learning Applications in Electronic Design Automation, Springer, 2023, edited by Haoxing Ren and Jiang Hu. (**Invited Book Chapter**)
- [B1] **Yibo Lin** and David Z. Pan, “[Machine Learning in Physical Verification, Mask Synthesis, and Physical Design](#)”, Machine Learning in VLSI Computer-Aided Design, Springer, 2018, edited by Abe Elfedel, Duane Boning and Xin Li. (**Invited Book Chapter**)

期刊论文

- [J51] Peiyu Liao, Dawei Guo, Zizheng Guo, Siting Liu, Zhitang Chen, Wenlong Lv, **Yibo Lin** and Bei Yu, “[DREAMPlace 4.0: Timing-driven Placement with Momentum-based Net Weighting and Lagrangian-based Refinement](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- [J50] Zuodong Zhang, Zizheng Guo, **Yibo Lin**, Runsheng Wang and Ru Huang, “[AVATAR: An Aging- and Variation-Aware Dynamic Timing Analyzer for Error-Efficient Computing](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- [J49] Binwu Zhu, Xinyun Zhang, **Yibo Lin**, Bei Yu and Martin Wong, “[DRC-SG 2.0: Efficient Design Rule Checking Script Generation via Key Information Extraction](#)”, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2023.
- [J48] Guannan Guo, Tsung-Wei Huang, **Yibo Lin**, Zizheng Guo, Sushma Yellapragada and Martin Wong, “[A GPU-accelerated Framework for Path-based Timing Analysis](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- [J47] Zizheng Guo, Tsung-Wei Huang and **Yibo Lin**, “[Accelerating Static Timing Analysis using CPU-GPU Heterogeneous Parallelism](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- [J46] Zhuomin Chai, Yuxiang Zhao, Wei Liu, **Yibo Lin**, Runsheng Wang and Ru Huang, “[Circuit-Net: An Open-Source Dataset for Machine Learning in VLSI CAD Applications with Improved Domain-Specific Evaluation Metric and Learning Strategies](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- [J45] Jing Mai, Jiarui Wang, Zhixiong Di and **Yibo Lin**, “[Multi-Electrostatic FPGA Placement Considering SLICEL-SLICEM Heterogeneity, Clock Feasibility, and Timing Optimization](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- [J44] Yufei Chen, Zizheng Guo, Runsheng Wang, Ru Huang, **Yibo Lin** and Cheng Zhuo, “[Dynamic Supply Noise Aware Timing Analysis With JIT Machine Learning Integration](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2023. (accepted)
- [J43] Zhixiong Di, Runzhe Tao, Jing Mai, Lin Chen and **Yibo Lin**, “[LEAPS: Topological-Layout-Adaptable Multi-Die FPGA Placement for Super Long Line Minimization](#)”, IEEE Transactions on Circuits and Systems I, Dec, 2023.

- [J42] Peiyu Liao, Yuxuan Zhao, Dawei Guo, **Yibo Lin** and Bei Yu, “[Analytical Die-to-Die 3D Placement With Bistratal Wirelength Model and GPU Acceleration](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2023. (accepted)
- [J41] Xiaohan Gao, Haoyi Zhang, Siyuan Ye, Mingjie Liu, David Z. Pan, Linxiao Shen, Runsheng Wang, **Yibo Lin** and Ru Huang, “[Post-Layout Simulation Driven Analog Circuit Sizing](#)”, SCIENCE CHINA Information Sciences, Oct, 2023.
- [J40] **Yibo Lin**, Avi Ziv and Haoxing Ren, “[Introduction to the Special Issue on Machine Learning for CAD/EDA](#)”, ACM Transactions on Design Automation of Electronic Systems (TODAES), Mar, 2023.
- [J39] Xinfu Zhang, Zuodong Zhang, **Yibo Lin**, Zhigang Ji, Runsheng Wang and Ru Huang, “[Efficient Aging-Aware Standard Cell Library Characterization Based on Sensitivity Analysis](#)”, IEEE Transactions on Circuits and Systems II: Express Briefs, Oct, 2022.
- [J38] Siting Liu, Yuan Pu, Peiyu Liao, Hongzhong Wu, Rui Zhang, Zhitang Chen, Wenlong Lv, **Yibo Lin** and Bei Yu, “[FastGR : Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2022.
- [J37] Zhuomin Chai, Yuxiang Zhao, **Yibo Lin**, Wei Liu, Runsheng Wang and Ru Huang, “[CircuitNet: An Open-Source Dataset for Machine Learning Applications in Electronic Design Automation \(EDA\)](#)”, SCIENCE CHINA Information Sciences, Sep, 2022.
- [J36] Xiaohan Gao, Haoyi Zhang, Mingjie Liu, Linxiao Shen, David Z. Pan, **Yibo Lin**, Runsheng Wang and Ru Huang, “[Interactive Analog Layout Editing with Instant Placement and Routing Legalization](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2022.
- [J35] Wei Li, Jialu Xia, Yuzhe Ma, Jialu Li, **Yibo Lin** and Bei Yu, “[Adaptive Layout Decomposition with Graph Embedding Neural Networks](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jan, 2022.
- [J34] **Yibo Lin**, “[模拟电路版图自动化与智能设计](#)”, 中国计算机学会通讯, Dec, 2021.
- [J33] Zizheng Guo, Mingwei Yang, Tsung-Wei Huang and **Yibo Lin**, “[A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Large Designs](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Nov, 2021.
- [J32] Martin Rapp, Hussam Amrouch, **Yibo Lin**, Bei Yu, David Z. Pan, Marilyn Wolf and Jörg Henkel, “[MLCAD: A Survey of Research in Machine Learning for CAD](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Nov, 2021. (**Invited Keynote paper**)
- [J31] **Yibo Lin**, Tong Qu, Zongqing Lu, Yajuan Su and Yayi Wei, “[Asynchronous Reinforcement Learning Framework and Knowledge Transfer for Net Order Exploration in Detailed Routing](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2021.

- [J30] Tsung-Wei Huang, Dian-Lun Lin, Chun-Xun Lin and **Yibo Lin**, “[Taskflow: A Lightweight Parallel and Heterogeneous Task Graph Computing System](#)”, IEEE Transactions on Parallel and Distributed Systems (TPDS), Aug, 2021.
- [J29] **Yibo Lin**, Xiaohan Gao, Tinghuan Chen and Bei Yu, “[机器学习辅助数字集成电路后端设计方法](#)”, 微纳电子与智能制造, Feb, 2021.
- [J28] Cheng Zhuo, Zizheng Guo, Xiao Dong, Qing He and **Yibo Lin**, “[先进工艺下的数字签核](#)”, 微纳电子与智能制造, Feb, 2021.
- [J27] Yibai Meng, Wuxi Li, **Yibo Lin** and David Z. Pan, “[elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jan, 2021.
- [J26] Wei Li, Yuzhe Ma, Qi Sun, Zhang Lu , **Yibo Lin**, Iris Hui-Ru Jiang, Bei Yu and David Z. Pan, “[OpenMPL: An Open Source Layout Decomposer](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Dec, 2020.
- [J25] Tsung-Wei Huang, **Yibo Lin**, Chun-Xun Lin, Guannan Guo and Martin Wong, “[Cpp-Taskflow: A General-purpose Parallel Task Programming System at Scale](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sep, 2020.
- [J24] Hao Chen, Mingjie Liu, Biying Xu, Keren Zhu, Xiyuan Tang, Shaolan Li, **Yibo Lin**, Nan Sun and David Z. Pan, “[MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII](#)”, IEEE Design & Test, Sep, 2020.
- [J23] Jing Chen, Mohamed Baker Alawieh, **Yibo Lin**, Maolin Zhang, Jun Zhang, Yufeng Guo and David Z. Pan, “[Automatic Selection of Structure Parameters of Silicon on Insulator Lateral Power Device Using Bayesian Optimization](#)”, IEEE Electron Device Letters (EDL), Aug, 2020.
- [J22] Ying Chen, **Yibo Lin**, Rui Chen, Lisong Dong, Ruixuan Wu, Tianyang Gai, Le Ma, Yajuan Su and Yayi Wei, “[EUV Multilayer Defect Characterization via Cycle-Consistent Learning](#)”, Optics Express, Jun, 2020.
- [J21] **Yibo Lin**, Zixuan Jiang, Jiaqi Gu, Wuxi Li, Shounak Dhar, Haoxing Ren, Brucek Khailany and David Z. Pan, “[DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2020. (**Best Paper Award**)
- [J20] Junzhe Cai, Changhao Yan, Yudong Tao, **Yibo Lin**, Sheng-Guo Wang, David Z. Pan and Xuan Zeng, “[A Novel and Unified Full-chip CMP Model Aware Dummy Fill Insertion Framework with SQP-Based Optimization Method](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2020.
- [J19] Mohamed Baker Alawieh, **Yibo Lin**, Zaiwei Zhang, Meng Li, Qixing Huang and David Z. Pan, “[GAN-SRAF: Sub-Resolution Assist Feature Generation using Generative Adversarial Networks](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May, 2020.
- [J18] **Yibo Lin**, Wuxi Li, Jiaqi Gu, Haoxing Ren, Brucek Khailany and David Z. Pan, “[ABCDPlace: Accelerated Batch-based Concurrent Detailed Placement on Multi-threaded CPUs and GPUs](#)”,

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Feb, 2020.

- [J17] Jing Chen, Mohamed Baker Alawieh, **Yibo Lin**, Maolin Zhang, Jun Zhang, Yufeng Guo and David Z. Pan, “[Powernet: SOI Lateral Power Device Breakdown Prediction With Deep Neural Networks](#)”, IEEE Access, Feb, 2020.
- [J16] Ying Chen, **Yibo Lin**, Lisong Dong, Tianyang Gai, Rui Chen, Yajuan Su, Yayi Wei and David Z. Pan, “[SoulNet: Ultrafast Optical Source Optimization Utilizing Generative Neural Networks for Advanced Lithography](#)”, Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), Nov, 2019.
- [J15] **Yibo Lin**, Meng Li, Yuki Watanabe, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima and David Z. Pan, “[Data Efficient Lithography Modeling with Transfer Learning and Active Data Selection](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct, 2019.
- [J14] Ying Chen, **Yibo Lin**, Tianyang Gai, Yajuan Su, Yayi Wei and David Z. Pan, “[Semi-Supervised Hotspot Detection with Self-Paced Multi-Task Learning](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Apr, 2019.
- [J13] Jing Chen, **Yibo Lin**, Yufeng Guo, Maolin Zhang, Mohamed Baker Alawieh and David Z. Pan, “[Lithography Hotspot Detection Using a Double Inception Module Architecture](#)”, Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), Mar, 2019.
- [J12] **Yibo Lin**, Bei Yu, Meng Li and David Z. Pan, “[Layout Synthesis for Topological Quantum Circuits with 1D and 2D Architectures](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Aug, 2018.
- [J11] Meng Li, Bei Yu, **Yibo Lin**, Xiaoqing Xu, Wuxi Li and David Z Pan, “[A practical split manufacturing framework for trojan prevention via simultaneous wire lifting and cell insertion](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2018.
- [J10] Xiaoqing Xu, **Yibo Lin**, Meng Li, Tetsuaki Matsunawa, Shigeki Nojima, Chikaaki Kodama, Toshiya Kotani and David Z. Pan, “[Subresolution Assist Feature Generation With Supervised Data Learning](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2018.
- [J9] **Yibo Lin**, Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J Alpert and David Z. Pan, “[MrDP: Multiple-row detailed placement of heterogeneous-sized cells for advanced nodes](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun, 2018.
- [J8] Wuxi Li, **Yibo Lin**, Meng Li, Shounak Dhar and David Z. Pan, “[UTPlaceF 2.0: A High-Performance Clock-Aware FPGA Placement Engine](#)”, ACM Transactions on Design Automation of Electronic Systems (TODAES), Jun, 2018.
- [J7] **Yibo Lin**, Bei Yu and David Z. Pan, “[High performance dummy fill insertion with coupling and uniformity constraints](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sep, 2017.

- [J6] **Yibo Lin**, Bei Yu, Biying Xu and David Z. Pan, “[Triple patterning aware detailed placement toward zero cross-row middle-of-line conflict](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2017.
- [J5] Xiaoqing Xu, **Yibo Lin**, Meng Li, Jiaojiao Ou, B. Cline and D. Z. Pan, “[Redundant local-Loop insertion for unidirectional routing](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul, 2017.
- [J4] **Yibo Lin**, Bei Yu, Yi Zou, Zhuo Li, Charles J Alpert and David Z. Pan, “[Stitch aware detailed placement for multiple e-beam lithography](#)”, Integration, the VLSI Journal, Jun, 2017. (**Best Paper Award**)
- [J3] **Yibo Lin**, Xiaoqing Xu, Bei Yu, Ross Baldick and David Z. Pan, “[Triple/quadruple patterning layout decomposition via linear programming and iterative rounding](#)”, Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), Jun, 2017.
- [J2] Bei Yu, Xiaoqing Xu, Subhendu Roy, **Yibo Lin**, Jiaojiao Ou and David Z. Pan, “[Design for manufacturability and reliability in extreme-scaling VLSI](#)”, Science China Information Sciences, May, 2016. (**Invited paper**)
- [J1] Bei Yu, Xiaoqing Xu, Jih-Rong Gao, **Yibo Lin**, Zhuo Li, Charles Alpert and David Z. Pan, “[Methodology for standard cell compliance and detailed placement for triple patterning lithography](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May, 2015.

会议论文

- [C103] Tsung-Yi Ho, Sadaf Khan, Jinwei Liu, Yi Liu, Zhengyuan Shi, Ziyi Wang, Qiang Xu, Evangeline F.Y. Young, Bei Yu, Ziyang Zheng, Binwu Zhu, Keren Zhu, Yiqi Che, Yun Liang, **Yibo Lin**, Guojie Luo, Guangyu Sun, Runsheng Wang, Xinming Wei, Chenhao Xue, Haoyi Zhang, Zuodong Zhang, Yuxiang Zhao, Sunan Zou, Lei Chen, Yu Huang, Min Li, Dimitrios Tsaras, Mingxuan Yuan, Hui-Ling Zhen, Zhufei Chu, Wenji Fang, Xingquan Li and Zhiyao Xie, “[The Dawn of AI-Native EDA: Promises and Challenges of Large Circuit Models](#)”, arXiv preprint, 2024.
- [C102] Jiarui Wang, Xun Jiang and **Yibo Lin**, “Top-Level Routing for Multiply-Instantiated Blocks with Topology Hashing”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun, 2024.
- [C101] Yufan Du, Zizheng Guo, Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin**, Runsheng Wang and Ru Huang, “PowPrediCT: Cross-Stage Power Prediction with Circuit-Transformation-Aware Learning”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun, 2024.
- [C100] Haoyi Zhang, Jiahao Song, Xiaohan Gao, Xiyuan Tang, **Yibo Lin**, Runsheng Wang and Ru Huang, “EasyACIM: An End-to-End Automated Analog CIM with Synthesizable Architecture and Agile Design Space Exploration”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun, 2024.
- [C99] Zichen Kong, Xiyuan Tang, Wei Shi, Yiheng Du, **Yibo Lin** and Yuan Wang, “PVTsizing: A Turbo-RL-Based Batch-Sampling Optimization Framework for PVT-Robust Analog Circuit Synthesis”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun, 2024.

- [C98] Yuan Pu, Fangzhou Liu, Yu Zhang, Zhuolun He, Kai-Yuan Chao, **Yibo Lin** and Bei Yu, “Lesyn: Placement-aware Logic Resynthesis for Non-Integer Multiple-Cell-Height Designs”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun, 2024.
- [C97] Wan Luan Lee, Dian-Lun Lin, Tsung-Wei Huang, Shui Jiang, Tsung-Yi Ho, **Yibo Lin** and Bei Yu, “G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jun, 2024.
- [C96] Xiaohan Gao, Haoyi Zhang, Zhu Pan, **Yibo Lin**, Runsheng Wang and Ru Huang, “Migrating Standard Cells for Multiple Drive Strengths by Routing Imitation”, IEEE/ACM International Symposium of EDA (ISEDA), Xi’an, China, May 10-13, 2024.
- [C95] Qipan Wang, Tianxiang Zhu, **Yibo Lin**, Runsheng Wang and Ru Huang, “ATSim3D: Towards Accurate Thermal Simulator for Heterogeneous 3D IC Systems Considering Nonlinear Leakage and Conductivity”, IEEE/ACM International Symposium of EDA (ISEDA), Xi’an, China, May 10-13, 2024.
- [C94] Jing Mai, Jiarui Wang, Yifan Chen, Zizheng Guo, Xun Jiang, Yun Liang and **Yibo Lin**, “Open-PARF 3.0: Robust Multi-Electrostatics Based FPGA Macro Placement Considering Cascaded Macros Groups and Fence Regions”, IEEE/ACM International Symposium of EDA (ISEDA), Xi’an, China, May 10-13, 2024.
- [C93] Xun Jiang, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin**, Runsheng Wang and Ru Huang, “[Circuit-Net 2.0: An Advanced Dataset for Promoting Machine Learning Innovations in Realistic Chip Design Environment](#)”, International Conference on Learning Representations (ICLR), Vienna, Austria, May 7-11, 2024.
- [C92] Zizheng Guo, Tsung-Wei Huang, Jin Zhuo, Cheng Zhuo, **Yibo Lin**, Runsheng Wang and Ru Huang, “[Heterogeneous Static Timing Analysis with Advanced Delay Calculator](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.
- [C91] Haoyi Zhang, Xiaohan Gao, Zilong Shen, Jiahao Song, Xiaoxu Cheng, Xiyuan Tang, **Yibo Lin**, Runsheng Wang and Ru Huang, “[SAGERoute 2.0: Hierarchical Analog and Mixed Signal Routing Considering Versatile Routing Scenarios](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), Valencia, Spain, Mar 24-28, 2024.
- [C90] Yuan Pu, Tinghuan Chen, Zhuolun He, Chen Bai, Haisheng Zheng, **Yibo Lin** and Bei Yu, “[IncreMacro: Incremental Macro Placement Refinement](#)”, ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024. (**Best Paper Nomination**)
- [C89] Yu Zhang, Yuan Pu, Fangzhou Liu, Peiyu Liao, Kaiyuan Chao, Keren Zhu, **Yibo Lin** and Bei Yu, “[Multi-Electrostatics Based Placement for Non-Integer Multiple-Height Cells](#)”, ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.
- [C88] Siting Liu, Jiayi Jiang, Zhuolun He, Ziyi Wang, **Yibo Lin** and Bei Yu, “[Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs](#)”, ACM International Symposium on Physical Design (ISPD), Taipei, Mar 12-15, 2024.
- [C87] Cheng-Hsiang Chiu, Zhicheng Xiong, Zizheng Guo, Tsung-Wei Huang and **Yibo Lin**, “[An Efficient Task-parallel Pipeline Programming Framework](#)”, International Conference on High-

Performance Computing in Asia-Pacific Region (HPC Asia), Nagoya, Japan, Jan, 2024. (accepted)

- [C86] Jing Mai, Jiaru Wang, Zhixiong Di, Guojie Luo, Yun Liang and **Yibo Lin**, “[OpenPARF: An Open-Source Placement and Routing Framework for Large-Scale Heterogeneous FPGAs with Deep Learning Toolkit](#)”, International Conference on ASIC (ASICON), Nanjing, China, Oct, 2023. (**Invited paper**)
- [C85] Yifan Chen, Zaiwen Wen, Yun Liang and **Yibo Lin**, “[Stronger Mixed-Size Placement Backbone Considering Second-Order Information](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct, 2023.
- [C84] Xun Jiang, Zizheng Guo, Zhuomin Chai, Yuxiang Zhao, **Yibo Lin**, Runsheng Wang and Ru Huang, “[Accelerating Routability and Timing Optimization with Open-Source AI4EDA Dataset CircuitNet and Heterogeneous Platforms](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, Oct, 2023. (**Invited paper**)
- [C83] Kexing Zhou, Yun Liang, **Yibo Lin**, Runsheng Wang and Ru Huang, “[Khronos: Fusing Memory Access for Improved Hardware RTL Simulation](#)”, IEEE/ACM International Symposium on Microarchitecture (MICRO), Toronto, Canada, Oct, 2023.
- [C82] Zizheng Guo, Zuodong Zhang, Xun Jiang, Wuxi Li, **Yibo Lin**, Runsheng Wang and Ru Huang, “General-Purpose Gate-Level Simulation with Partition-Agnostic Parallelism”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.
- [C81] Qipan Wang, Ping Liu, Liguang Jiang, Mingjie Liu, **Yibo Lin**, Runsheng Wang and Ru Huang, “MTL-Designer: An Integrated Flow for Analysis and Synthesis of Microstrip Transmission Line”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.
- [C80] Peiyu Liao, Hongduo Liu, **Yibo Lin**, Bei Yu and Martin Wong, “On a Moreau Envelope Wirelength Model for Analytical Global Placement”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.
- [C79] Siting Liu, Ziyi Wang, Fangzhou Liu, **Yibo Lin**, Bei Yu and Martin Wong, “Concurrent Sign-off Timing Optimization via Deep Steiner Points Refinement”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.
- [C78] Su Zheng, Lancheng Zou, Siting Liu, **Yibo Lin**, Bei Yu and Martin Wong, “Mitigating Distribution Shift for Congestion Optimization in Global Placement”, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul 9-13, 2023.
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专利

- [P10] **林亦波**, 郭资政, “一种可微分时序驱动的芯片布局优化方法”, Chinese Patent, CN202210793017.1, Aug 29, 2022. (submitted)
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特邀报告

国际会议特邀报告

- [T7] “Tutorial: Deep Learning Enabled Timing Optimization in Physical Design”, in ACM/IEEE Design Automation Conference (DAC), San Francisco, Jul 9-13, 2023.
- [T6] “Timing Analysis and Optimization on Heterogeneous CPU-GPU Platforms”, in International Workshop on Logic & Synthesis (IWLS), Virtual, Jul 18-21, 2022.
- [T5] “DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement”, in ACM/IEEE Design Automation WebiNar (DAWN), Virtual, Apr 11-12, 2022.
- [T4] “DREAMPlace 3.X: Exploring Advanced Constraints and Multi-GPU Acceleration”, in China Semiconductor Technology International Conference (CSTIC), Shanghai, China, Mar 14-15, 2021.
- [T3] “Deep Learning for Mask Synthesis and Verification: A Survey”, in IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 18-21, 2021.

- [T2] "Tutorial: GPU Acceleration in VLSI Back-end Design: Overview and Case Studies", in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Virtual, Nov 2-5, 2020.
- [T1] "DREAMPlace 2.0: Open-Source GPU-Accelerated Global and Detailed Placement for Large-Scale VLSI Designs", in China Semiconductor Technology International Conference (CSTIC), Shanghai, China, Jun 26, 2020.

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- [T7] "A Timing Engine Inspired Graph Neural Network Model for Pre-Routing Slack Prediction", CCF Chip 芯片大会, 南京, Jul 29-31, 2022.
- [T6] "Exploring AI-assisted Optimization Opportunities in Placement and Routing", 华为 Strategy and Technology Workshop (STW), 深圳, Oct 14-16, 2021.
- [T5] "A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Static Timing Analysis", ChinaDA, 北京, Jul 10-11, 2021.
- [T4] "深度学习辅助布局布线优化", 中国计算机协会青年精英大会 (CCF-YEF), 沈阳, May 15, 2021.
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