芯片设计自动化与智能优化
Optimization and Machine Learning in VLSI Design Automation

林亦波，北京大学高能效计算与应用中心助理教授。2013 年毕业于上海交通大学微电子系，获得理学学士学位。此后分别于 2017 年和 2018 年在美国德克萨斯大学奥斯汀分校电子与计算机工程系获得硕士和博士学位。2019 年 6 月加入北京大学信息科学技术学院。他曾获 2020 年国际物理设计专题研讨会（ISPD）、2019 年设计自动化大会（DAC）、2018 年 Integration 期刊、2016 年 SPIE Advanced Lithography 会议的最佳论文奖。他目前的研究兴趣包括基于机器学习的设计自动化算法以及 GPU/FPGA 加速。

参考书

Handbook of Algorithms for Physical Design Automation
Charles J. Alpert, Dinesh p. Mehta, Sachin S. Sapatnekar

- Item Weight : 4.32 pounds
- Hardcover : 1024 pages
- ISBN-10 : 0849372429
- ISBN-13 : 978-0849372421
- Product Dimensions : 7.2 x 2 x 10 inches
- Publisher : Auerbach Publications; 1st Edition (November 12, 2008)

简介，中英文

本课程将向学生介绍计算机辅助大规模芯片设计的自动化算法（EDA，是现代芯片产业的重要组成部分），包括：逻辑综合、布局布线、时序分析、基于机器学习的自动化算法及硬件加速、可制造性优化、FPGA 芯片布局布线、热门课题等等。同时，该课程会辅以实际 EDA 软件应用项目开发，从而使学生获得近距离设计和应用自动化算法的机会。该课程由本人主讲，并鼓励和指导学生参与国内外 EDA 竞赛。本课程将采用中英文双语教学，面向对 EDA 未来发展感兴趣的，具有一定创新精神，对科研学术有一定兴趣的本科学生。本课程的学习对于帮助学生深入理解计算机辅助芯片设计，设计和应用算法/软件解决实际问题，建立全面科学的知识体系，激发学生的求知欲和创新潜能，具有重要的意义。

This is an undergraduate-level course on electronic design automation (EDA) for modern integrated circuits (or we call computer aided design, CAD). This course provides an overview of the fundamental IC design flow and algorithms, including logic synthesis, placement and routing, timing analysis, etc. We will also cover the most recent progress in machine learning assisted EDA, hardware acceleration, design for manufacturability, FPGA CAD, and so on. In the

course project, we encourage students to participate international CAD contests and interact with researchers all over the world. Students will receive a systematic study of CAD algorithms and learn to develop algorithms and software to automate modern IC design.

开课计划承诺/开设历史

1. 开课计划和开课承诺：注明未来三年计划开课学期及其他相关承诺
计划未来三年每年春季学期开课。
2. 开课历史：无

课程大纲

1. 课程基本目的
a. 在理论方面
   1) 了解基本芯片设计流程步骤;
   2) 了解芯片设计流程中各步骤常用算法，包括图算法、数学规划等;
   3) 了解 EDA 算法中的常见数据结构，如网表、多边形存储等;
   4) 了解机器学习、硬件加速等技术在 EDA 算法中的应用。
b. 在实践方面
   1) 掌握从实际设计问题抽象到计算机算法和数学问题的能力;
   2) 熟练使用 C/C++等语言实现高效 EDA 算法;
   3) 简历编写和维护较大 codebase 系统的能力。

内容提要及相应学时分配

1. Introduction: from electric symbols to the real physical world 基础背景介绍 (4 学时)
More details:
   a) We will introduce how a circuit is designed and implemented in the physical world.
   b) We will cover the typical design flow and methodology widely used in the industry.
   c) We will highlight the fundamental challenges from high level.

2. Logic synthesis: manipulating circuit graph / 逻辑综合 (8 学时)
   a. Logic optimization / 逻辑优化（4 学时）
   b. Technology mapping / 工艺映射（4 学时）
More details:
   a) We will introduce how we represent the circuit in a graph and optimize the circuits with graph transformation.
   b) We will cover common operations for logic optimization.
   c) We will formulate the mathematical problems for technology mapping and explore potential solutions.

3. Placement: from facility location problem to ASIC placement / 布局 (8 学时)

a. Partitioning / 分割（2 学时）
b. Floorplanning / 布图规划（2 学时）
c. Placement / 布局（4 学时）

More details:

a) We will introduce typical problems in placement and their relationship with well-known problems in operating research.
b) We will introduce the algorithm development for partitioning, floorplanning, and placement in the history.
c) We will learn to formulate integer programming and nonlinear optimization problems for placement related tasks.

4. Routing: from vehicle routing to VLSI routing / 布线 (8 学时)

a. Tree generation / 布线拓扑树生成（2 学时）
b. Routing / 布线（4 学时）
c. Track assignment / 布线轨道分配（2 学时）

More details:

a) We will introduce typical routing flow for large-scale IC designs.
b) We will extend the minimum spanning tree, Prim, and Dijkstra algorithms for tree generation.
c) We will explain the widely-used A* shortest path and maze routing algorithms for IC routing.
d) We will introduce relaxation techniques for solving NP-hard problems.

5. Timing analysis / 时序分析 (8 学时)

a. Wire delay models / 互联线延迟模型（2 学时）
b. Static timing analysis / 静态时序分析（4 学时）
c. Incremental timing and CPPR / 递进式分析和悲观路径过滤（2 学时）

More details:

a) We will introduce various delay modeling techniques and their mathematical insights.
b) We will explain the standard procedure on static timing analysis and related graph traversal tasks.
c) We will expand to recent topics on incremental timing analysis and common pessimism path removal and the emerging computation challenges.

6. Advanced topics / 新兴技术 (8 学时)

a. Machine learning in EDA / 机器学习辅助 EDA（2 学时）
b. Distributed computing and hardware acceleration / 分布式计算与硬件加速（2 学时）
c. Design for manufacturability / 可制造性设计与优化（2 学时）
d. FPGA placement and routing / FPGA 芯片布局布线（2 学时）

More details:

a) We will cover the recent successful machine learning techniques for solving EDA problems.
b) We will introduce how to speedup the design flow with distributed computing and hardware acceleration.
c) We will introduce the design challenges in advanced technology nodes and explain what is design-technology co-optimization.
d) We will extend the placement and routing algorithms from ASIC to FPGA and learn the specific challenges.

7. Course project presentation / 课程项目展示 (4 学时)
More details:
a) Students will present their experience and results on the course projects and discuss with each other on how to improve the existing algorithms.

教学方式

课堂讲授（90%），讨论和报告（10%）

学生成绩评定办法

平时成绩 50%，其中包含平时课堂参与 10%，4 次 lab 作业（40%）
课程项目及展示 50%