Mengming Li

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Summary

I am a Ph.D. student at the Electronic and Computer Engineering Department of the Hong Kong University of Science and Technology (HKUST), advised by Prof. Zhiyao Xie. Before that, I obtained a master's degree from Zhejiang University, and a bachelor's degree from Guangdong Ocean University.

Education

Hong Kong University of Science and Technology Hong Kong, China
PhD September 2024 – Present
Supervisor: Zhiyao Xie.

Zhejiang University Zhejiang, China
Master September 2020 – March 2023
Supervisor: Kai Bu. *GPA: 3.76/4, rank: 1/48*

Guangdong Ocean University Guangdong, China
Bachelor September 2016 – June 2020
GPA: 3.69/5, rank: top 10%

Publications

Profile-Guided Temporal Prefetching
Mengming Li, Qijun Zhang, Yichuan Gao, Wenji Fang, Yao Lu, Yongqing Ren, and Zhiyao Xie.
*The 52th International Symposium on Computer Architecture (**ISCA 2025**).*

Integrating Prefetcher Selection with Dynamic Request Allocation Improves Prefetching Efficiency
Mengming Li, Qijun Zhang, Yongqing Ren, Zhiyao Xie.
*The 31th IEEE International Symposium on High-Performance Computer Architecture (**HPCA 2025**).*

unXpec: Breaking Undo-based Safe Speculation
Mengming Li, Chenlu Miao, Yilong Yang, Kai Bu.
*The 28th IEEE International Symposium on High-Performance Computer Architecture (**HPCA 2022**).* **(The first HPCA paper from Zhejiang University)**

TreasureCache: Hiding Cache Evictions against Side-Channel Attacks
Mengming Li, Kai Bu, Chenlu Miao, Kui Ren.
*IEEE Transactions on Dependable and Secure Computing (**TDSC**)*

PF-LLM: Large Language Model Hinted Hardware Prefetching
Ceyu Xu, Xiangfeng Sun, Weihang Li, Chen Bai, Bangyan Wang, **Mengming Li**, Zhiyao Xie, and Yuan Xie.
*ACM International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS 2026**) (**Corresponding Author**).*

SwiftDir: Secure Cache Coherence without Overprotection
Chenlu Miao, Kai Bu, **Mengming Li**, Shaowu Mao, Jianwei Jia.
*The 55th IEEE/ACM International Symposium on Microarchitecture (**MICRO 2022**).* **(The first MCIRO paper from Zhejiang University)**

Hitchhiker: Accelerating ORAM with Dynamic Scheduling
Jingsen Zhu, **Mengming Li**, Xingjian Zhang, Kai Bu, Miao Zhang, Tianqi Song.
*IEEE Transactions on Computers (**TC**)*

Research interests

CPU Core Design for Improving PPA (Performance, Power and Area)
Profile-Guided Optimizations (PGO)
Computer Architecture and Security, Side Channel Attacks and Defenses

Jobs

Intel Labs Beijing, China
Research Scientist April 2023 – September 2024
1. Profiling the memory access block of RISC-V CPU core to find the bottleneck.
2. Microarchitecture design (with simulator Gem5 and RTL language Chisel) for CPU cache and its prefetchers.
3. Collaborate with the backend team to optimize the PPA and timing for the designed microarchitectures.

Internship

Intel Labs Beijing, China
CPU Architecture Research Intern May 2022 – March 2023
Performance modeling and microarchitecture design on RISC-V CPU

China Southern Power Grid Guangzhou, China
Research Intern Jul 2021 – Aug 2021
Application of Security Chips in the power field

Awards & Honors

ISCA Travel Grant	2025
Outstanding Graduates of Zhejiang Province	2023
Outstanding Graduates of Zhejiang University	2023
National Scholarship	2022
Outstanding Graduates of Guangdong Ocean University	2020
Second Prize, National Computer Games Tournament (Chinese Association for Artificial Intelligence)	2018
Second-class Scholarship, Guangdong Ocean University	2017, 2018