1. Description

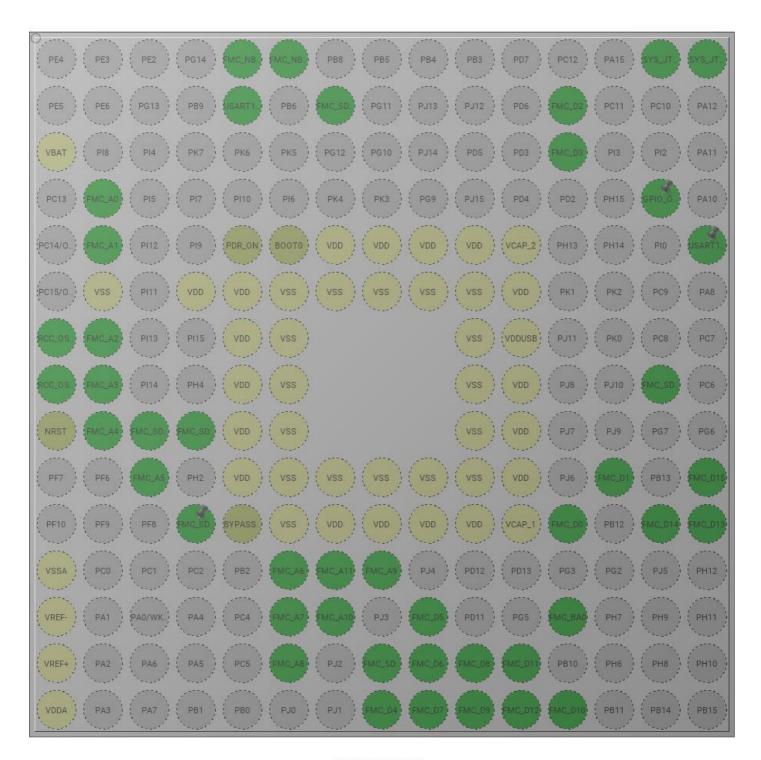
1.1. Project

Project Name	FMC_SDRAM
Board Name	32F746GDISCOVERY
Generated with:	STM32CubeMX 4.25.0
Date	05/11/2018

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746NGHx
MCU Package	TFBGA216
MCU Pin number	216

2. Pinout Configuration



STM32F746NGHx TFBGA216 (Top view)

3. Pins Configuration

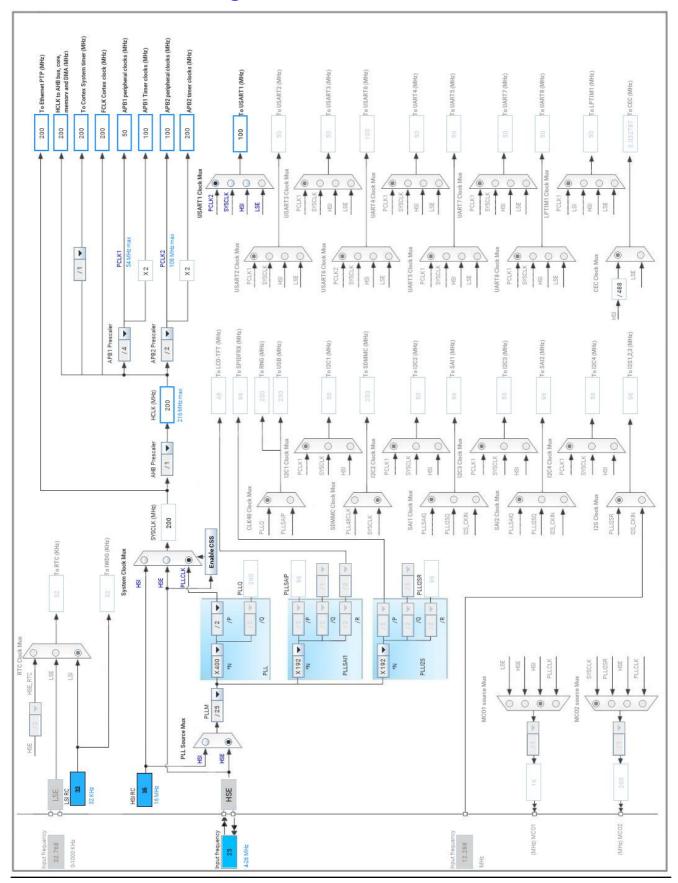
Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA216	(function after		Function(s)	
	reset)		(3)	
A5	PE1	I/O	FMC_NBL1	
A6	PE0	I/O	FMC_NBL0	
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
B5	PB7	I/O	USART1_RX	
B7	PG15	I/O	FMC_SDNCAS	
B12	PD0	I/O	FMC_D2	
C1	VBAT	Power	0_52	
C12	PD1	I/O	FMC_D3	
D2	PF0	I/O	FMC_A0	
D14	PI1 *	I/O	GPIO_Output	
E2	PF1	I/O	FMC_A1	
E5	PDR_ON	Reset	· ·	
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDD	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
E15	PA9	I/O	USART1_TX	
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	PF2	I/O	FMC_A2	
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	

Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA216	(function after		Function(s)	
11 50/1210	reset)		r directori(e)	
H2	PF3	I/O	FMC_A3	
H5	VDD		FIVIC_A3	
		Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDD	Power	FMO ODOLK	
H14	PG8	I/O	FMC_SDCLK	
J1	NRST PF4	Reset I/O	FMC A4	
J2			FMC_A4	
J3	PH5	1/0	FMC_SDNWE	
J4	PH3	I/O	FMC_SDNE0	
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
K3	PF5	I/O	FMC_A5	
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K13	PD15	I/O	FMC_D1	
K15	PD10	I/O	FMC_D15	
L4	PC3	I/O	FMC_SDCKE0	
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
L12	PD14	I/O	FMC_D0	
L14	PD9	I/O	FMC_D14	
L15	PD8	I/O	FMC_D13	
M1	VSSA	Power		
M6	PF12	I/O	FMC_A6	
M7	PG1	I/O	FMC_A11	
M8	PF15	I/O	FMC_A9	

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
N1	VREF-	Power		
N6	PF13	I/O	FMC_A7	
N7	PG0	I/O	FMC_A10	
N9	PE8	I/O	FMC_D5	
N12	PG4	I/O	FMC_BA0	
P1	VREF+	Power		
P6	PF14	I/O	FMC_A8	
P8	PF11	I/O	FMC_SDNRAS	
P9	PE9	I/O	FMC_D6	
P10	PE11	I/O	FMC_D8	
P11	PE14	I/O	FMC_D11	
R1	VDDA	Power		
R8	PE7	I/O	FMC_D4	
R9	PE10	I/O	FMC_D7	
R10	PE12	I/O	FMC_D9	
R11	PE15	I/O	FMC_D12	
R12	PE13	I/O	FMC_D10	

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



Page 6

5. IPs and Middleware Configuration

5.1. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 2 banks

Address: 12 bits Data: 16 bits

Byte enable: 16-bit byte enable

5.1.1. SDRAM 1:

SDRAM control:

Bank SDRAM bank 1

Number of column address bits 8 bits

Number of row address bits 12 bits

CAS latency 2 memory clock cycles *

Write protection Disabled

SDRAM common clock 2 HCLK clock cycles *

SDRAM common burst read Enabled *

SDRAM common read pipe delay 0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay 2 *

Exit self-refresh delay 6 *

Self-refresh time 4 *

SDRAM common row cycle delay 6 *

Write recovery time 2 *

SDRAM common row precharge delay 2 *

Row to column delay 2 *

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 6 WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Over Drive Enabled

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

5.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.4. USART1

Mode: Asynchronous

5.4.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity) *

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable
TX Pin Active Level Inversion Disable
RX Pin Active Level Inversion Disable
Data Inversion Disable
TX and RX Pins Swapping Disable

Overrun Enable
DMA on RX Error Enable
MSB First Disable

* User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
		_		·	, ,	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PH0/OSC_I N	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_O UT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
USART1	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PI1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable Preenmption Priority		SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true 0		0	
PVD interrupt through EXTI line 16		unused		
Flash global interrupt		unused		
RCC global interrupt	unused			
USART1 global interrupt	unused			
FMC global interrupt	unused			
FPU global interrupt	unused			

^{*} User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746NGHx
Datasheet	027590_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	FMC_SDRAM
Project Folder	/home/eivanov/stm32/edu/FMC_SDRAM
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.11.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	

9. Software Pack Report