9.3 Loopback Output Timing

Loopback strobe LBDQS to Loopback data LBDQ relationship is illustrated in Figure 203.

- tLBQSH describes the single-ended LBDQS strobe high pulse width
- tLBQSL describes the single-ended LBDQS strobe low pulse width
- tLBDQSQ describes the latest valid transition of LBDQ measured at both rising and falling edges of LBDQS
- tLBQH describes the earliest invalid transition of LBDQ measured at both rising and falling edges of LBDQS
- tLBDVW describes the data valid window per device per UI and is derived from (tLBQH-tLBDQSQ) of each UI on a given DRAM

Table 439 — Loopback Output Timing Parameters for DDR5-3200 to 4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback Timing													
Loopback LBDQS Output Low Time	tLBQSL	0.7	-	0.7	-	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.7	-	0.7	-	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK/2	1
Loopback LBDQ Output Time from LBDQS	tLBQH	3.6	-	3.6	-	3.6	-	3.6	-	3.6	-	tCK/2	1
Loopback Data valid window (tLBQH-tLBDQSQ) of each UI per DRAM	tLBDVW	3.4	-	3.4	-	3.4	-	3.4	-	3.4	-	tCK/2	1
NOTE 1 Based on Loopback 4-way interleave setting (see Section 3.5.54)													

Table 440 — Loopback Output Timing Parameters for DDR5-5200 to 6400

Speed		DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback Timing											
Loopback LBDQS Output Low Time	tLBQSL	TBD	-	TBD	-	TBD	-	TBD	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	TBD	-	TBD	-	TBD	-	TBD	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	TBD	-	TBD	-	TBD	-	TBD	-	tCK/2	1
Loopback LBDQ Output Time from LBDQS	tLBQH	TBD	-	TBD	-	TBD	-	TBD	-	tCK/2	1
Loopback Data valid window (tLBQH-tLBDQSQ) of each UI per DRAM	tLBDVW	TBD	-	TBD	-	TBD	-	TBD	-	tCK/2	1
NOTE 1 Based on Loopback 4-way interleave setting (see Section 3.5.54)											

9.3 Loopback Output Timing (Cont'd)

Table 441 — Loopback Output Timing Parameters for DDR5-6800 to 8400

Speed		DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback Timing													
Loopback LBDQS Output Low Time	tLBQSL	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	tCK/2	1
Loopback LBDQ Output Time from LB-DQS	tLBQH	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	tCK/2	1
Loopback Data valid window (tLBQH-tLBDQSQ) of each UI per DRAM	tLBDVW	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	tCK/2	1

Note(s):
1: Based on Loopback 4-way interleave setting (see MR53)

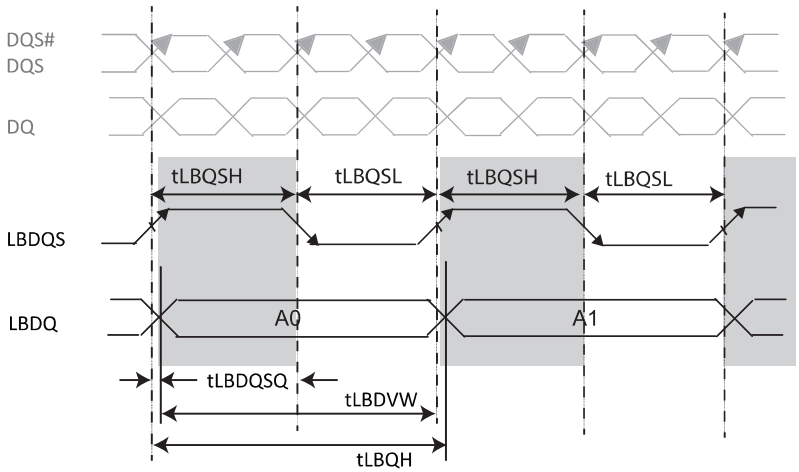

Figure 203 — Loopback Strobe to Data Relationship

9.3.1 Alert_n Output Drive Characteristic

A functional representation of the output buffer is shown in Figure 204. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |} \quad \text{under the condition that } RON_{Pu} \text{ is off}$$

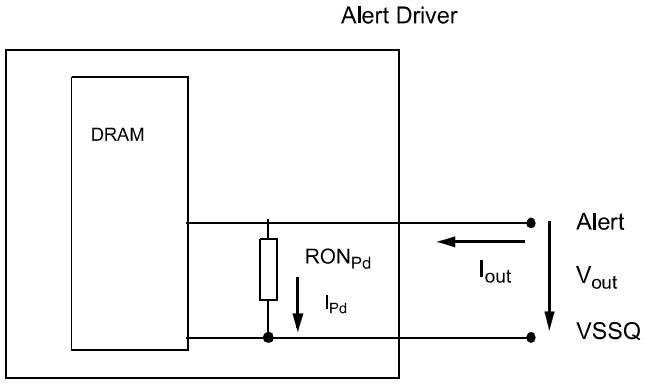

Figure 204 — Output Buffer Function

Table 442 — RON_{Pd} Vout Values

Resistor	Vout	Min	Max	Unit	NOTE
RON_{Pd}	VOLdc= 0.1* VDDQ	0.3	1.1	$R_{ZQ}/7$	
	V_{OMdc} = 0.8* VDDQ	0.4	1.1	$R_{ZQ}/7$	
	V_{OHdc} = 0.95* VDDQ	0.4	1.25	$R_{ZQ}/7$	

9.3.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied to the Test Output Pin during Connectivity Test (CT) Mode.

The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|Iout|}$$

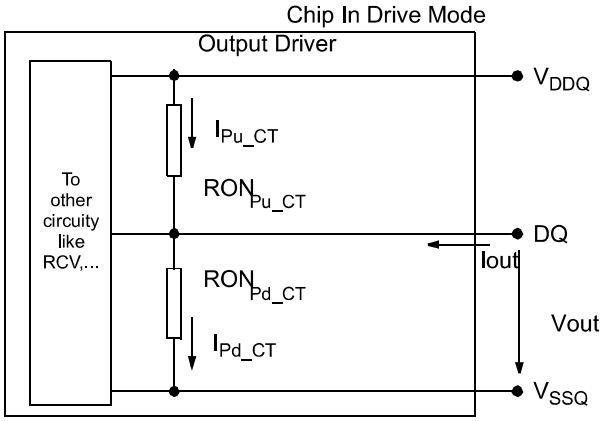

Figure 205 — Output Driver

Table 443 — RONNOM_CT Vout Values

RONNOM_CT	Resistor	Vout	Max	Units	NOTE
34Ω	RONPd_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2
	RONPu_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2

NOTE 1 Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.
NOTE 2 Uncalibrated drive strength tolerance is specified at +/- 30%