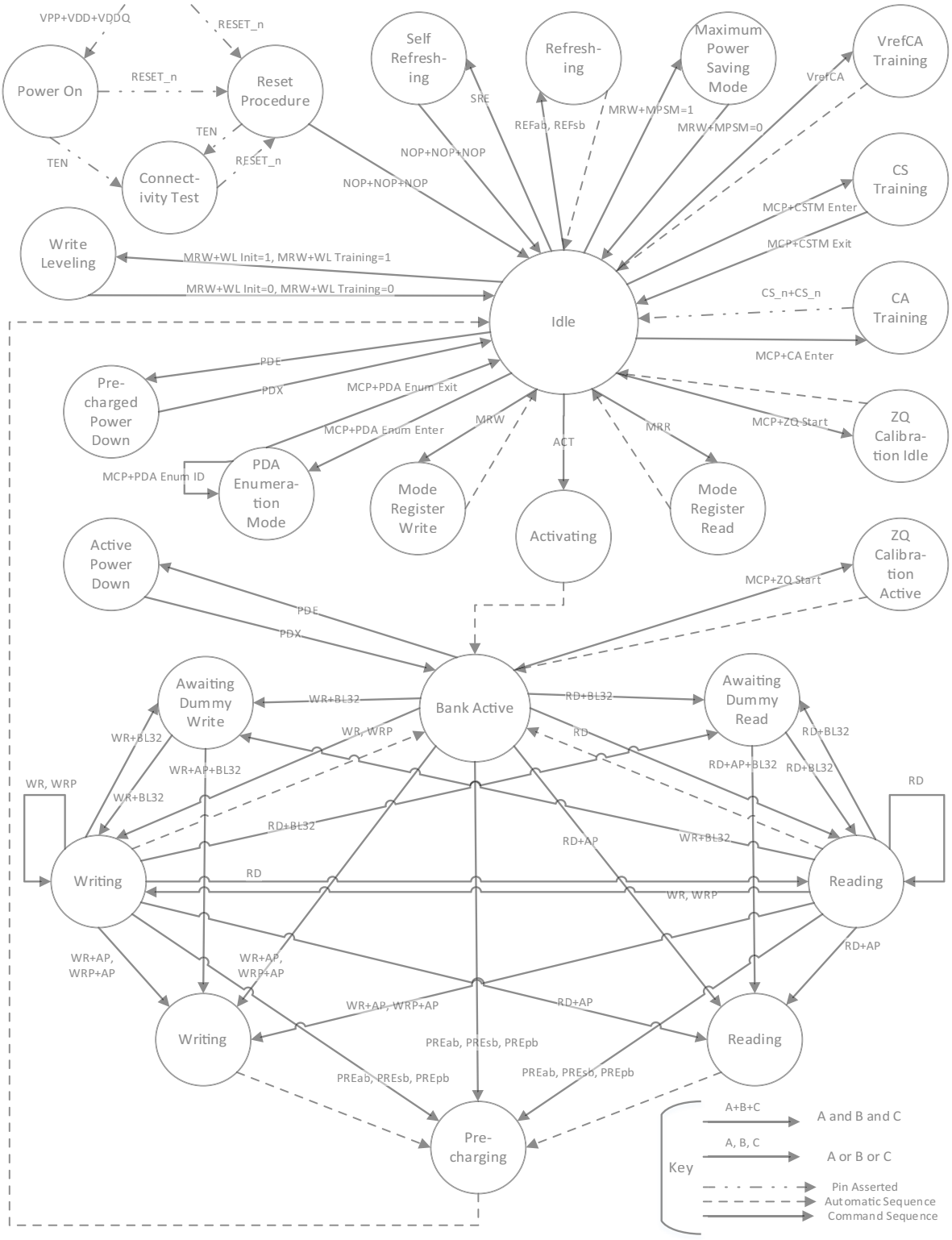
3 Functional Description

3.1 Simplified State Diagram



LIGHT GREY - All Light Grey text is defined as something that should be considered TBD. The content may be accurate or the same as previous technologies but has not yet been reviewed or determined to be the working assumption.

4 DDR5 SDRAM Command Description and Operation

4.1 Command Truth Table

- Notes 1, 2 & 14 apply to the entire Command truth table
- To improve command decode time, the table has been optimized to orient all 1-cycle commands together and all 2-cycle commands together; allowing CA1 to be used to identify the difference between a 1-cycle and a 2-cycle command.

[BG=Bank Group Address, BA=Bank Address, R=Row Address, C=Column Address, MRA=Mode Register Address, OP=Op Code, CID=Chip ID, DDPID=Dual Die Package ID, CW=Control Word, X=Don't Care, V=Valid].

Table 241 — Command Truth Table

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Activate	ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2/ DDPID	11,17,20,21, 23,24
		H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/ R17	
RFU	RFU	L	H	L	L	L	L	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
RFU	RFU	L	**H**	**L**	**L**	**L**	**H**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	
		H	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	
Write Pattern	WRP	L	**H**	**L**	**L**	**H**	**L**	**H**	**BA0**	**BA1**	**BG0**	**BG1**	**BG2**	**CID0**	**CID1**	**CID2/ DDPID**	**11,15,18,19, 20,21,23,24**
		H	**V**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**	**V**	**H**	**H**	**V**	**CID3**	
Write Pattern w/ Auto Precharge	WRPA	L	**H**	**L**	**L**	**H**	**L**	**H**	**BA0**	**BA1**	**BG0**	**BG1**	**BG2**	**CID0**	**CID1**	**CID2/ DDPID**	**11,15,18,19, 20,21,23,24**
		H	**V**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**	**V**	**AP=L**	**H**	**V**	**CID3**	
RFU	RFU	L	**H**	**L**	**L**	**H**	**H**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	
		H	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	
Mode Register Write	MRW	L	H	L	H	L	L	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V/ DDPID	8,11,13,20, 22,23,24
		H	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	V	CW	V	V	V	
Mode Register Read	MRR	L	H	L	H	L	H	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V/ DDPID	8,13,20,22, 23,24,25,26
		H	L	L	V	V	V	V	V	V	V	V	CW	V	V	V	
Write	WR	L	**H**	**L**	**H**	**H**	**L**	**BL*=L**	**BA0**	**BA1**	**BG0**	**BG1**	**BG2**	CID0	**CID1**	**CID2/ DDPID**	**8,12,15,19, 20,21,23,24**
		H	**V**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**	**V**	**H**	WR_ Partial=L	**V**	**CID3**	
Write w/Auto Precharge	WRA	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2/ DDPID	8,12,15,19, 20,21,23,24
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=L	WR_ Partial=L	V	CID3	
Read	RD	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2/ DDPID	8,15,19,20, 21,23,24
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	H	V	V	CID3	
Read w/Auto Precharge	RDA	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2/ DDPID	8,15,19,20, 21,23,24
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=L	V	V	CID3	
VrefCA Command	VrefCA	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	L	V/ DDPID	22,23,24
VrefCS Command	VrefCS	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	H	V/ DDPID	22,23,24
Refresh All	REFab	L	H	H	L	L	H	CID3	V	V	V or RIR	H	L	CID0	CID1	CID2/ DDPID	3,21,23,24, 27, 28
Refresh Management All	RFMab	L	H	H	L	L	H	CID3	V	V	V	L	L	CID0	CID1	CID2/ DDPID	3,20,21,23, 24
Refresh Same Bank	REFsb	L	H	H	L	L	H	CID3	BA0	BA1	V or RIR	H	H	CID0	CID1	CID2/ DDPID	4,20,21,23, 24,27, 28
Refresh Management Same Bank	RFMsb	L	H	H	L	L	H	CID3	BA0	BA1	V	L	H	CID0	CID1	CID2/ DDPID	4,20,21,23, 24
Precharge All	PREab	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2/ DDPID	5,20,21,23, 24
Precharge Same Bank	PREsb	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2/ DDPID	6,20,21,23, 24

Table 241 — Command Truth Table (Cont'd)

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Precharge	PREpb	L	H	H	L	H	H	CID3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2/ DDPID	7,20,21,23, 24
RFU	RFU	L	H	H	H	L	L	V	V	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	L	H	H	H	L	H	V	V	V	V	H	L	V	V	V	9
Self Refresh Entry w/ Frequency Change	SREF	L	H	H	H	L	H	V	V	V	V	L	L	V	V	V	9
Power Down Entry	PDE	L	H	H	H	L	H	V	V	V	V	V	H	ODT=L	V	V	10,16
MPC	MPC	L	H	H	H	H	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V/ DDPID	20,22,23,24
NOP	NOP	L	H	H	H	H	H	V	V	V	V	V	V	V	V	V	
Power Down Exit	PDX	L	H	H	H	H	H	V	V	V	V	V	V	V	V	V	
Deselect	DES	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

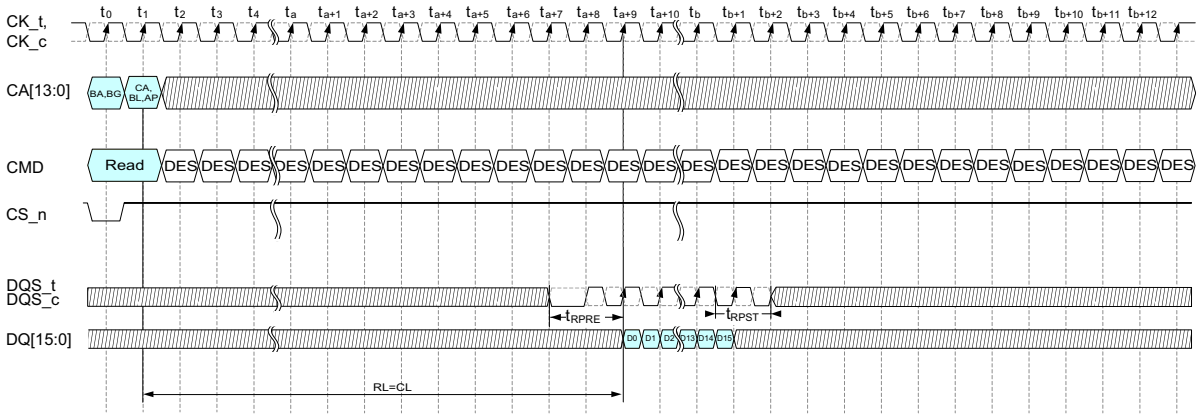
NOTE 1 V means H or L (a defined logic level). X means don't care in which case the signal may be floated.
NOTE 2 Bank group addresses BG[2:0] and Bank addresses BA[1:0] determine which bank is to be operated upon in a specific bank group.
NOTE 3 The Refresh All and Refresh Management All commands are applied to all banks in all bank groups. CA6 and CA7 are required to be valid ("V")
NOTE 4 The Refresh Same Bank and Refresh Management Same Bank commands refresh the same bank in all bank group bits. The bank bits, BA0 and BA1 on CA6 and CA7, respectively, specify the bank within each bank group.
NOTE 5 The Precharge All command applies to all open banks in all bank groups.
NOTE 6 The Precharge Same Bank command applies to the same bank in all bank groups. The bank bits specify the bank within each bank group.
NOTE 7 The Precharge command applies to a single bank as specified by bank address and bank group bits.
NOTE 8 CS_n=LOW during the 2nd cycle of a two cycle command controls ODT in non-target ranks for WR, RD and MRR commands.
NOTE 9 The SRE command places the DRAM in self refresh state
NOTE 10 The PDE command places the DRAM in power down state
NOTE 11 Two cycle commands with no ODT control (ACT, MRW, WRP). DRAM does not execute the command if it receives CS as LOW on 2nd cycle.
NOTE 12 WR command with WR_partial = Low indicates a partial write command. This is to help DRAM start an internal read for 'read modify write'.
NOTE 13 If CW=Low during the MRW command then DRAM should execute the command, Mode Register will be written. If CW=HIGH then DRAM ignores the MRW command, and the Mode Register is not changed. During MRR commands the DRAM ignores the value of the CW bit, MRR will be executed if CW=Low or CW=High.
NOTE 14 CID[3:0] bits are used for 3DS stacking support.
NOTE 15 If CA5:BL*=L, the command places the DRAM into the alternate Burst mode described by MR0[1:0] instead of the default Burst Length 16 mode.
NOTE 16 ODT=L is defined to allow On Die Termination (ODT) to persist when the device is in Power Down Mode.
NOTE 17 CID3/R17 is a multi-mode pin allowing for either 16H 3DS stacking with the CID3 bit usage or R17 for high bit density monolithic usage. These usages are mutually exclusive.
NOTE 18 Write Pattern only supports BL16 and BL32.
NOTE 19 When CID3 is not used, its CA decode is VALID.
NOTE 20 In the case of a DRAM where the density or stacking doesn't require CA[13] the ball location for that function (considering the state of MIR) shall be connected to VDDQ, and the DRAM shall decode CA[13]=L so that the proper selection of die and RA is provided.
NOTE 21 CID2/DDPID is a multi-mode pin allowing for either 3DS stacking with CID2 or DDP packaging with DDPID. Use of 3DS and DDP are mutually exclusive.
NOTE 22 V/DDPID is a multi-mode pin where the DDPID is used for DDP packages only.
NOTE 23 Any command using DDPID shall issue a NOP to non-selected device.
NOTE 24 NT-ODT behavior is not influenced by DDPIP value
NOTE 25 CA[0:1] =[L:L] on the second cycle for burst ordering.
NOTE 26 When host issue MRR with CRC enabled, data comes out with CRC bit.
NOTE 27 If the Refresh Management Required bit is "0" (MR58 OP[0]=0), CA9 is only required to be valid ("V").
NOTE 28 If the Refresh Interval Rate indicator bit is disabled (MR4:OP[3]=0), CA8 is only required to be valid ("V"). If the Refresh Interval Rate indicator bit is enabled (MR4:OP[3]=1), the host will set CA8=H for REF commands issued at the 1x refresh interval rate and CA8=L for REF commands issued at the 2x refresh interval rate.

4.7 Read Operation

The Read Operation causes the DRAM to retrieve and output data stored in its array. The Read Operation is initiated by the Read Command during which the beginning column address and bank/group address for the data to be retrieved from the array is provided. The data is driven by the DRAM on its DQ pins RL (CL) cycles after the Read Command along with the proper waveform on the DQS inputs. Read Latency (RL or CL) is defined from the Read command to data and is not affected by the Read DQS offset timing (MR40 OP[2:0]).

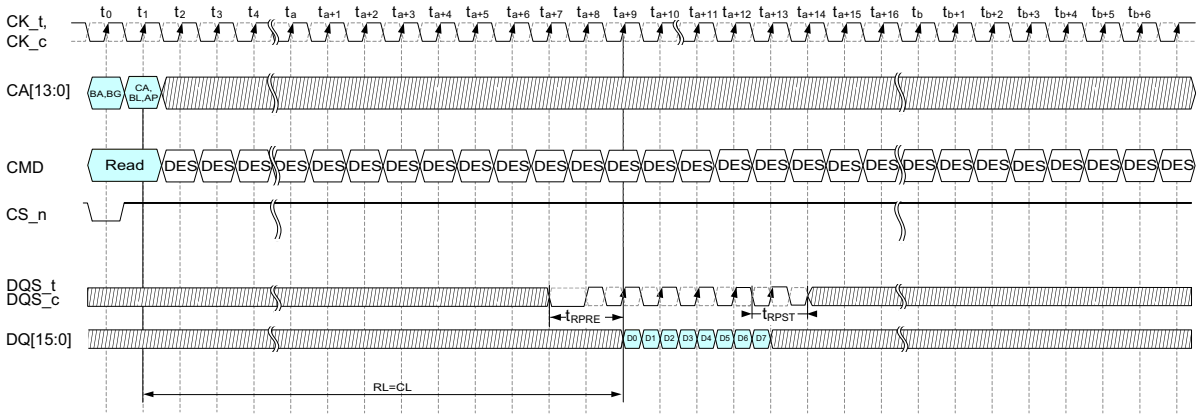
4.7.1 Read Burst Operation

During a READ or WRITE command, DDR5 shall support BC8, BL16, BL32 (optional) and BL32 OTF (optional) during the READ or WRITE. MR0[1:0] is used to select burst operation mode.



NOTE 1 BL=16, Preamble = 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 3 In this example, Read DQS Offset Timing is set to 0 Clocks.

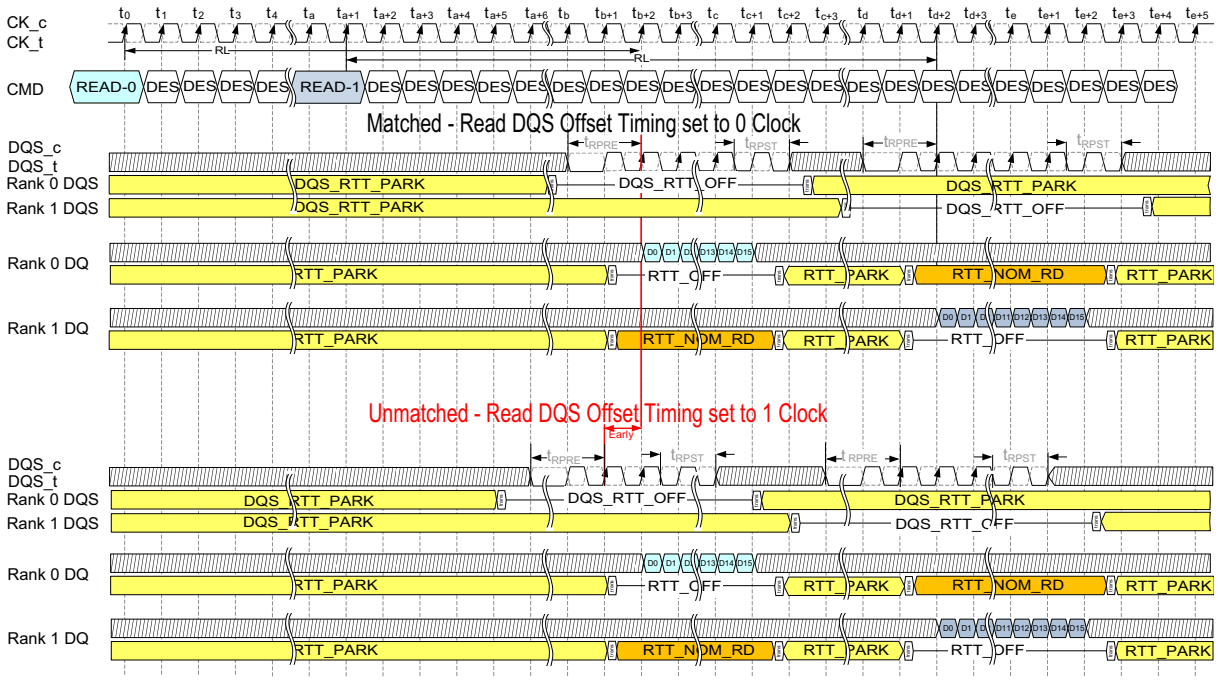
Figure 27 — Read Burst Operation (BL16)



NOTE 1 BC=8, Preamble = 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 3 In this example, Read DQS Offset Timing is set to 0 Clocks
NOTE 4 In non-CRC mode, DQS_t and DQS_c stop toggling at the completion of the BC8 data bursts, plus the postamble.

Figure 28 — Read Burst Operation (BC8)

4.7.1 Read Burst Operation (Cont'd)



NOTE 1 BL=16, Preamble = 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 3 Two different examples are shown side by side, the top with the default setting for Read DQS Offset = 0 Clock, the lower with a 1 Clock setting. In the lower case, the DQS is started 1 clock earlier than normal with respect to RL (CL).
NOTE 4 In both cases, the Data does not move

Figure 29 — Read to Read, Different Ranks Operation with Read DQS Offset Usage (BL16)

4.7.2 Burst Read Operation Followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by tRTP.min. A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1 The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.
2 The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are shown in Figure 30 and Figure 31.