Seguridad Informatica - Fall 2024

Module IV: Physical security

Lecture 2

Cache-based side channels

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IMDEA Software Institute

Module IV

- Lecture 1 — Introduction
- Lecture 2 — Cache-based side channel attacks
- Lecture 3 — Speculative execution attacks
- Lecture 4 — Non-interference
- Lecture 5 — Automated detection of speculative leaks

Module IV

- Lecture 1 — Introduction
- Lecture 2 — Cache-based side channel attacks
- Lecture 3 — Speculative execution attacks
- Lecture 4 — Non-interference
- Lecture 5 — Automated detection of speculative leaks

Recommended readings

D. Osvik, A. Shamir, E. Tromer — Cache attacks and countermeasures: the case of AES

Available at https://eprint.iacr.org/2005/271.pdf

Y. Yarom, K. Falkner — Flush+Reload: a high resolution, low noise L3 cache side-channel attack

Available at https://www.usenix.org/system/files/conference/usenixsecurity14/sec14-paper-yarom.pdf

What is a side-channel attack?

What is a side-channel attack?

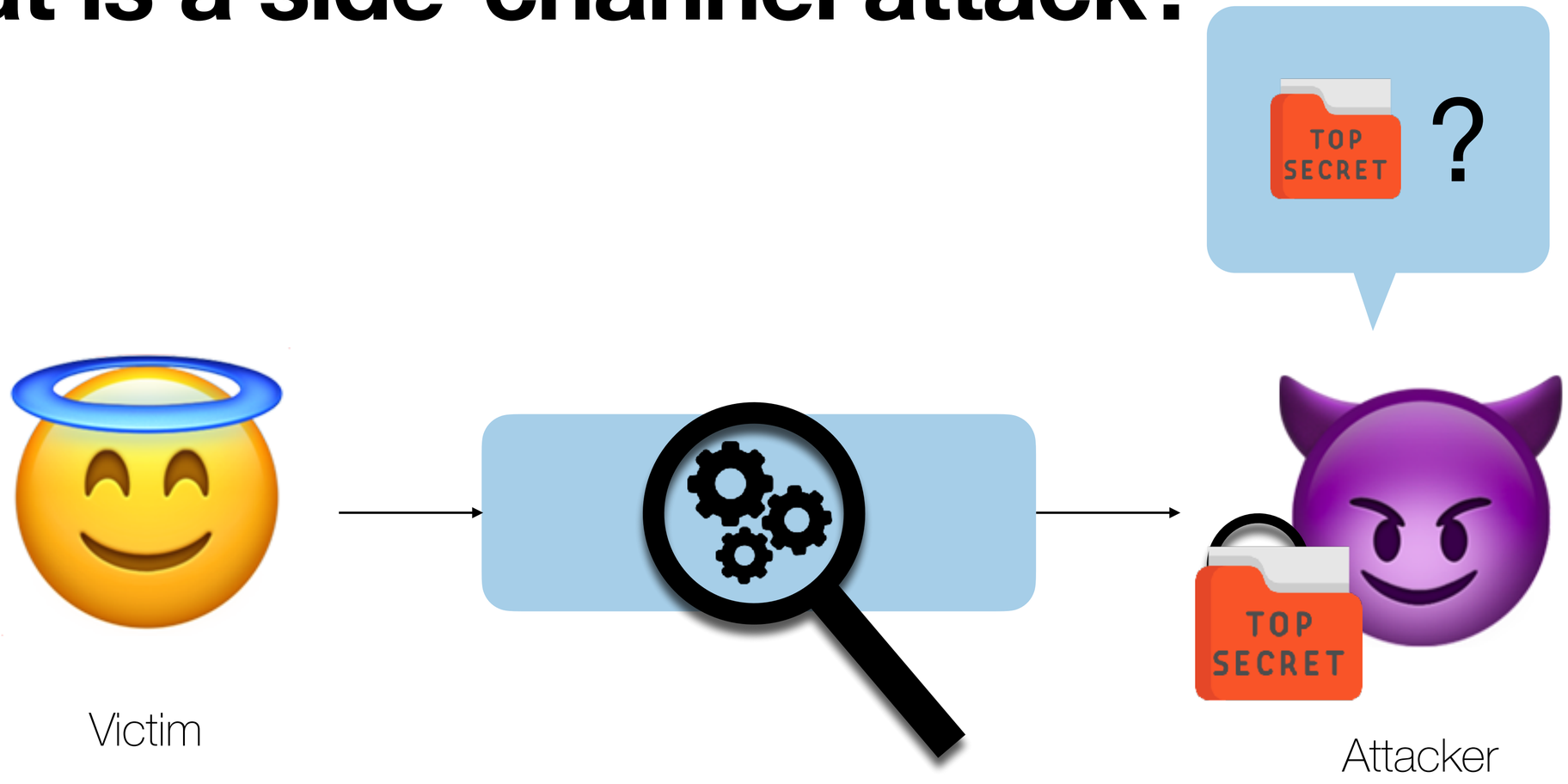
Victim

What is a side-channel attack?

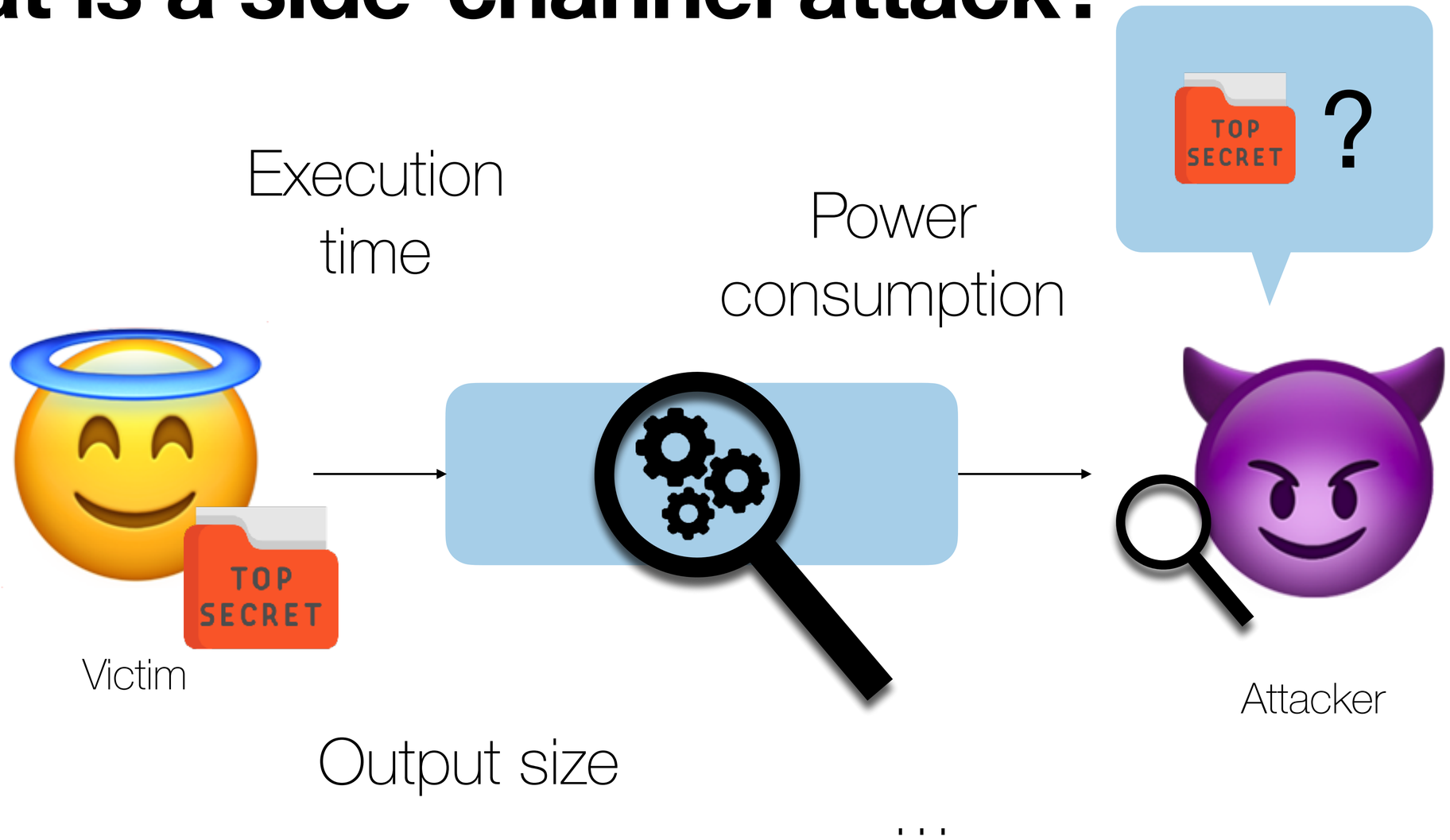
Victim

Attacker

What is a side-channel attack?



What is a side-channel attack?



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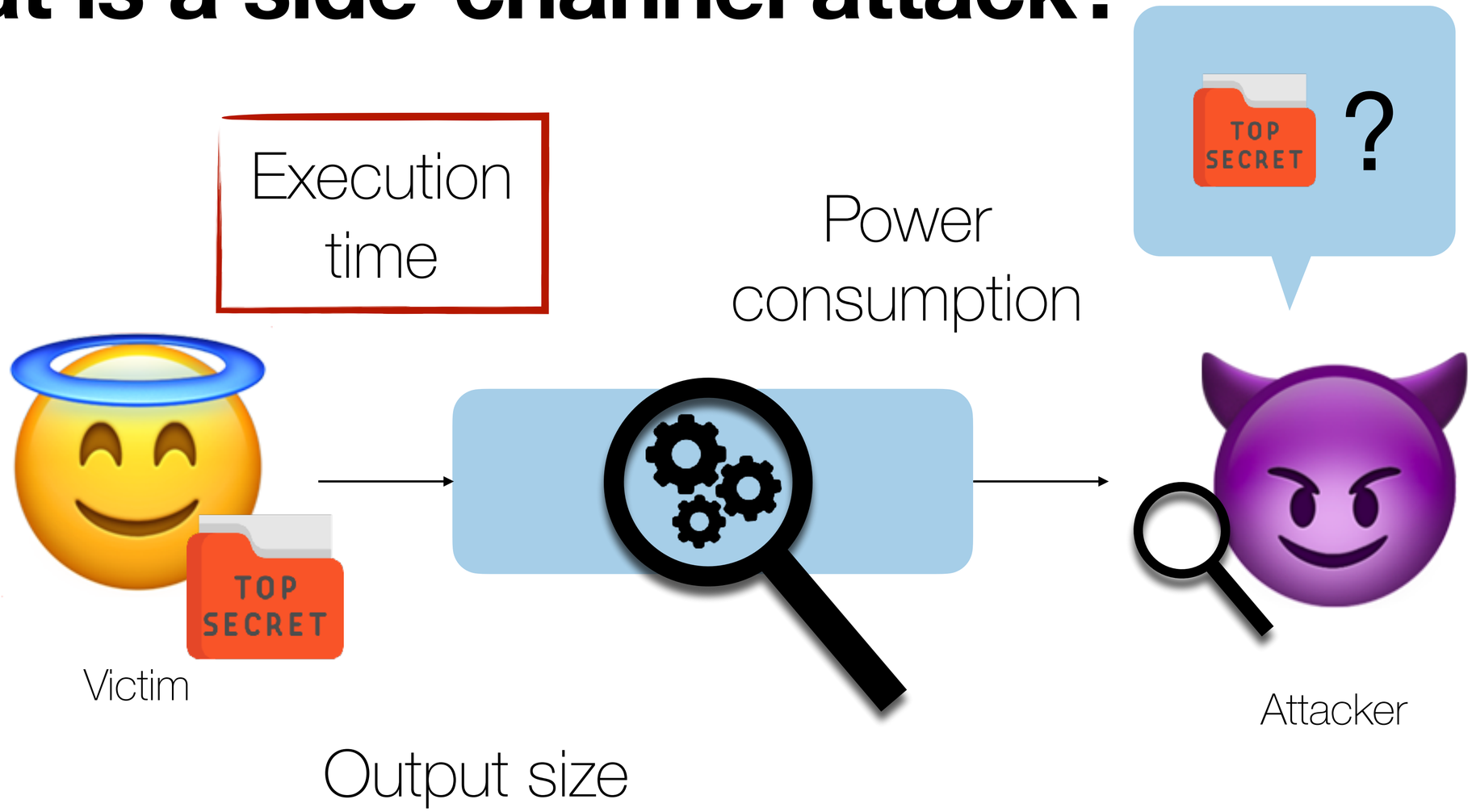
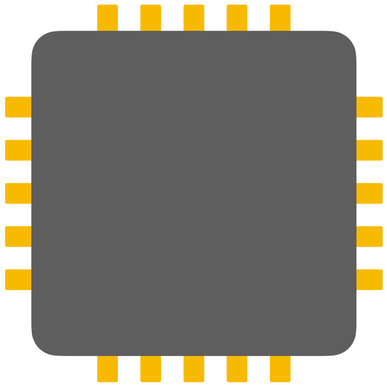
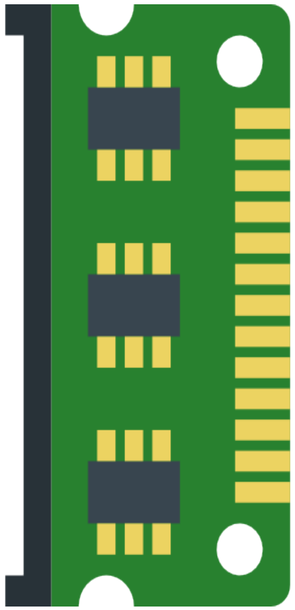


Processors and caches

Processors and memory



Processor

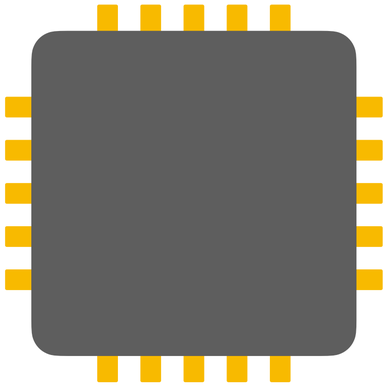


Main memory
(DRAM)

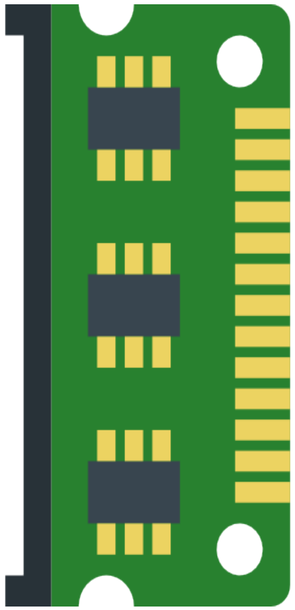
DRAM latency for Intel i7-4770 (Haswell)

Processors and memory

```
x = array[idx];
```



Processor



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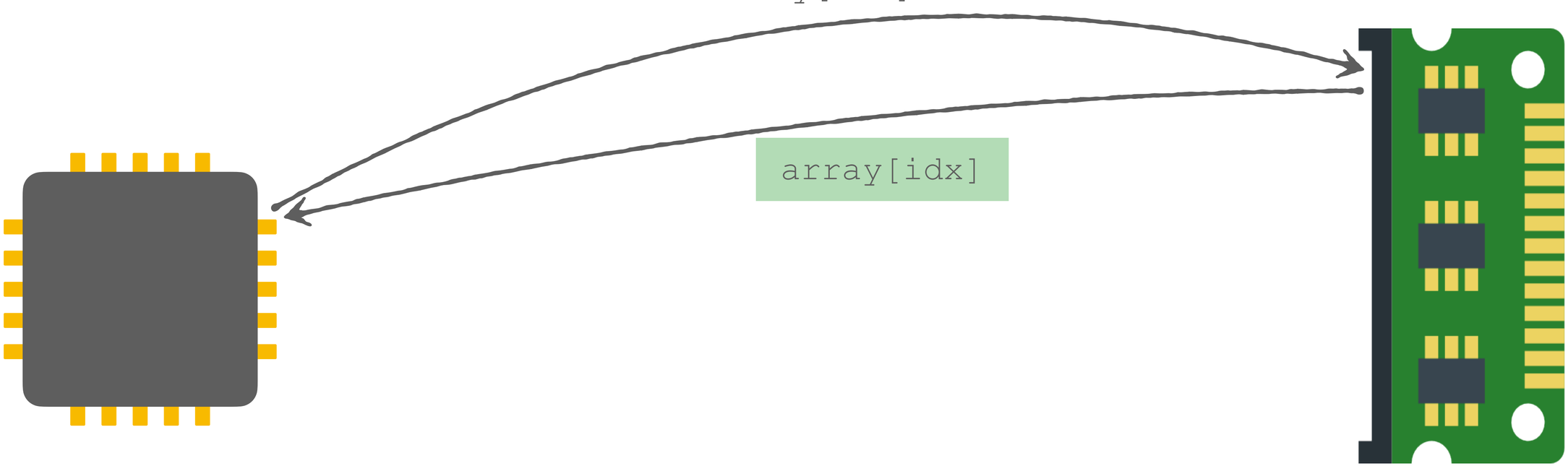
36 cycles + 57 ns / ~67 ns



DRAM latency for Intel i7-4770 (Haswell)

Processors and memory

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y = array[idx];
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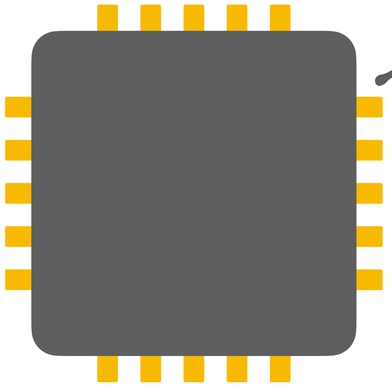
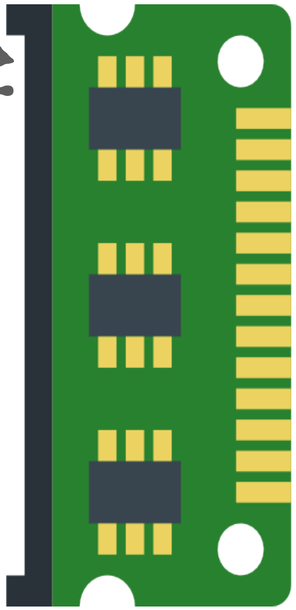
36 cycles + 57 ns / ~67 ns

array[idx]?

array[idx]



Processor



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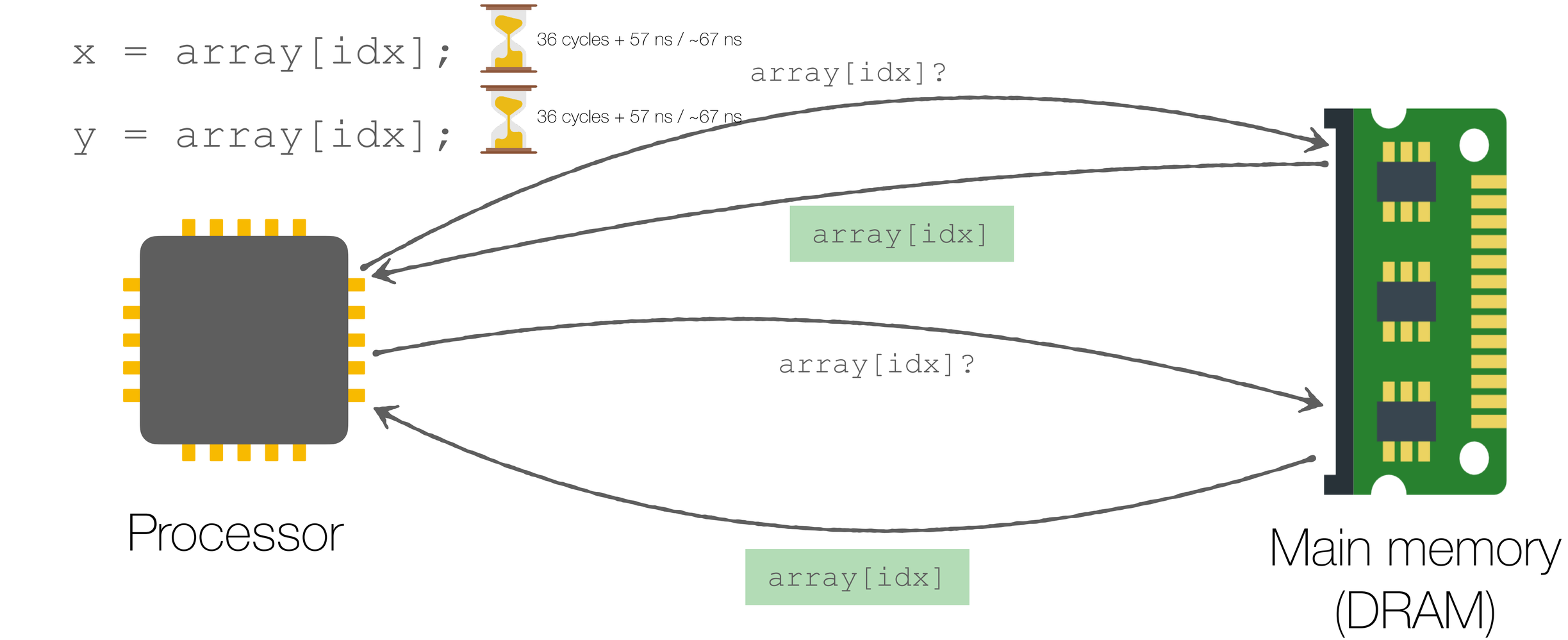

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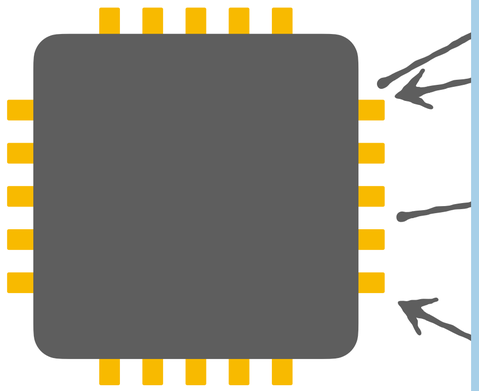
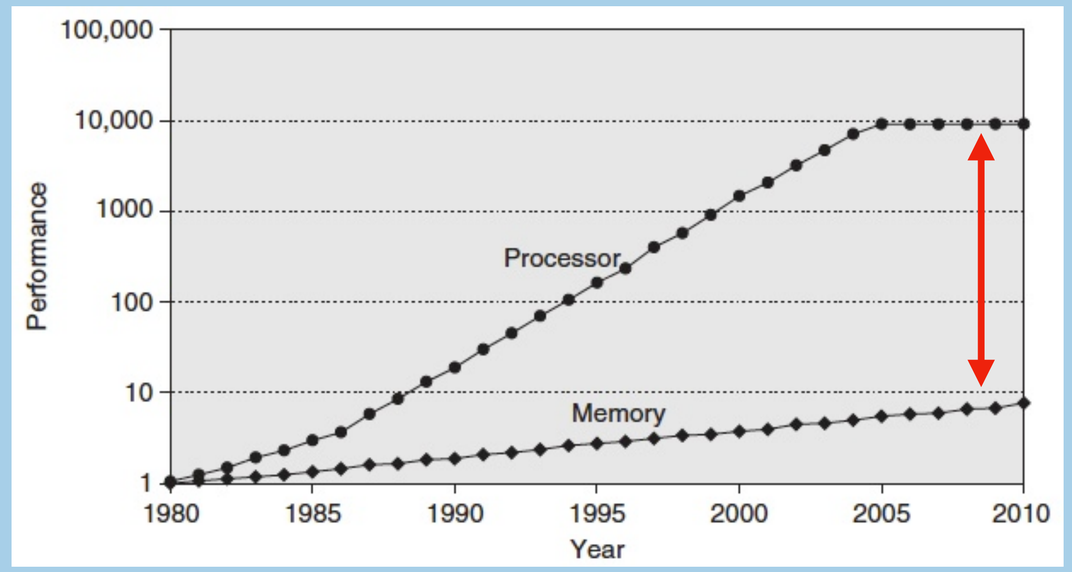


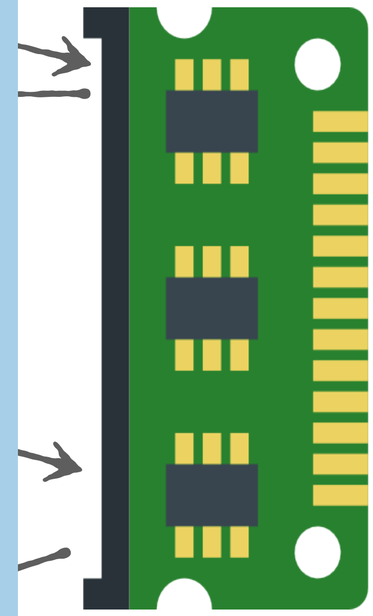
Processor

We have a problem…



Source: Hennesy, Patterson - Computer architectures: a quantitative approach

```
array[idx]
```



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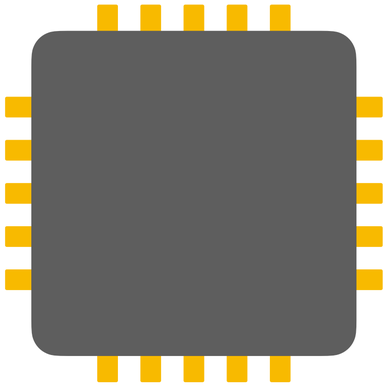
Caches to the rescue!



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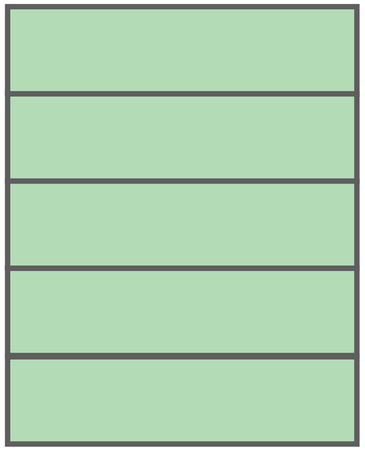
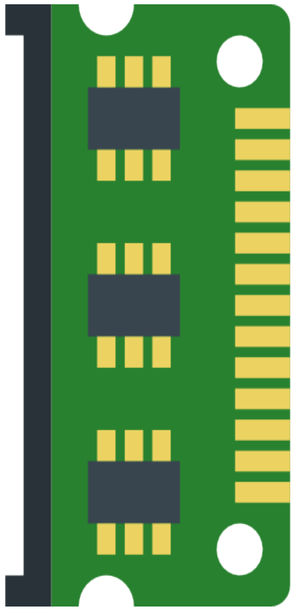


Cache



Main memory
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DRAM and L1 latency for Intel i7-4770 (Haswell)

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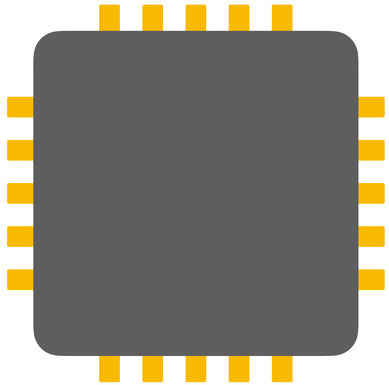

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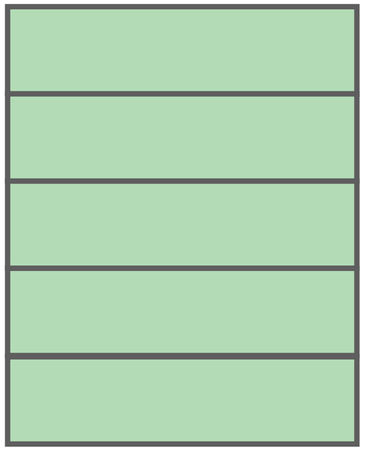

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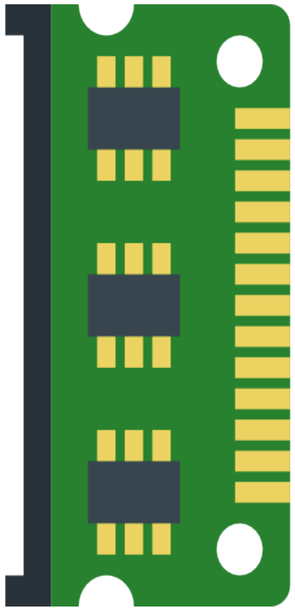

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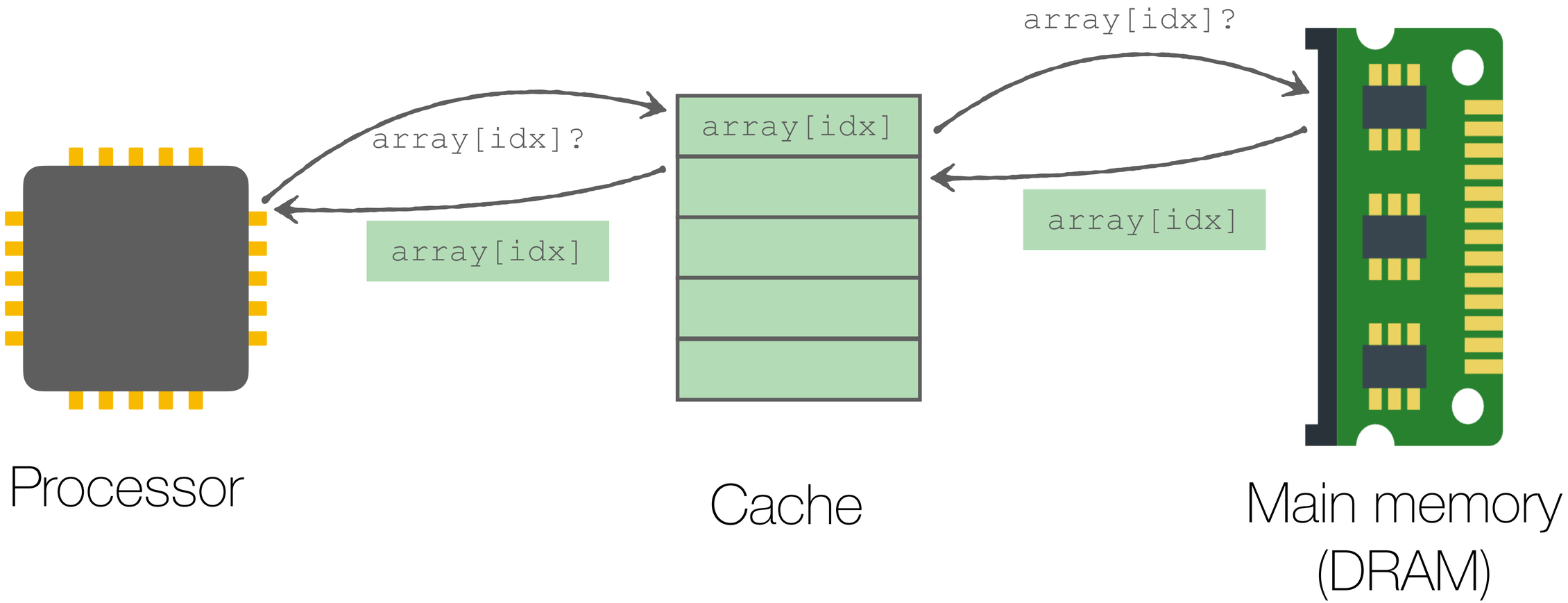

DRAM and L1 latency for Intel i7-4770 (Haswell)

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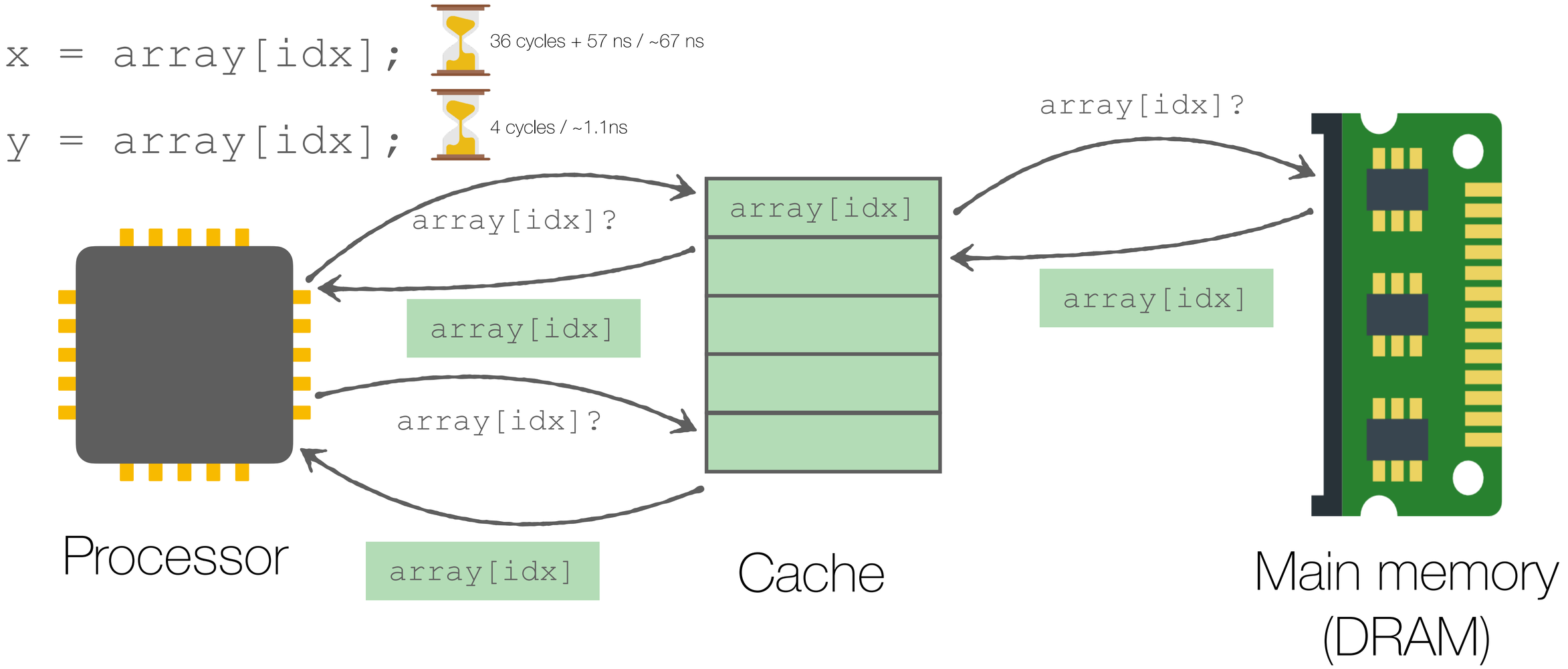
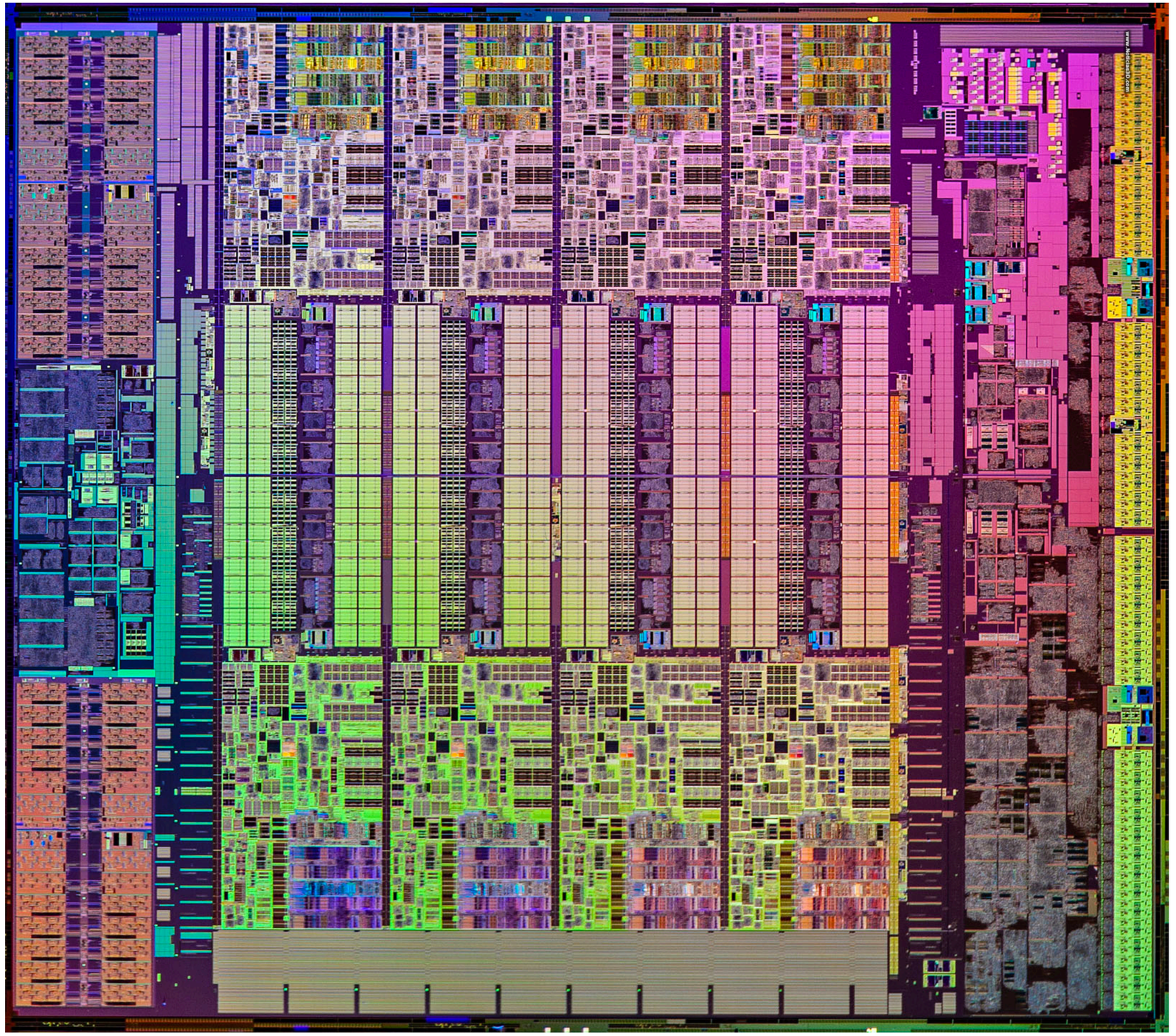


DRAM and L1 latency for Intel i7-4770 (Haswell)

Processors 101

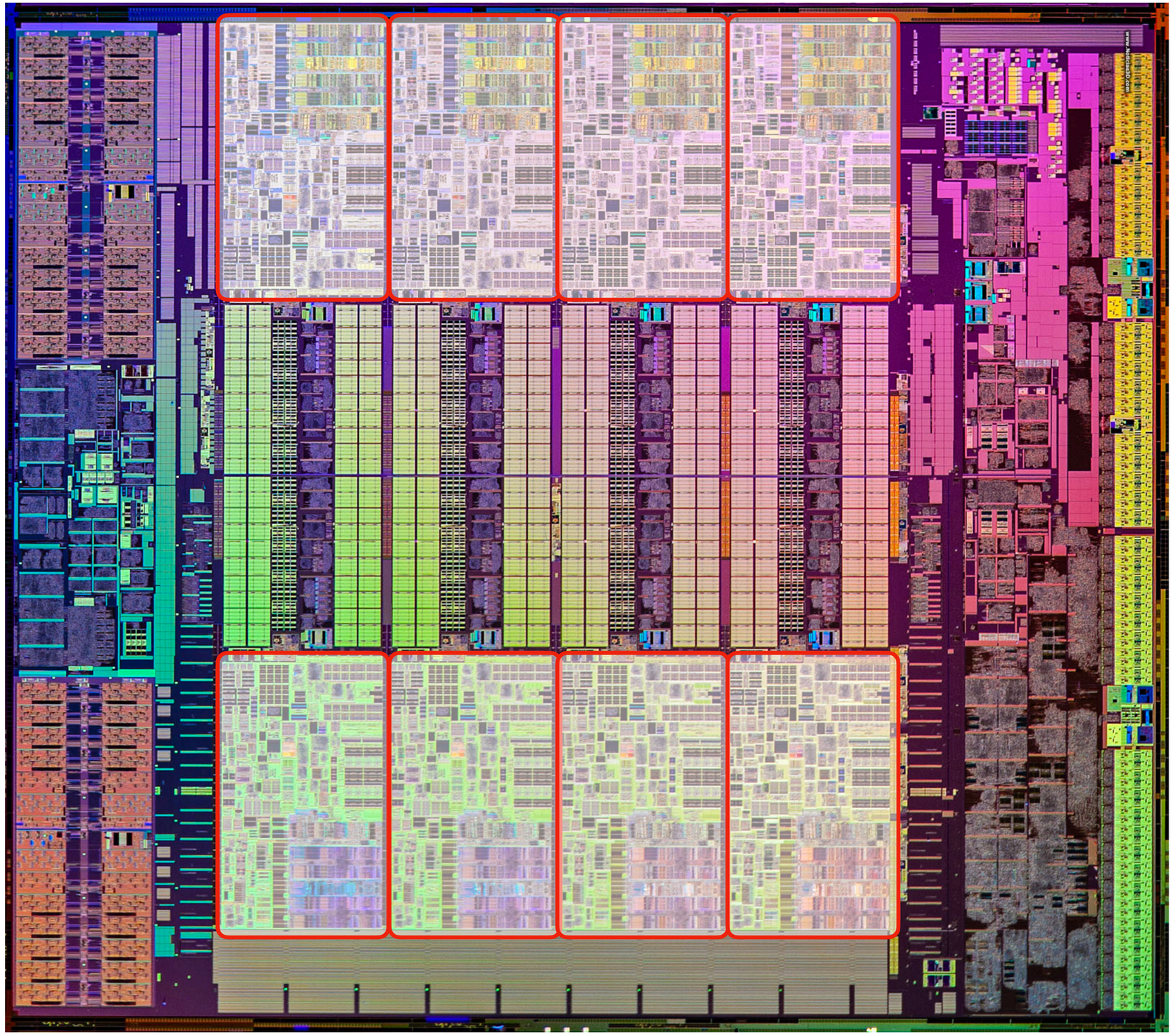


Picture of Intel “Haswell-E” Eight Core CPU

Processors 101

CORE

Execute instructions



Picture of Intel “Haswell-E” Eight Core CPU

Processors 101

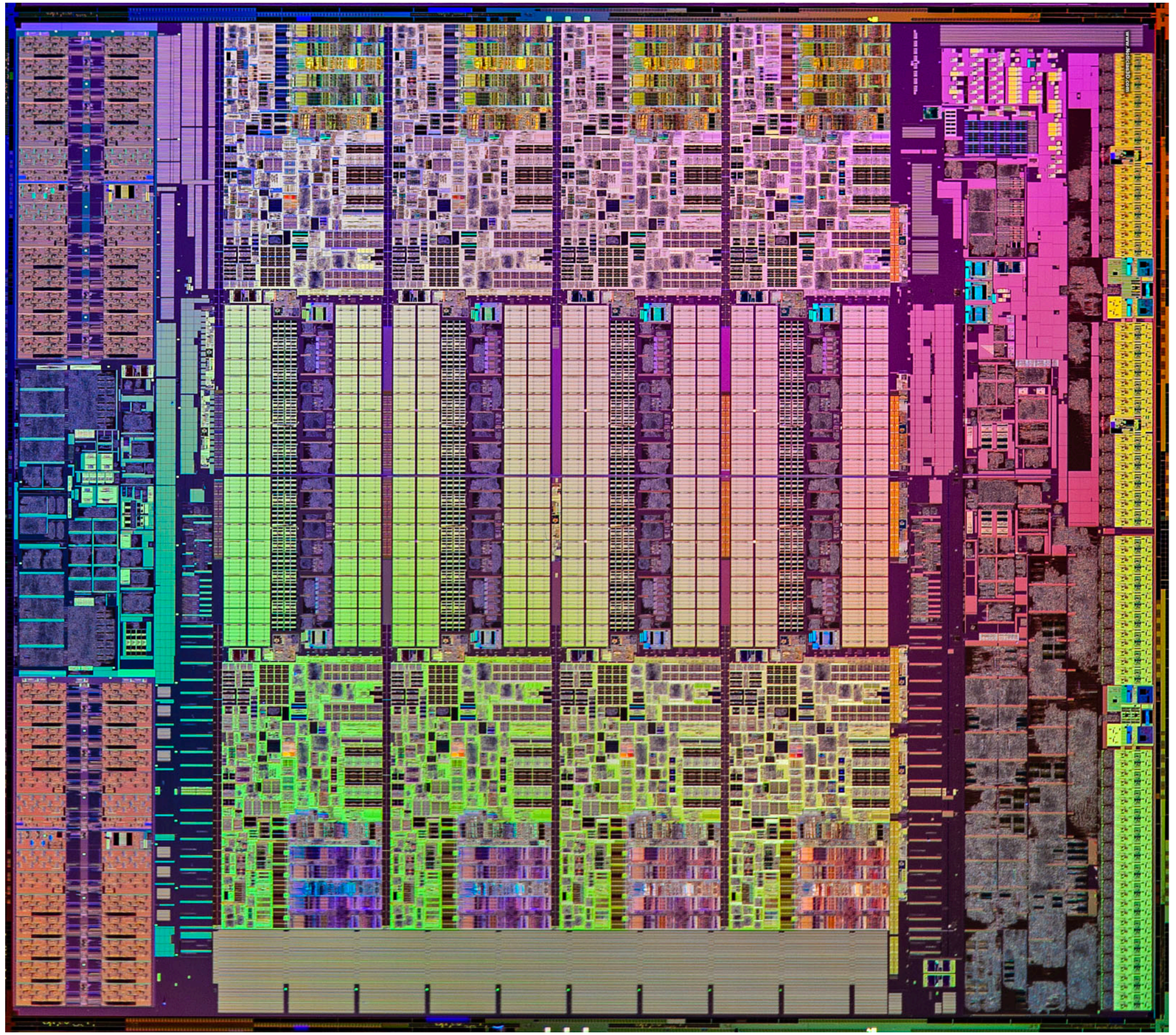
CORE

Execute instructions

CACHE

Memory storing recently accessed data

Speed up computation by reducing interaction with DRAM



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Processors 101

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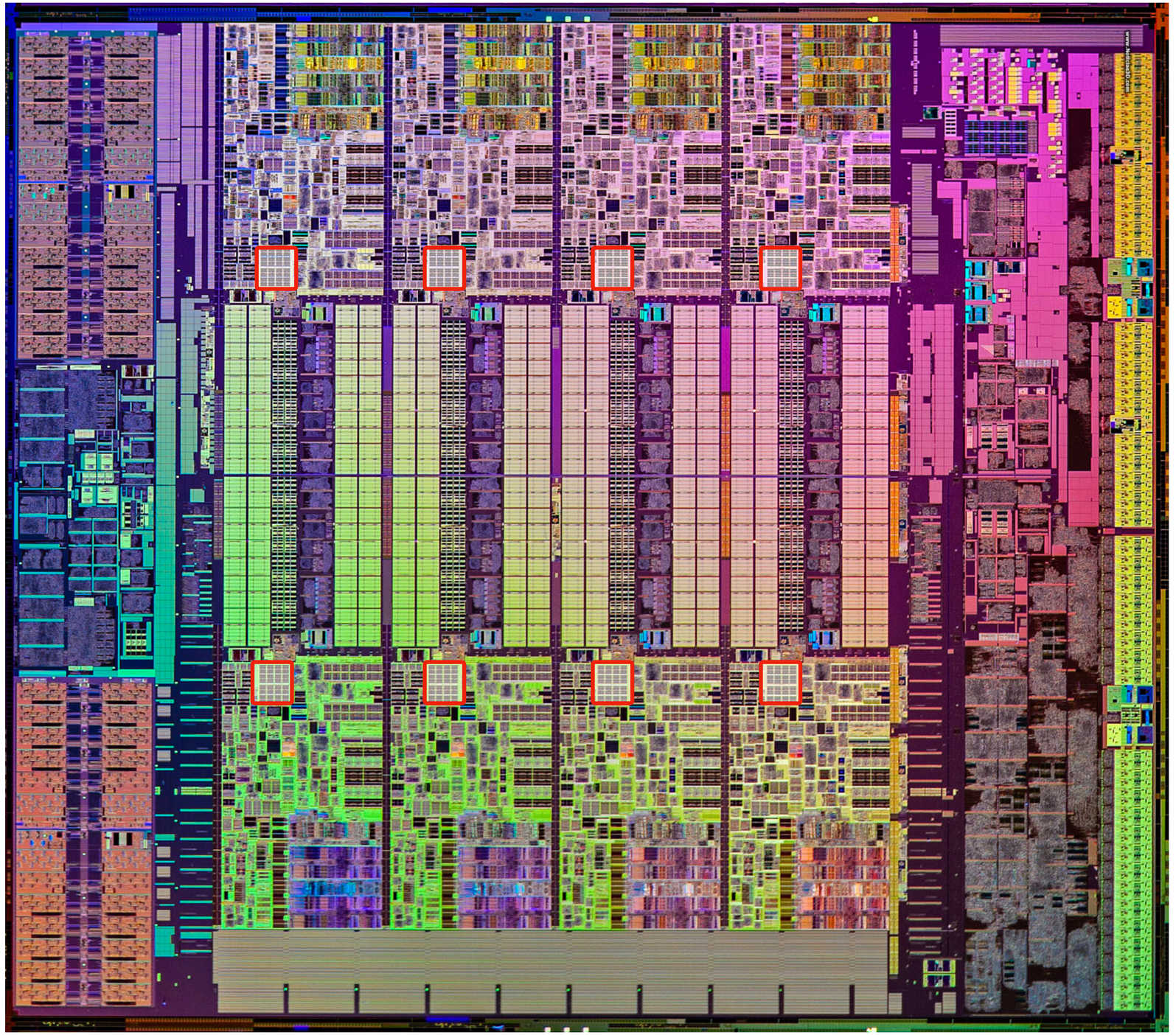

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Processors 101

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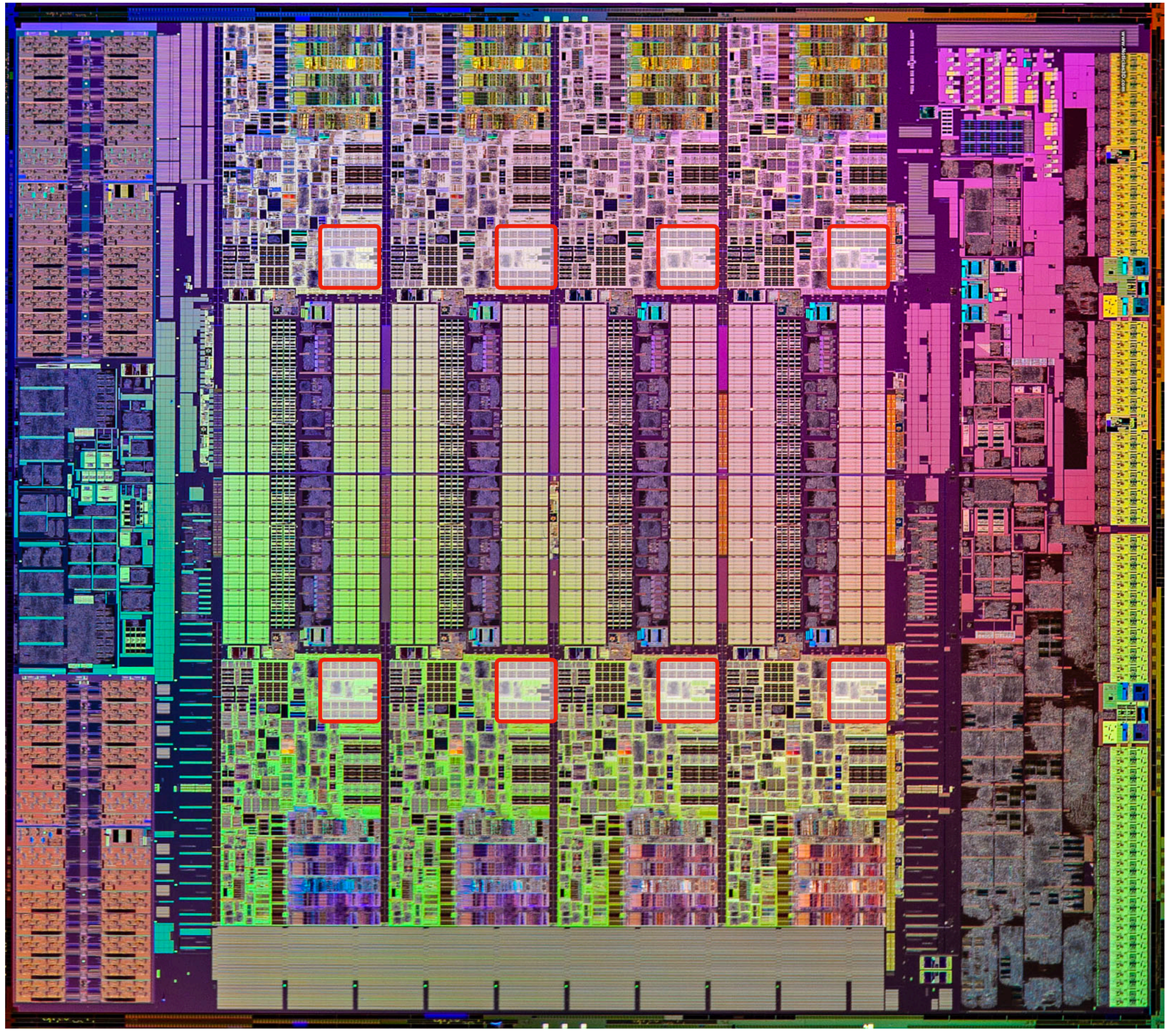

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Processors 101

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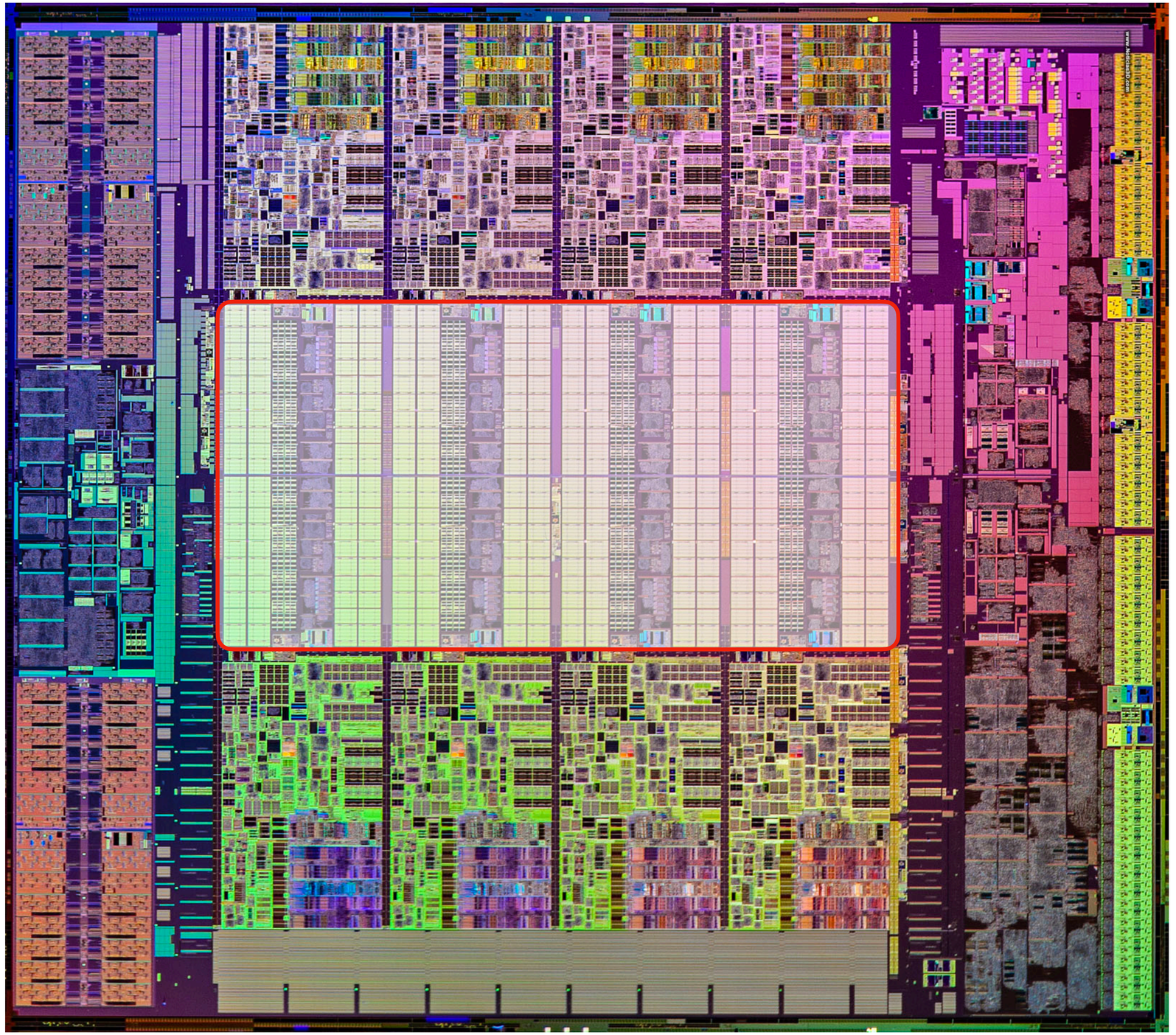

Picture of Intel “Haswell-E” Eight Core CPU

Caches 101

```
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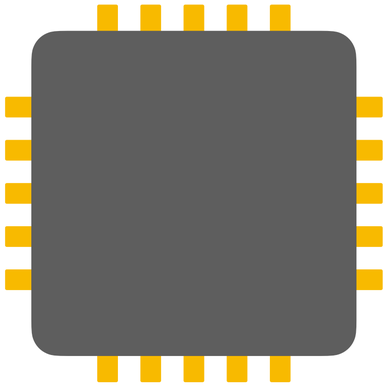
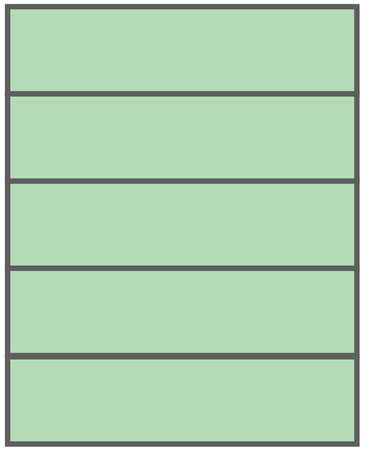
```



Processor



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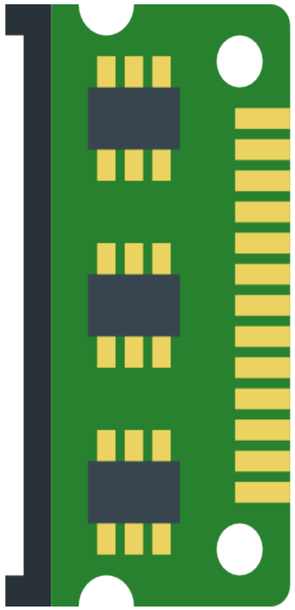

Main memory
(DRAM)

Caches 101

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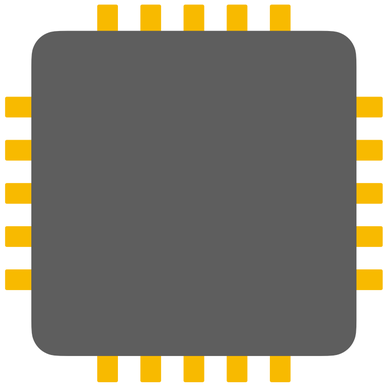

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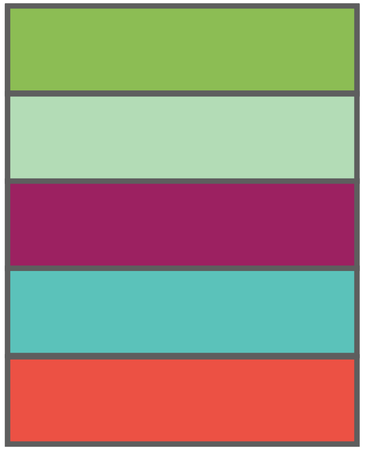
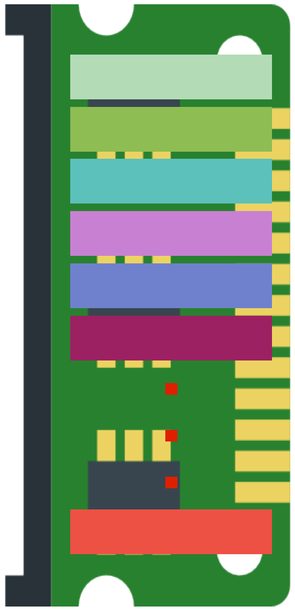


Cache

Divided in ***blocks***



Main memory
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Caches 101

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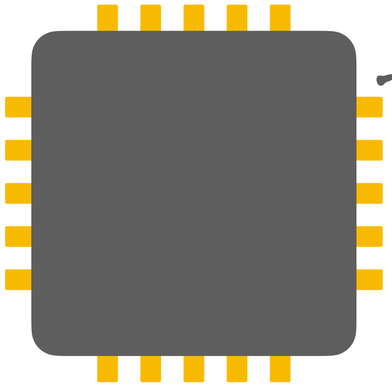
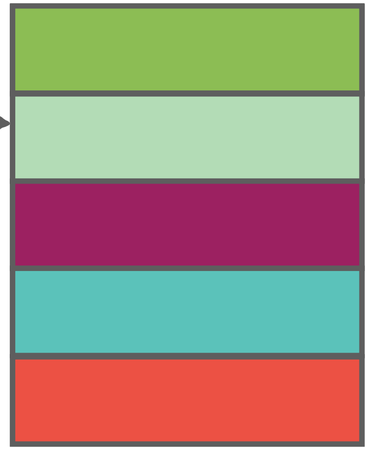
1. Address translation

0x401000





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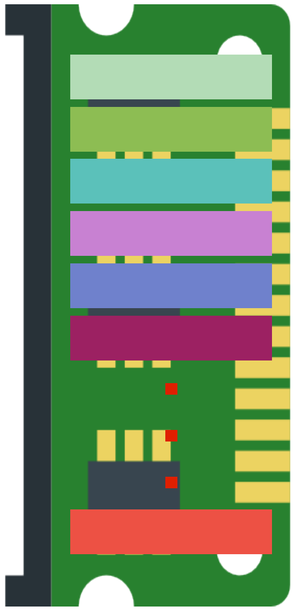


Processor

Cache

Main memory (DRAM)

Caches 101

Results in a ***cache hit*** or ***miss***

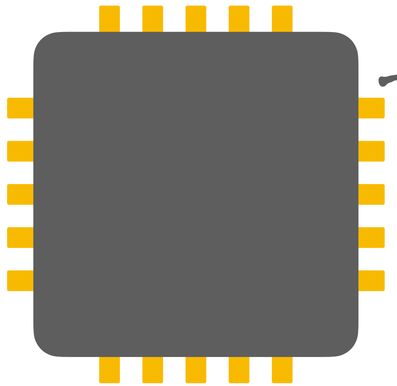
Divided in ***blocks***

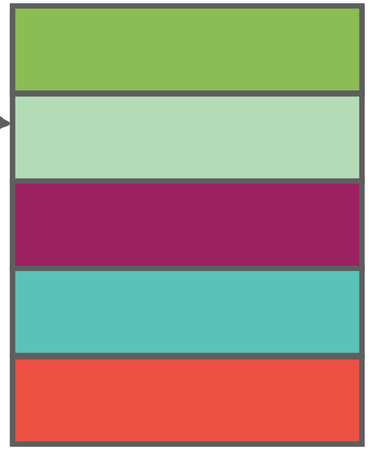
```
x = array[idx];
```

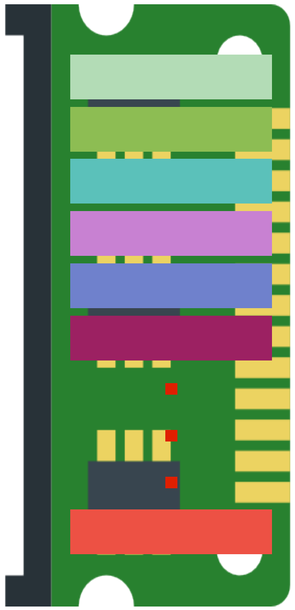
1. Address translation

2. Cache lookup

0x401000





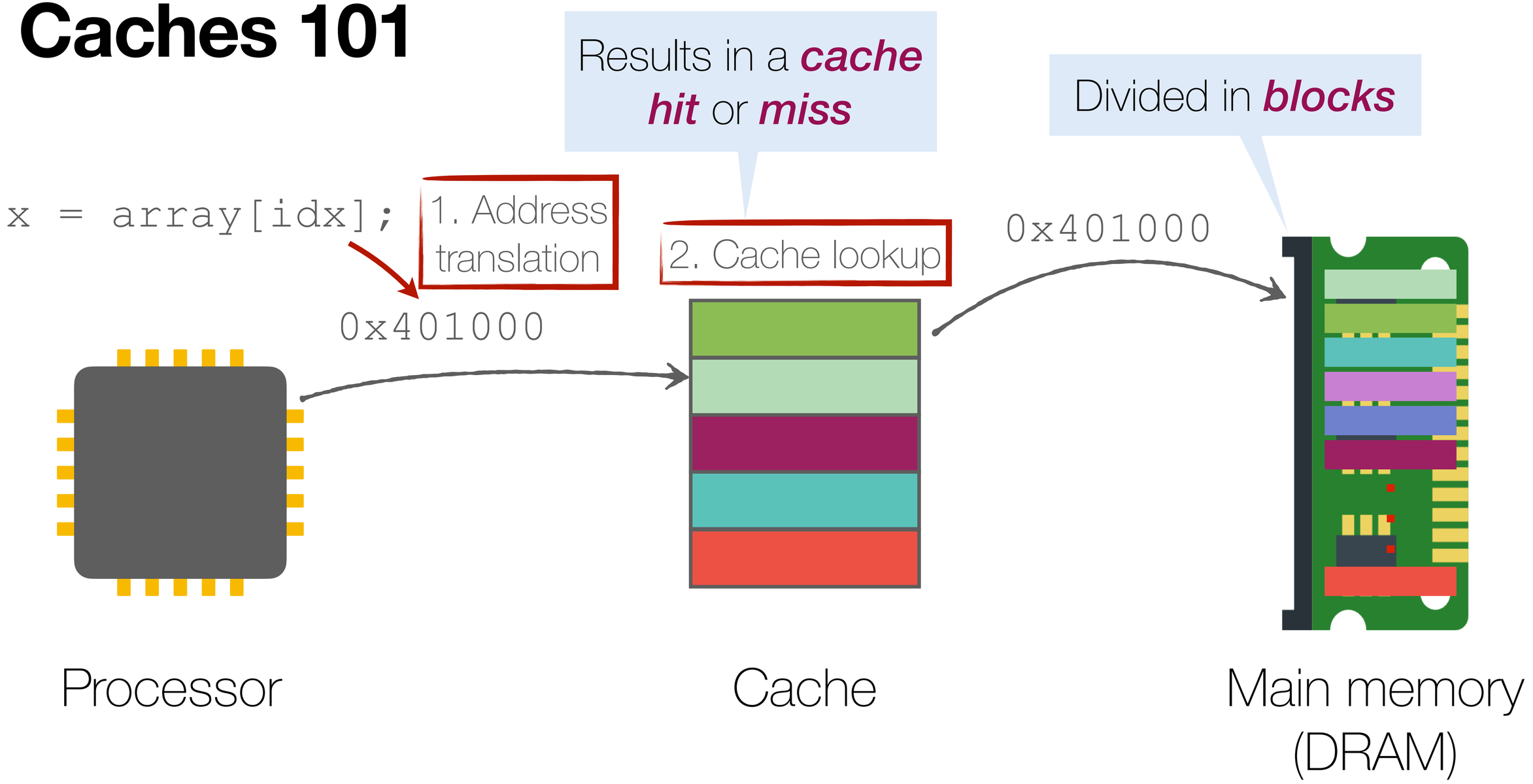


Processor

Cache

Main memory (DRAM)

Caches 101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Processor
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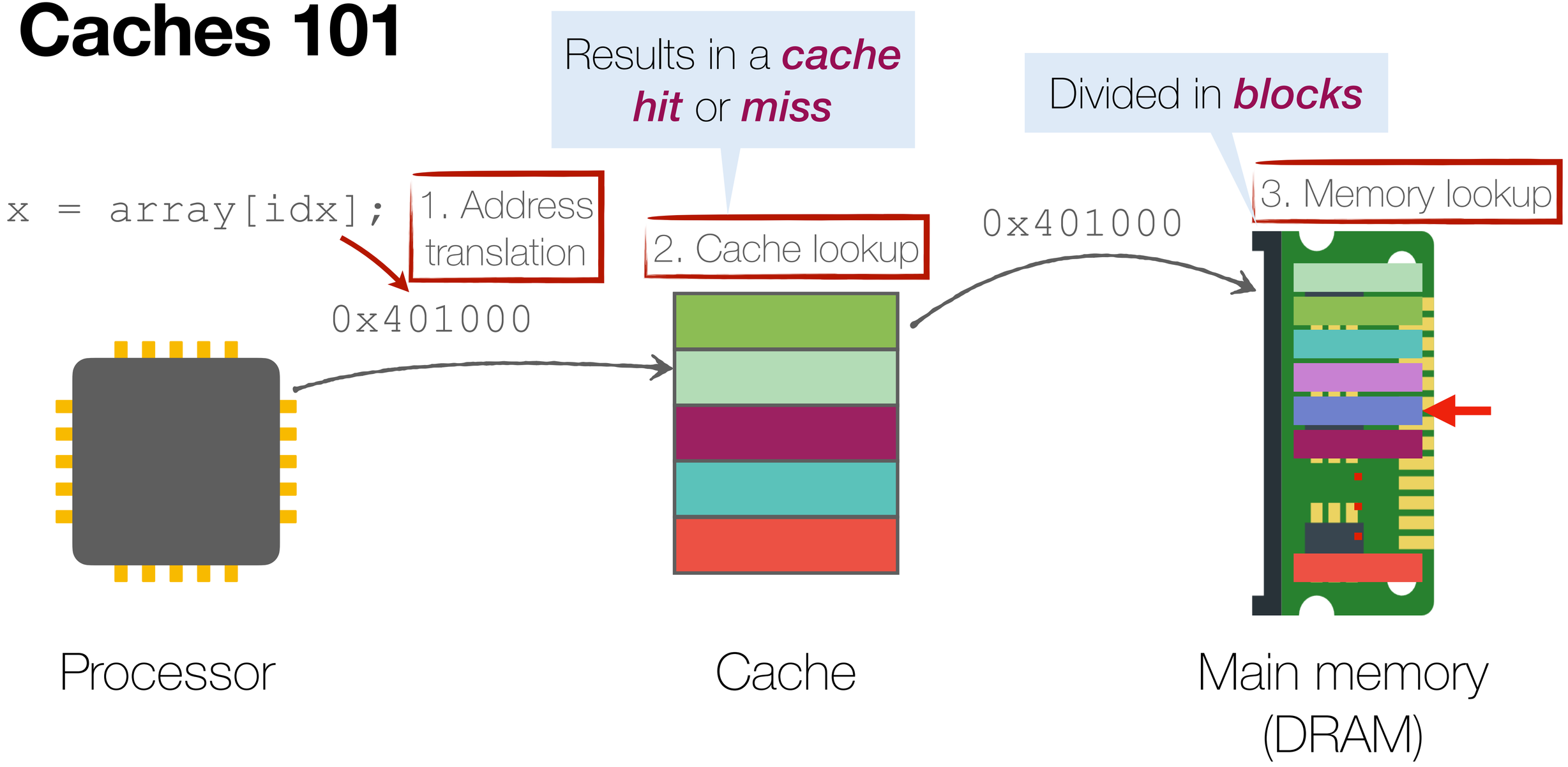
Main memory (DRAM)

Caches 101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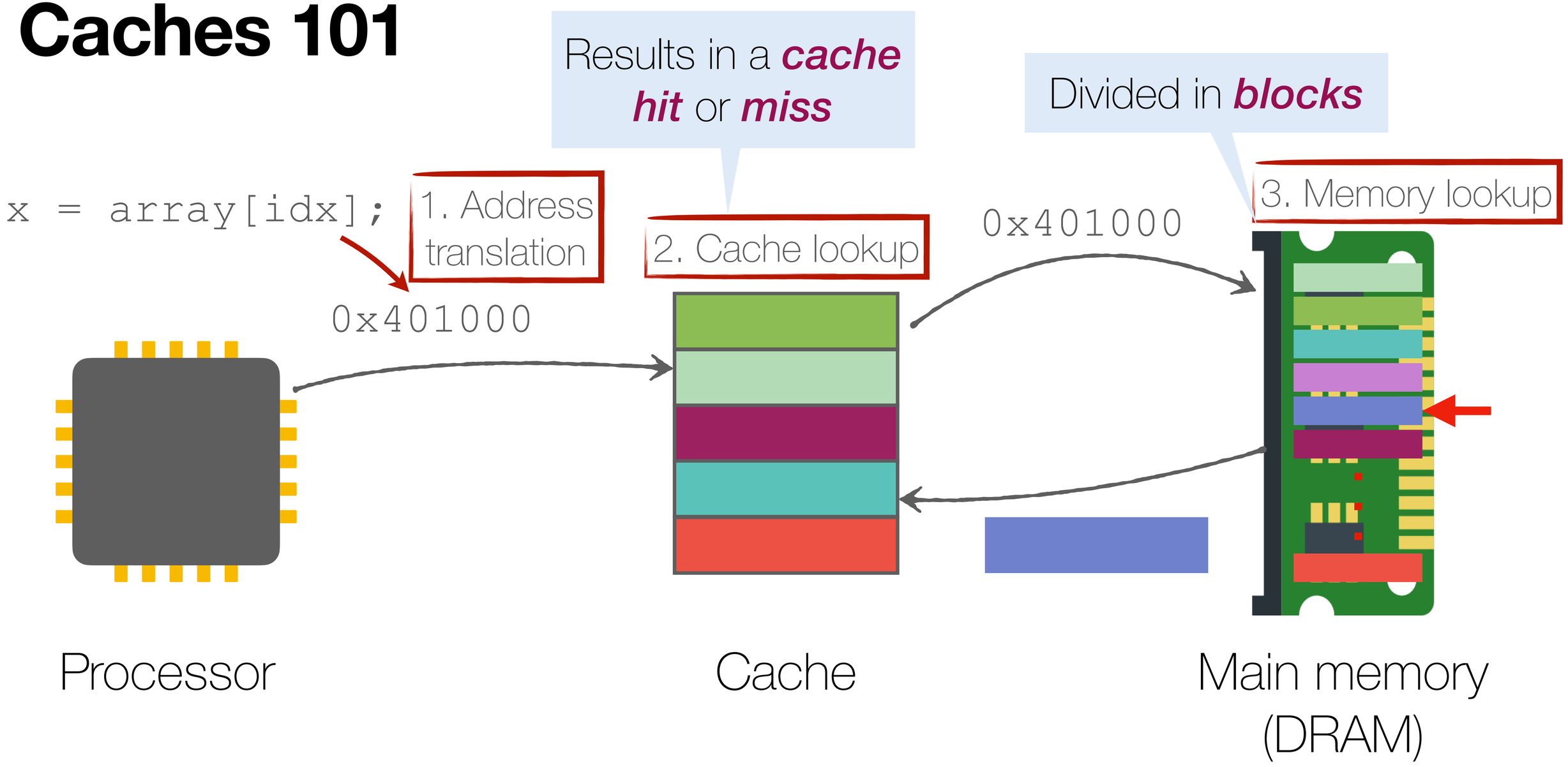
Caches 101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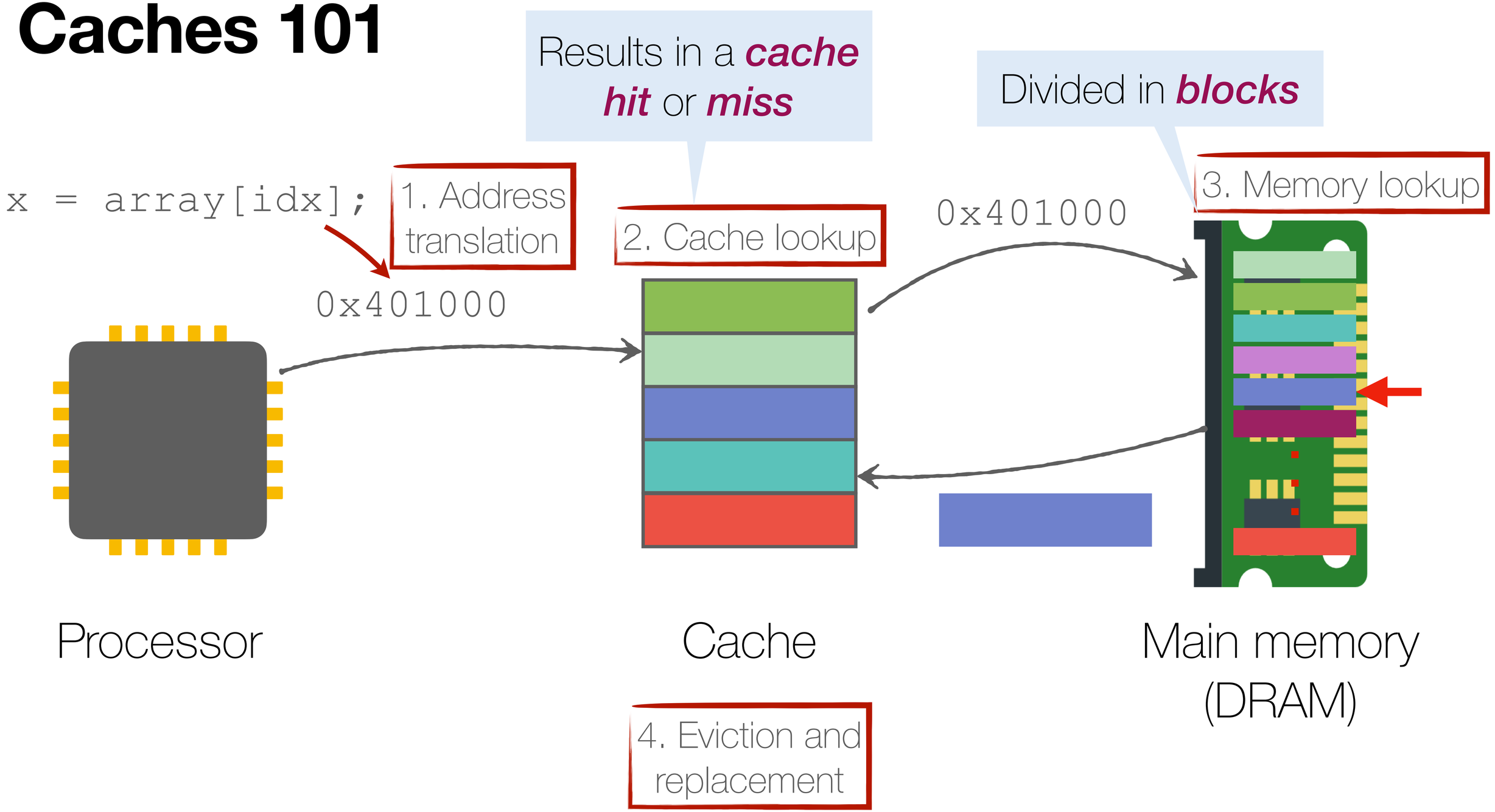
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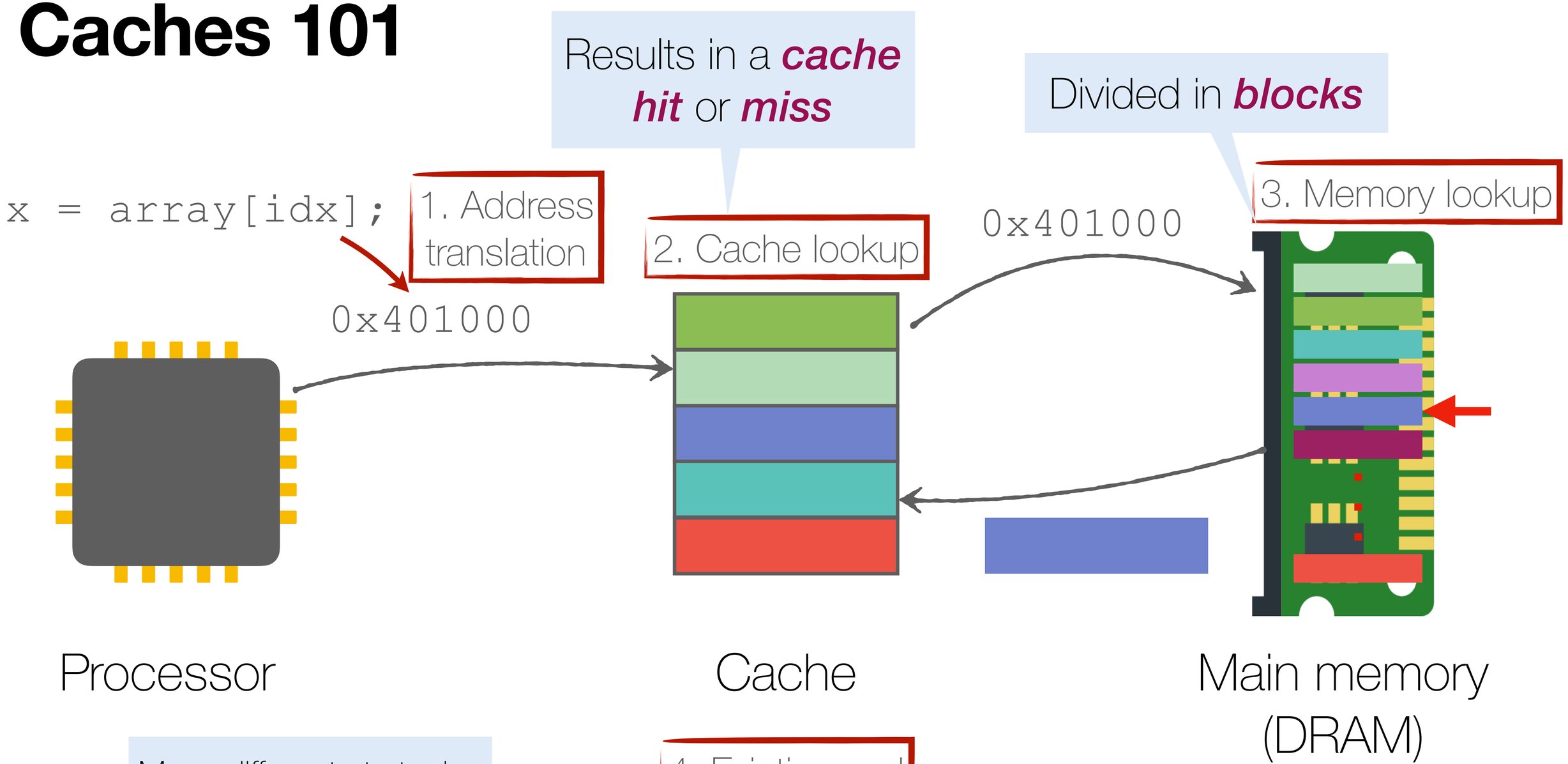
Cache
Main memory (DRAM)
4. Eviction and replacement

Caches 101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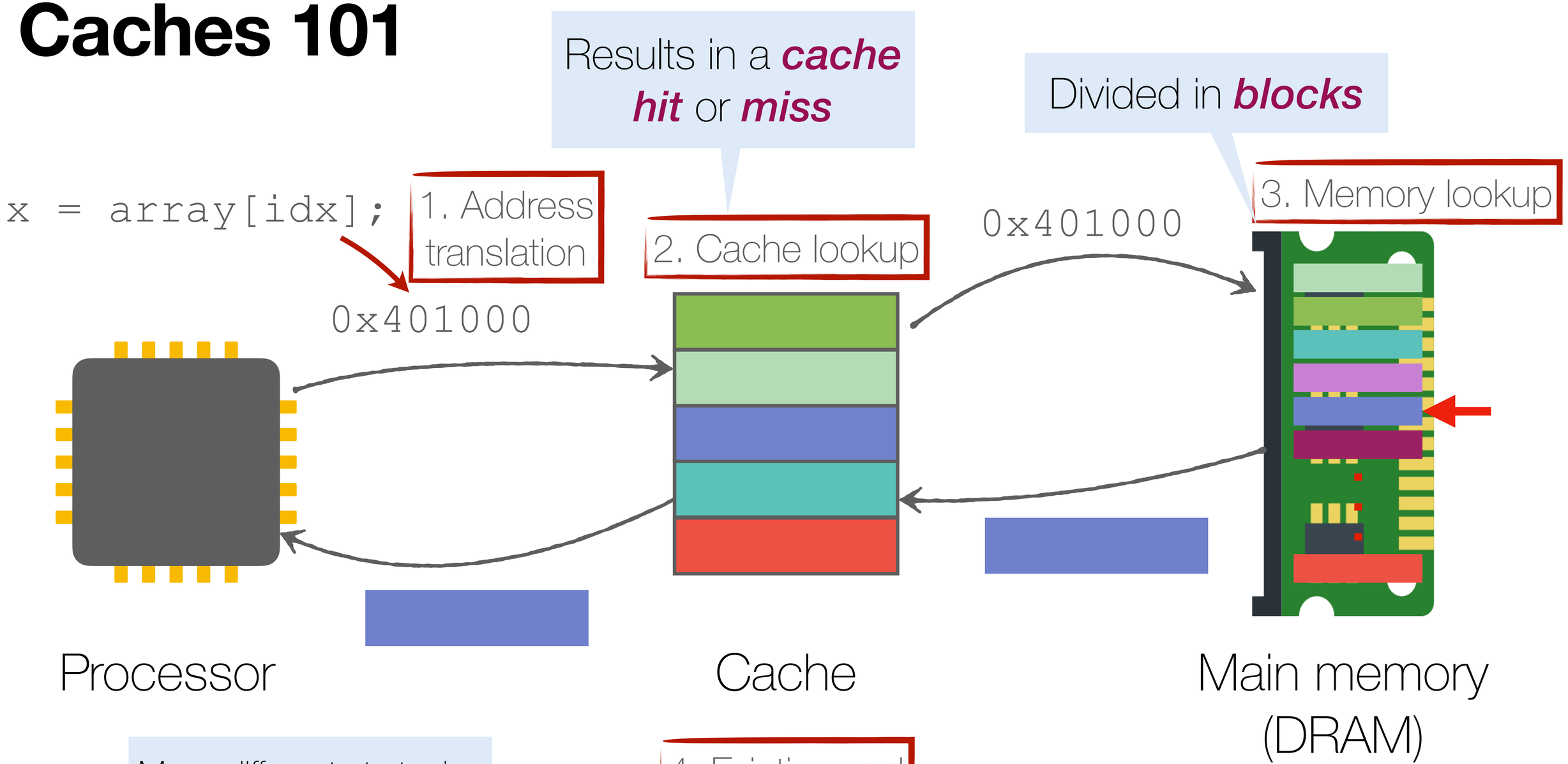
Caches 101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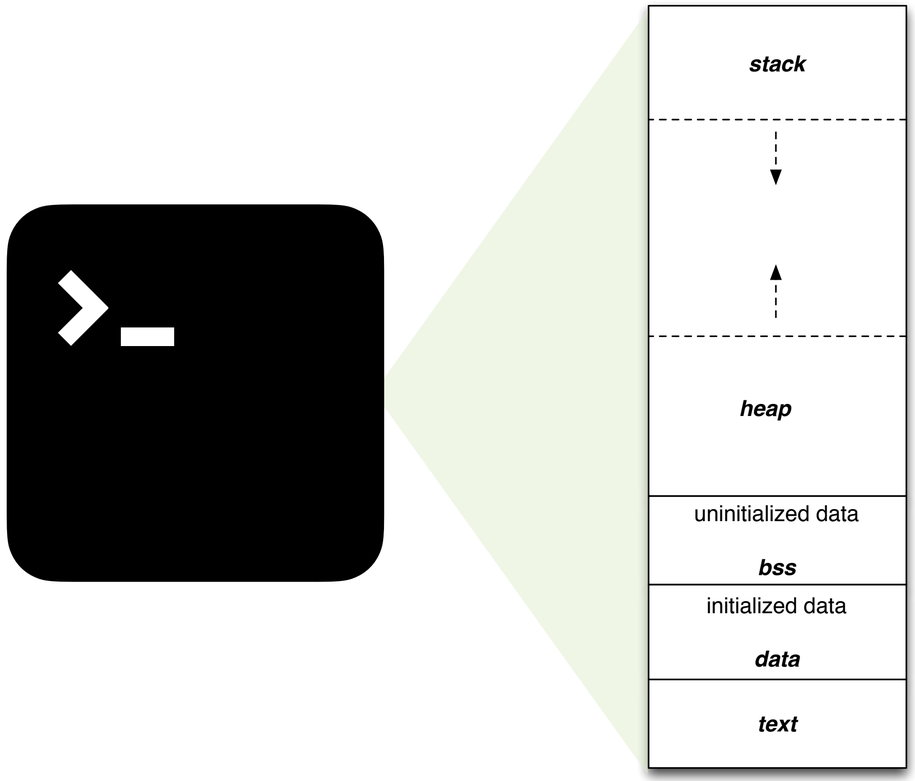
Virtual and physical addresses

Virtual and physical addresses

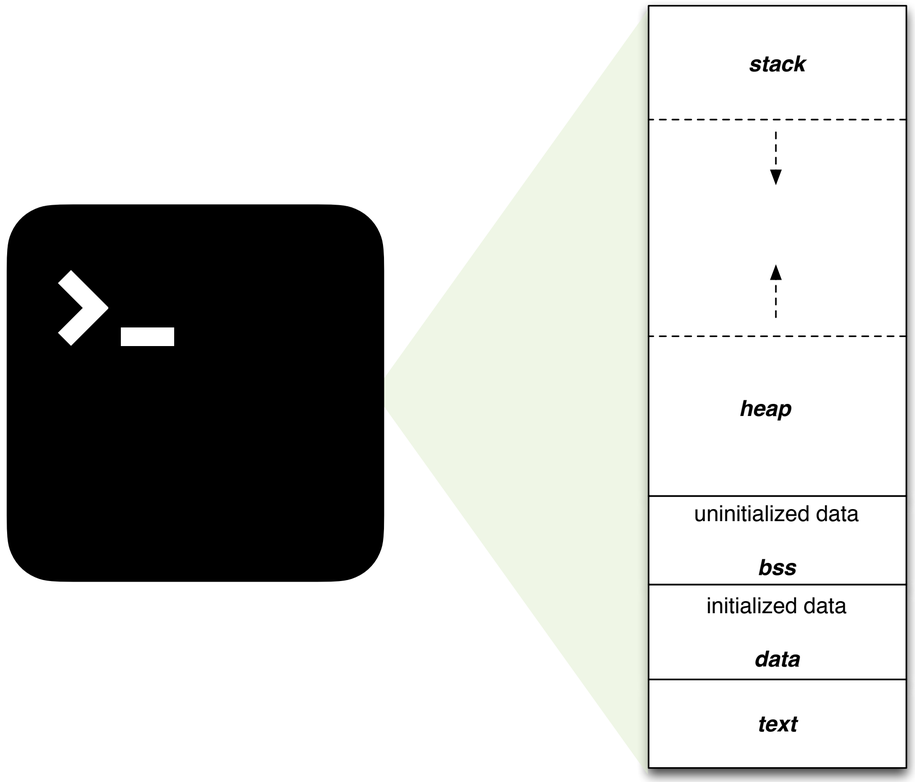


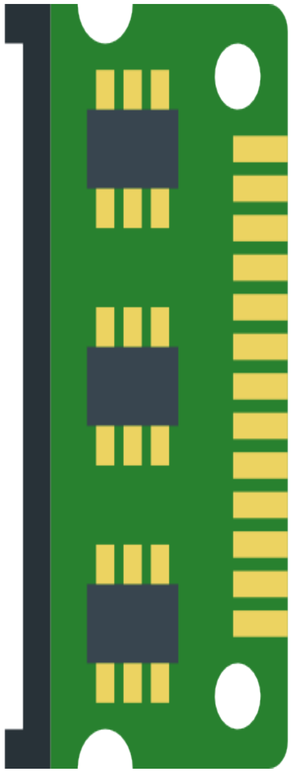
Virtual memory

Abstraction allowing processes to treat ***memory*** as ***linear*** and ***isolated***

Virtual memory layout from https://en.wikipedia.org/wiki/File:Program_memory_layout.pdf

Virtual and physical addresses



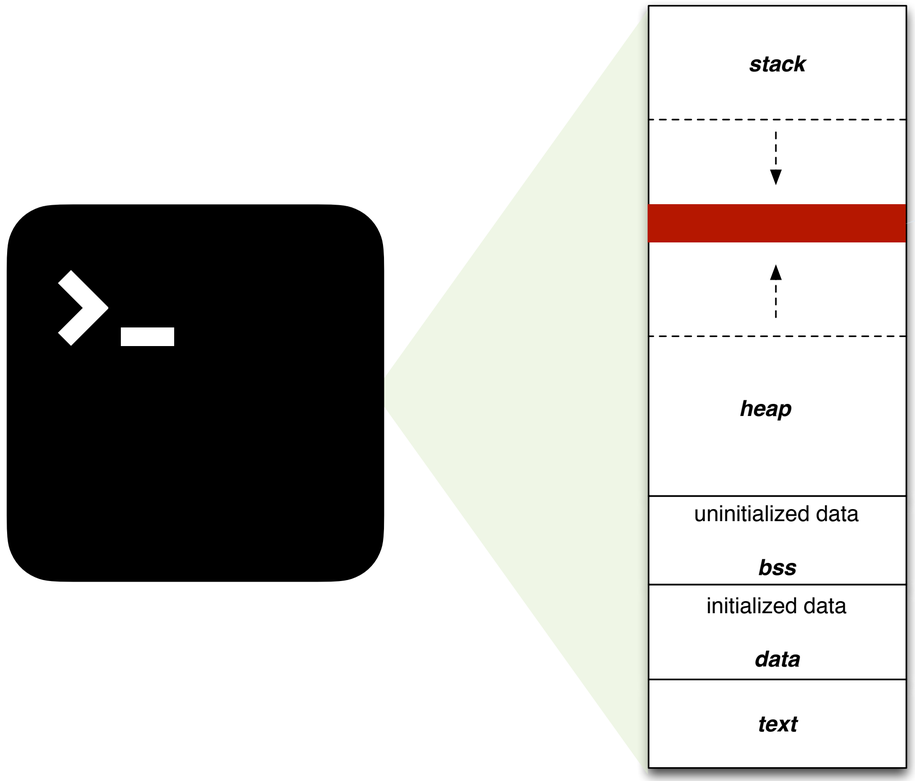


Virtual memory
Abstraction allowing processes to treat ***memory*** as ***linear*** and ***isolated***

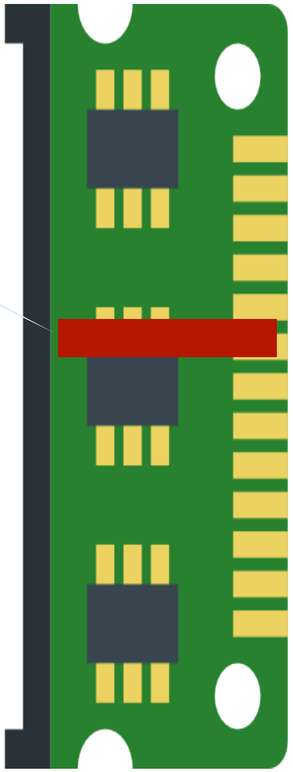
OS + ***memory management unit***
map ***virtual*** addresses to ***physical*** addresses

Virtual memory layout from https://en.wikipedia.org/wiki/File:Program_memory_layout.pdf

Virtual and physical addresses



Virtual and physical memory divided in ***pages*** of 2^p bytes



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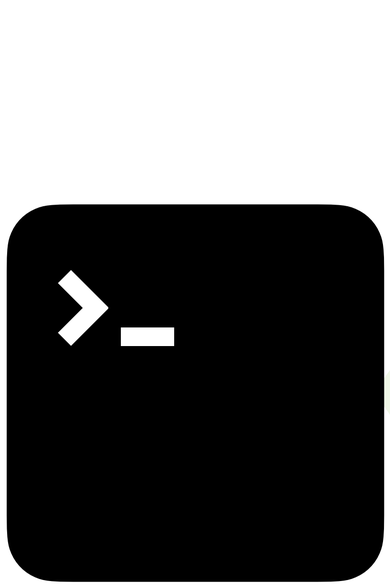
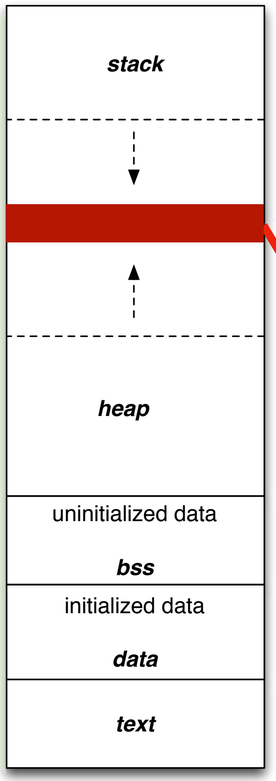
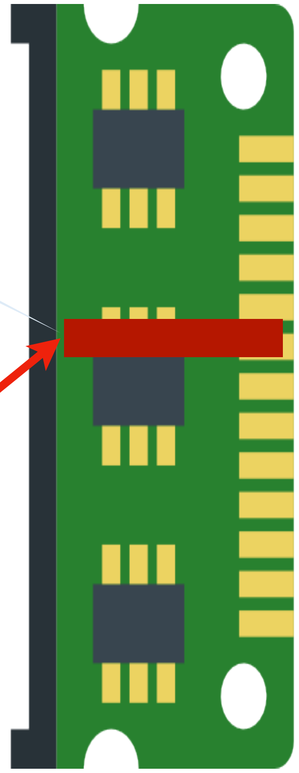
Virtual and physical addresses





Virtual and physical memory divided in ***pages*** of 2^p bytes

Mapping is stored in ***page table***
Last p bits are the same



Virtual memory
Abstraction allowing processes to treat ***memory*** as ***linear*** and ***isolated***

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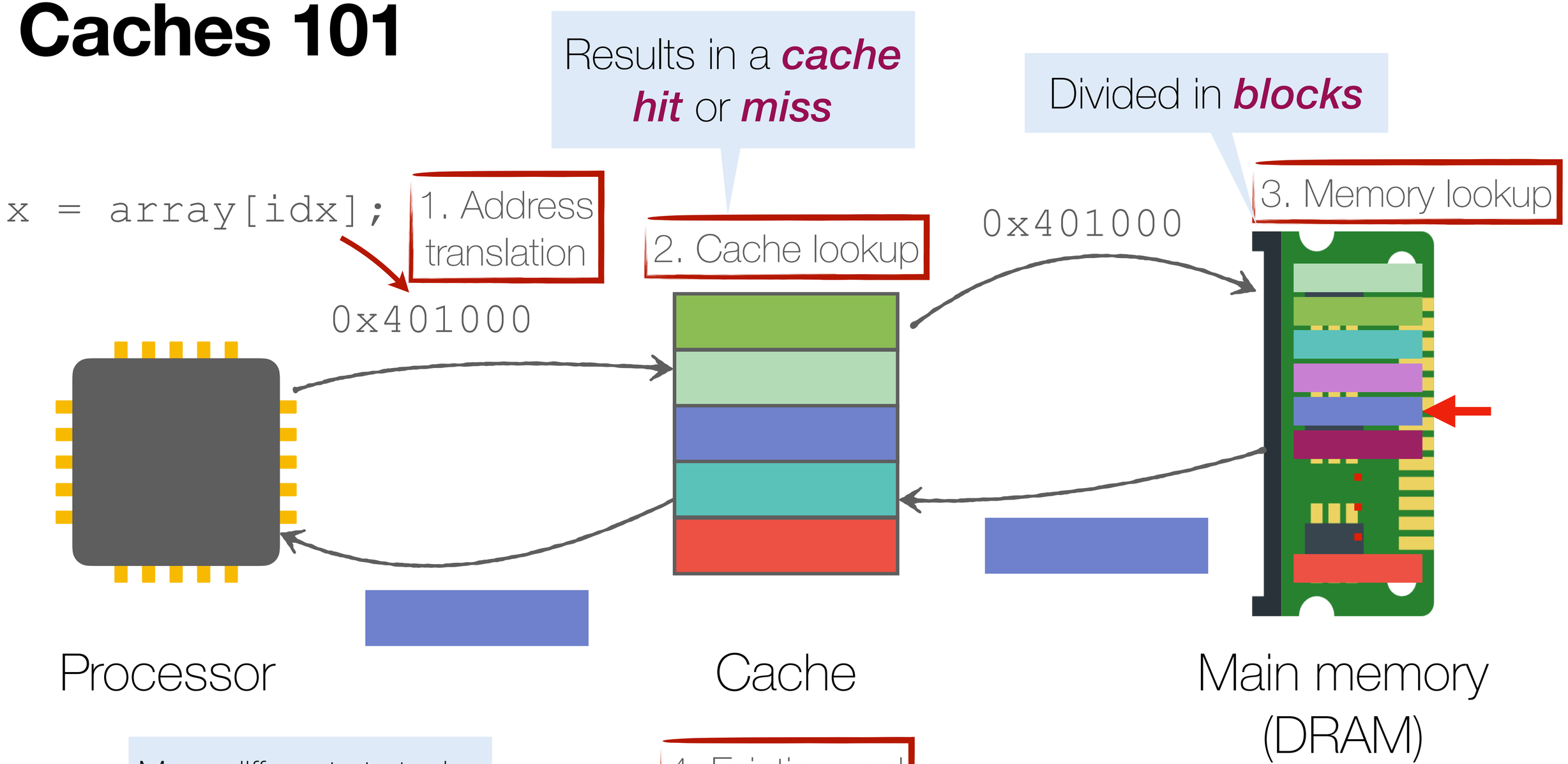
Virtual memory layout from https://en.wikipedia.org/wiki/File:Program_memory_layout.pdf

Caches 101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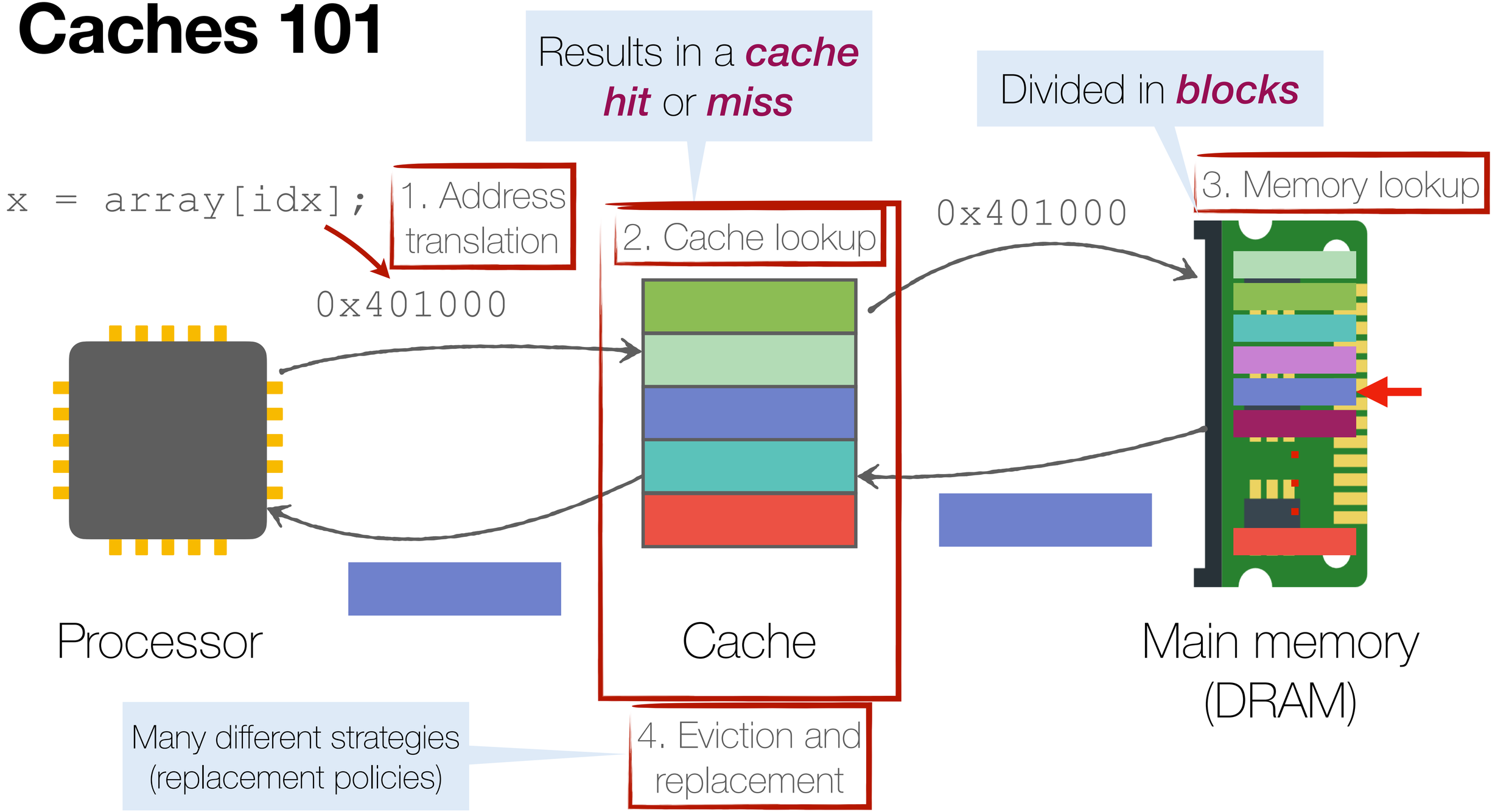
Caches 101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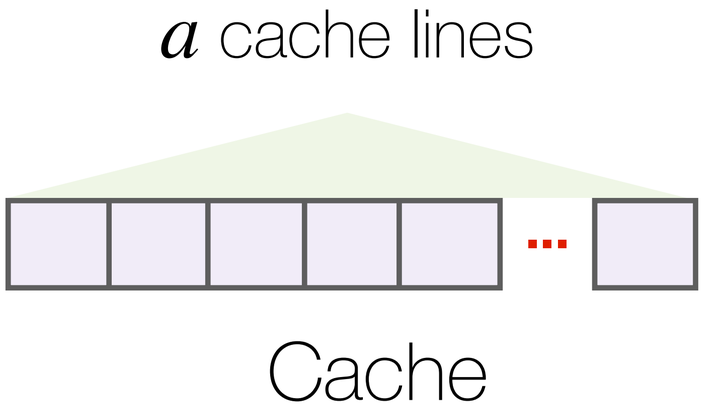
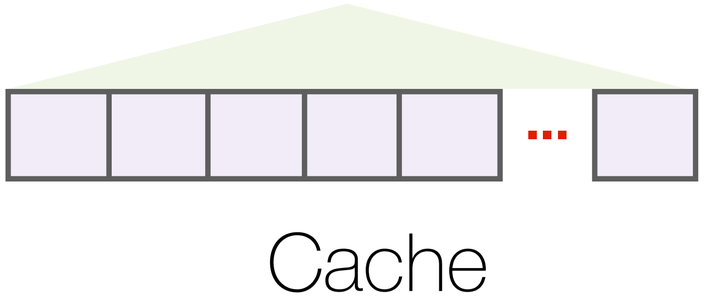
Fully associative caches

Fully associative caches



Divided in ***cache lines***
each one storing a ***block***

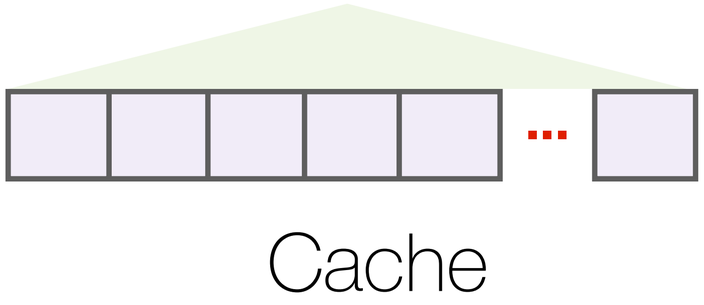
Fully associative caches



Memory divided in ***blocks*** of 2^l bits

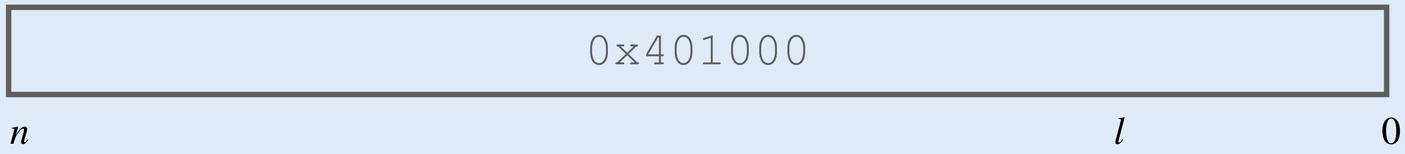
Divided in ***cache lines***
each one storing a ***block***

Fully associative caches



Memory divided in ***blocks*** of 2^l bits

Mapping ***addresses*** to cache



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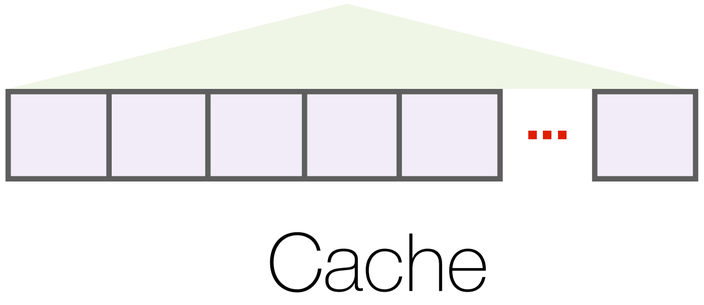

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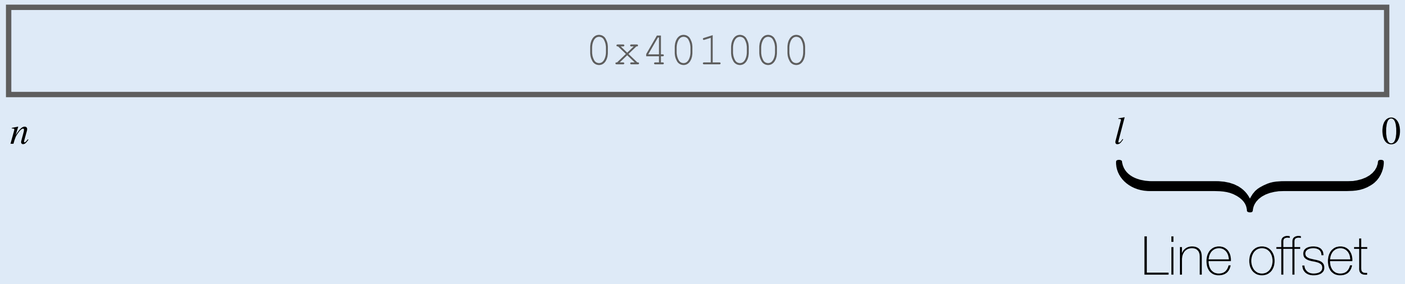

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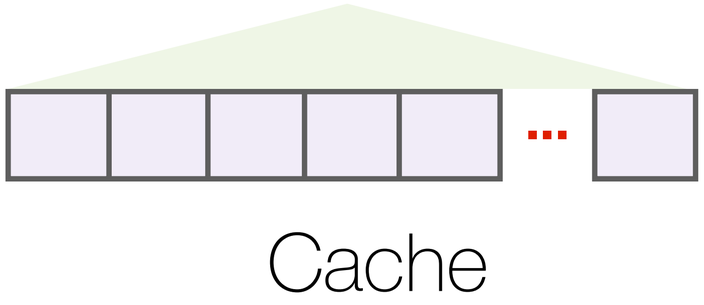
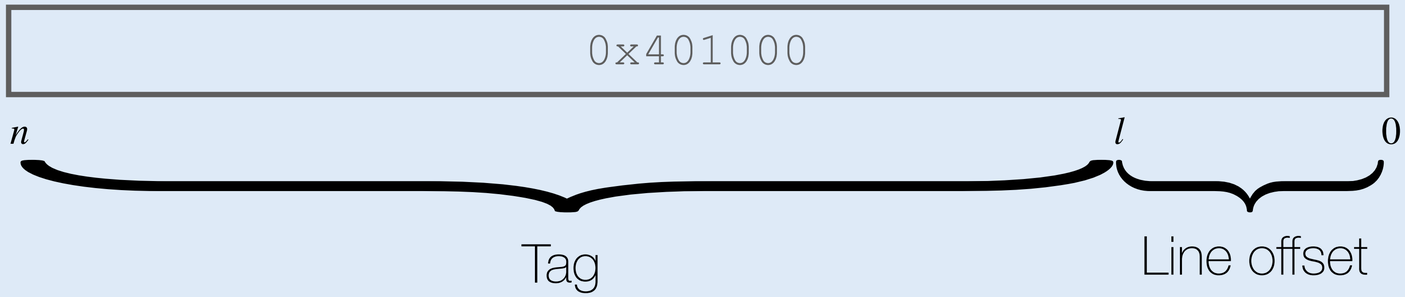


Memory divided in ***blocks*** of 2^l bits

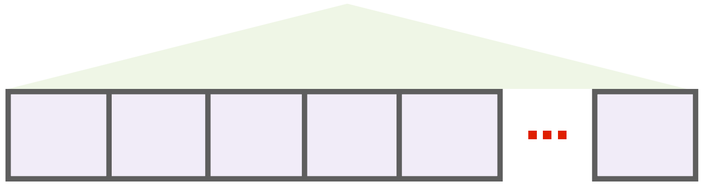
Mapping ***addresses*** to cache



Divided in ***cache lines***
each one storing a ***block***

Fully associative caches

a cache lines



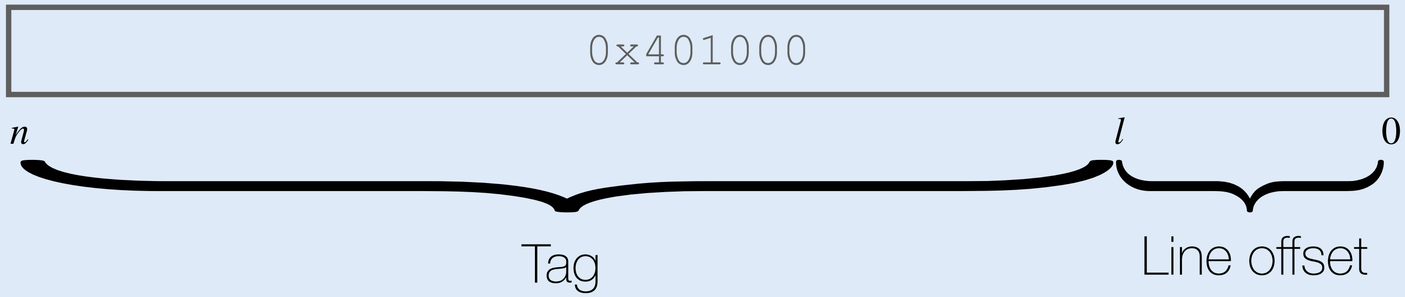
Cache

Divided in ***cache lines***
each one storing a ***block***

Memory divided in ***blocks*** of 2^l bits

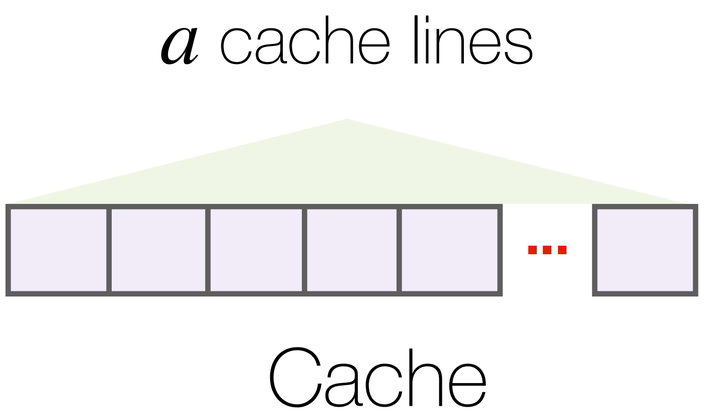
Mapping ***addresses*** to cache

Physical address



A ***memory block*** can fit in ***any*** of the cache lines

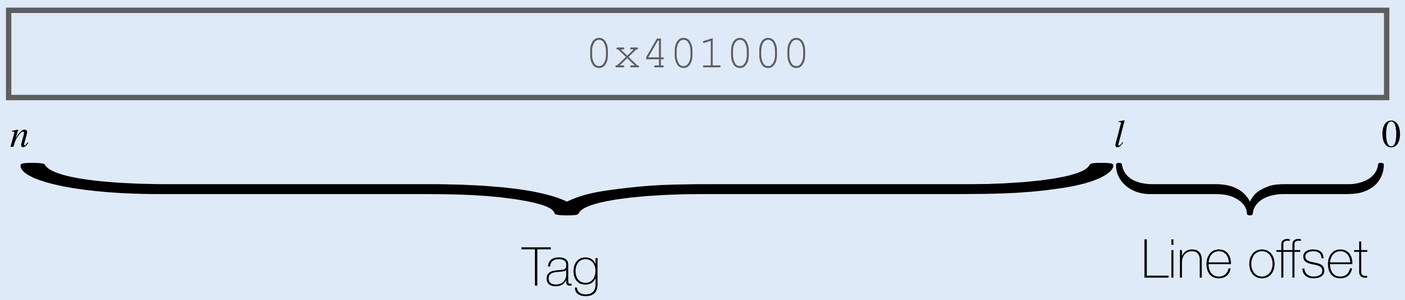
Fully associative caches



Divided in ***cache lines*** each one storing a ***block***

Memory divided in ***blocks*** of 2^l bits

Mapping ***addresses*** to cache

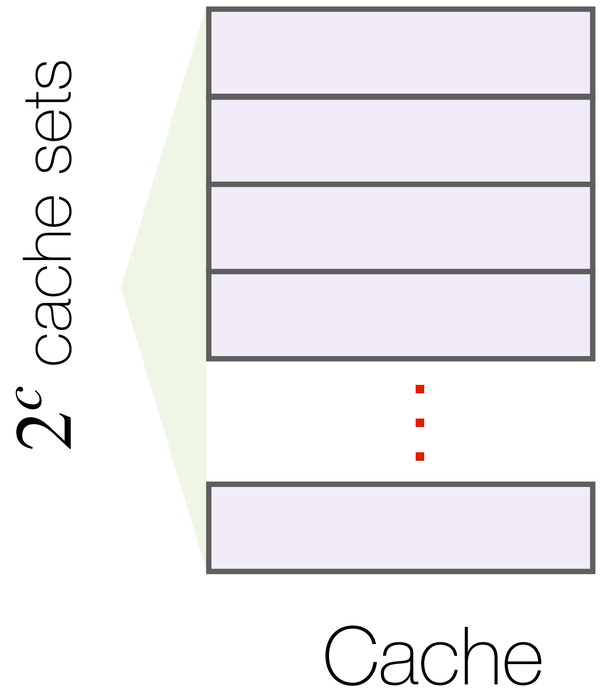


A ***memory block*** can fit in ***any*** of the cache lines

Expensive to implement

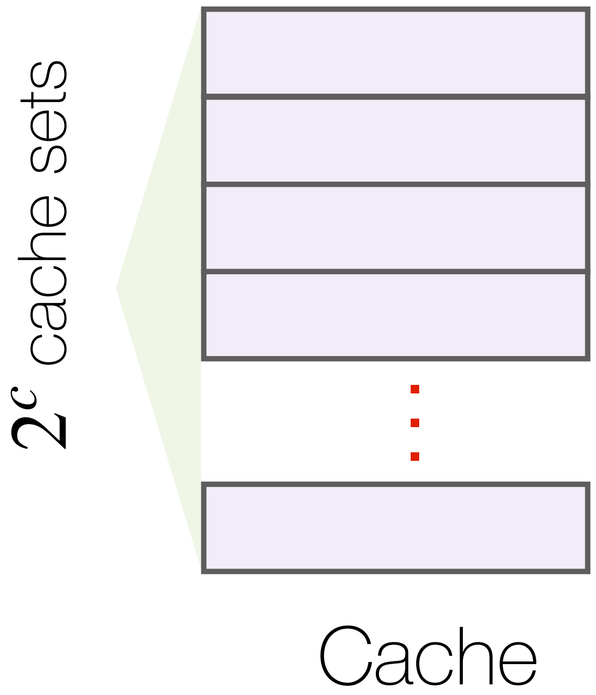
Directly mapped cache

Directly mapped cache



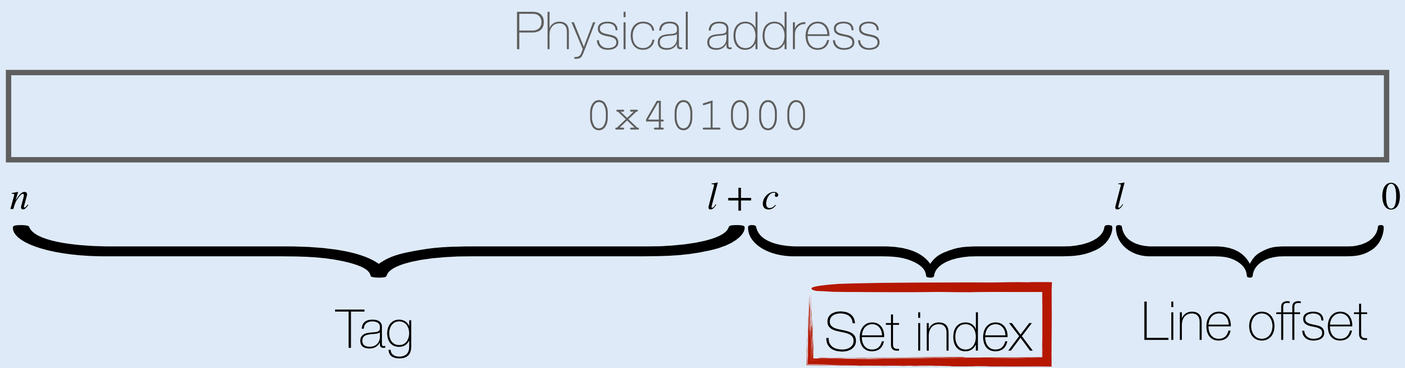
Divided in ***cache sets*** each one with 1 ***cache line***

Directly mapped cache



Memory divided in ***blocks*** of 2^l bits

Mapping ***addresses*** to cache



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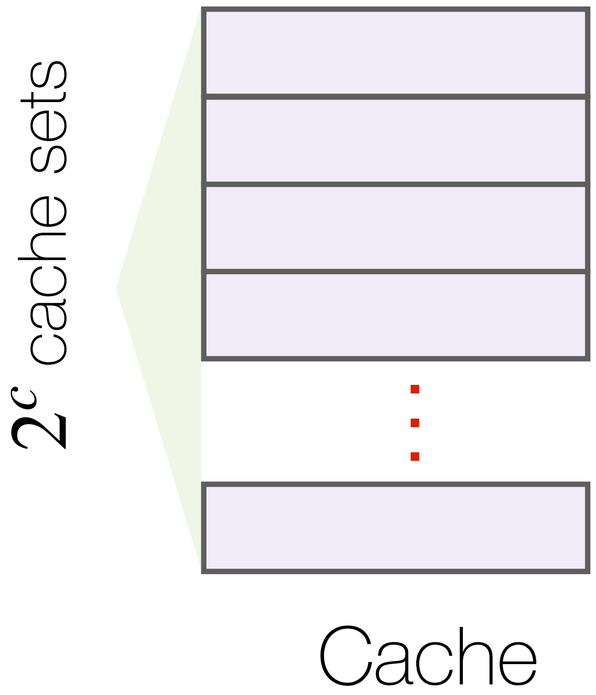

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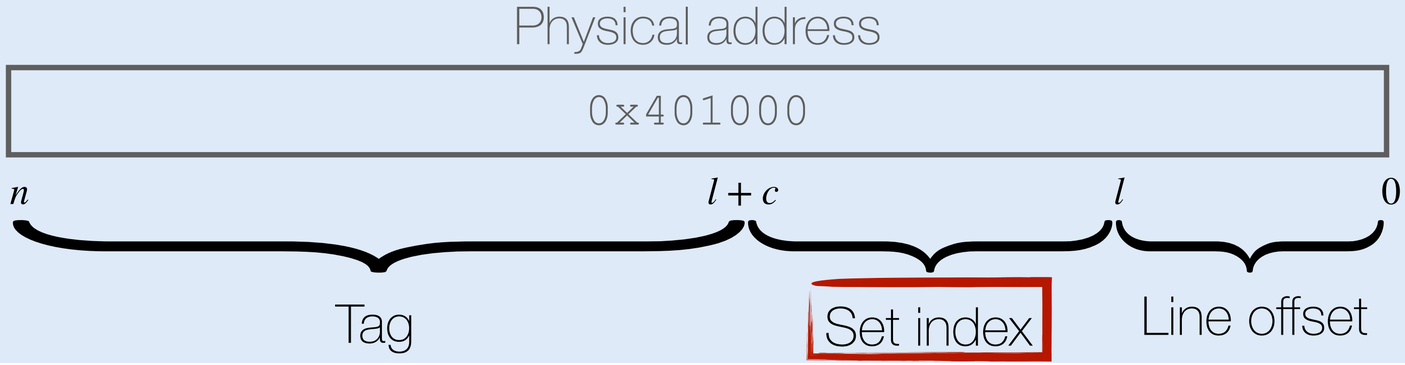
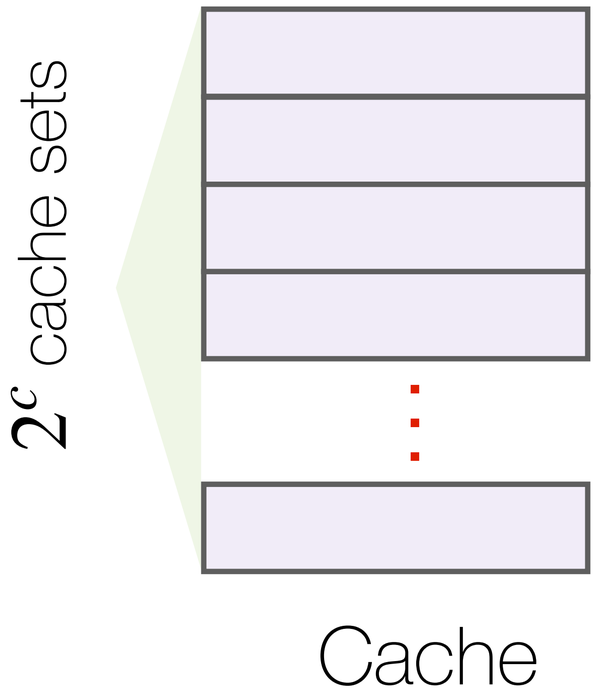


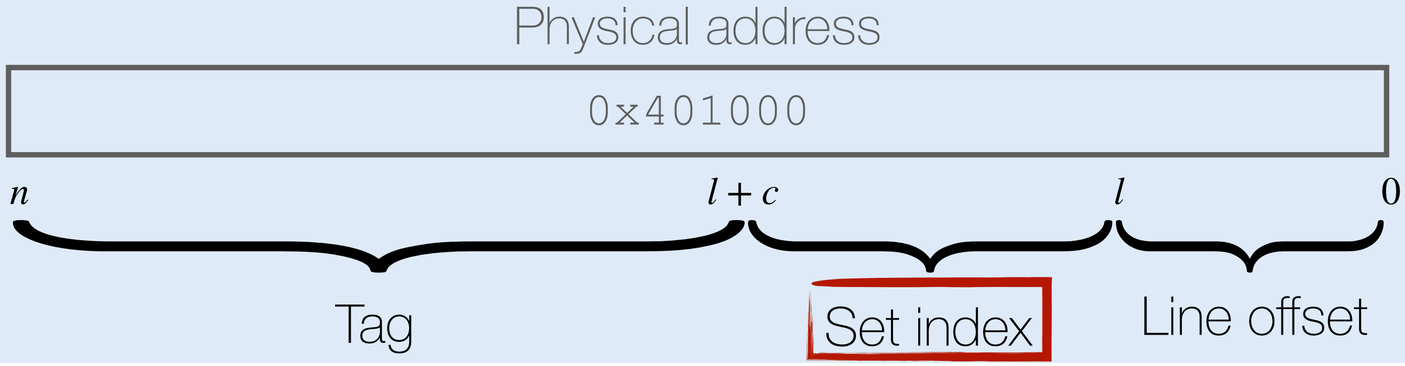
Addresses with the ***same set index*** map to the ***same cache set***

Directly mapped cache



Memory divided in ***blocks*** of 2^l bits

Mapping ***addresses*** to cache



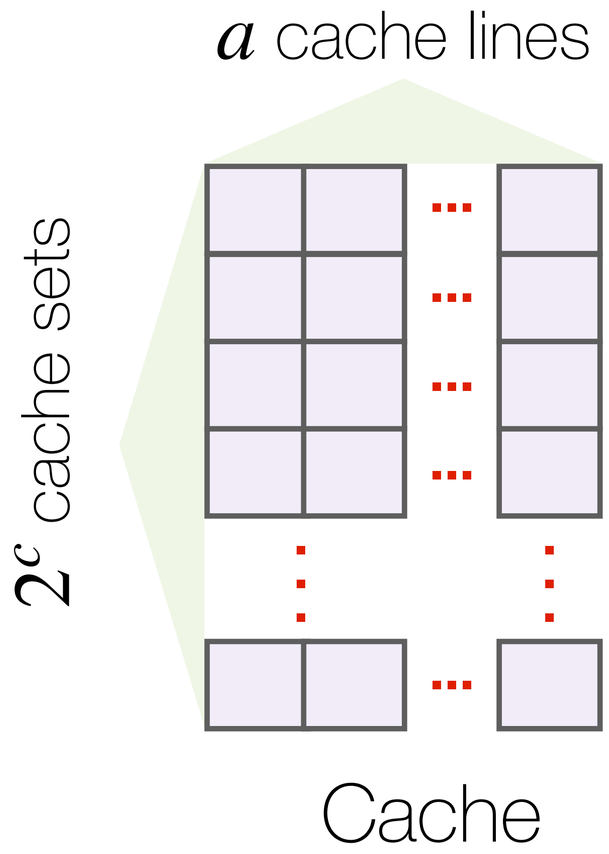
Addresses with the ***same set index*** map to the ***same cache set***

Divided in ***cache sets*** each one with 1 ***cache line***

Only ***1 block*** per set

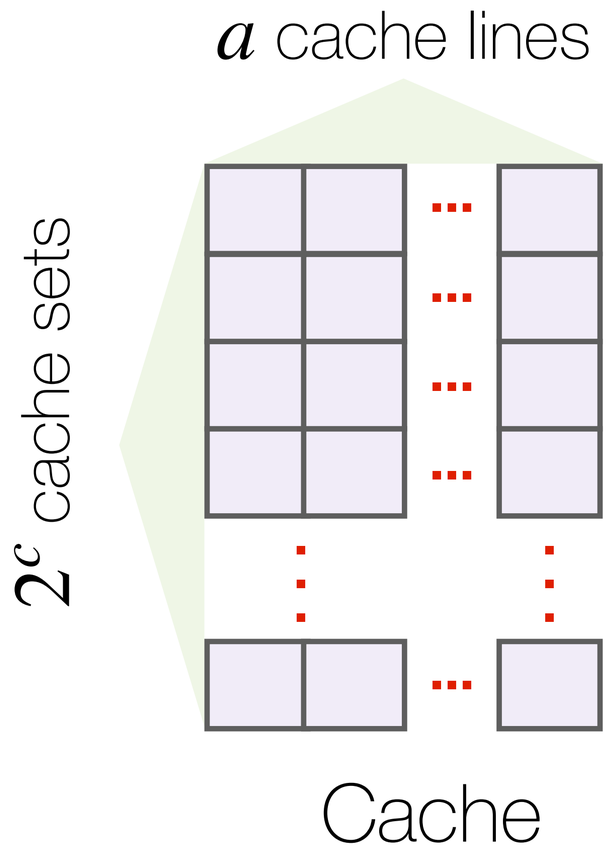
Set-associative caches

Set-associative caches



Divided in ***cache sets*** each one split into ***cache lines***

Set-associative caches



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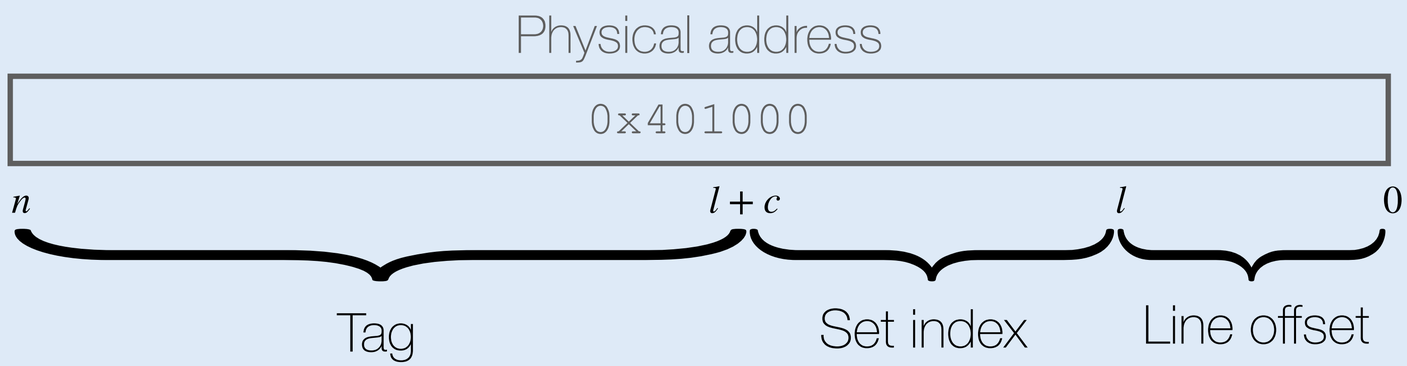
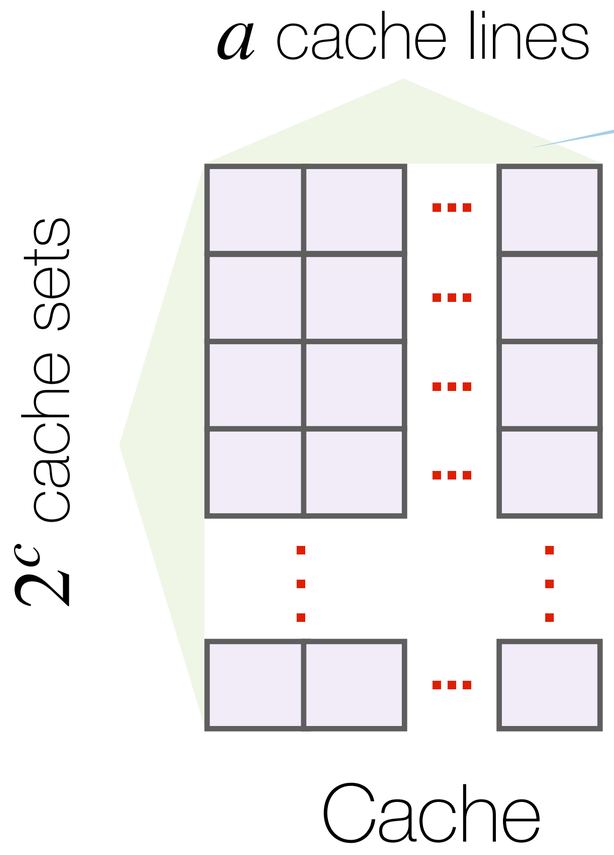


Addresses with the ***same set index*** map to the ***same cache set***

Set-associative caches

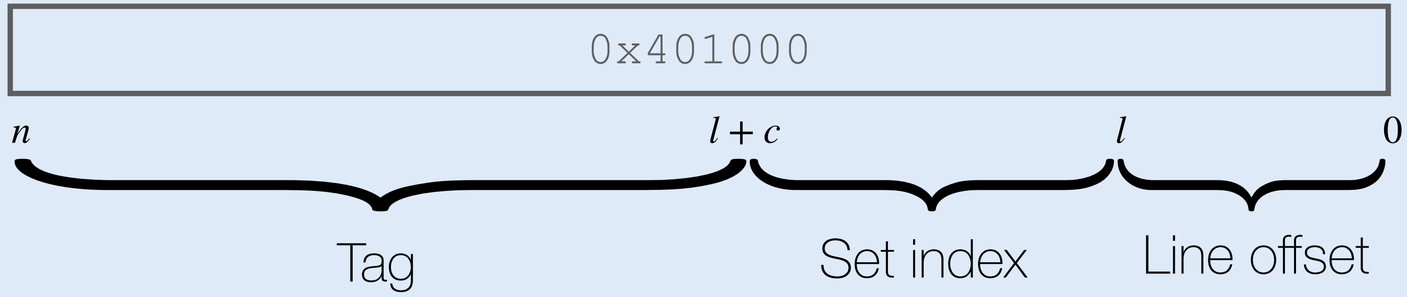
Intel Haswell
L1: 64 cache sets, 8 lines each
L3: 8192 cache sets, 16 lines each



Divided in ***cache sets*** each one split into ***cache lines***

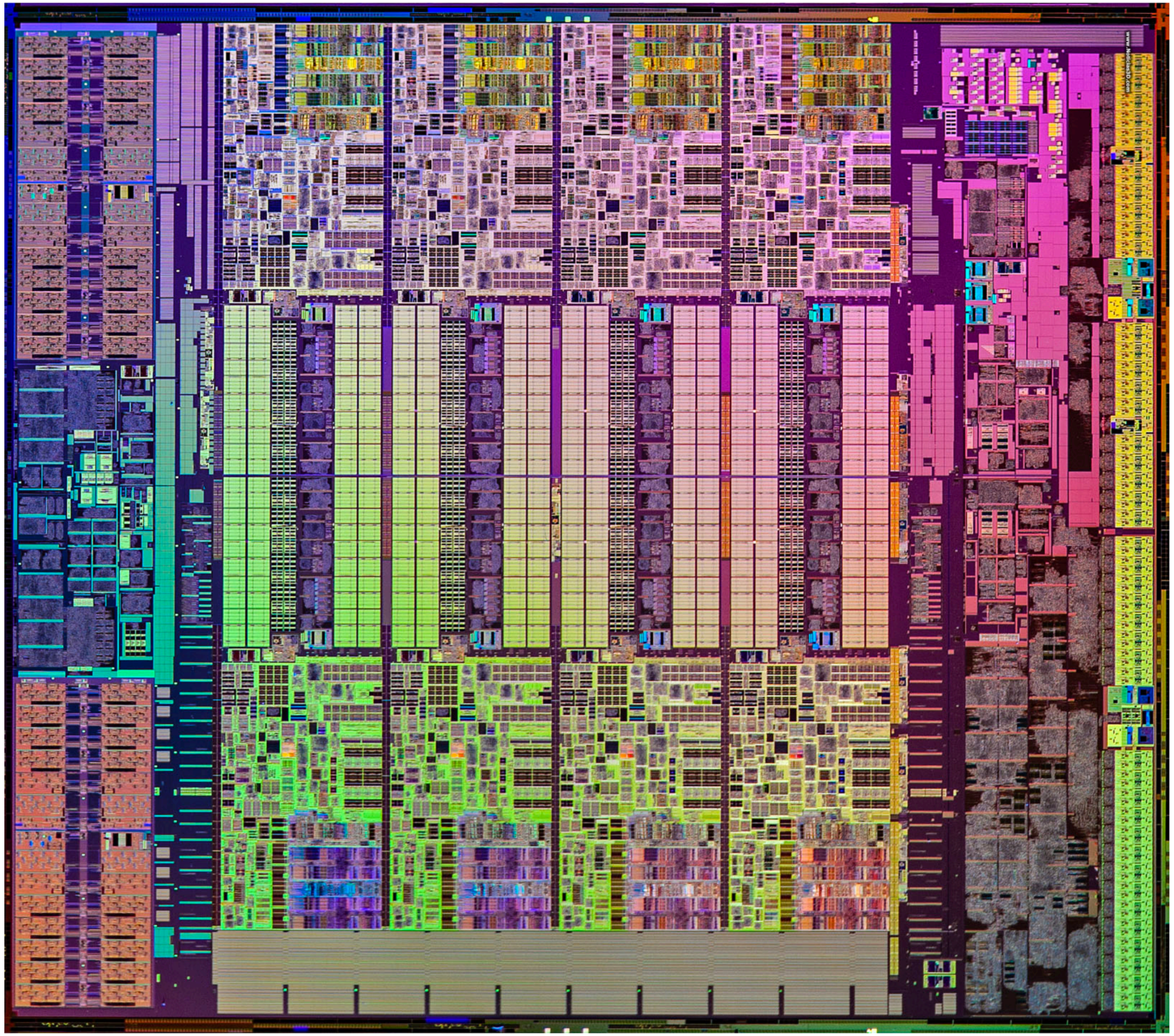
Memory divided in ***blocks*** of 2^l bits

Mapping ***addresses*** to cache



Addresses with the ***same set index*** map to the ***same cache set***

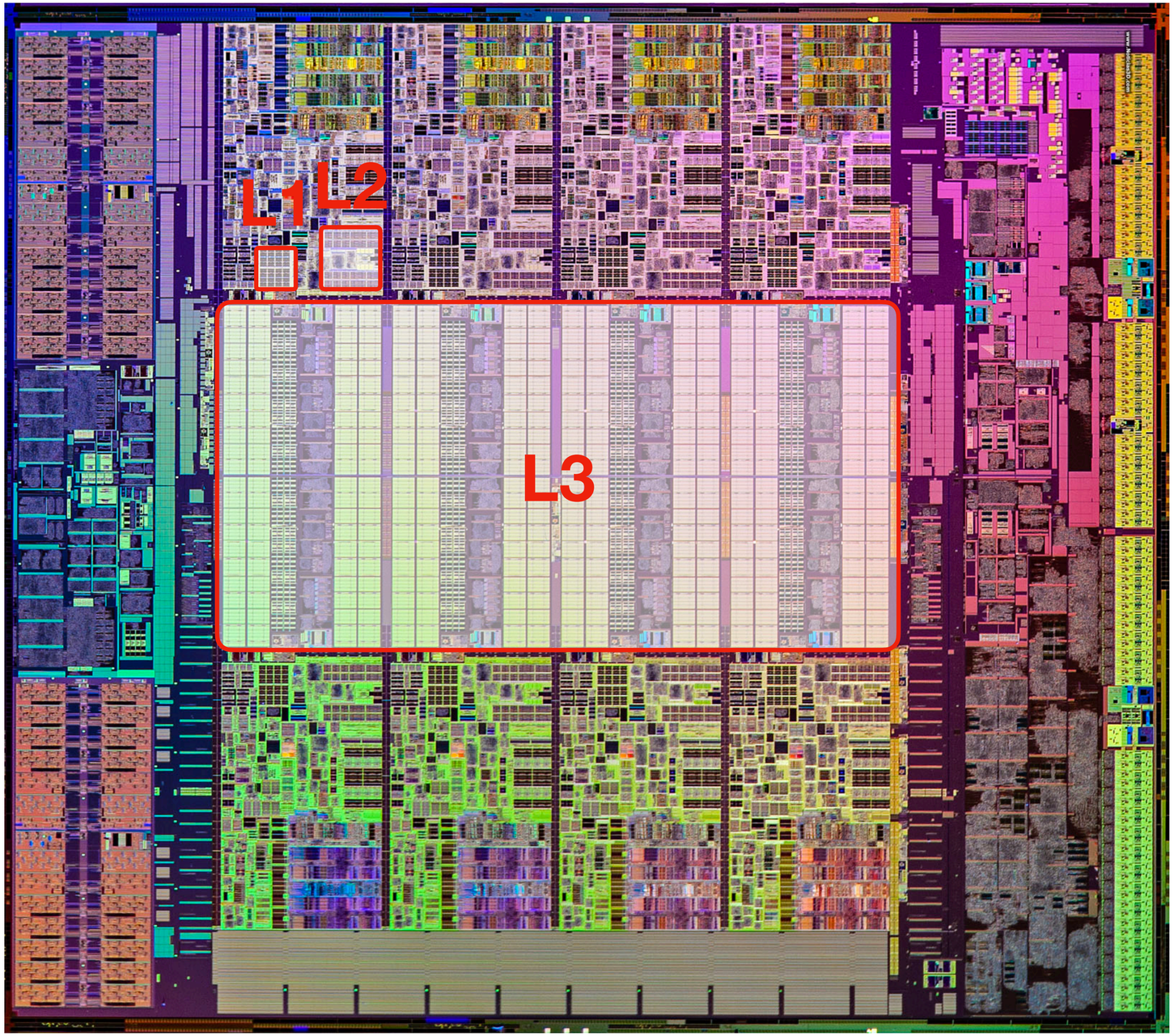
Cache hierarchy



Picture of Intel “Haswell-E” Eight Core CPU

Cache hierarchy

Processors have ***multiple levels*** of caches

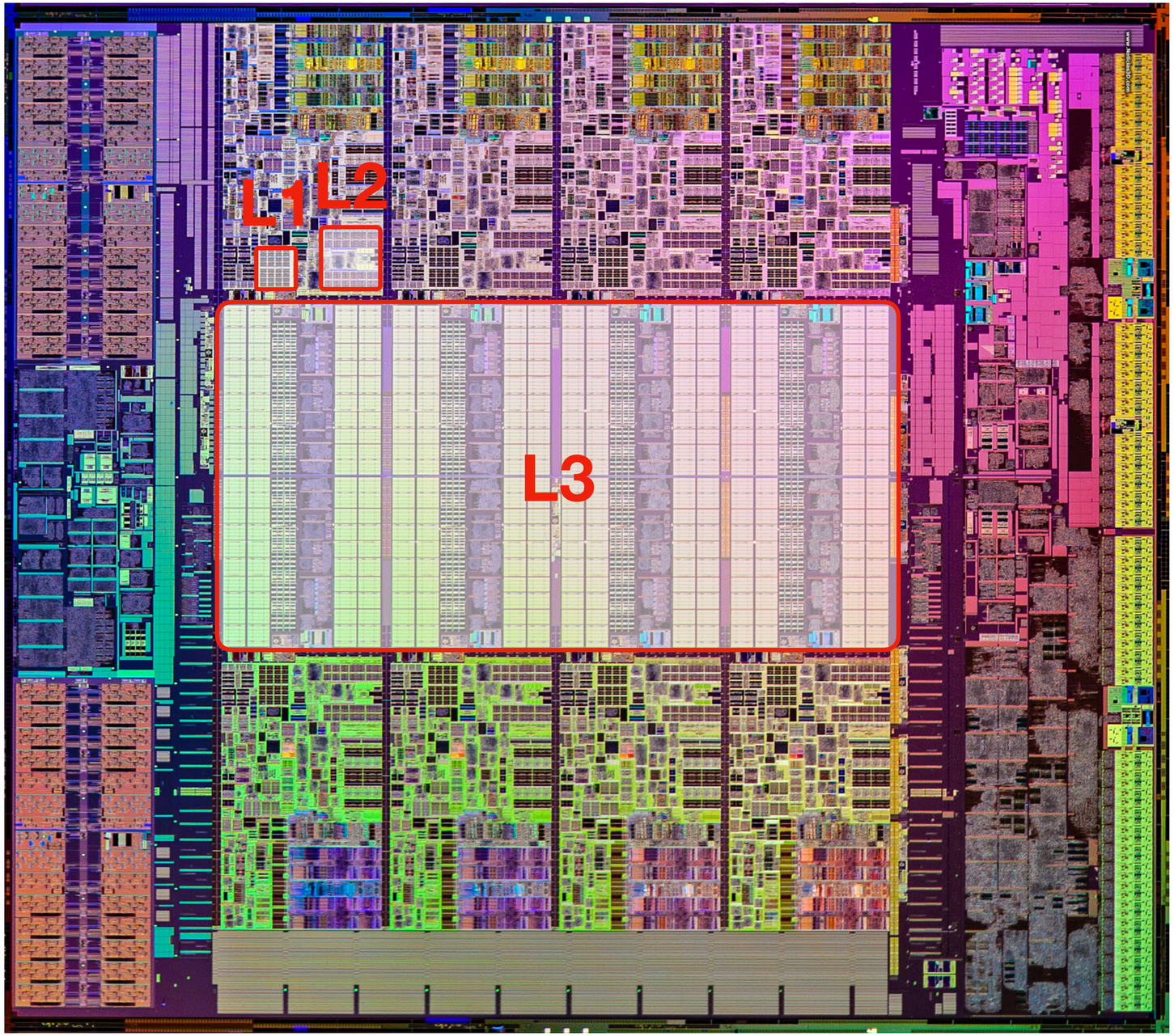


Picture of Intel “Haswell-E” Eight Core CPU

Cache hierarchy

Processors have ***multiple levels*** of caches

Memory ***requests*** travel through the ***hierarchy***



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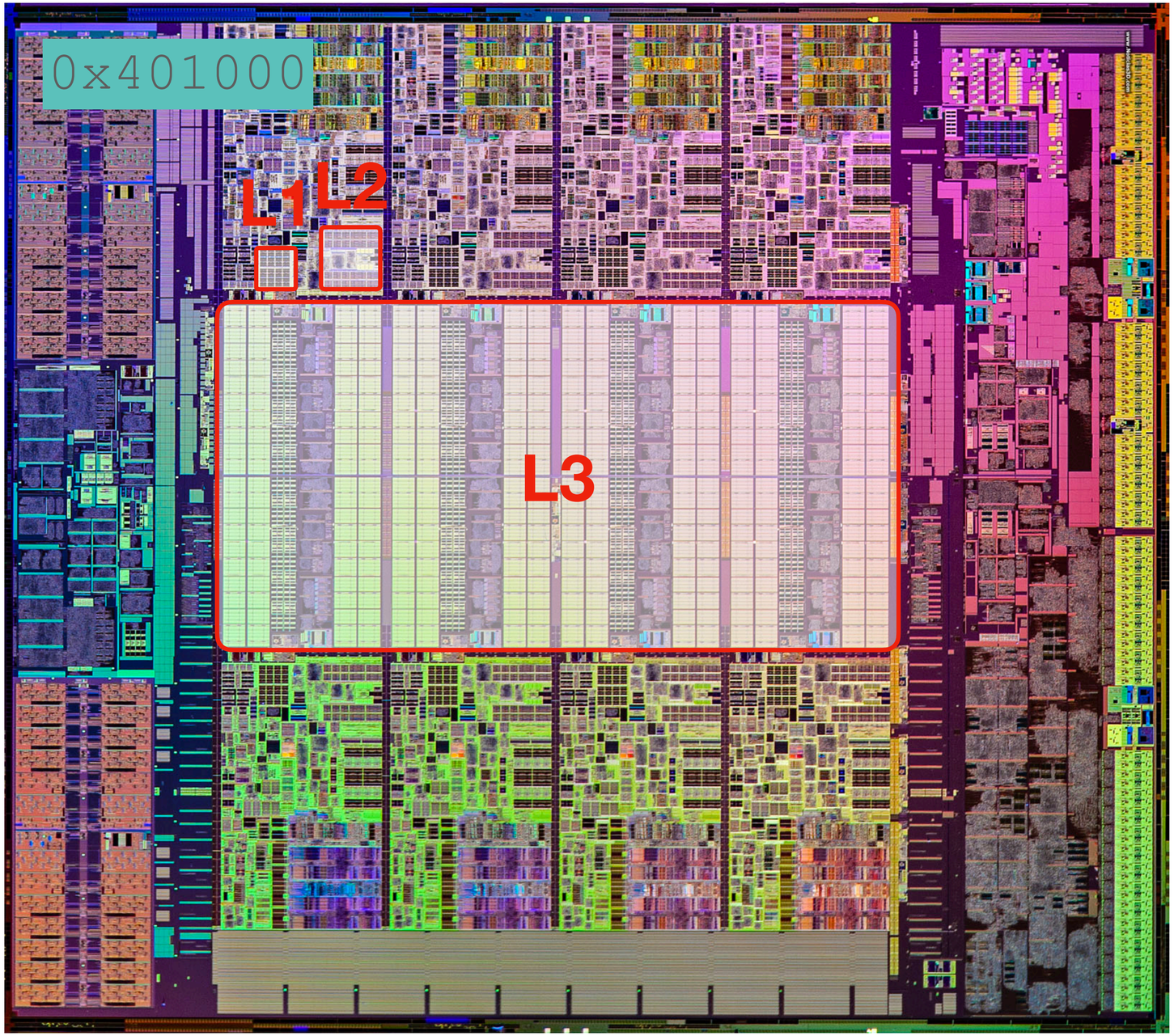

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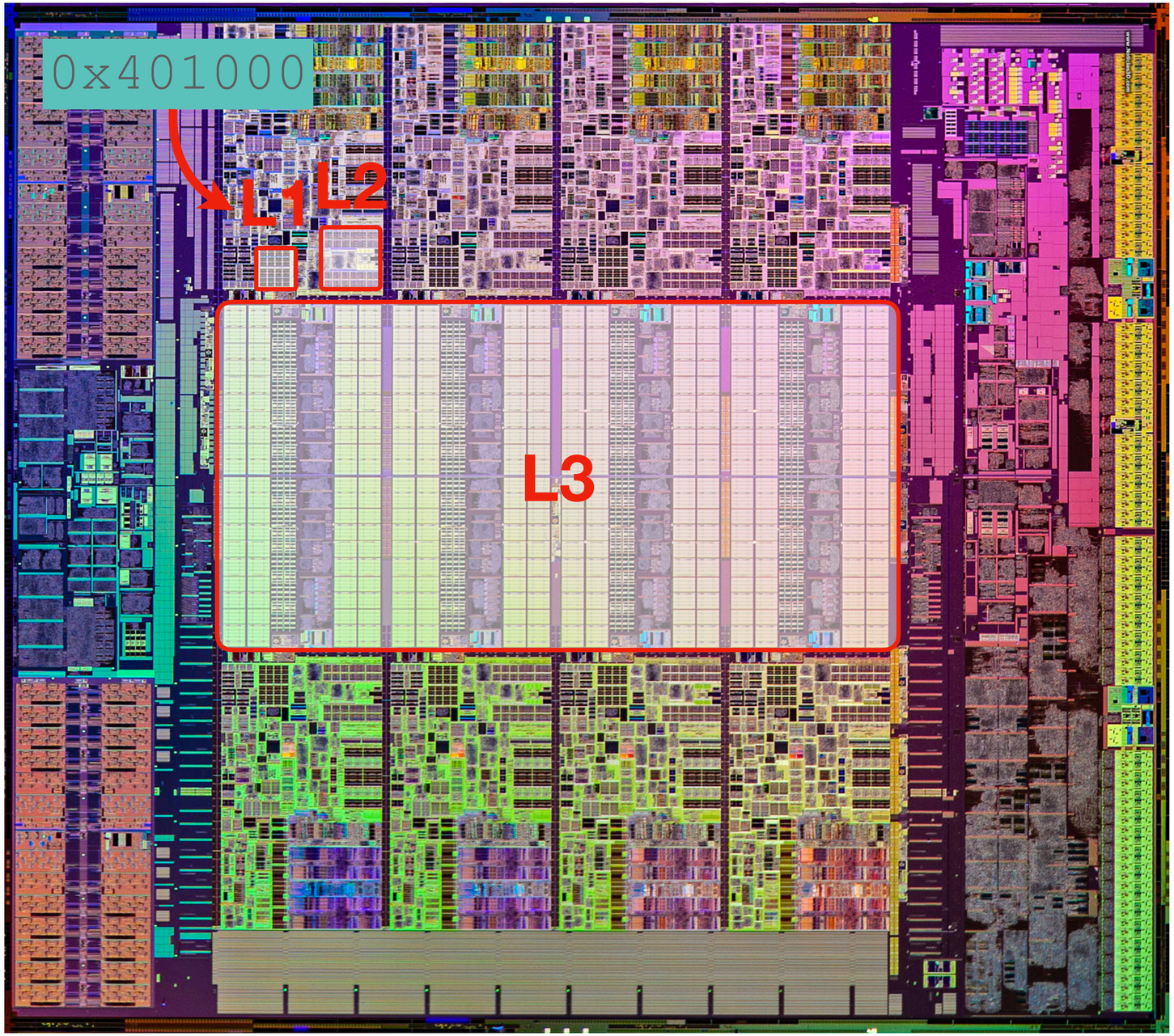

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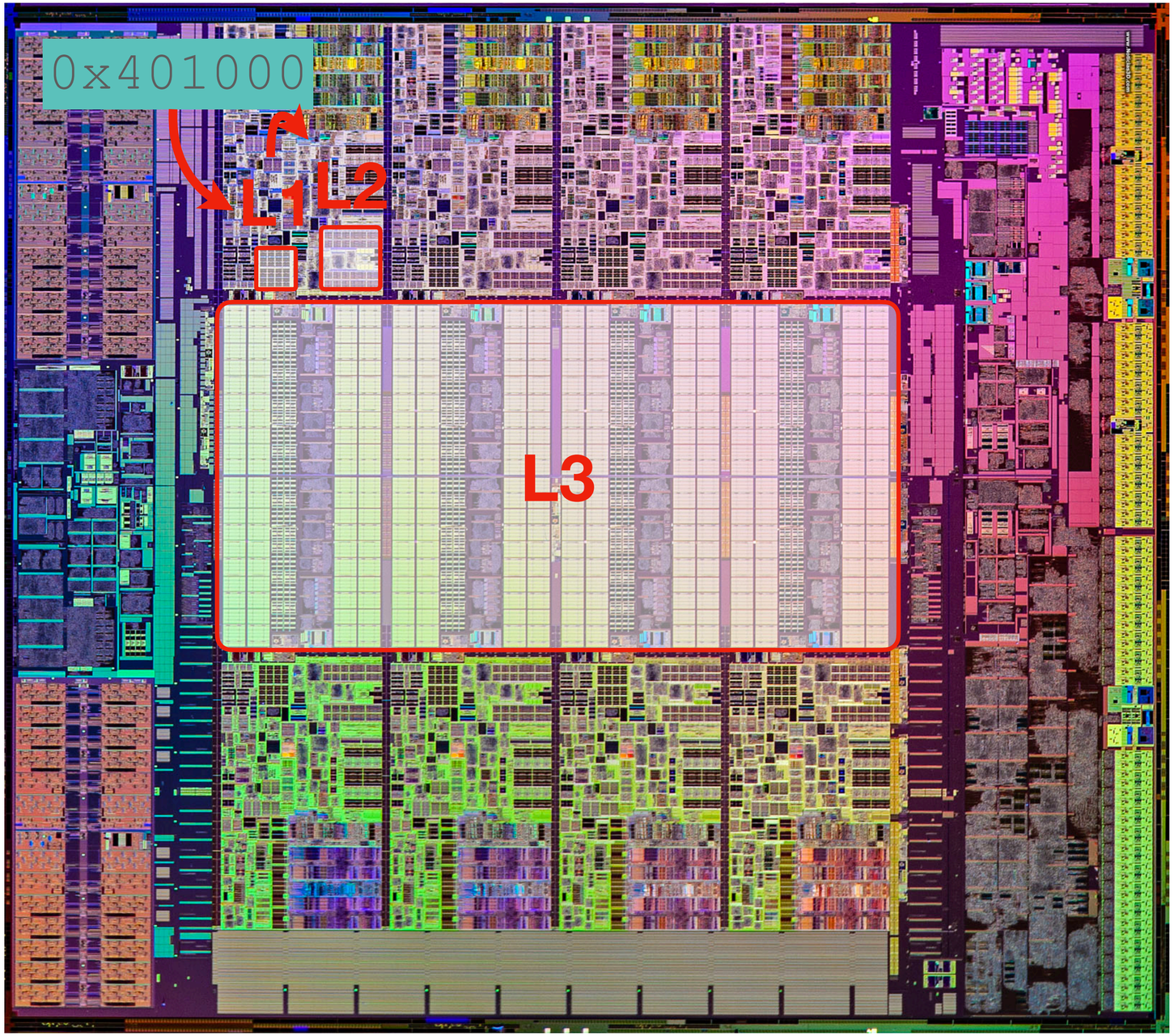

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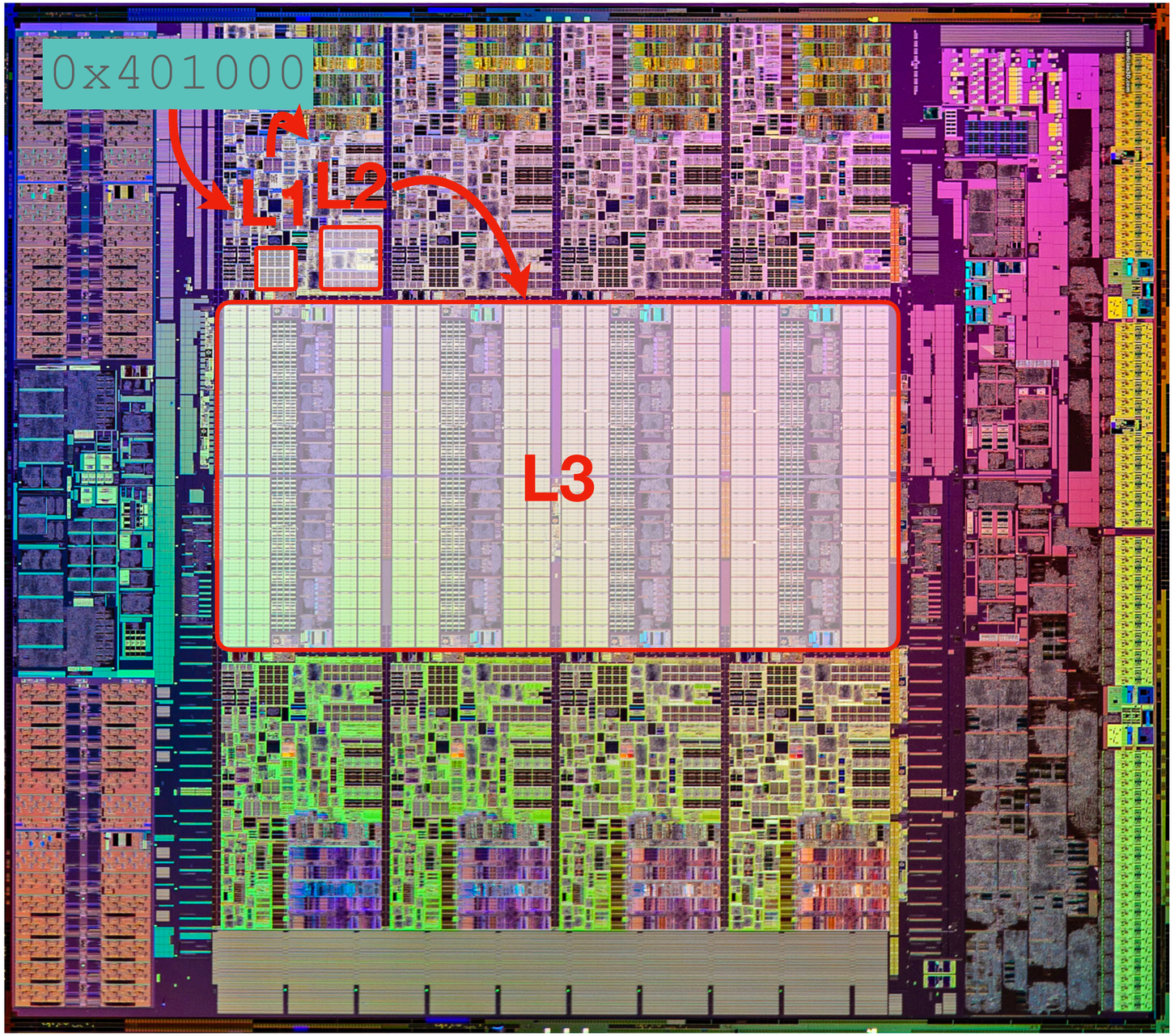
Processors have ***multiple levels*** of caches

Memory ***requests*** travel through the ***hierarchy***



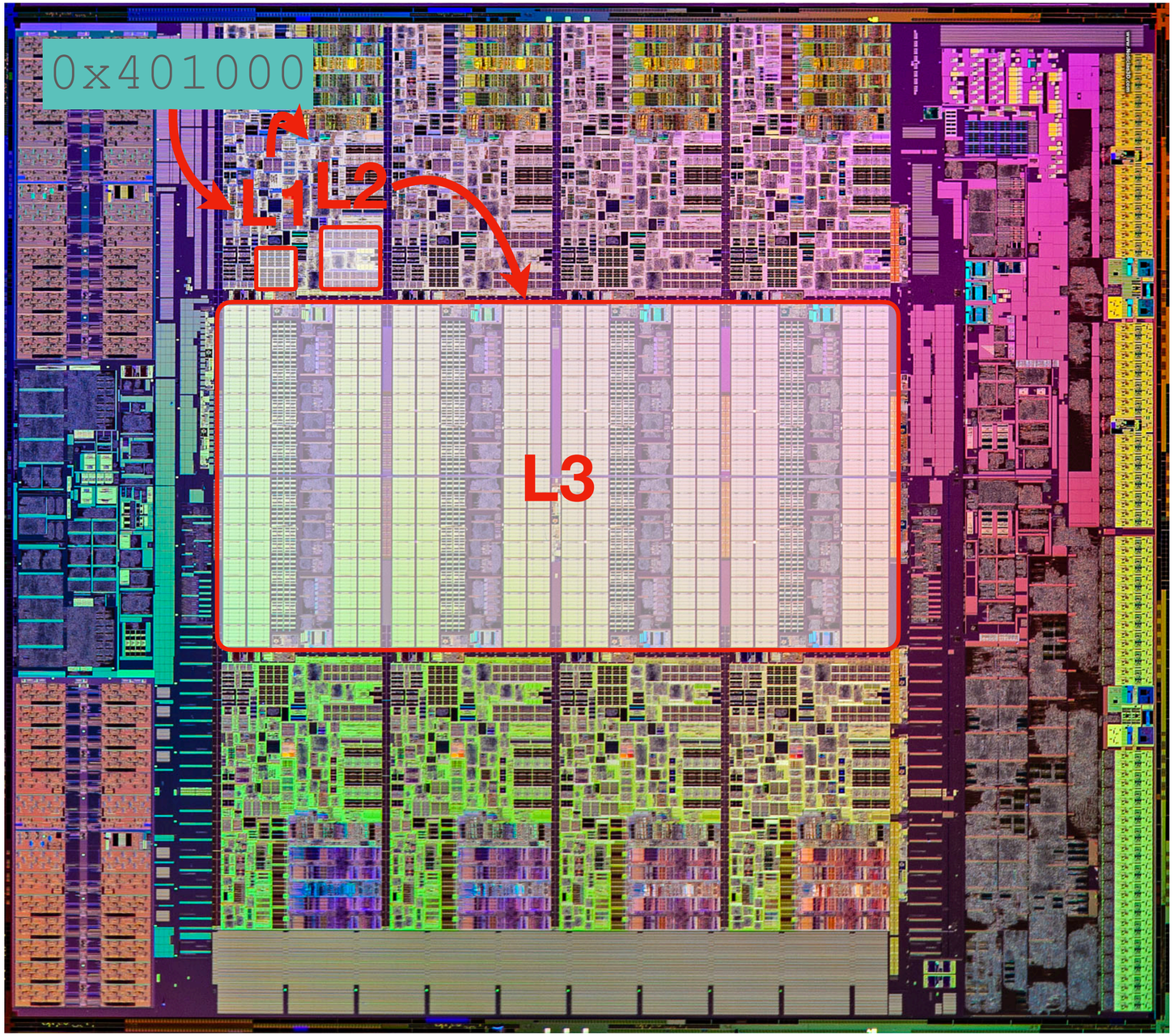
Picture of Intel “Haswell-E” Eight Core CPU

Cache hierarchy

Processors have ***multiple levels*** of caches

Memory ***requests*** travel through the ***hierarchy***

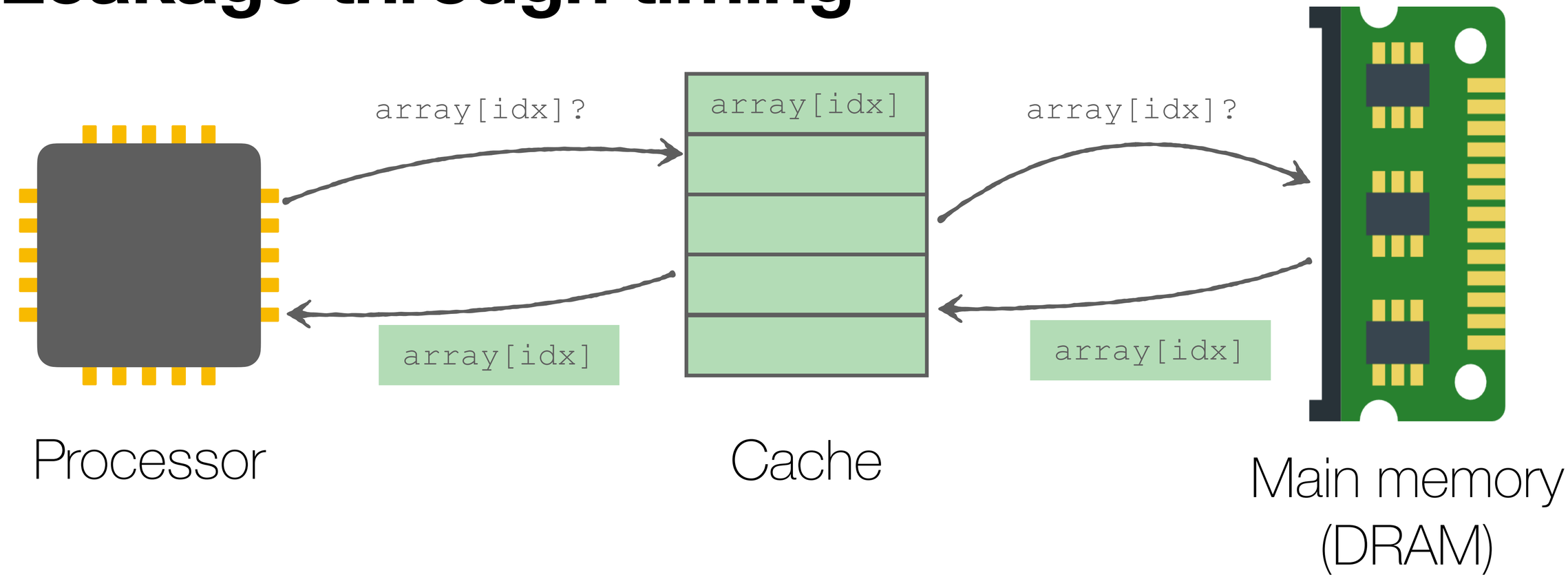
Cache hierarchy can be ***inclusive***, ***exclusive***, or ***neither***



Picture of Intel “Haswell-E” Eight Core CPU

Caches and side channels

Leakage through timing



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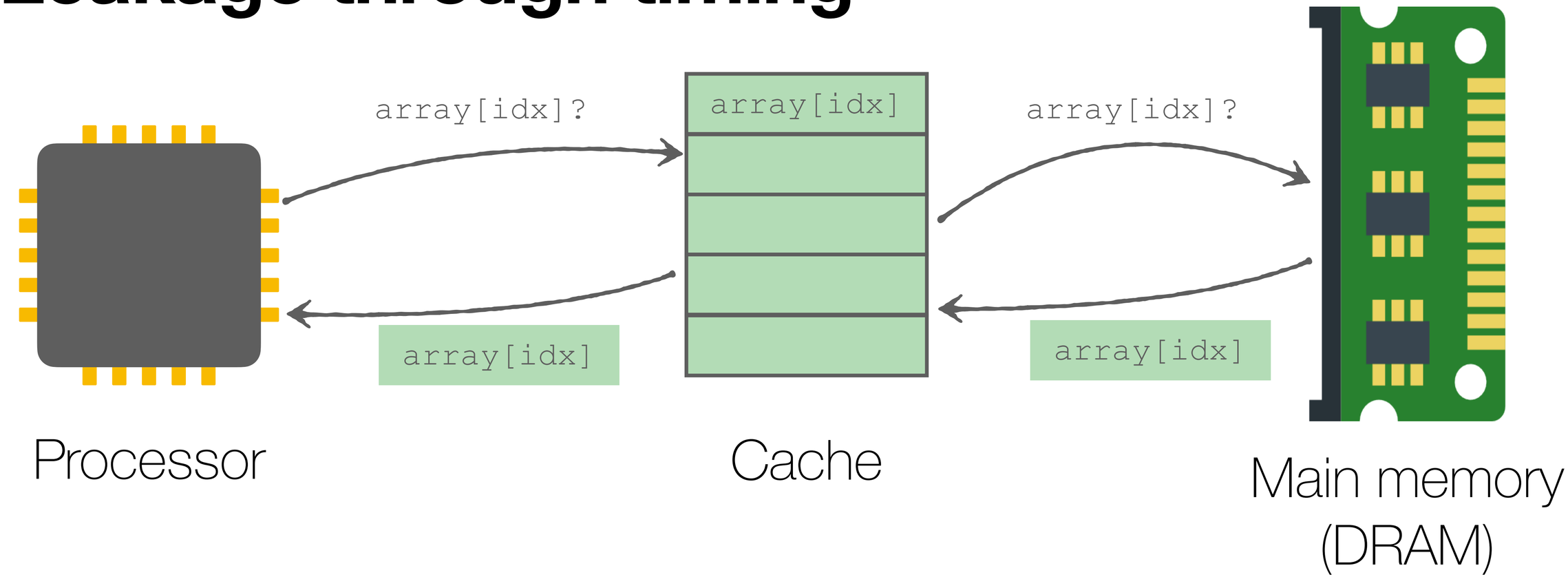
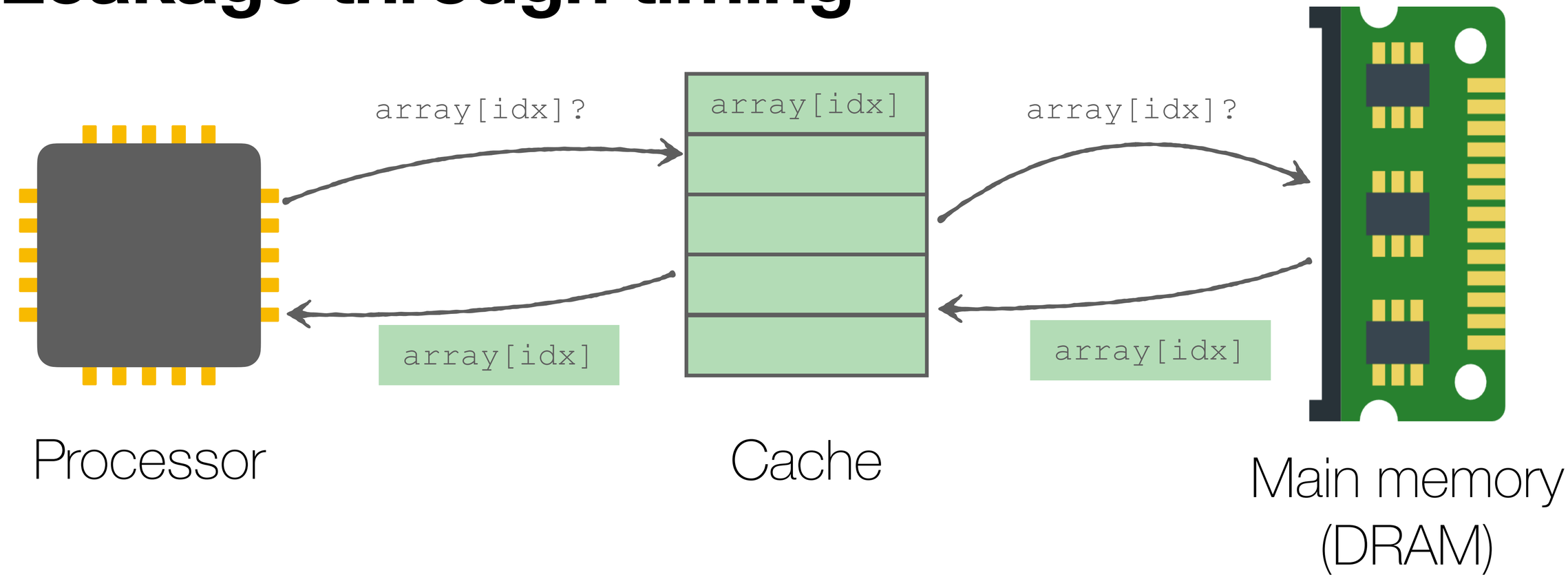


Latency of memory operations ***leaks*** information about ***cache state***

Leakage through timing

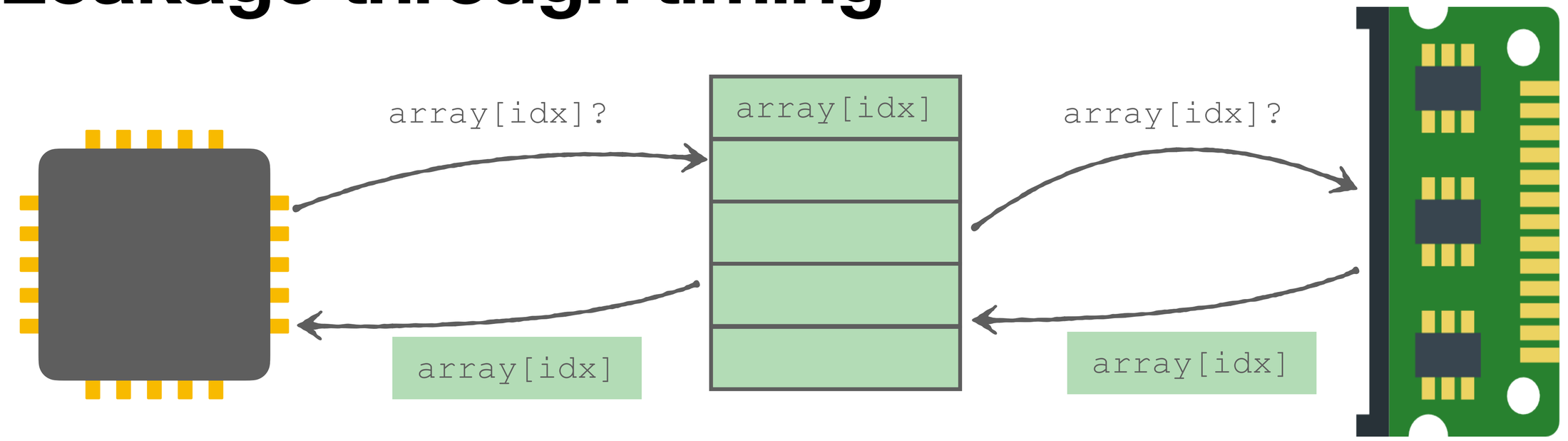


Latency of memory operations ***leaks*** information about ***cache state***

Cache hit —> block already ***in*** cache

Cache miss —> block ***not in*** cache

Leakage through timing



Latency of memory operations ***leaks*** information about ***cache state***

Cache hit —> block already ***in*** cache
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Cache state depends on ***prior*** memory ***accesses***

Leakage through timing

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Goal:
Building primitive for
observing victim's
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Leakage through timing

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Why?

In many cryptographic implementations, ***memory accesses*** leak information about the ***key***

Leakage through timing

Goal:
Building primitive for ***observing*** victim's ***memory accesses***

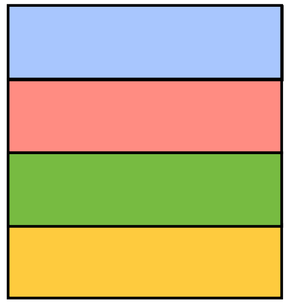
Why?

In many cryptographic implementations, ***memory accesses*** leak information about the ***key***

- Key-dependent memory accesses (e.g., lookup tables in AES or DES)
- Key-dependent control-flow (e.g., Square-and-Multiply in RSA)

Ex: Cache-based Side Channel

Main memory



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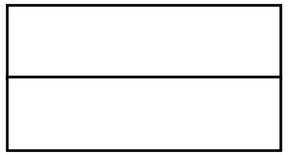

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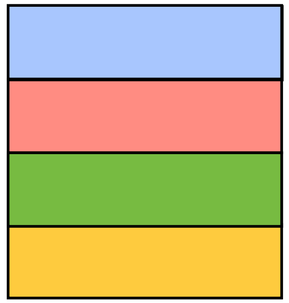

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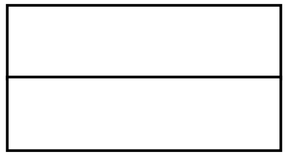

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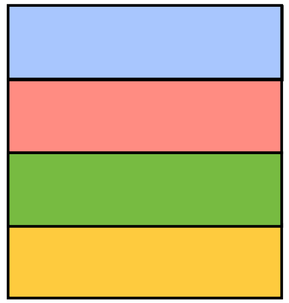

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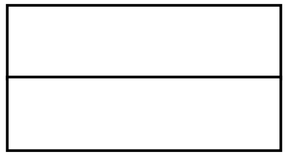

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Ex: Cache-based Side Channel

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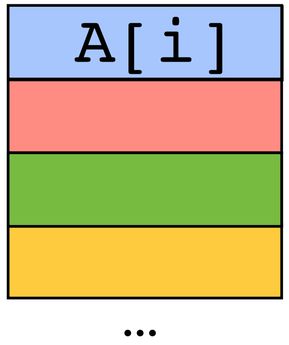

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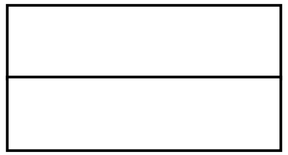

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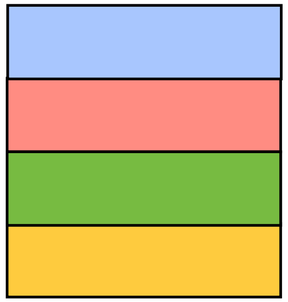

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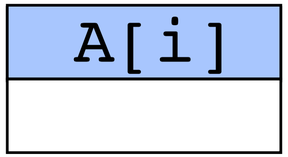

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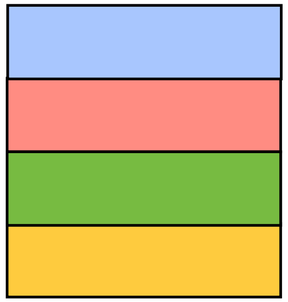

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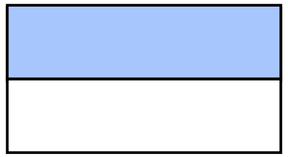

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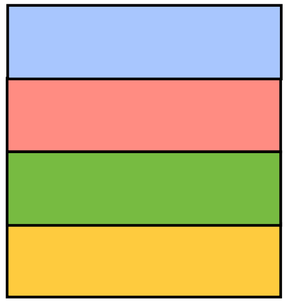

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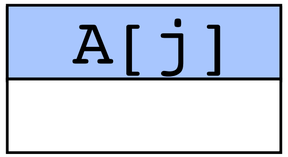

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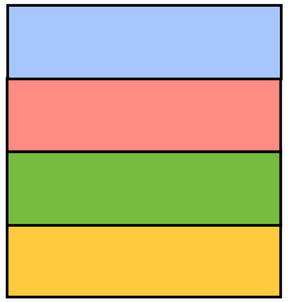

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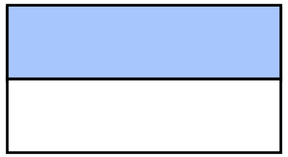

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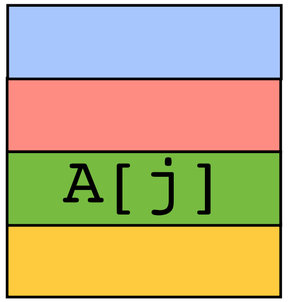

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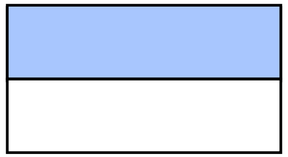

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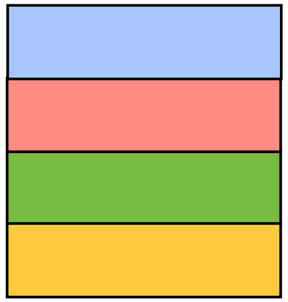

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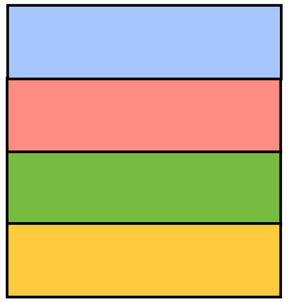

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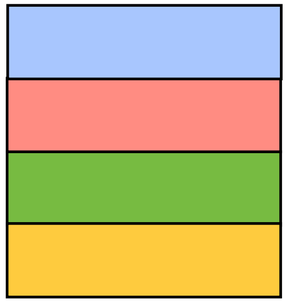
```

Latency of lookups ***leaks relation*** between indices

Ex: Cache-based Side Channel

Main memory



...

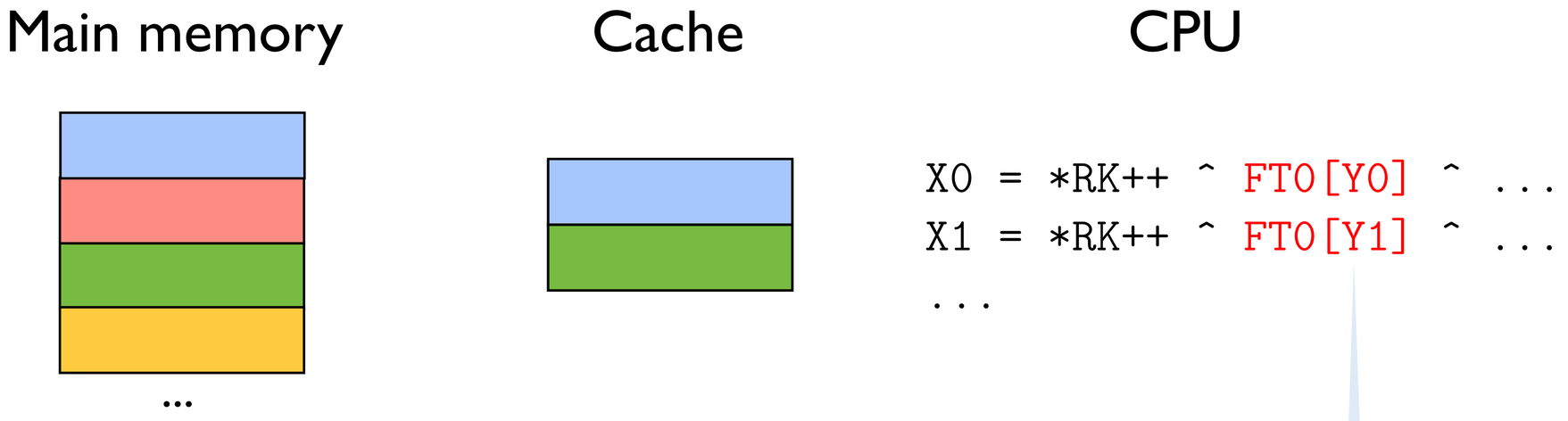
Cache

CPU

```
X0 = *RK++ ^ FT0[Y0] ^ ...
X1 = *RK++ ^ FT0[Y1] ^ ...
...
```

Code from PolarSSL AES implementation using T-tables

Ex: Cache-based Side Channel



- First attacks: 2005 (Bernstein/Shamir)
- Increasingly effective attacks: 2013… (Yarom/…)

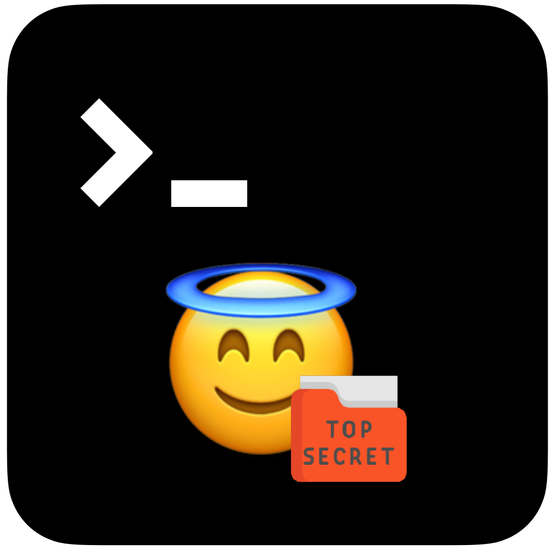
Two classes of attacks

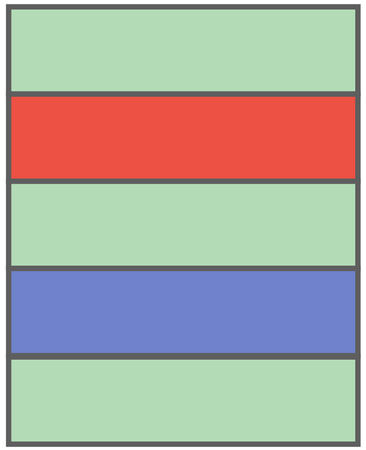
Two classes of attacks

Attacks that ***infer memory accesses*** from ***victim's execution time***

Attacks that ***infer memory accesses*** from ***cache state***

Inferring memory accesses from exec. time





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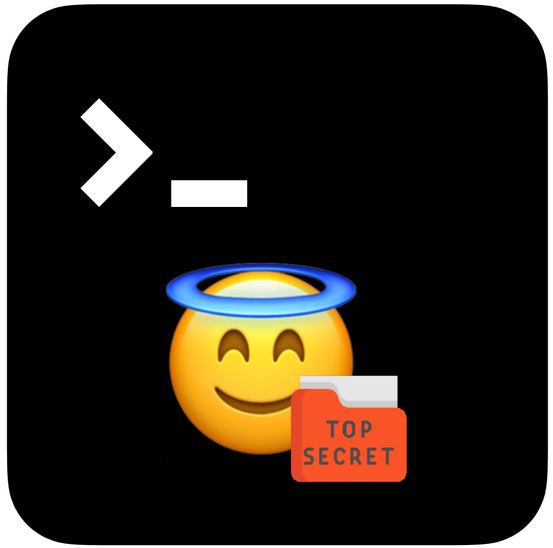

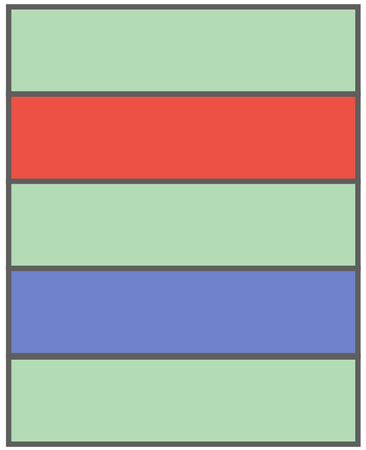

Cache

Victim's ***execution time*** depends on ***initial cache state*** and performed ***memory accesses***

Inferring memory accesses from exec. time

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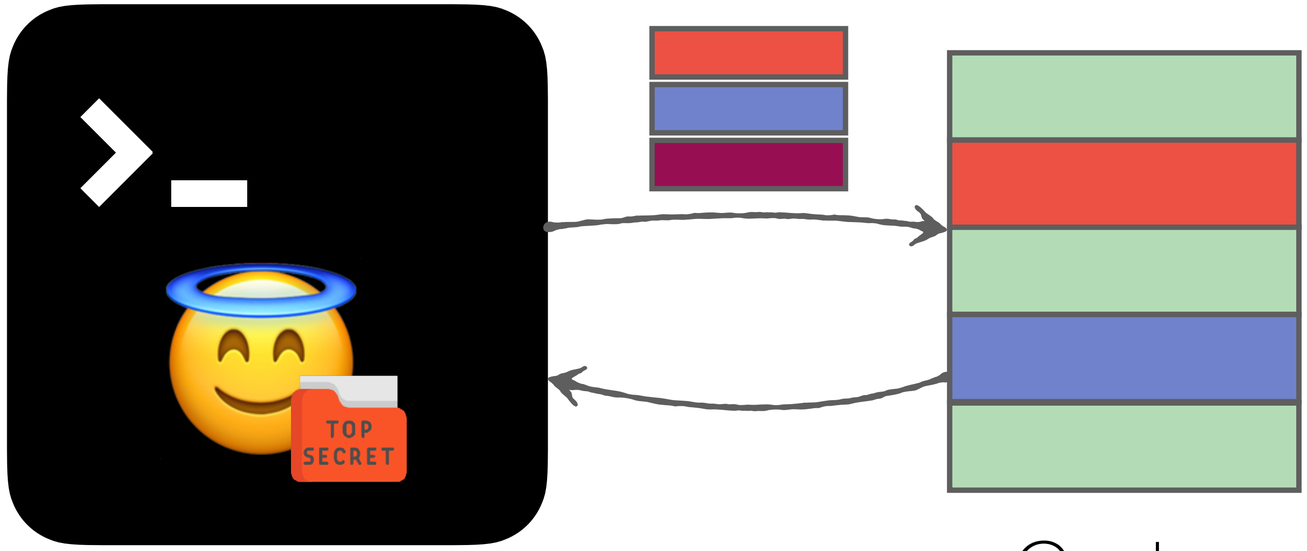

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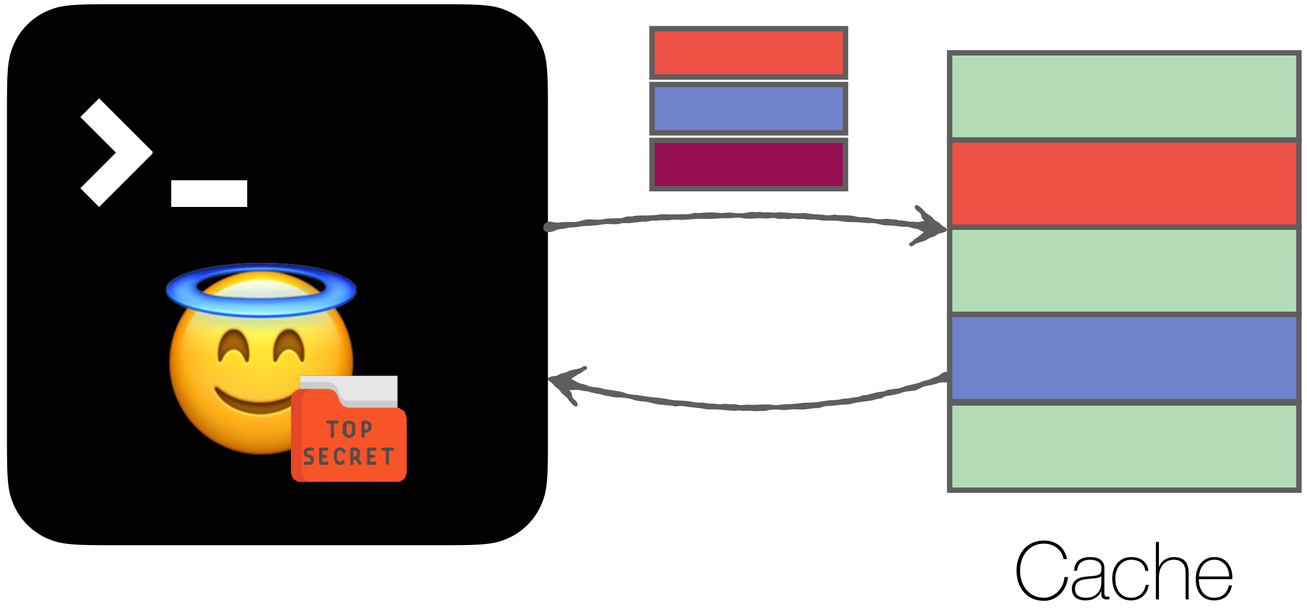

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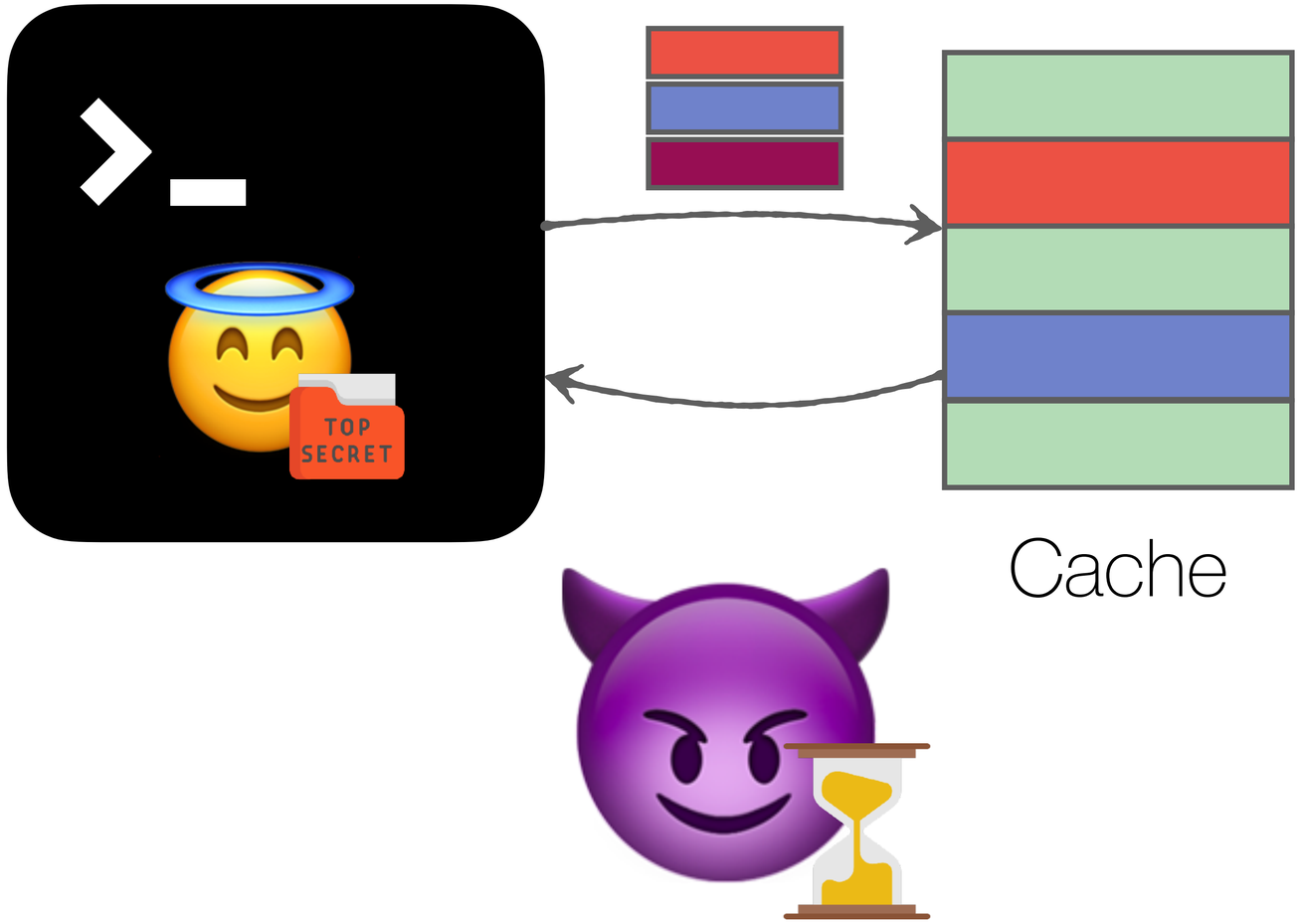
Attacker measures ***victim's execution time*** and infers information about ***memory accesses***

Inferring memory accesses from exec. time



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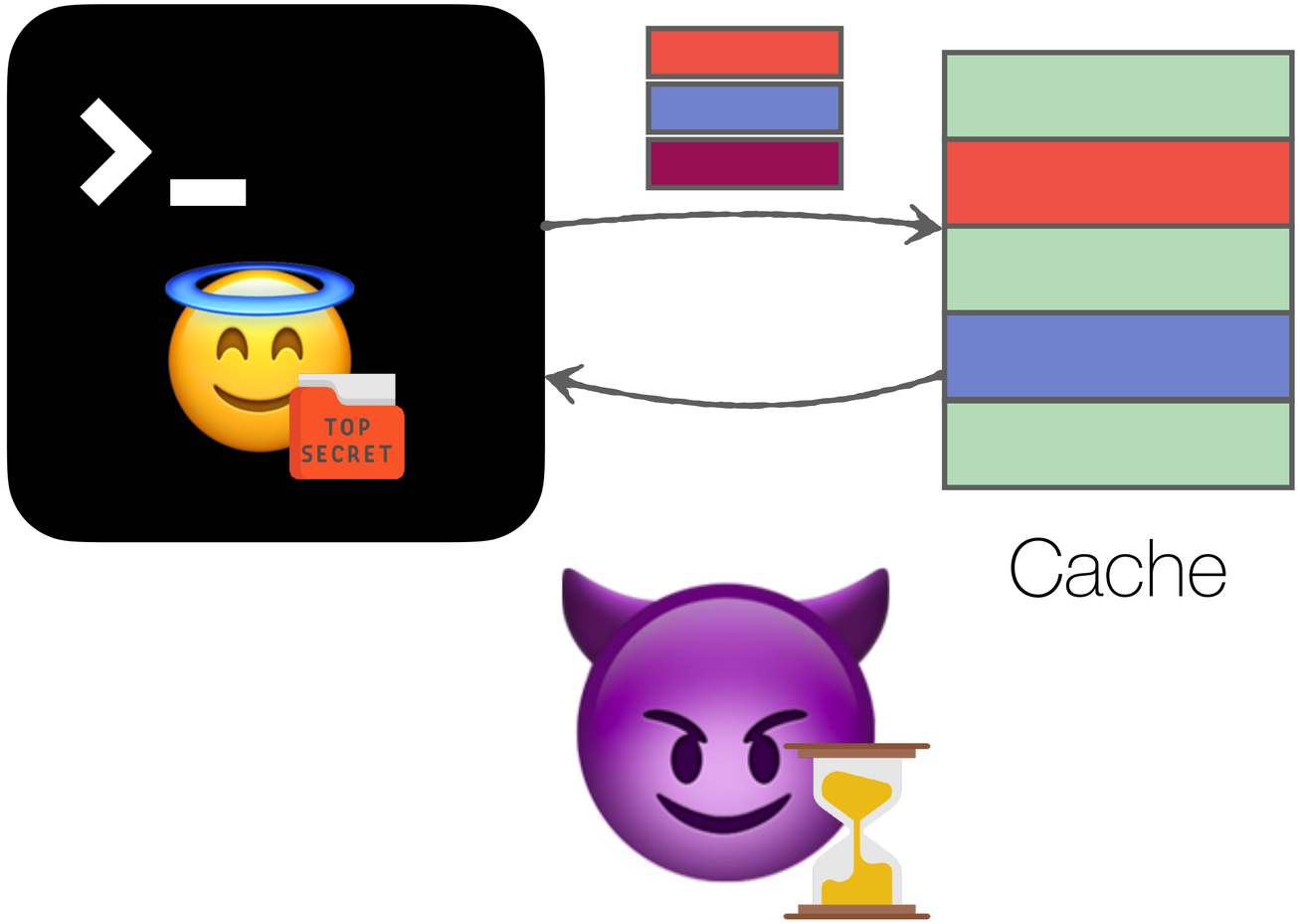

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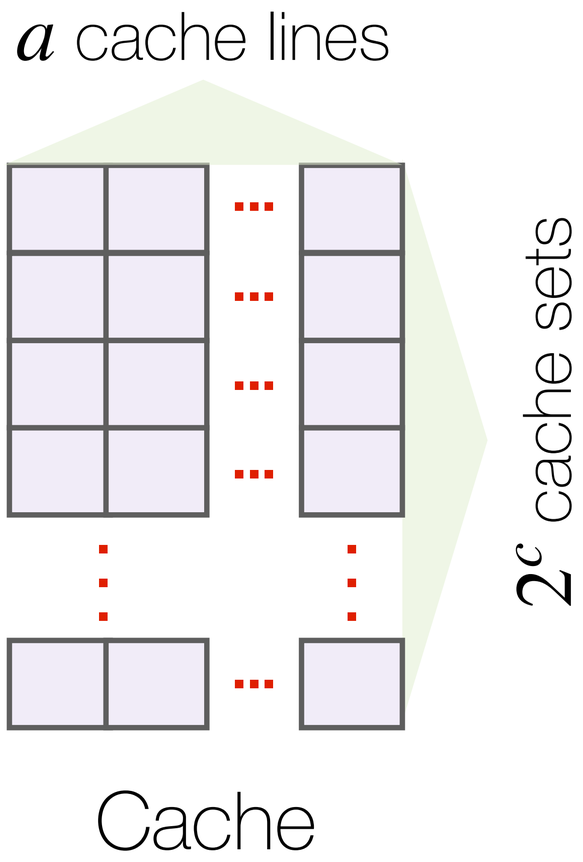
Noisy measurements

Evict+Time



D. Osvik, A. Shamir, E. Tromer — Cache attacks and countermeasures: the case of AES— 2005

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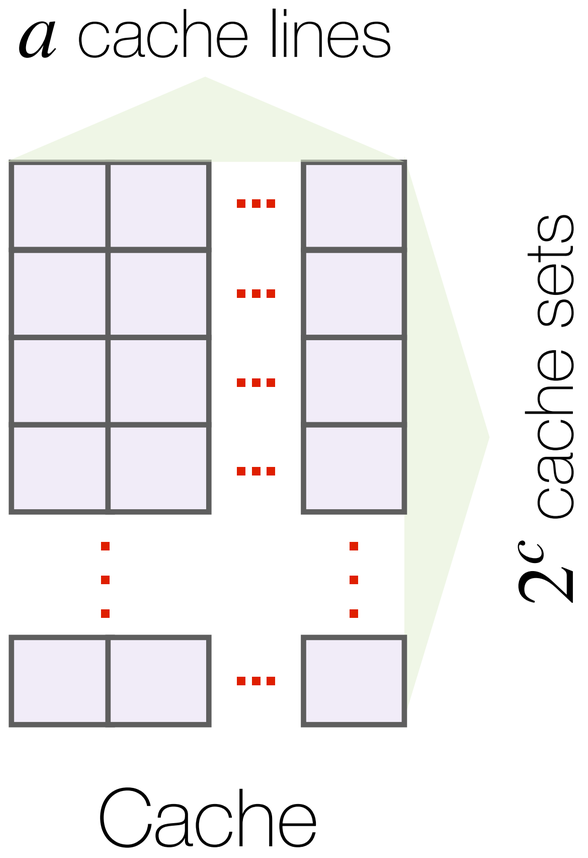

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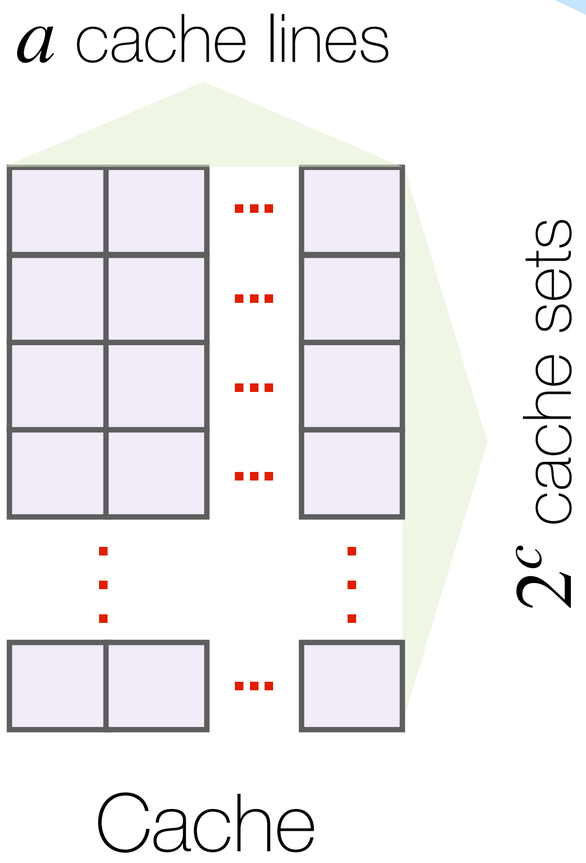
D. Osvik, A. Shamir, E. Tromer — Cache attacks and countermeasures: the case of AES— 2005

Evict+Time

Attacker controls when victim starts



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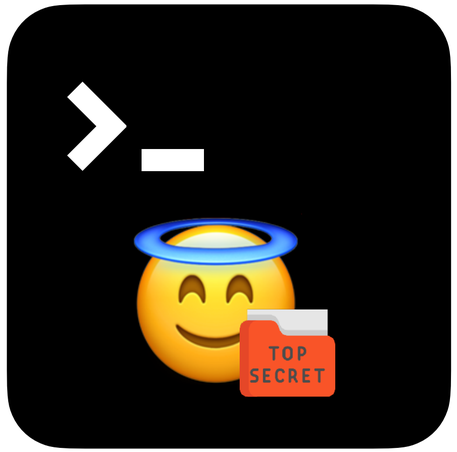

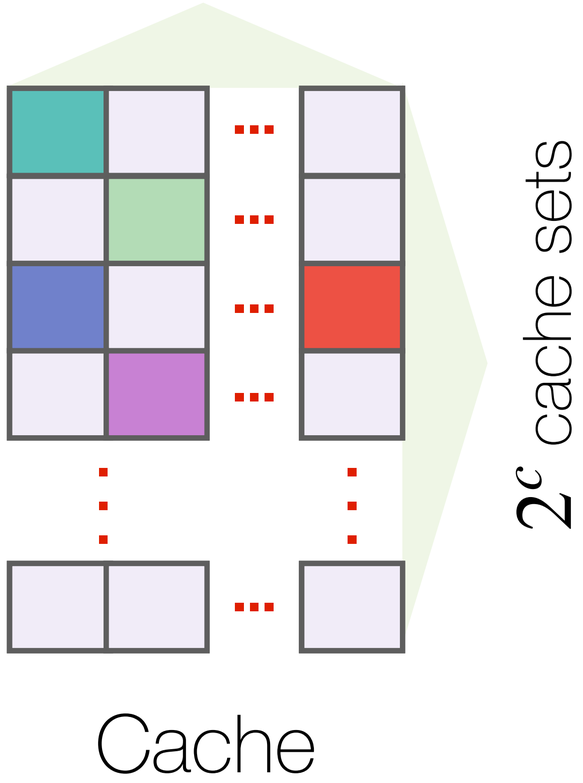

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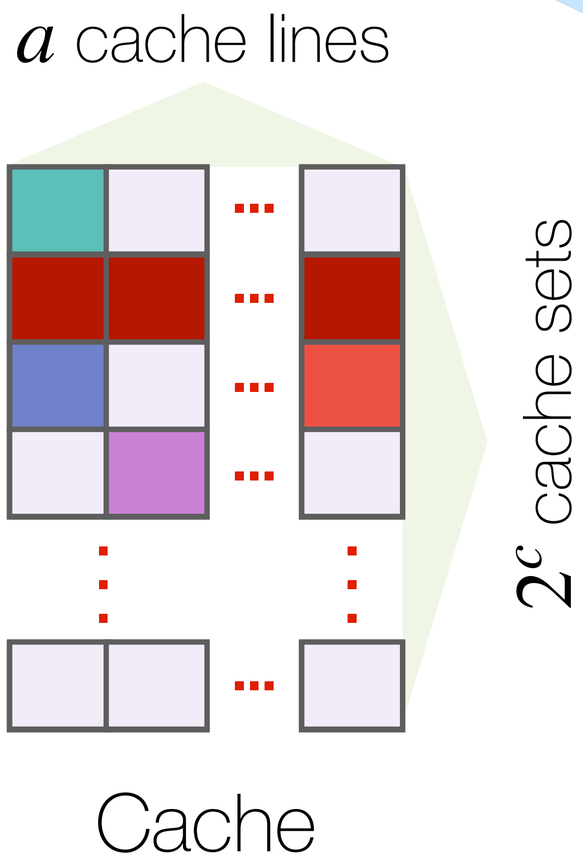

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2. ***Evict:*** Attacker ***removes*** victim's data from cache set

D. Osvik, A. Shamir, E. Tromer — Cache attacks and countermeasures: the case of AES— 2005

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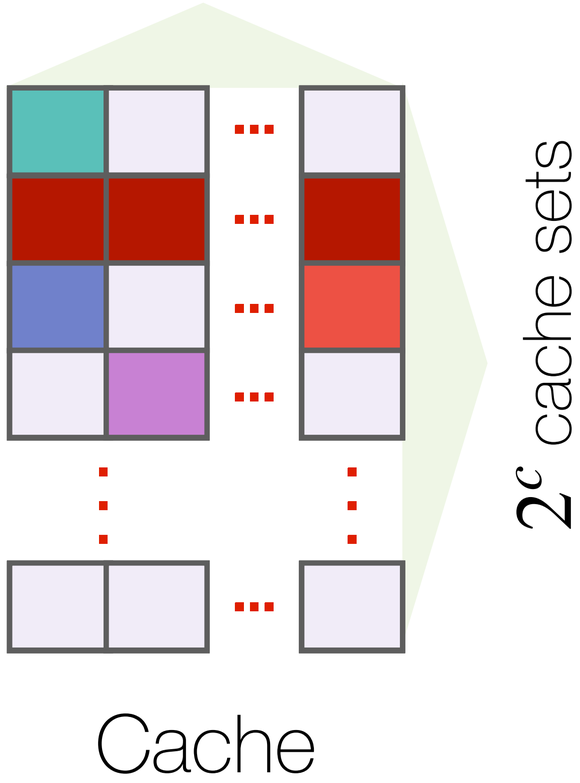
Attacker controls when victim starts

Eviction set needed: more than a blocks targeting the cache set



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D. Osvik, A. Shamir, E. Tromer — Cache attacks and countermeasures: the case of AES— 2005

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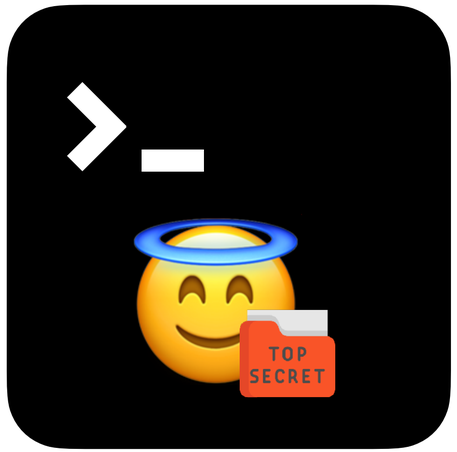

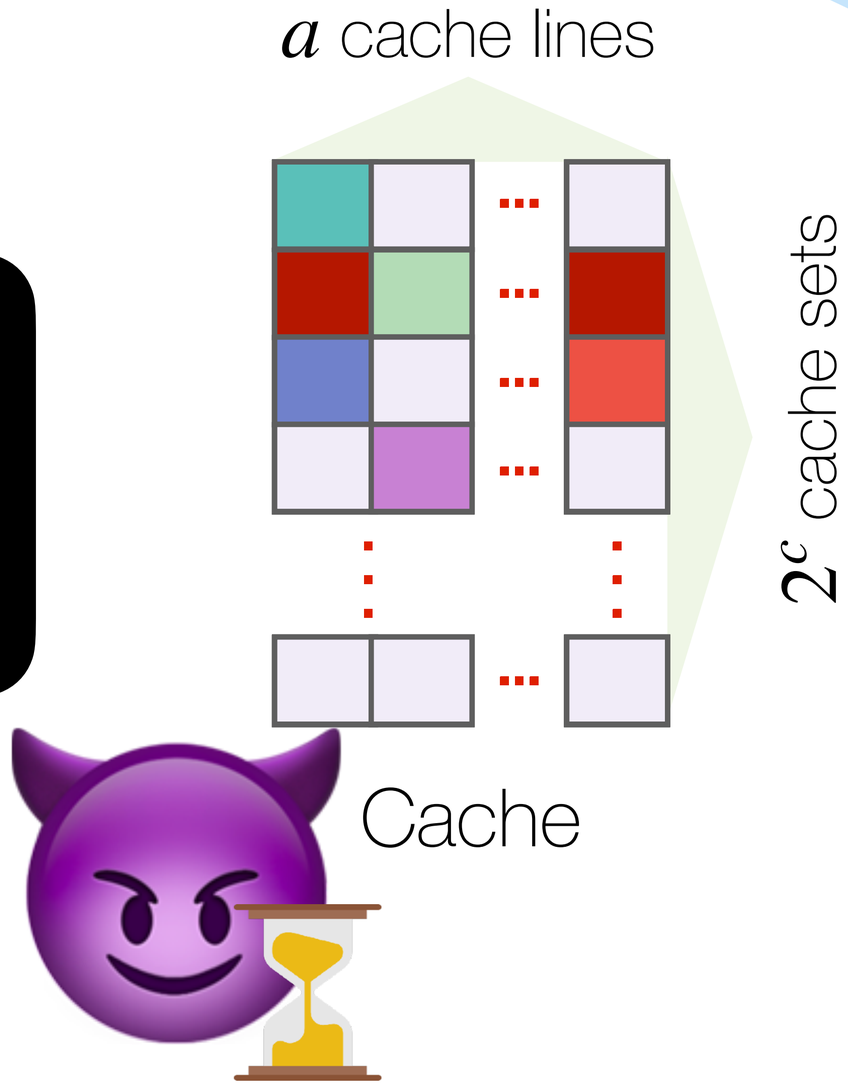

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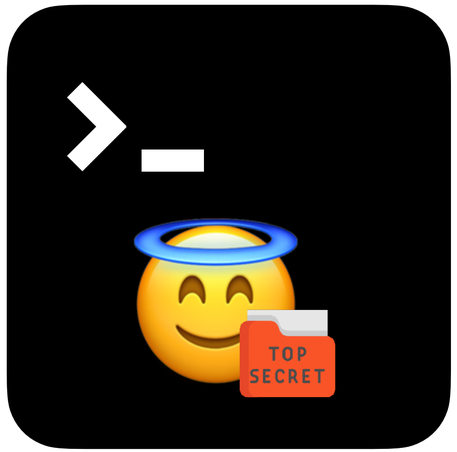

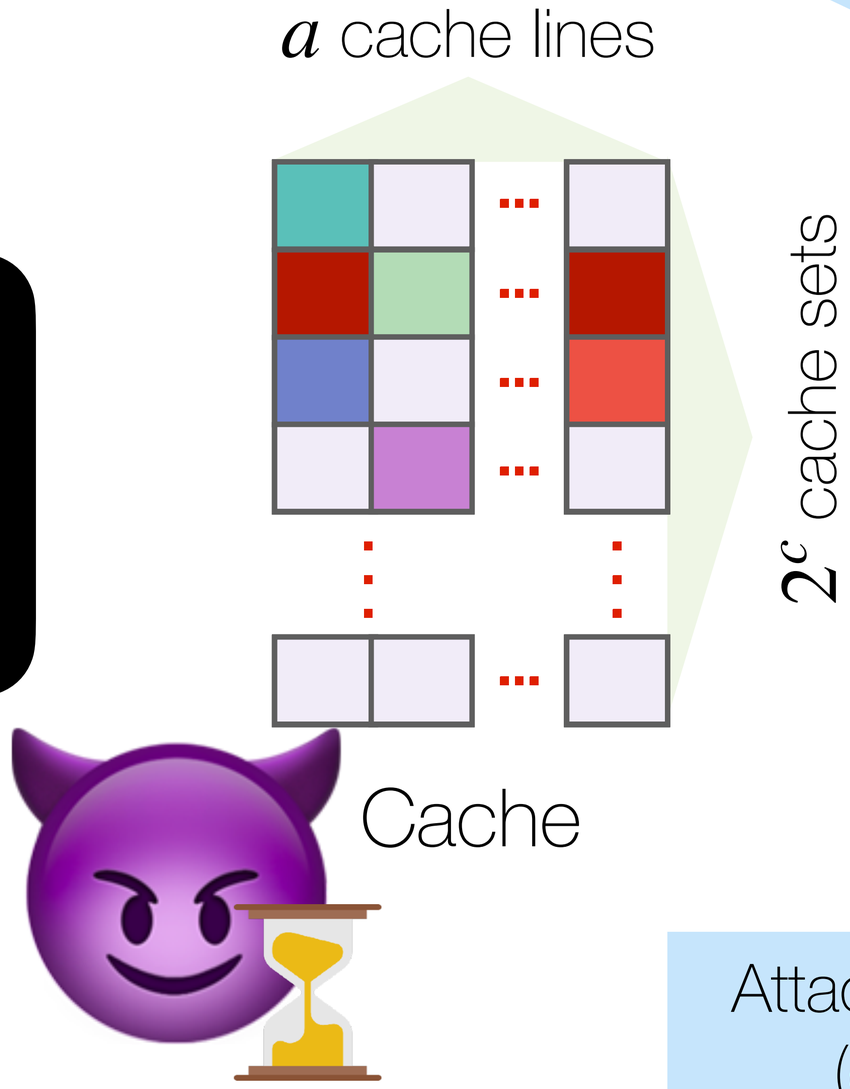

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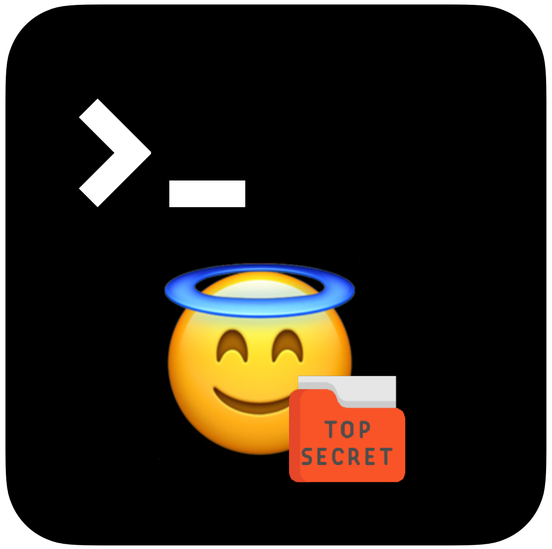
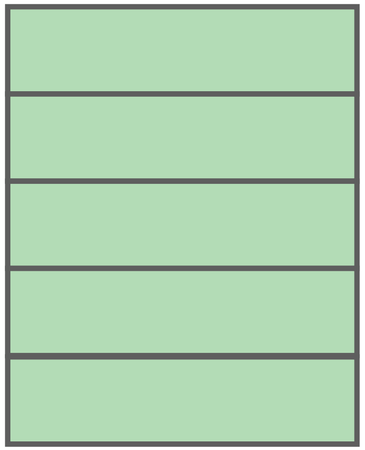
Attacker learns if ***cache miss*** happened (***cache set*** has been ***accessed***)

D. Osvik, A. Shamir, E. Tromer — Cache attacks and countermeasures: the case of AES— 2005

Inferring memory accesses from cache state





Cache

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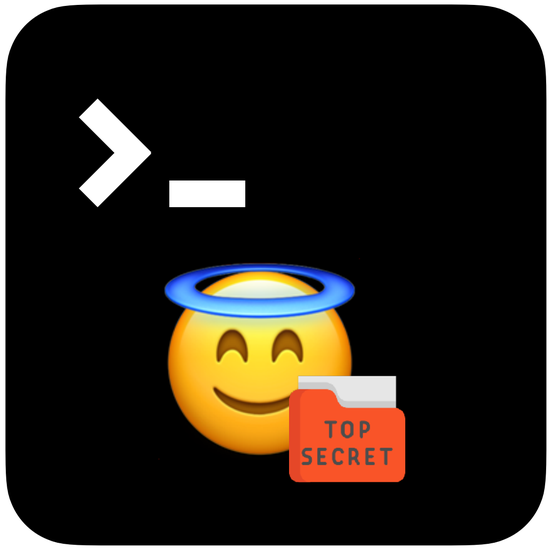

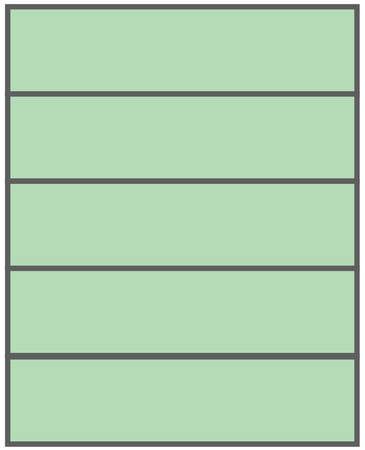

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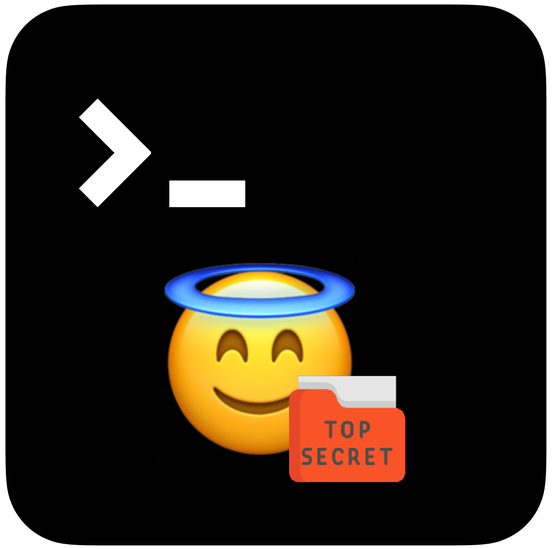

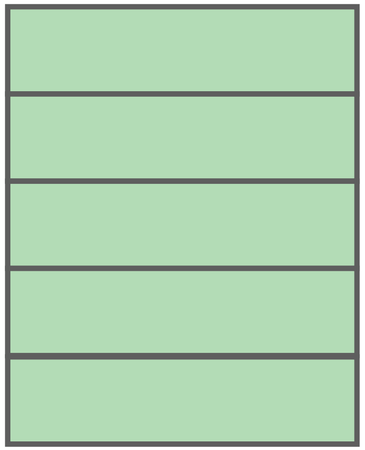

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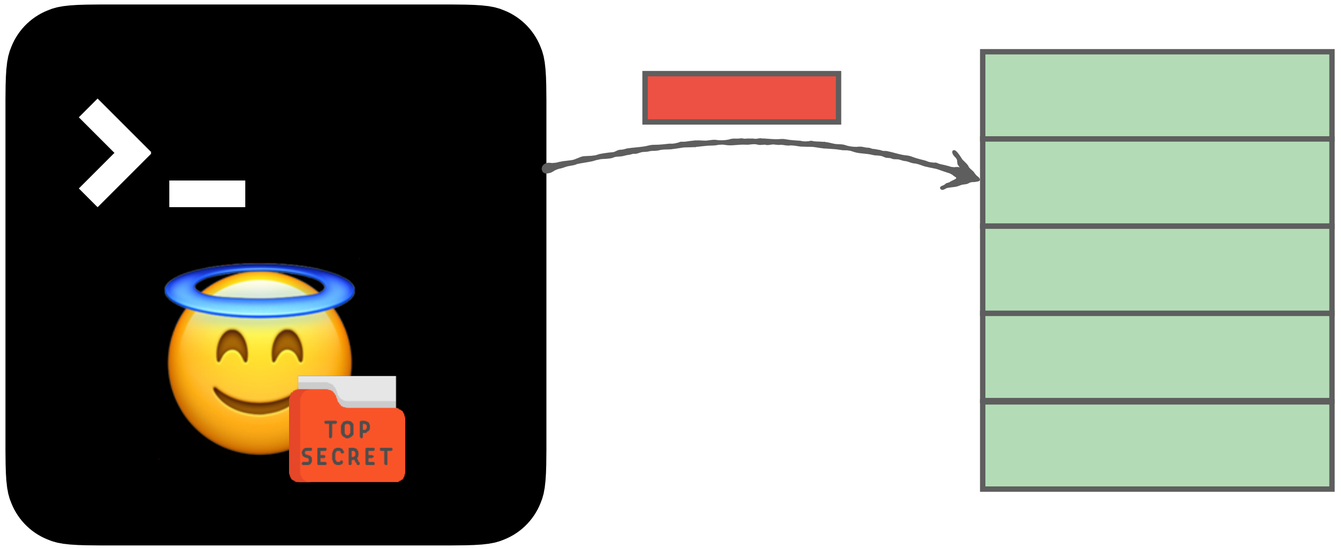

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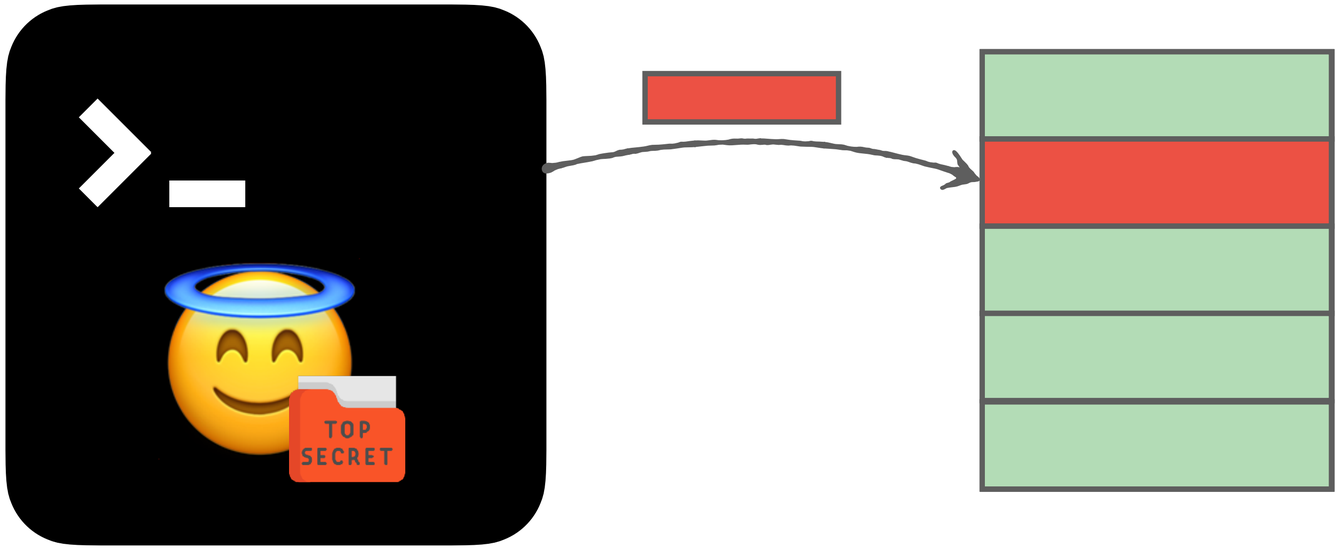

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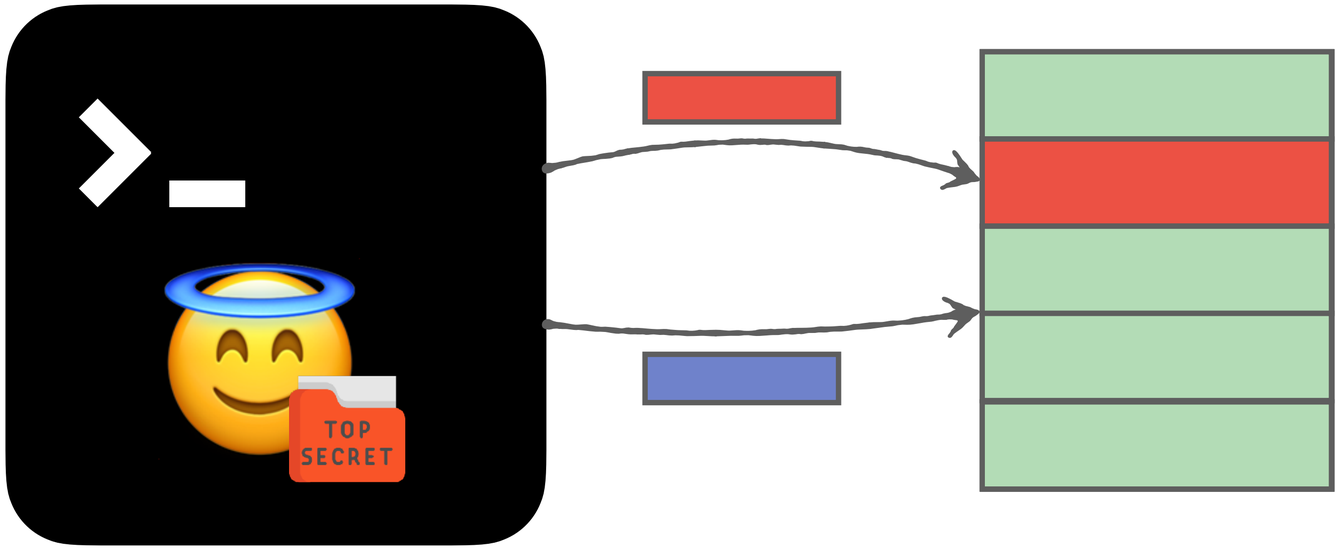

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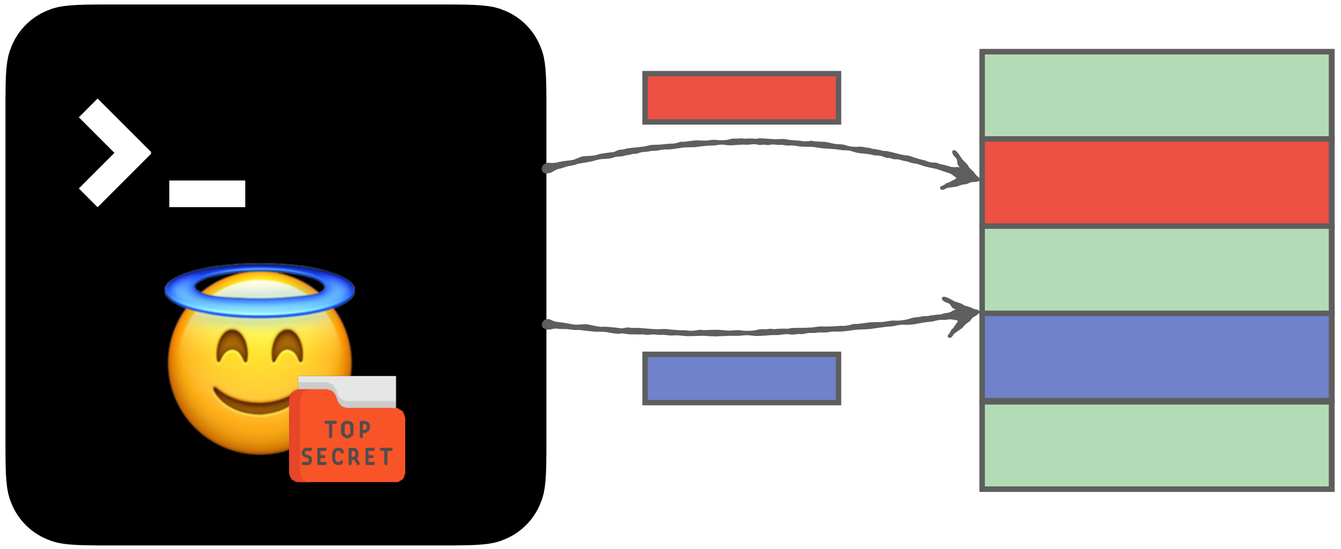

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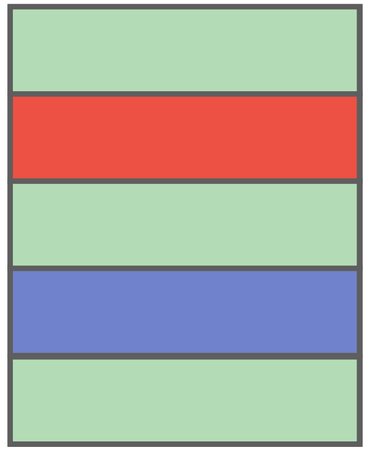

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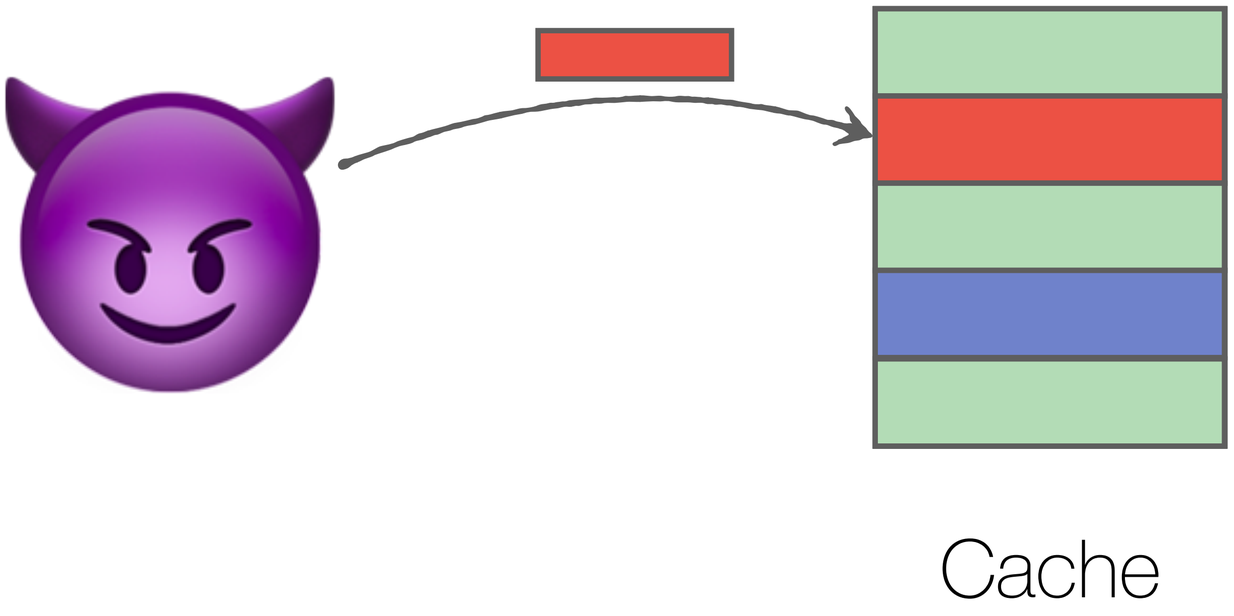

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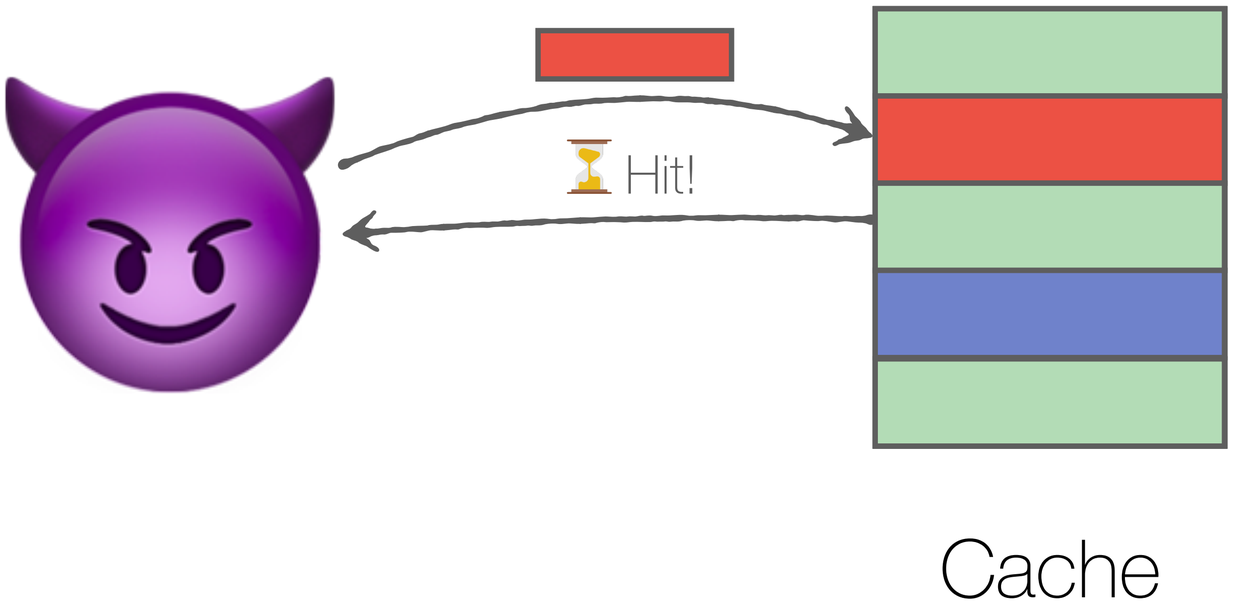

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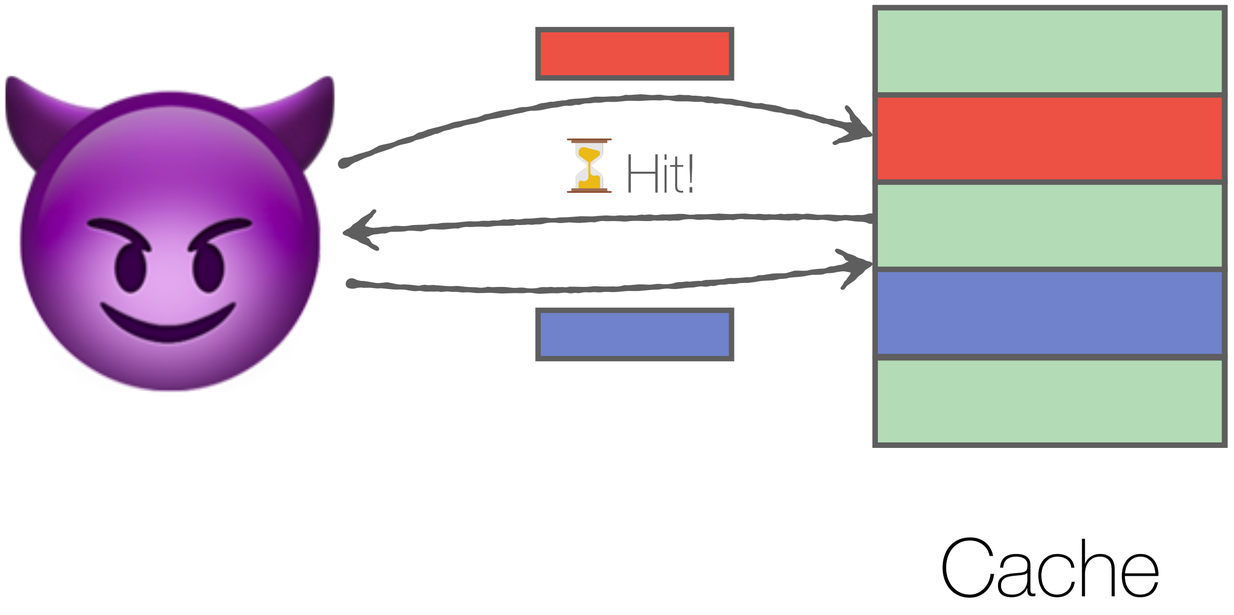

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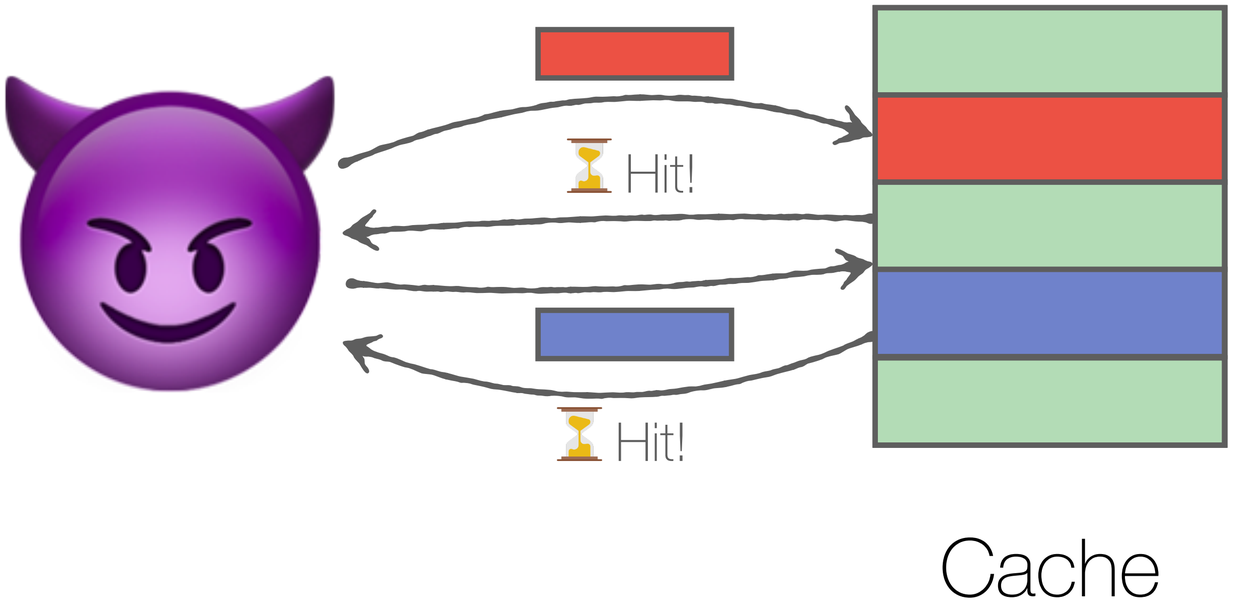

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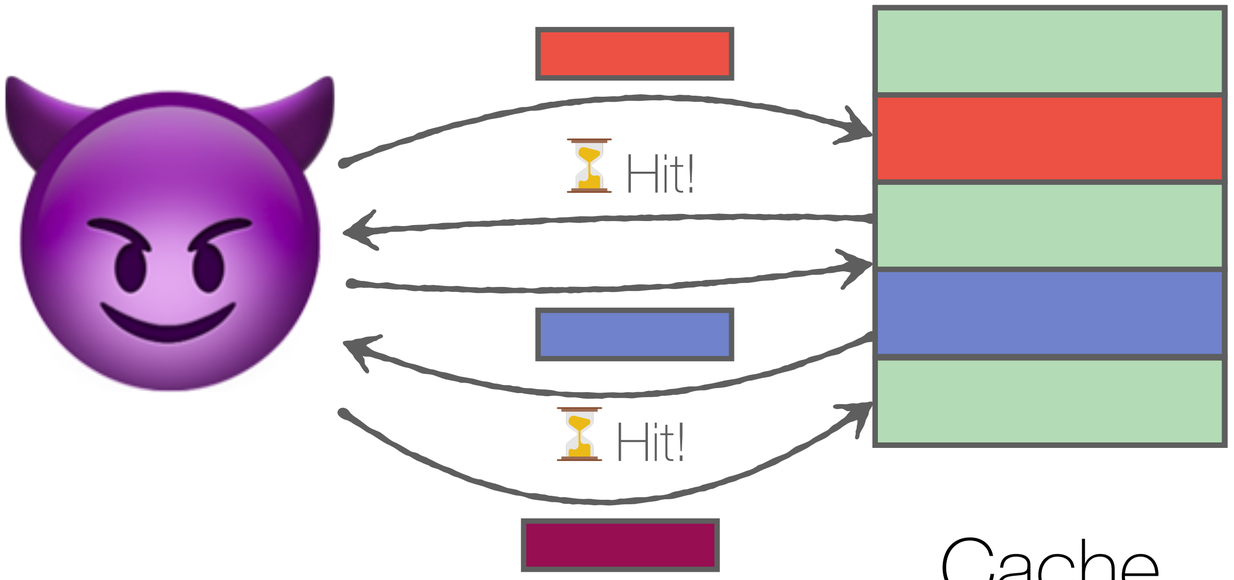

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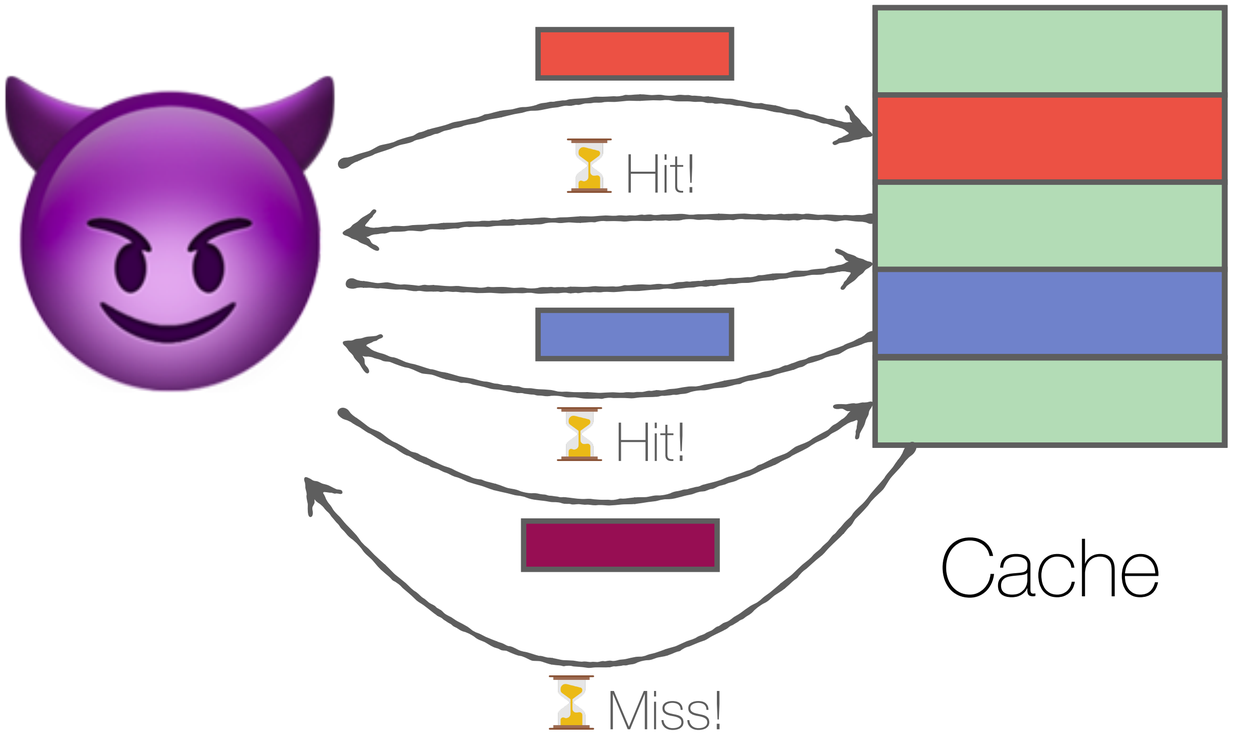

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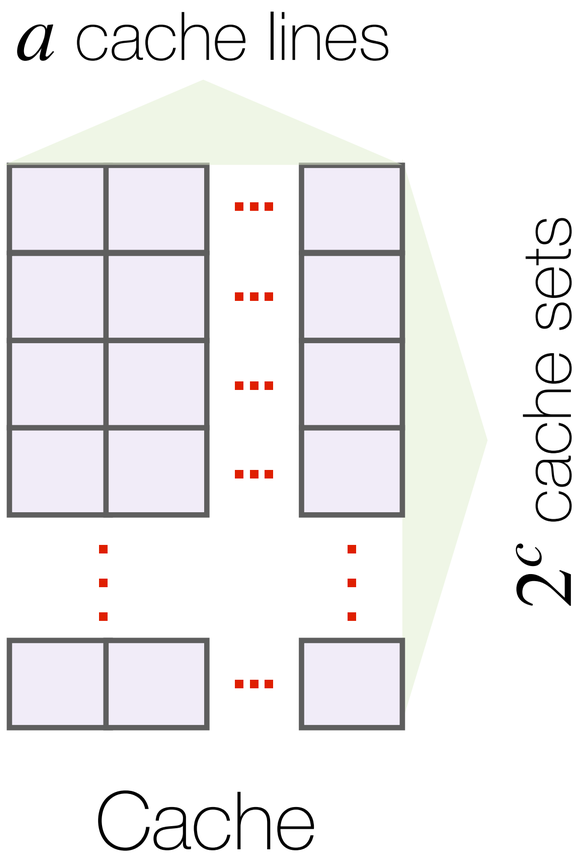

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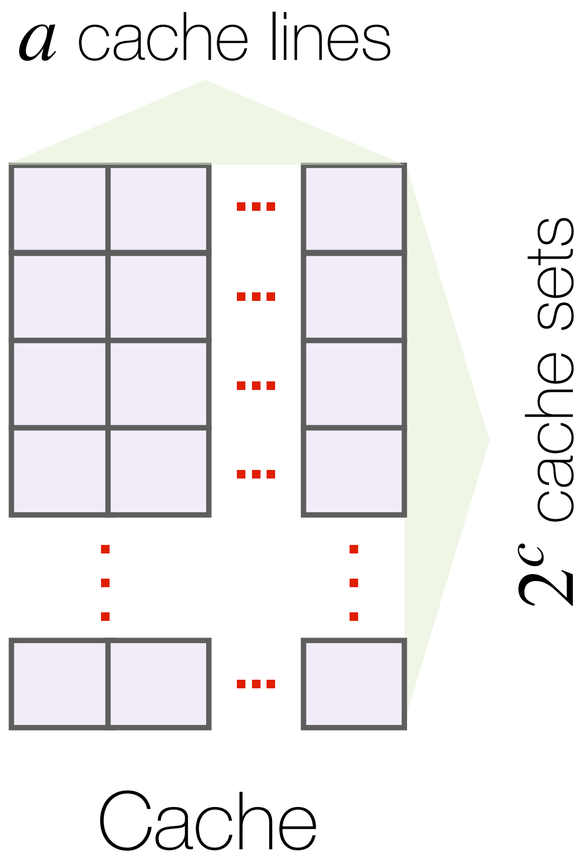

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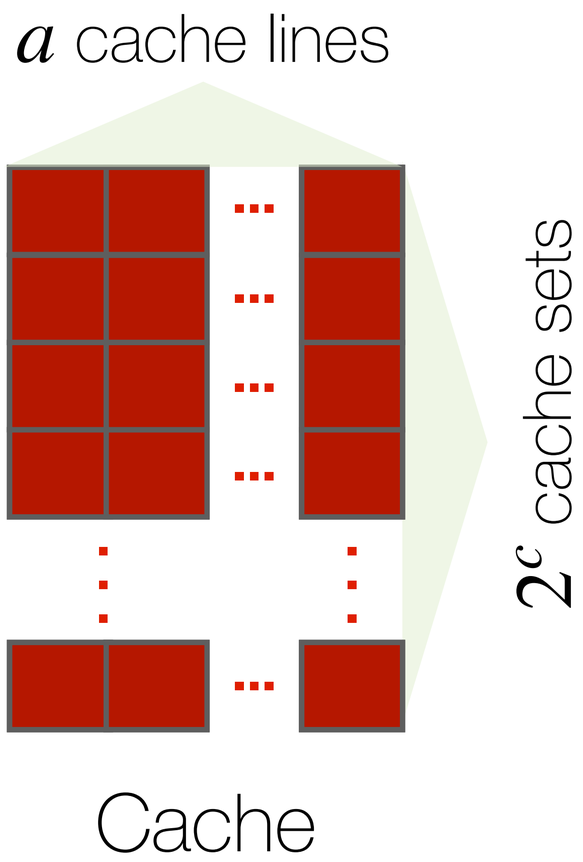

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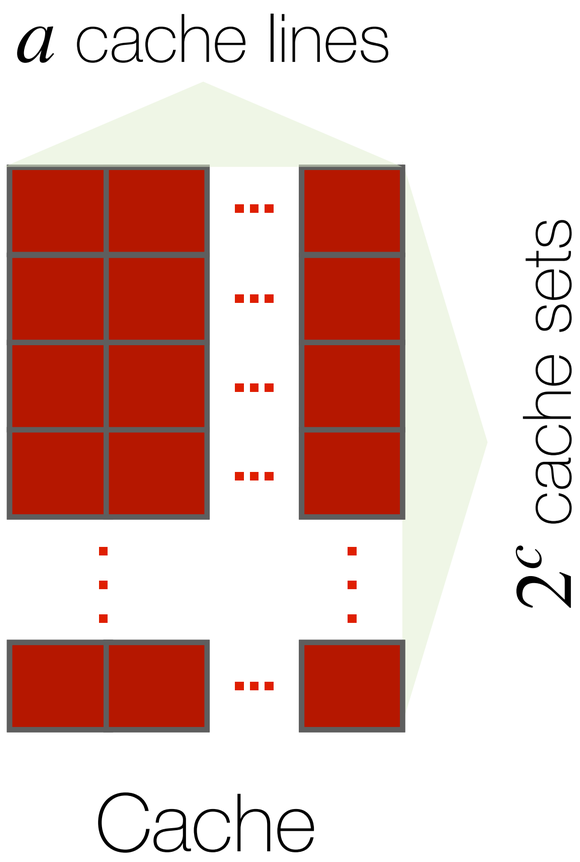

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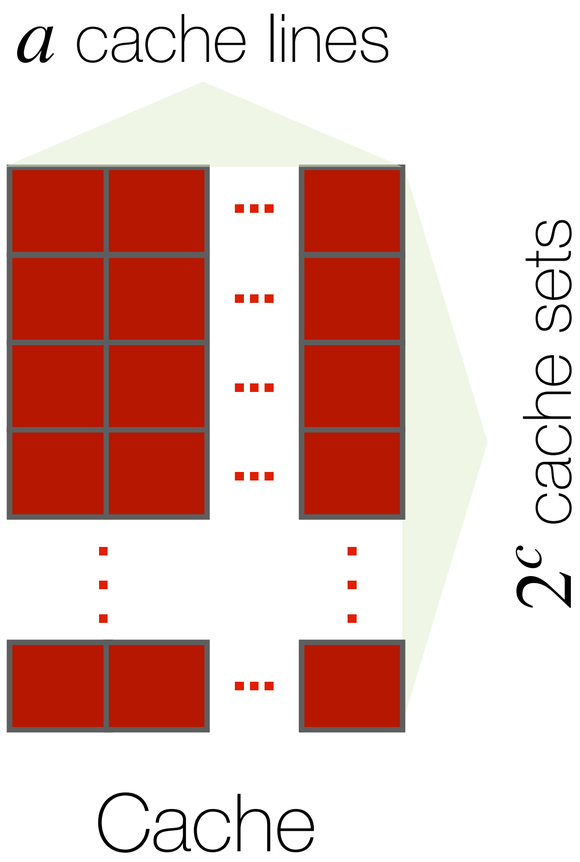

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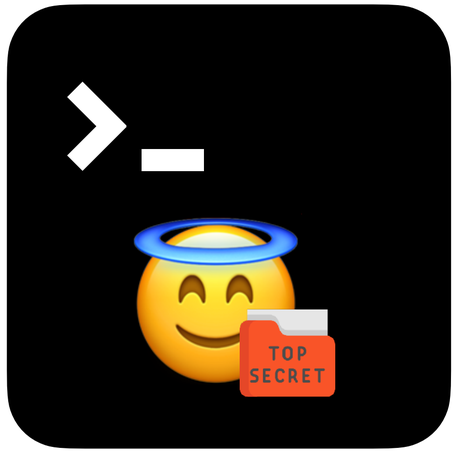

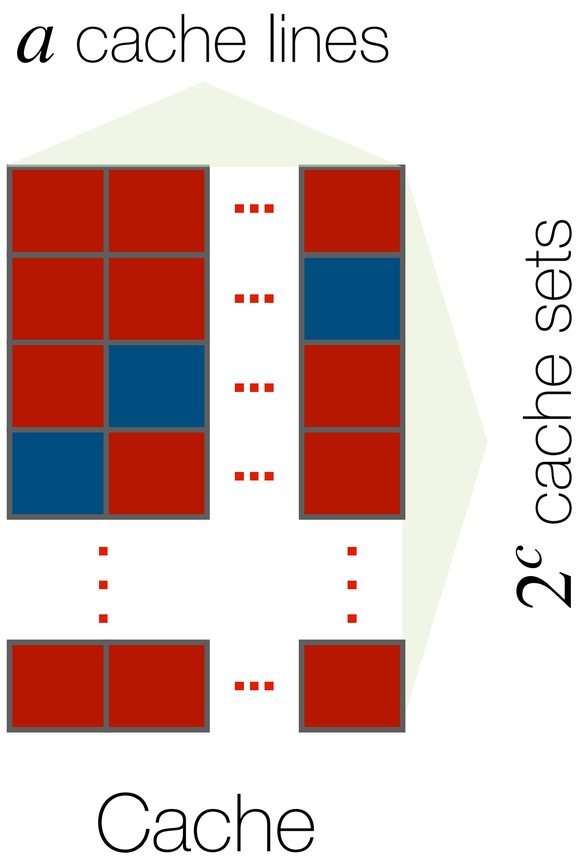

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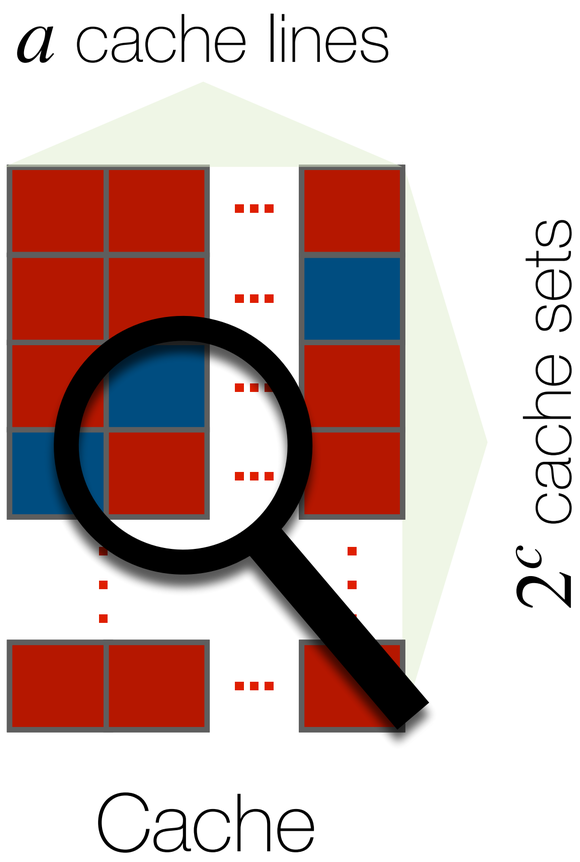

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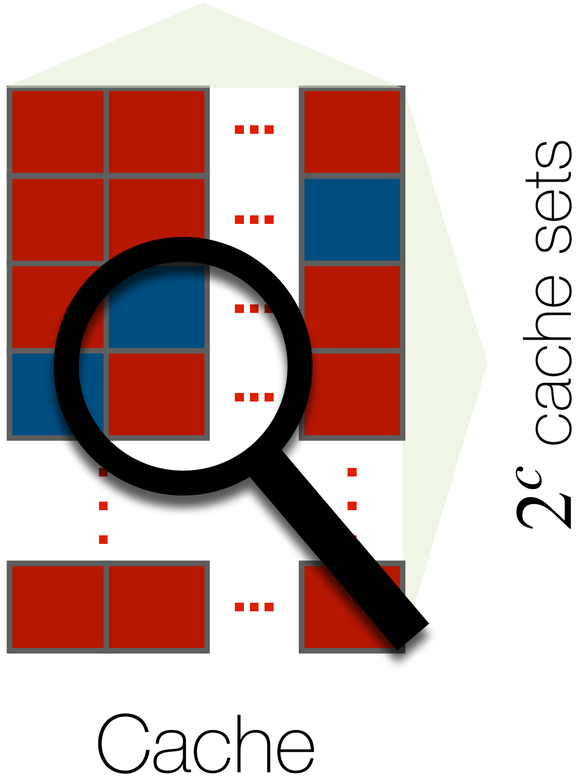

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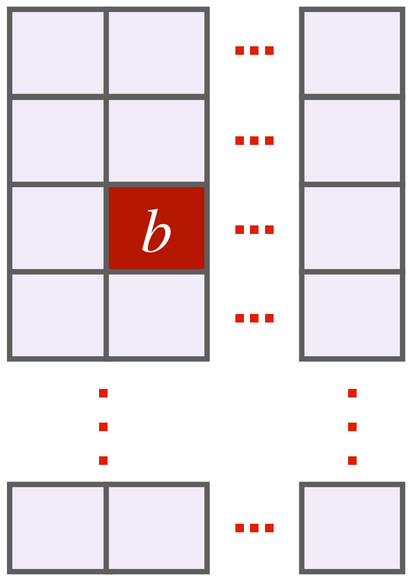

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Attacker and ***victim*** share some memory block b

Y. Yarom, K. Falkner — Flush+Reload: a high resolution, low noise L3 cache side-channel attack — Usenix Security 2014

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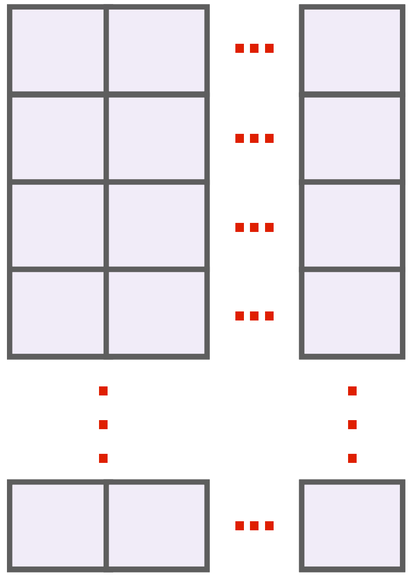

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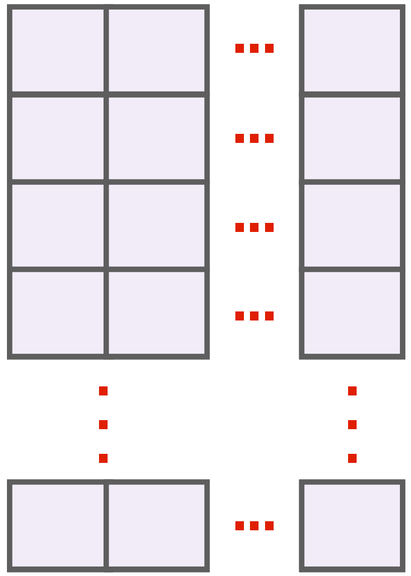

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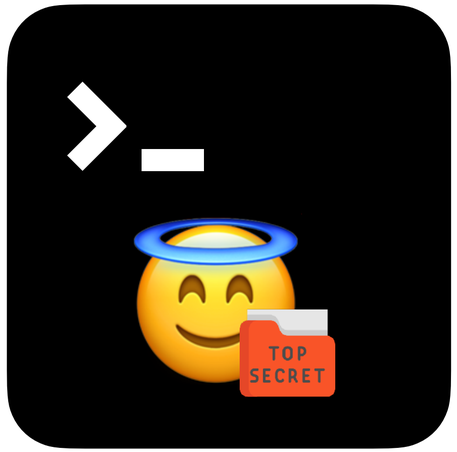

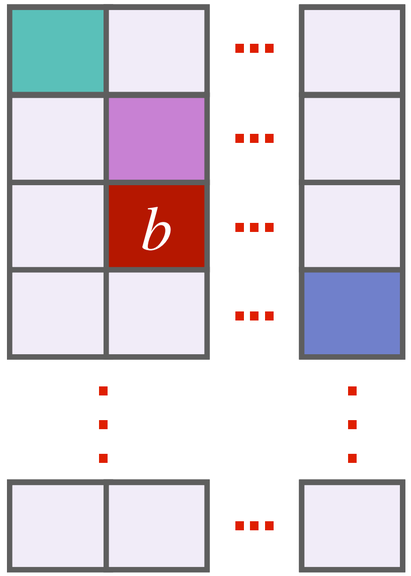

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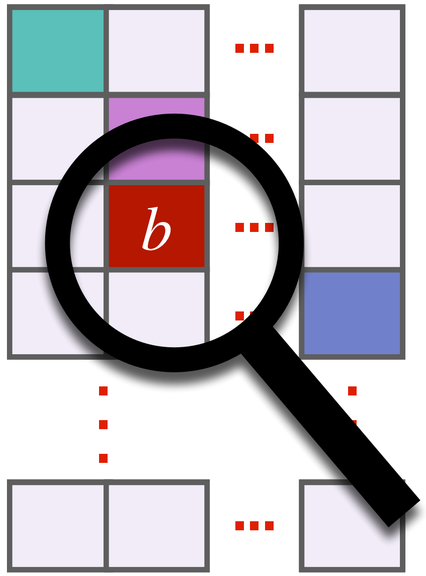

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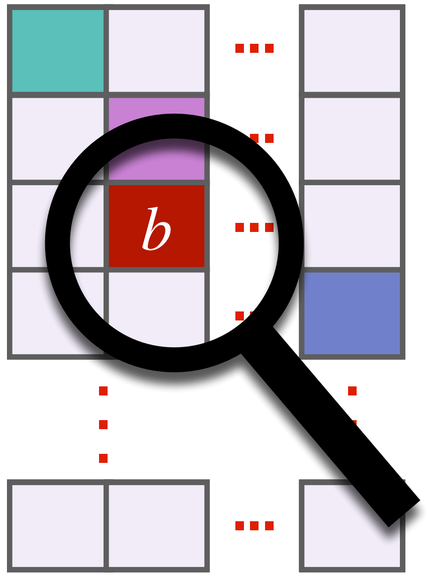

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What can we do with such attacks?

- Prime + Probe and Evict+Time used to recover AES keys
- Flush + Reload used to recover keys from RSA implementation of GnuPG
- They can be run even from Javascript
- Stream videos across Amazon EC2 instances (see https://youtu.be/yPZmiRi_c-o)

Countermeasures

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- Make ***timing measurements*** difficult
  - Not too effective

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- Make ***timing measurements*** difficult
  - Not too effective
- ***Constant-time programming***
  - Make memory accesses and control-flow independent of secrets!

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- ***Constant-time programming***
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Hardware countermeasures

Countermeasures

Software countermeasures

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- ***Isolation*** between different processes/security domains
  - Cache coloring/slicing, …

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Hardware countermeasures

- ***Isolation*** between different processes/security domains
  - Cache coloring/slicing, …
- Secure ***randomized caches***
  - Makes targeting ***specific cache sets*** more challenging

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Cache-based attacks can be used as ***building blocks*** in other attacks