

Advanced Computer Architecture

(60001)

Chapter 1

Pipelines

For the sake of example, we're using MIPS, which is a reduced instruction set design (every instruction is 32-bits wide, making it easy to decode);

- **register-register** two source registers and a destination register



For example, ADD R8, R6, R4 sets the value of R8 to be the sum of R6 and R4.

- **register-immediate** one source and one destination register, immediate operand (e.g. adding)



Examples of this include;

- LW R2, 100(R3) R2 <- Memory[R3+100]
 source register is to be added to an immediate constant, could be useful for accessing fields of a struct (field offset is the constant) by using the base of the object
- SW R5, 100(R6) Memory[R6+100] <- R5
 same as above, but for storing
- ADDI R4, R5, 50 R4 <- R5 + signExtend(50)
 note the sign extend; since we have a 16-bit immediate value, if it's a negative number, it needs to be padded to 32-bit

- **branch**



Two registers, for example if the contents are equal, then branch. One challenge is that the address would have to fit in the immediate field, therefore it's not an **absolute** address, but one that's **relative** to the current program counter. Note that it's multiplied by 4, as it's a fixed size. For example, BEQ R5, R7, 25; if R5 = R7, then update PC <- PC + 4 + 25*4, otherwise PC <- PC + 4 (we update it regardless).

- **jump / call**



Unconditional branch, allowing for a jump to anywhere in the full address space of the machine.

The top bits are occupied by the opcode. Register specifier fields also occupy fixed positions in the instruction allowing immediate access to the registers before the instruction finishes decoding. In MIPS, we can have up to 32 registers in the machine as the width of the register specifier fields is 5 ($2^5 = 32$). The largest signed immediate operand is determined by the width of the immediate field, similarly the range of addresses of a conditional jump is the same (albeit scaled by 4). A general machine would execute this in a loop (the slides contain a diagram of this with the components);

```

1 Instr = Mem[PC]; PC += 4;
2 rs1 = Reg[Instr.rs1];
3 rs2 = Reg[Instr.rs2];
4 imm = signExtend(Instr.imm);
5 Operand1 = if (Instr.op == BRANCH) then PC else rs1
6 Operand2 = if (immediateOperand(Instr.op)) then imm else rs2
7 res = ALU(Instr.op, Operand1, Operand2)
8 switch (Instr.op) {
9     case BRANCH:
10         if (rs1 == 0) then PC = PC + imm*4; continue;
11     case STORE:
12         Mem[res] = rs1; continue
13     case LOAD:
14         Imd = Mem[res]
15 }
16 Reg[Instr.rd] = if (Instr.op == LOAD) then Imd else res

```

The 5 steps of the MIPS datapath are as follows - the pipelined design introduces pipeline buffers between each stage;

1. instruction fetch
2. instruction decode, register fetch
3. execute, address calculation
4. memory access
5. write back

The pipeline buffers allow the result of a stage to be latched in the buffer, to be used in the next clock cycle. This allows each instruction to progressively move down the pipeline on each successive clock tick. Without pipelining, the entire pipeline would operate on one clock cycle, however the number of gates along the path would determine the clock cycle time / rate - a non-pipelined processor would run slowly as there is a long path. In a pipelined design, the cycle time is determined by the slowest of the stages, but the length of each stage is controlled to allow for the highest possible rate.

In addition to this, there is also a decode which controls what is being done (which sources to read from, for example a branch would use PC rather than a register). The control signals configure the multiplexers (MUX), ALU, and read / write to memory. The signal is carried with the corresponding instruction along the pipeline.

Initially the pipeline is empty. With each successive cycle after the first, more of the pipeline will be used, with a new instruction being fetched at each cycle, and the preceding instruction being passed to the next pipeline stage.

Pipeline doesn't make each individual instruction complete quicker; it doesn't help the **latency** of an instruction, but rather the **throughput** of the entire workload. The pipelining doesn't add much cost as we're using the same hardware, other than latches which add some transistor count and energy consumption. Adding more stages to a pipeline could lead to the clock rate being dominated by the time the signal is spent in the latches.

However, there are a number of hazards to pipelining;

- **structural hazards** - particular hardware units may not be able to be used by two different pipeline stages in the same cycle

The *PS3* was based on a highly parallel multi-core processor chip. The processor had a conventional unit to run the Linux OS, but also 16 parallel accelerator units (fast but simple units, no cache, just a block of SRAM for instructions and data). In cycle 4, for the first instruction, it would be accessing memory, however in the same cycle, a later instruction would be trying to fetch the instruction from the **same** memory. A structural hazard occurs on simultaneous access; leading to load instructions causing an instruction fetch to stall. This causes a stall (delays the instruction until the next cycle), which introduces pipeline bubbles - a missed opportunity for an instruction to be processed; once a fetch is missed, subsequent steps can't do anything in next cycles. This was solved with a prefetch buffer, where a block of instructions was fetched at once. Instructions were reorganised at compile time.

- **data hazards** - an instruction depends on the result of an incomplete (still in pipeline) instruction (causes bubbles / stalls, can be overcome with forwarding)

Consider the following example;

```

1  ADD R1,R2,R3
2  SUB R4,R1,R3
3  AND R6,R1,R7
4  OR  R8,R1,R9
5  XOR R10,R1,R11

```

After the instruction is fetched in cycle one (for the **ADD**), R2 and R3 are read in in cycle 2, available in cycle 4, but only written back in cycle 5. For the **SUB** and **AND** instructions, the data would need to be sent back in time in the current idea of the pipeline, which obviously isn't feasible. **XOR** is possible, as the register read is in cycle 6. For **OR**, this is fine **if** the register write happens in the first half of the clock cycle, and the register read happens in the second half.

The previous assumption is that the value had to be written to the register before it could be used; however, at the end of cycle 3 the result of the **ADD** instruction is present in the latch after the execution stage, and could be fed directly into the ALU (same for the next instruction, but rather from the latch after the memory stage). The value needs to be delayed by one clock cycle, before forwarding.

The changes to the hardware to support this are as follows (see lecture slides for diagrams);

- add forwarding / bypass paths (to the MUX, mentioned next)
 - * result of the ALU from previous cycle (latch)
 - * the latch after memory, for forwarding the value to the next instruction but one
 - * final wire takes value from memory
- expand multiplexers before ALU to select where the operands should come from (choose one of the bypass wires if forwarding is needed)
- decode needs to control bigger multiplexers to select values from bypass paths for forwarding; decode will now need to track which registers are going to be updated by incomplete instructions (the decode stage knows where the operands are going to come from, as well as what operands are still in-flight)

Data hazards can still exist even with forwarding, for example with loads, as the memory access comes later in the pipeline;

```

1  LW  R1,0(R2)
2  SUB R4,R1,R6
3  AND R6,R1,R7
4  OR  R8,R1,R9

```

Recall that arithmetic may be involved to access memory, hence the stage has to come later. For the value that is required in cycle 4 (execution of **SUB**), the value is only available at the end of the cycle. There is nothing that can be done here, leading to a bubble (also known as a load-use stall). Stalls will also need to be implemented to support this.

Software scheduling can be performed to avoid load hazards (recall that bubbles are missed opportunities for execution). Consider the following code;

```
1  a = b + c
2  d = e - f
```

Slow code, without the optimisation takes 10 cycles, with 2 stalls;

```
1  LW    Rb,b
2  LW    Rc,c
3  STALL
4  ADD   Ra,Rb,Rc
5  SW    a,Ra
6  LW    Re,e
7  LW    Rf,f
8  STALL
9  SUB   Rd,Re,Rf
10 SW    d,Rd
```

However, the faster code swaps the order of execution by moving **LW Re,e** in place of the first stall and **SW a,Ra** in place of the second stall. This takes 8 cycles and has no stalls;

```
1  LW    Rb,b
2  LW    Rc,c
3  LW    Re,e
4  ADD   Ra,Rb,Rc
5  LW    Rf,f
6  SW    a,Ra
7  SUB   Rd,Re,Rf
8  SW    d,Rd
```

- **control hazards** - we assume that we already know the next instruction to fetch, however this may not be the case as we haven't decoded the previous instruction yet (may be a jump / branch)

Consider the following example, where we may risk stalling for three cycles;

```
1  BEQ R1,R3,36
2  AND R2,R3,R5
3  OR  R6,R1,R7
4  ADD R8,R1,R9
5  XOR R10,R1,R11 # instruction 36
```

After discovering the branch outcome at cycle 3, we may suffer a bad stall. This can be overcome by adding early branch determination. Add an adder to add the current PC to the immediate operand (in decode stage), add check with register file, and if it passes we can use the computed next PC value. All the logic for determining the branch outcome is moved as early as possible in the pipeline. This still introduces a delay for one cycle, as we have to fetch the next instruction regardless (while we're computing whether we should branch or not). If the branch is taken, the memory access and write back stages are blocked.

Simultaneous multi-threading can eliminate hazards. Without stalls, an instruction could be finished each cycle. Two program counters are maintained and the processing alternates between the two

counters. Each thread has its own program counter and own registers, thus eliminating issues with data hazards (can still occur with memory).

A simple pipeline with 5 stages can run at 5 - 9 GHz, limited by the **critical** path (slowest pipeline stage). The main tradeoff is to do more per cycle or to increase the clock rate.