CO112 - Hardware

Prelude

The content discussed here is part of CO112 - Hardware (Computing MEng); taught by Bernhard Kainz, and Bjoern Schuller, in Imperial College London during the academic year 2018/19. The notes are written for my personal use, and have no guarantee of being correct (although I hope it is, for my own sake). This should be used in conjunction with the notes, and lecture slides.

Notes - Lecture 1

This section will be covered in less detail, as we've gone through. However, we will need to change the notation we use in this course from the one used in logic, from using $\wedge$ to $\cdot$, $\vee$ to $+$, and from $\neg$ to $'$.

A	B	$A \cdot B$ (AND)	$A + B$ (OR)	A' (NOT)
0	0	0	0	1
0	1	0	1	1
1	0	0	1	0
1	1	1	1	0

Panopto - Lecture 14

Putting together a manual processor; generally the block diagram takes in a sequence of binary numbers, one sequence for data, and another for instructions. This will result in a binary number. Our design is based on the von Neumann architecture, which divides the processor into arithmetic units and registers, with a shared stream for data, and intstructions. Our model will be based on 8 bits.

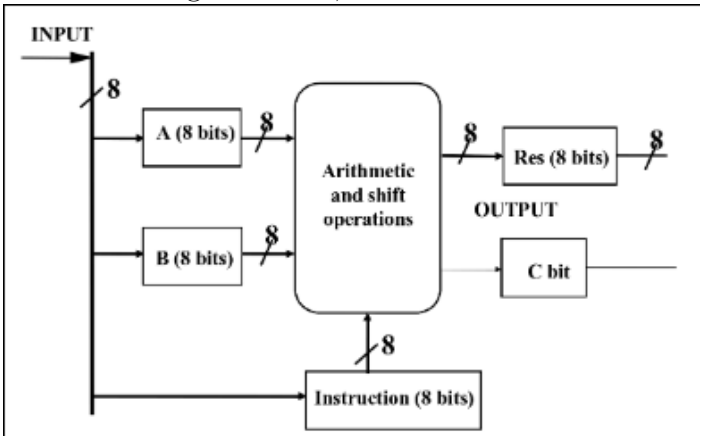
Our example action is to find the average of two numbers, A, and B, such that $R = \frac{A+B}{2}$. Since we are dealing with 8 bits, $A + B < 256$.

1. The first number is set up in input lines, and stored in register (A)
2. The same is done for the second number, and stored in register (B)
3. The arithmetic circuits are set to register (A) to (B).
4. The resulting sum is put into (A)
5. The shift circuits shift (A) one bit to the right, which is integer division by 2
6. Result is loaded into (Res).

In order to do this, we need a number of components;

- Registers
  - store data (A), and (B)
  - store result (Res)
  - one bit for carry (C)
  - store instruction (IR)
- Arithmetic circuits
  - 8-bit adder
  - 8-bit shifter

Note in the figure below, that the 8 means it is an 8-bit line.



Notes - Lecture 14