數位邏輯設計 Ch8 HW

注意事項：請寫出詳細計算與分析過程，不可以只寫答案!

Problems:

8.15 Complete the timing diagram for the gated latch show in Figure 8.103.

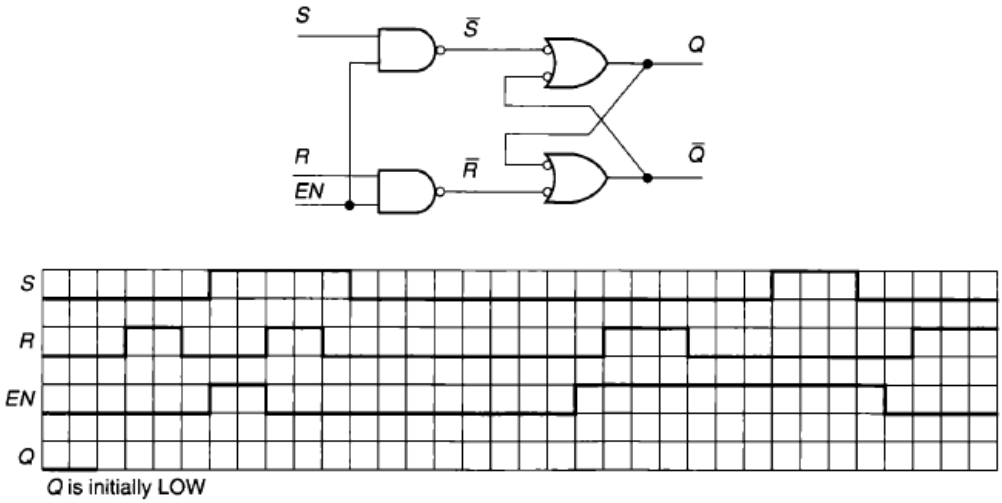

FIGURE 8.103 Problem 8.15: Gated Latch

8.35 Assume that all flip-flops in Figure 8.115 are initially set. Draw a timing diagram showing the *CLK*, Q_0, Q_1, and Q_2 waveforms when eight clock pulses are applied. Make a table showing each combination of Q_2, Q_1, and Q_0. What pattern do the outputs form over the period shown on the timing diagram?

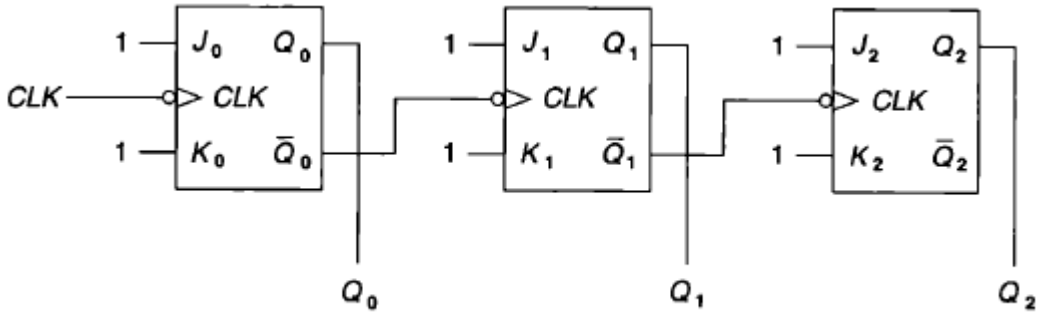

FIGURE 8.115 Problem 8.35: Flip-Flops

8.36 Refer to the JK flip-flop circuit in Figure 8.116. Is the circuit synchronous or asynchronous? Explain your answer.

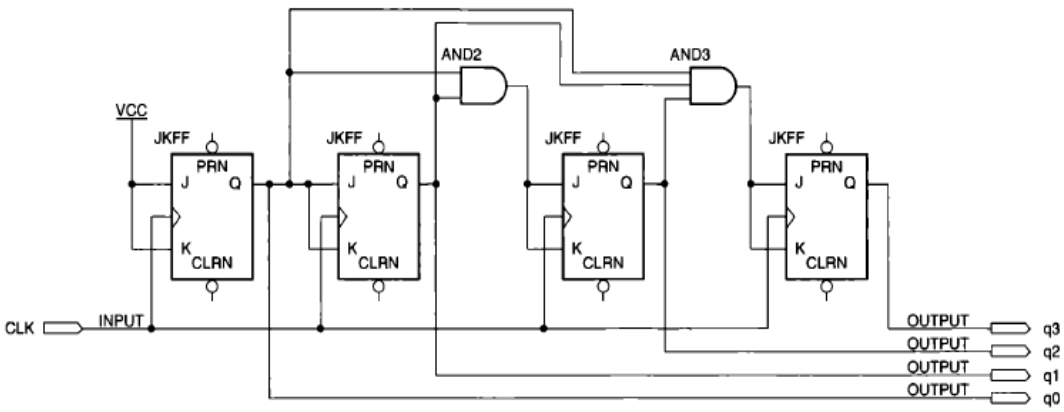

FIGURE 8.116 Problem 8.36: Flip-Flop Circuit