數位邏輯設計 Ch5 HW

注意事項：請寫出詳細計算與分析過程，不可以只寫答案!

Problems:

5.5 Write a VHDL file that describes the circuit shown in Figure 5.35. assuming that all ports are of type BIT.

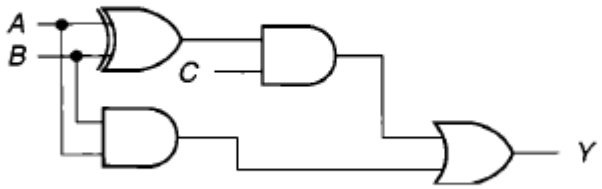

FIGURE 5.35 Problem 5.5: Logic Circuit

5.12 Write a VHDL file that implements the gates in Figure 5.36 using BIT_VECTORs.

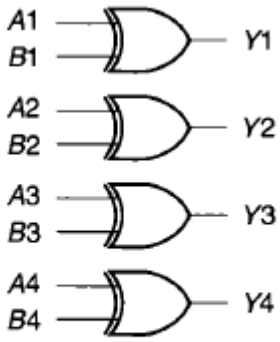

FIGURE 5.36 Problem 5.12: XOR Array

5.17 Use a selected signal assignment statement in VHDL file to encode the following truth table.

D_3	D_2	D_1	D_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

5.18 Write a VHDL file that implements the circuit for the 2-bit equality comparator, shown in Figure 5.37 (The circuit sets $Y = 1$ when $A_2A_1 = B_2B_1$. The circuit is studied in detail in Chapter 6.)

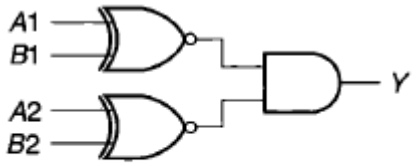

FIGURE 5.37 Problem 5.18: 2-Bit Equality Comparator

5.19 **a.** Write the Boolean expression and truth table for the logic circuit shown in Figure 5.38.

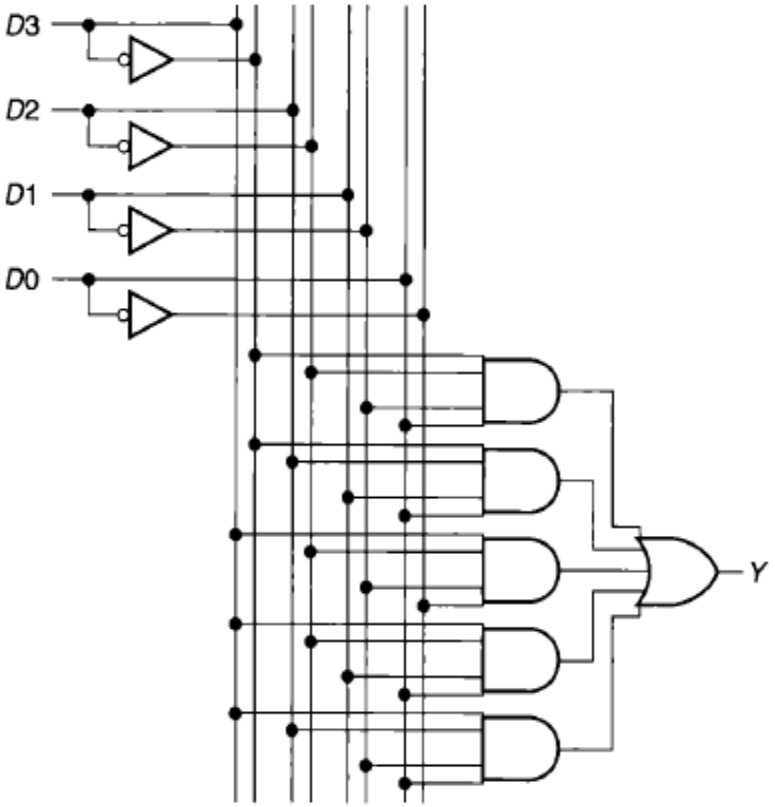

FIGURE 5.38 Problem 5.19: SOP Circuit

b. Which would be simpler to use in a VHDL description of the circuit in Figure 5.38, a concurrent signal assignment statement or a selected signal assignment statement? Why?

c. Write a VHDL file that describes the circuit in Figure 5.38, based on your choice in part b of this question.