Chapter 2

Logic Functions and Gates

2.1 Basic Logic Functions

- The three basic logic functions are:
  - AND (和)
  - OR (或)
  - NOT (非)

- Logic functions can be represented:
  - Algebraically（代數）
  - Using truth tables（真值表）
  - Using electronic circuits（電子電路）

Algebraic (代數)Representation

- Uses Boolean algebra（布林代數）
- Boolean variables have two states (binary).
- Boolean operators（運算子）include AND, OR, and NOT.

■ **KEY TERMS**

Boolean Algebra A system of algebra that operates on Boolean variables. The binary (two-state) nature of Boolean algebra makes it useful for analysis, simplification, and design of combinational logic circuits.

Boolean Expression An algebraic expression made up of Boolean variables and operators, such as AND, OR, or NOT. Also referred to as a **Boolean function** or a **logic function.**

Boolean Variable A variable having only two possible values, such as HIGH/LOW, 1/0, On/Off, or True/False.

Logic Gate An electronic circuit that performs a Boolean algebraic function.

Truth Table Representation

- Defines the output of a function for every possible combination of inputs.

A list of all possible input values to a digital circuit, listed in ascending binary order, and the output response for each input combination.

- A system with n inputs has 2^n possible combinations.

Electronic Circuit Representation

- Uses logic gates to perform Boolean algebraic functions.
- Gates can be represented by schematic symbols.
- Symbols can be either distinctive-shape(特殊形狀)
  or rectangular-outline(方形輪廓).

Distinctive-Shape Symbols Graphic symbols for logic circuits that show the function of each type of gate by a special shape.

Rectangular-Outline Symbols Rectangular logic gate symbols that conform to IEEE/ANSI Standard 91-1984.

NOT Function

- One input and one output.
- The output is the opposite logic level of the input.
- The output is the complement of the input.

NOT Function Boolean Representation

- Inversion is indicated by a bar over the signal to be inverted.

$$Y = \overline{A}$$

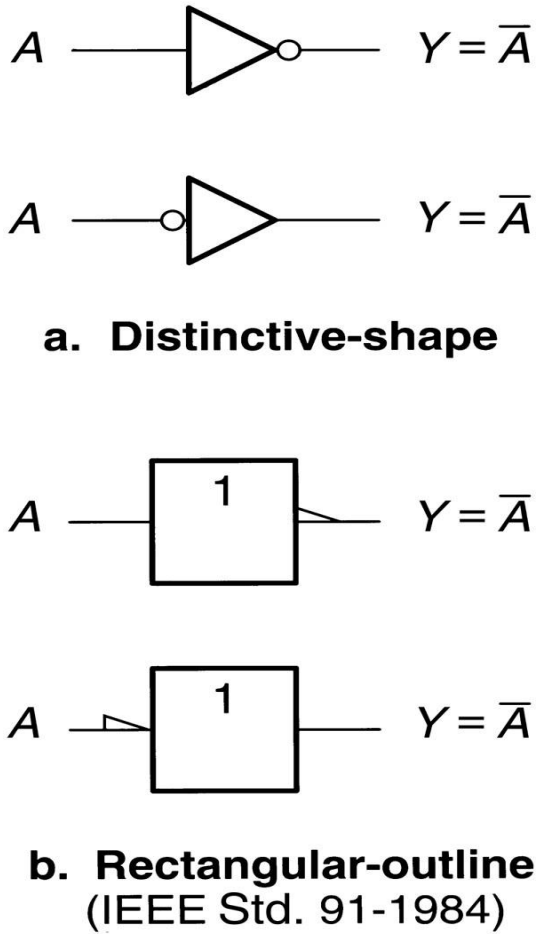
NOT Function Truth Table Representation

TABLE 2.1 NOT Function Truth Table

A	*Y*
0	1
1	0

NOT Function Electronic Circuit

- Called a NOT gate or, more usually, an Inverter.
- Distinctive-shape symbol is a triangle with inversion bubble.
- Rectangular-shape symbol uses "1" in the top center.



AND Function

- Two or more inputs, one output.
- Output is HIGH only when all of the inputs are HIGH.
- Output is LOW whenever any input is LOW.

A	*B*	*Y*
0	0	0
0	1	0
1	0	0
1	1	1

AND Boolean Representation

- AND symbol is "•" or nothing at all.

$$Y = A \bullet B$$

$$Y = AB$$

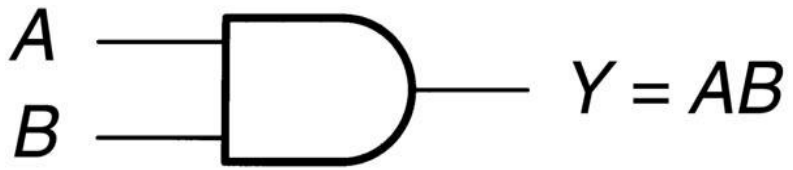
AND Truth Table Representation

TABLE 2.3 3-Input AND Function Truth Table

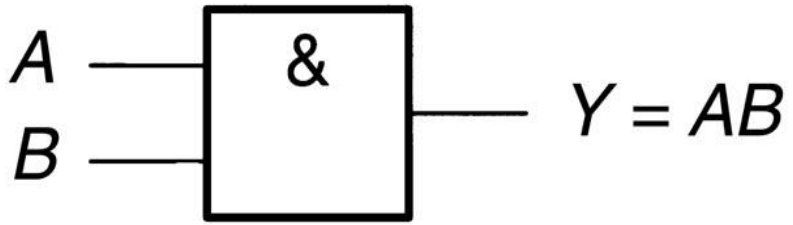
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

AND Function Electronic Circuit

- Called an AND gate.
- Distinctive-shape symbol uses AND designation.
- Rectangular-shape symbol use “&” as designator.



a. Distinctive-shape



b. Rectangular-outline

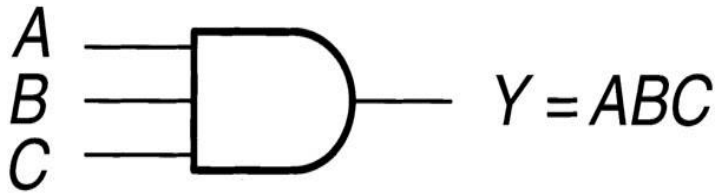
AND Function Electronic Circuit

Example:

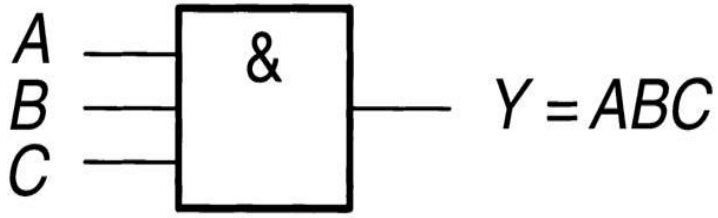
A circuit consists of a voltage source, a lamp, and two series switches. The lamp turns on when switches A and B are both closed. For any other condition of the switches, the lamp is off. Please plot the circuit.

Sol:

AND Function Electronic Circuit



a. Distinctive-shape



b. Rectangular-outline

A	*B*	*C*	*Y*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

OR Function

- Two or more inputs, one output.
- Output is HIGH whenever one or more input is HIGH.
- Output is LOW only when all of the inputs are LOW.

A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

OR Boolean Representation

- OR symbol is “+”.
- Y = A + B (“+”不能省略)

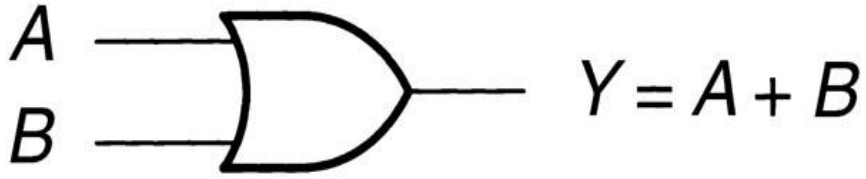
OR Truth Table Representation

TABLE 2.4b Complete Truth Table for a 2-Input OR Gate

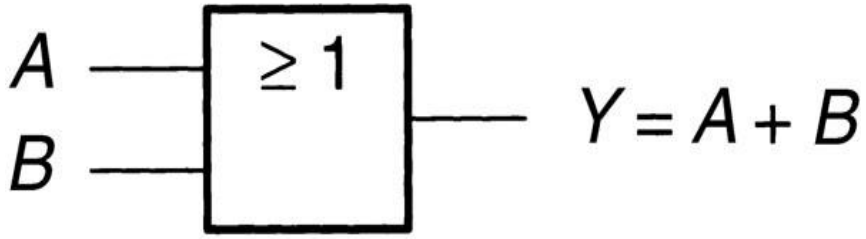
A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

OR Function Electronic Circuit

- Called an OR gate.
- Distinctive-shape symbol uses OR designation.
- Rectangular-shape symbol uses "≥" as designator.



a. Distinctive-shape



b. Rectangular-outline

Example 2.1

State which logic function is most suitable for the following operations. Draw a set of switches to represent each function.

1. A manager and one other employee both need a key to open a safe.
2. A light comes on in a storeroom when either (or both) of two doors is open. (Assume the switch closes when the door opens.)
3. For safety, a punch press requires two-handed operation.

Sol:

Active Level

- The logic level defined as “ON” for a circuit.
- When a logic HIGH is “ON”, the signal is active-HIGH.
- When a logic LOW is “ON”, the signal is active-LOW.

2.2 Derived Logic Functions
NAND Function

- Generated by inverting the output of the AND function.
- Output is HIGH whenever any input is LOW.
- Output is LOW only when all inputs are HIGH.

A	*B*	*Y*
0	0	1
0	1	1
1	0	1
1	1	0

NAND Boolean Representation

- Uses AND with an inversion overbar.

$$Y = \overline{A \bullet B}$$

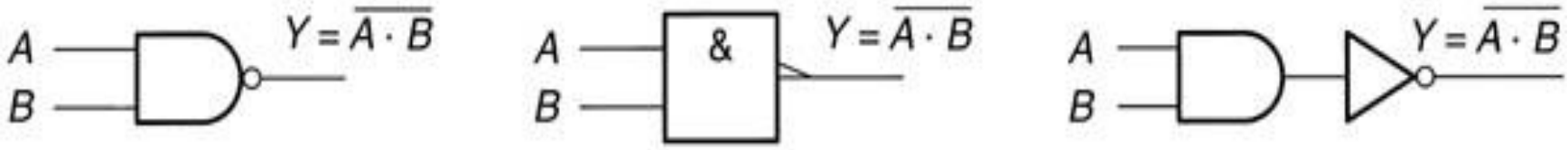
NAND Truth Table Representation

TABLE 2.6b Complete Truth Table for a 2-Input NAND Gate

A	*B*	*Y*
0	0	1
0	1	1
1	0	1
1	1	0

NAND Function Electronic Circuit

- Called a NAND gate.
- Uses the AND symbol with inversion on.



a. Distinctive-shape b. Rectangular-outline c. Equivalent circuit

NOR Function

- Generated by inverting the output of the OR function.
- Output is HIGH only when all inputs are LOW.
- Outputs is LOW whenever any input is HIGH.

A	*B*	*Y*
0	0	1
0	1	0
1	0	0
1	1	0

NOR Boolean Representation

- Uses OR with an inversion overbar.

$$Y = \overline{A + B}$$

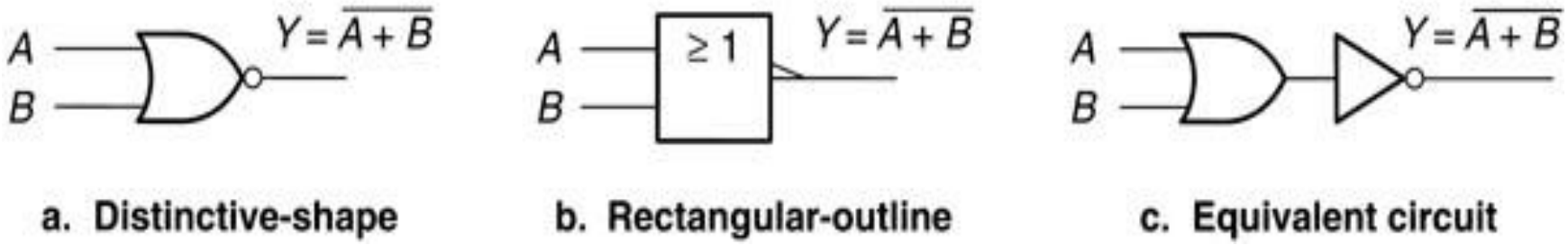
NOR Truth Table Representation

TABLE 2.7b Complete Truth Table of a NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NOR Function Electronic Circuit

- Called a NOR gate.
- Uses OR symbol with inversion on the output.



a. Distinctive-shape b. Rectangular-outline c. Equivalent circuit

3-Input NOR and NAND Function Truth Tables

- 3 Input NAND:

$$Y = \overline{A \bullet B \bullet C}$$

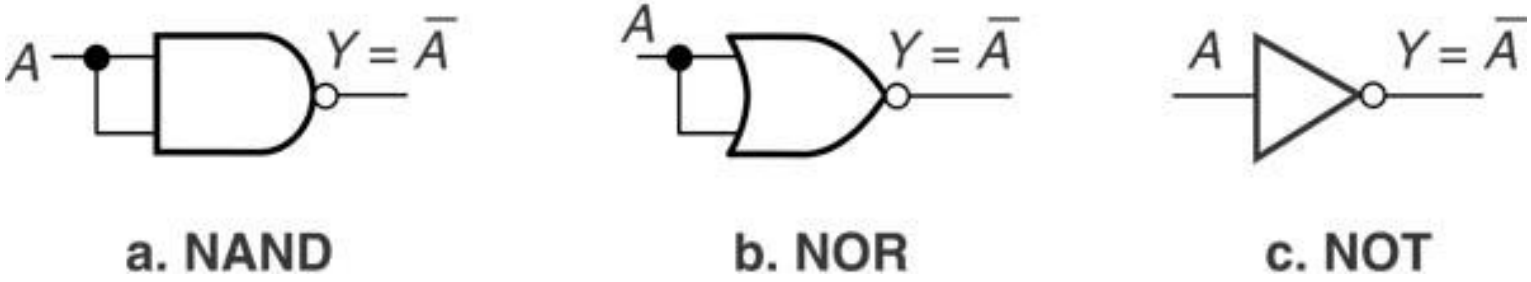
- 3 Input NOR:

$$Y = \overline{A + B + C}$$

A	*B*	*C*	$\overline{A \bullet B \bullet C}$	$\overline{A + B + C}$
0	0	0	1	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	0

NAND and NOR Gates as Inverters

Three equivalent ways of inverting an input:



a. NAND b. NOR c. NOT

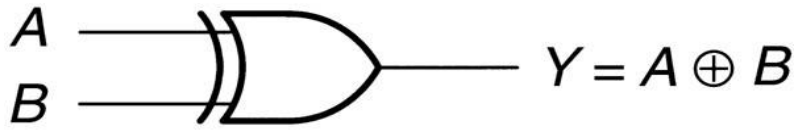
Truth Table:

Exclusive OR (XOR) Gate

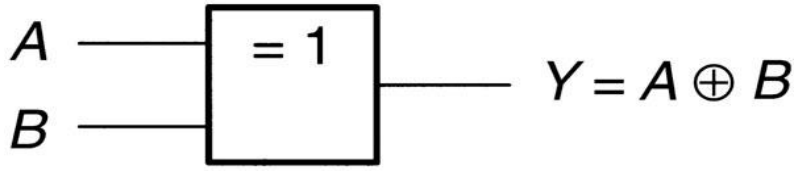
- Two inputs, one output.
- Output is HIGH when one, and only one, input is HIGH.
- Output is LOW when both inputs are equal – both HIGH or both LOW.

A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive OR (XOR) Gate



a. Distinctive-shape



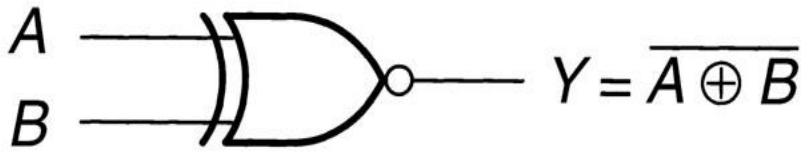
b. Rectangular-outline

Exclusive NOR (XNOR) Gate

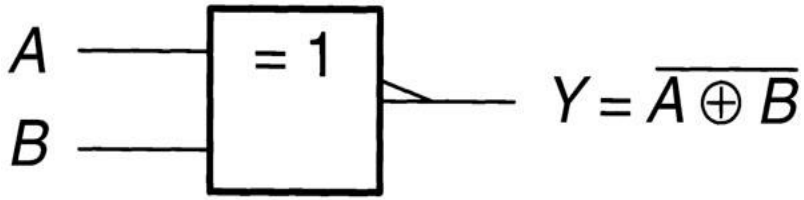
- Two inputs, one output.
- Output is HIGH when both inputs are equal – both HIGH or both LOW.
- Output is LOW when one, and only one, input is HIGH.

A	*B*	*Y*
0	0	1
0	1	0
1	0	0
1	1	1

Exclusive NOR (XNOR) Gate



a. Distinctive-shape

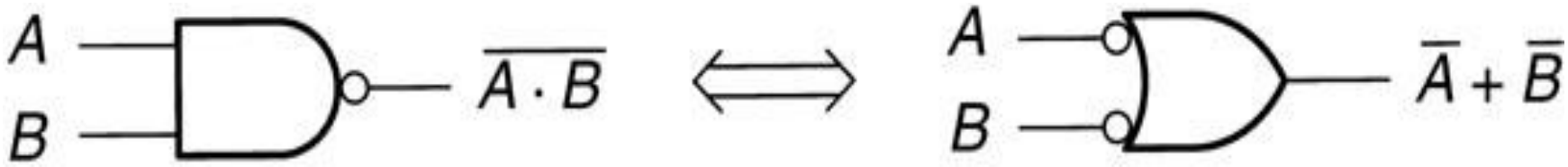


b. Rectangular-outline

2.3 DeMorgan's Theorems and Gate Equivalence

- A NAND gate can be represented by an AND gate with inverted output.

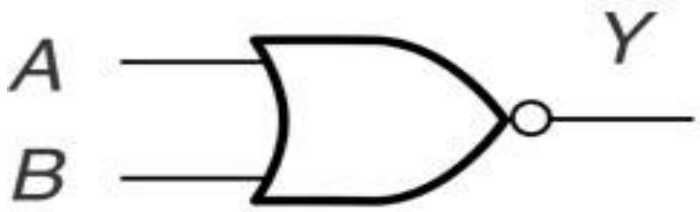
- A NAND gate can be represented by an OR gate with inverted inputs.

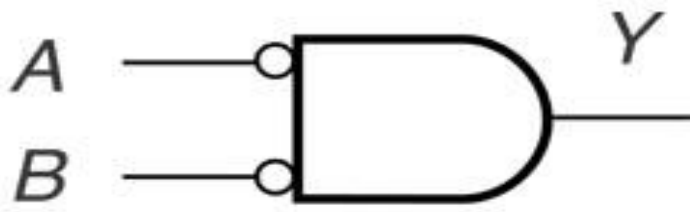


Gate Equivalence – NOR

- A NOR gate can be represented by an OR gate with inverted output.

- A NOR gate can be represented by an AND gate with inverted inputs.





Example 2.2

Analyze the shape, input, and output of the gates shown in Figure 2.22 and write a Boolean expression, a descriptive sentence, and a truth table of each one. Write an asterisk beside the active output level on each truth table. Describe how these gates relate to each other.

a. b.

Sol:

Gate Equivalence – DeMorgan Forms

- Change an AND function to an OR function and an OR function to an AND function.
- Invert the inputs.
- Invert the outputs.

轉換三步驟:

1. AND 變OR, OR變AND.
2. 輸入倒相.
3. 輸出倒相.

DeMorgan's Theorem - 1

- $\overline{A + B} = \overline{A} \bullet \overline{B}$

- $\overline{A \bullet B} = \overline{A} + \overline{B}$

- Break the line and change the sign

DeMorgan's Theorem - 2

- The following are two common errors associated with DeMorgan's Theorem:

- $\overline{A \bullet B} \neq \overline{A} \bullet \overline{B}$

- $\overline{A + B} \neq \overline{A} + \overline{B}$

Example 2.3

EXAMPLE 2.3

Analyze the gate in Figure 2.23 and write a Boolean expression, descriptive sentence, and truth table for the gate. Mark active output levels on the truth table with asterisks. Find the DeMorgan equivalent form of the gate and write its Boolean expression and description.

Sol:

Active Logic Levels

- Any INPUT or OUTPUT that has a BUBBLE is considered as active LOW.

- Any INPUT or OUTPUT that has no BUBBLE is considered as active HIGH.

Active Logic Levels - NOR

- $Y = \overline{A + B}$

TABLE 2.7b Complete Truth Table of a NOR Gate

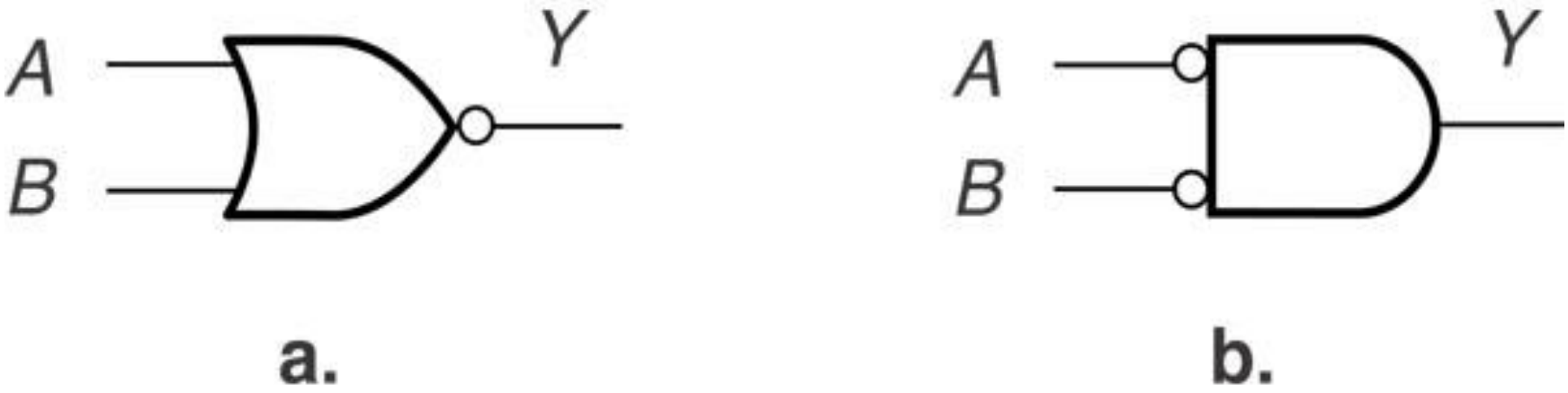
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

At least one input HIGH makes the output LOW.

- $Y = \overline{A} \bullet \overline{B}$

All inputs LOW make the output HIGH.

Active *Logic Levels - NOR*



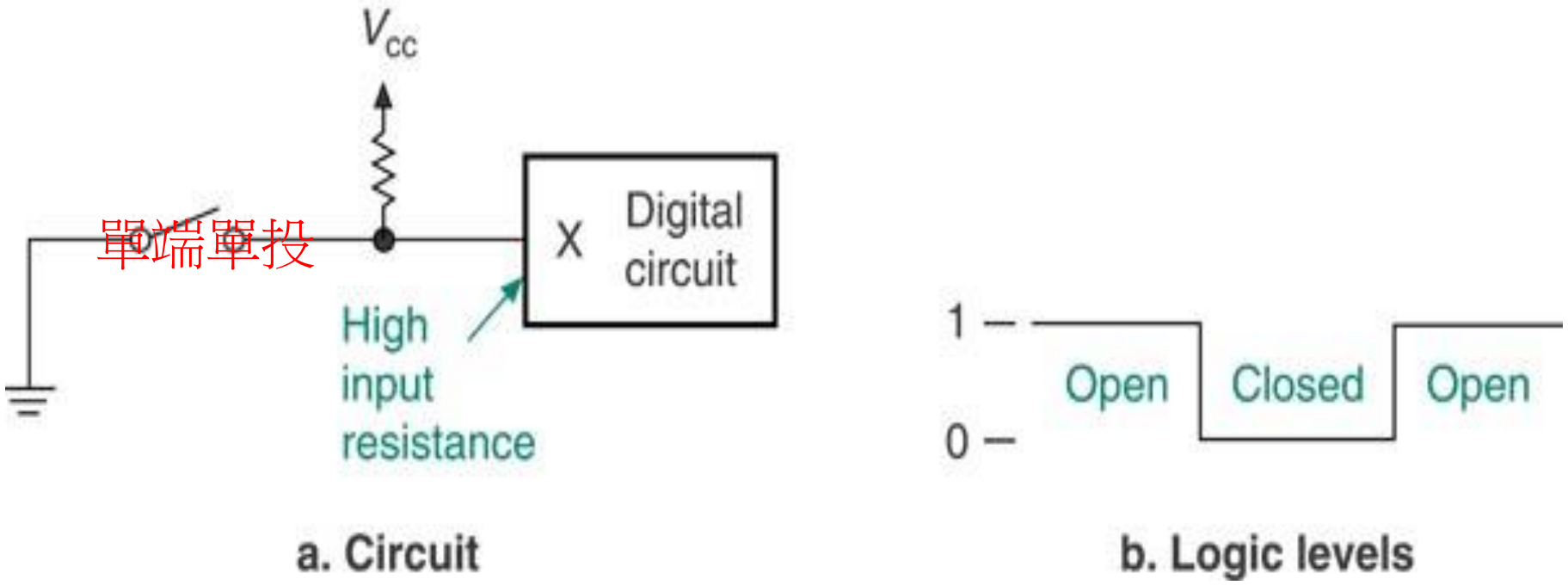
OR 只要有一個
AND全部都是

2.4 Logic Switches and LED Indicators

- Provides a logic HIGH or LOW depending on switch position.

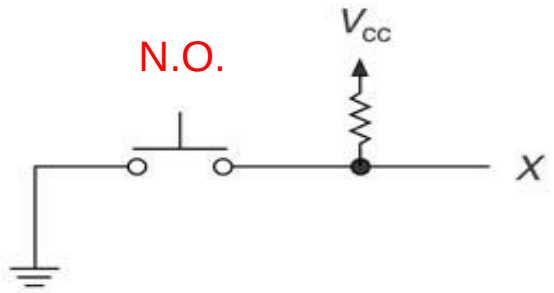
- Commonly used types include:
  1. Normally-open (N.O.) pushbutton
  2. Normally-closed (N.C.) pushbutton
  3. Single-pole single-throw (SPST)(單端單投)

Logic Switches

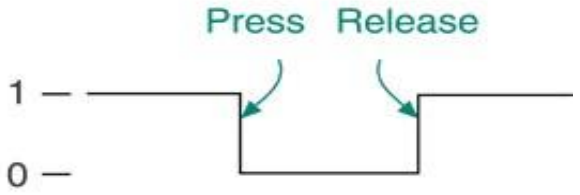


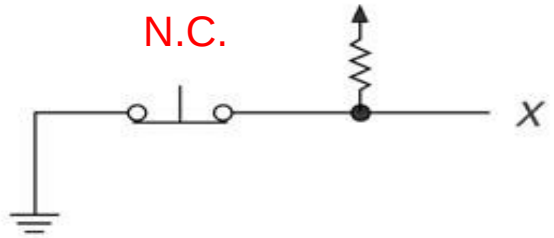
Single-pole single-throw (SPST)

Logic Switches

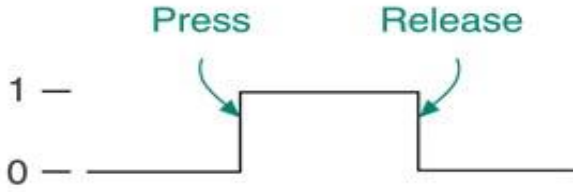


a. Normally open pushbutton



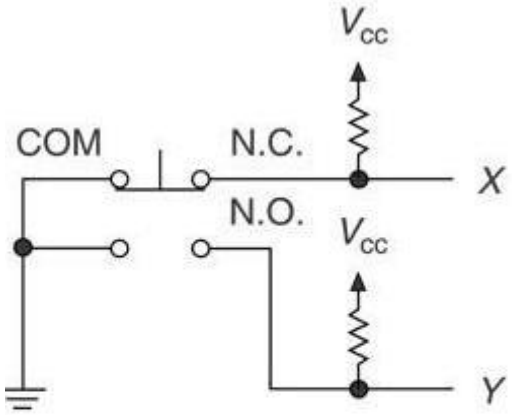


b. Normally closed pushbutton

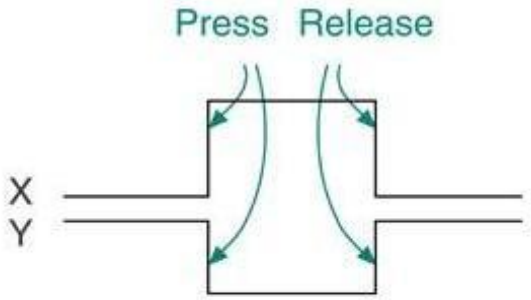


Logic Switches

- Two-pole push button allows for normally HIGH and normally LOW levels from the same switch.



c. Two-pole pushbutton

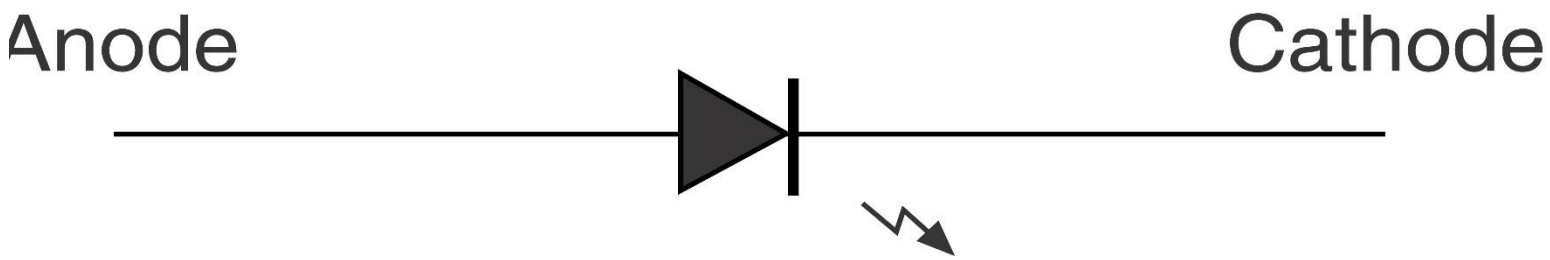


Light Emitting Diodes (LED's)

Light Emitting Diodes (LED's)

- Used to indicate the status of a digital output.
- Has two terminals the anode and the cathode.
- If the anode is approximately 1.5 V greater than the cathode, current flows and the LED illuminates.

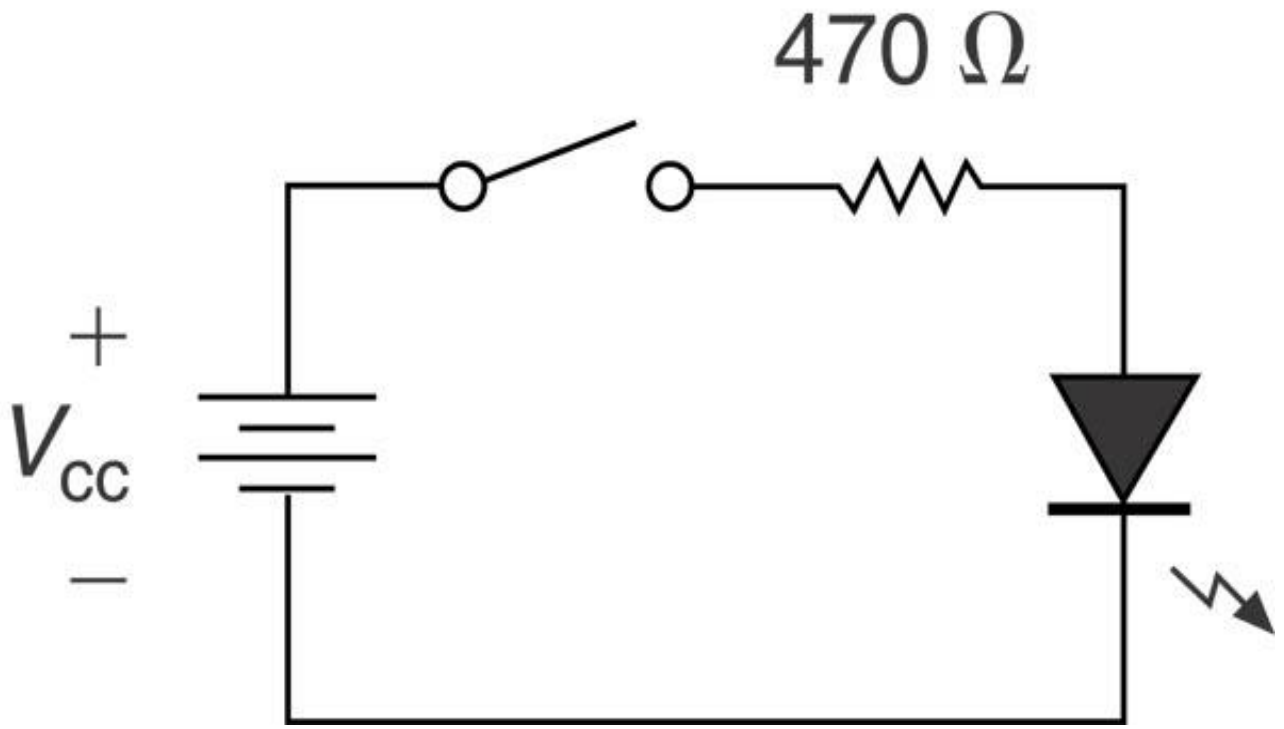
Light Emitting Diodes (LED's)



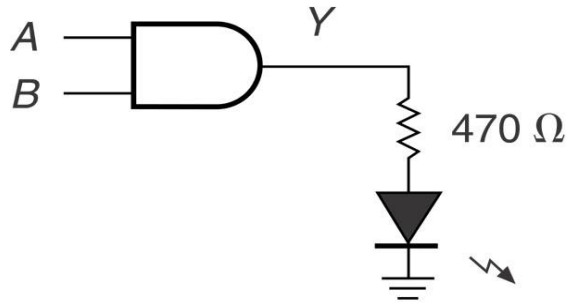
- Used to provide a visual indication of a logic state.

- Can be wired to display active-HIGH or active-LOW.

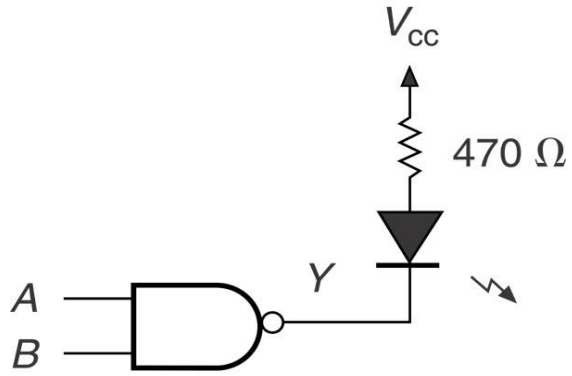
Condition for Light Emitting Diode (LED) illumination



Light Emitting Diodes



a. LED on when *Y* is HIGH



b. LED on when *Y* is LOW

2.5 Enable and Inhibit (禁止)Properties of Logic Gates

ENABLE:

- The input to a gate that allows the output to respond to other inputs.
- A logic LOW for an OR or NOR gate, a logic HIGH for an AND or NAND gate.

TABLE 2.4b Complete Truth Table for a 2-Input OR Gate

A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

TABLE 2.7b Complete Truth Table of a NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

TABLE 2.2b Complete Truth Table for a 2-Input AND Gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

TABLE 2.6b Complete Truth Table for a 2-Input NAND Gate

A	*B*	*Y*
0	0	1
0	1	1
1	0	1
1	1	0

Logic Gate Inhibit (Disable)

- The input to a gate that forces the output to ignore(忽略) any other input.
- A logic HIGH for an OR or NOR gate, a logic LOW for an AND or NAND gate.

TABLE 2.4b Complete Truth Table for a 2-Input OR Gate

A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

TABLE 2.7b Complete Truth Table of a NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

TABLE 2.2b Complete Truth Table for a 2-Input AND Gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

TABLE 2.6b Complete Truth Table for a 2-Input NAND Gate

A	*B*	*Y*
0	0	1
0	1	1
1	0	1
1	1	0

Logic Gate

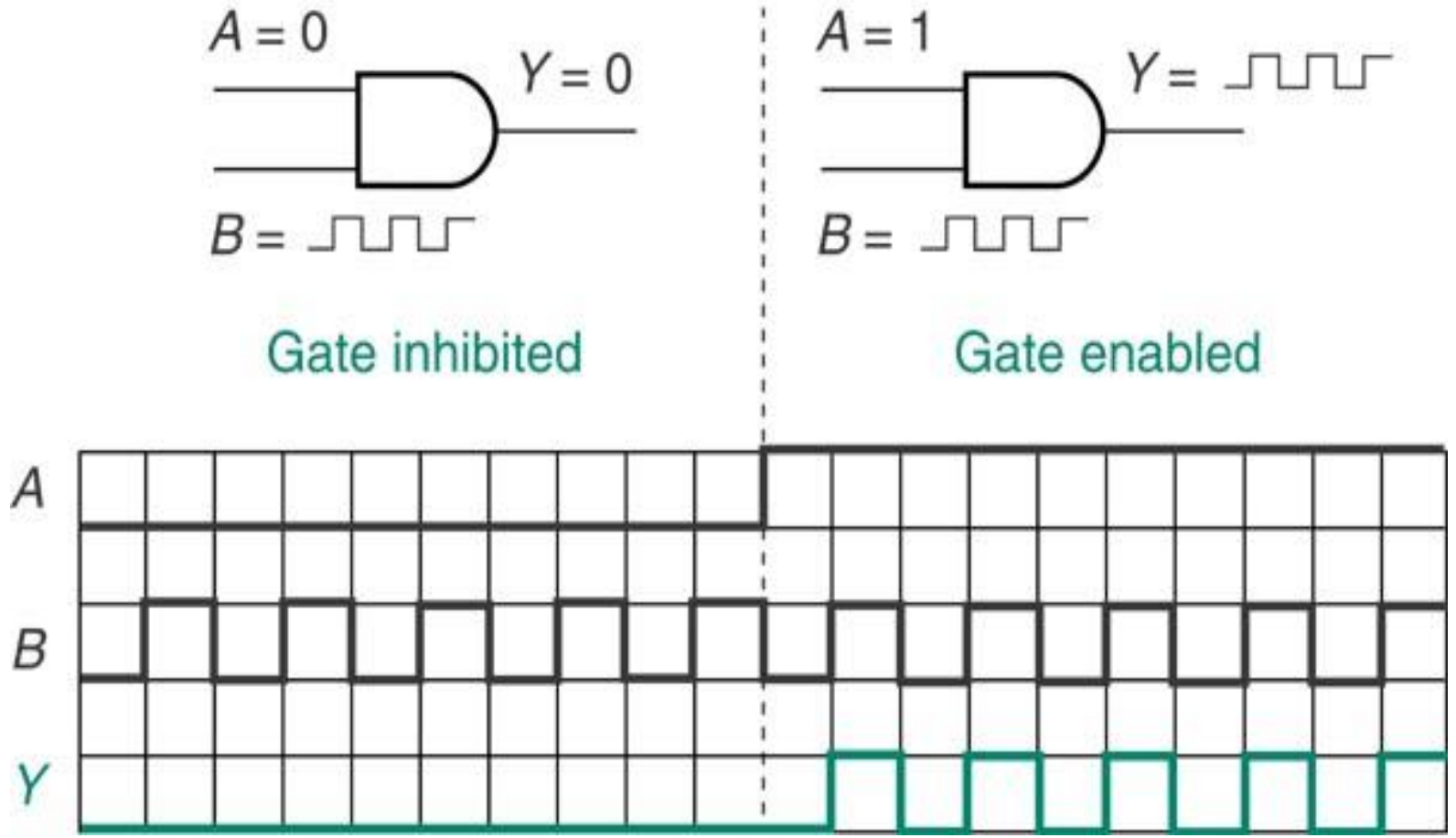
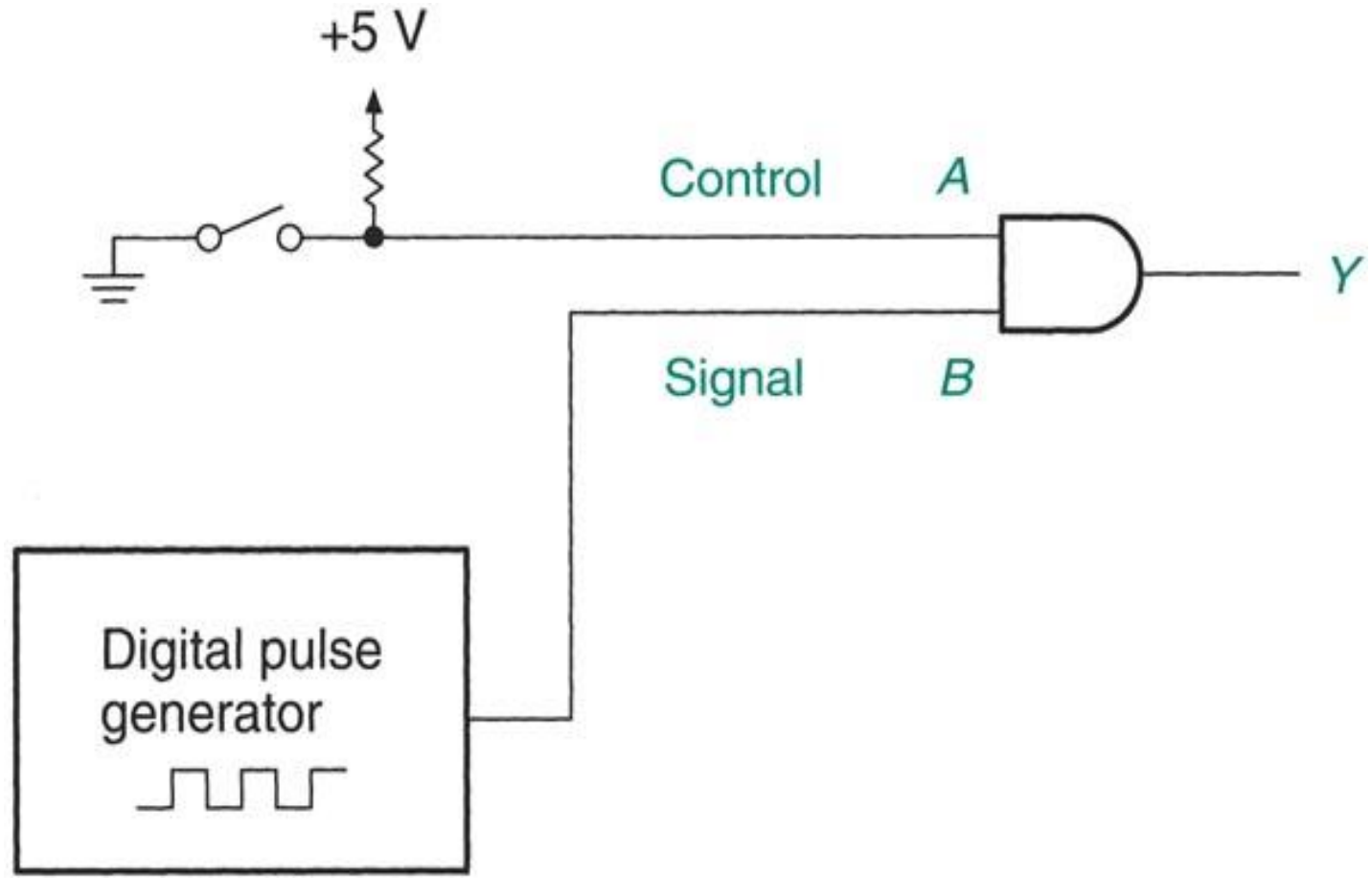


Fig. 2.32

Logic Gate

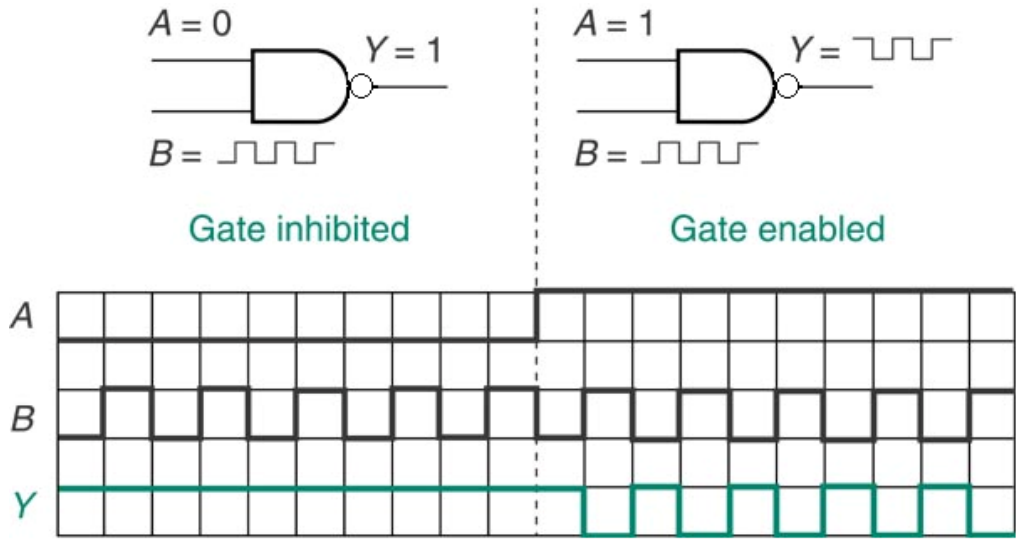


Example 2.4

Use the method just described to draw the output waveform of an OR gate if the input waveforms of *A* and *B* are the same as in Figure 2.32. Indicate the enable and inhibit portions of the timing diagram.

Sol:

NAND Gate



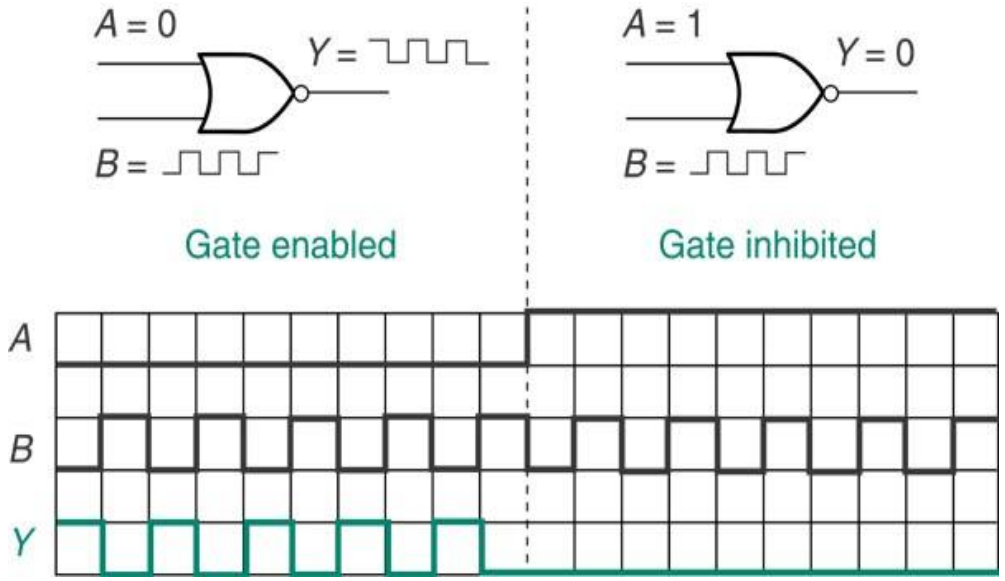
- Truth table:

TABLE 2.17 NAND Truth Table Showing Enable/Inhibit Properties

A	B	Y	
0	0	1	($Y = 1$)
0	1	1	Inhibit
1	0	1	($Y = \bar{B}$)
1	1	0	Enable

Error in Fig 2.35 (book p51)

NOR Gate

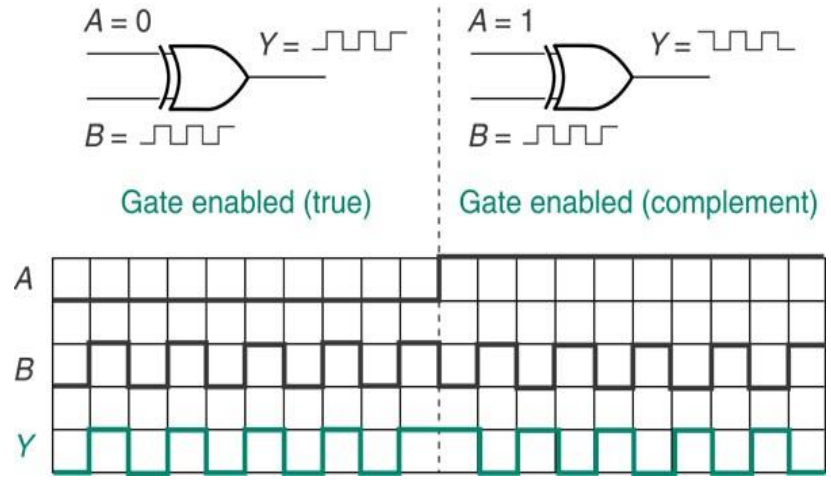


- Truth table:

TABLE 2.18 NOR Truth Table Showing Enable/Inhibit Properties

A	*B*	*Y*	
0	0	1	$(Y = \bar{B})$
0	1	0	Enable
1	0	0	$(Y = 0)$
1	1	0	Inhibit

XOR Gate



- Truth table:

TABLE 2.19 XOR Truth Table Showing Dynamic Properties

A	*B*	*Y*	
0	0	0	($Y = B$)
0	1	1	Enable
1	0	1	($Y = \bar{B}$)
1	1	0	Enable

Summary of Enable/Inhibit Properties

Control	AND	OR	NAND	NOR	XOR	XNOR
$A = 0$	$Y = 0$	$Y = B$	$Y = 1$	$Y = \overline{B}$	$Y = B$	$Y = \overline{B}$
$A = 1$	$Y = B$	$Y = 1$	$Y = \overline{B}$	$Y = 0$	$Y = \overline{B}$	$Y = B$

Tristate Buffer

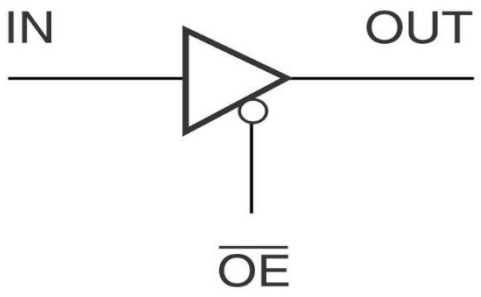
High-Impedance State The output state of a tristate buffer that is neither logic HIGH nor logic LOW, but is electrically equivalent to an open circuit. (Abbreviation: Hi-Z.)

Tristate Buffer A gate having three possible output states: logic HIGH, logic LOW, and high-impedance.

Bus A common wire or parallel group of wires connecting multiple circuits.

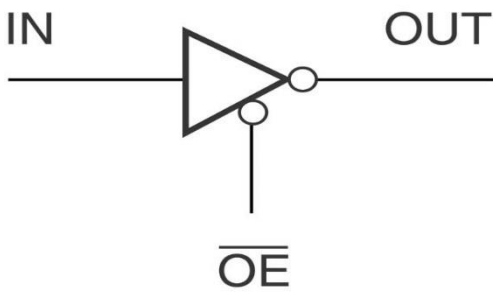
Tristate Buffer

- Three output states, HIGH, LOW and high-impedance (高阻抗).



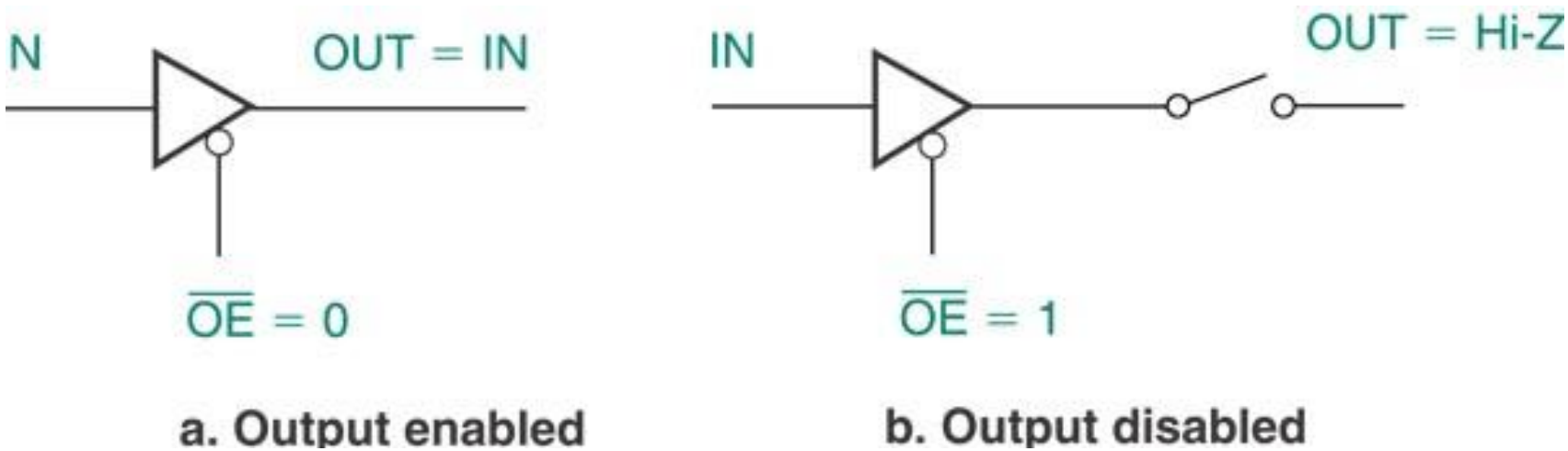
a. Noninverting

- Requires a separate input to control which output state is selected.



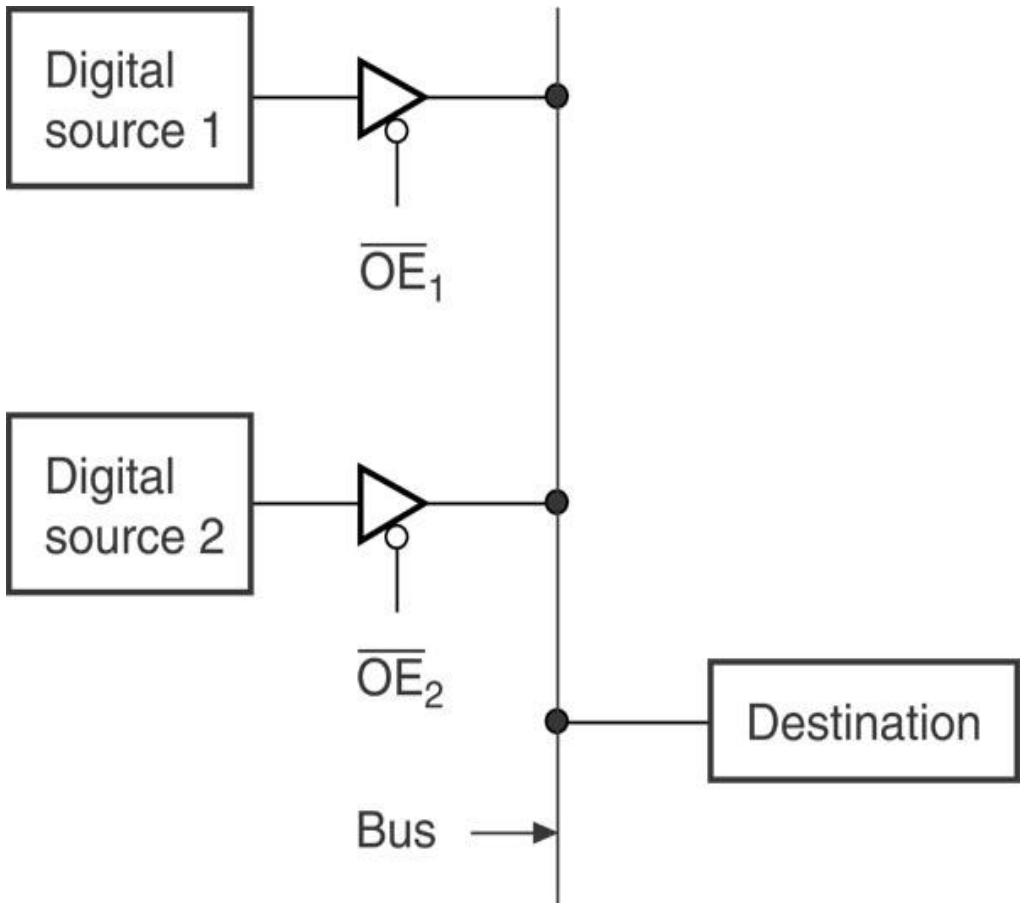
b. Inverting

Tristate Buffer



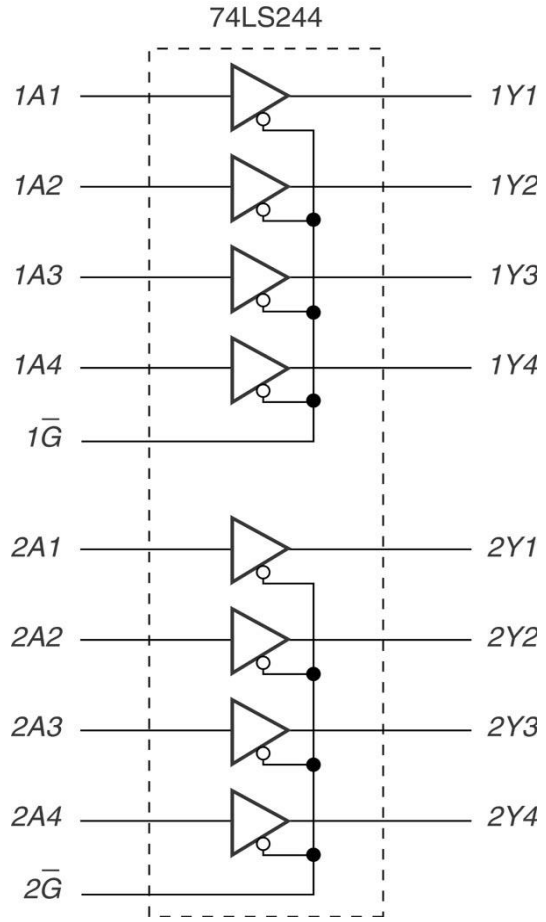
Tristate Buffer Utilization

- Used to connect multiple outputs together.
- Used in controlling the operation of buses.



The 74LS244 Octal Tri-State Buffer

- Contains two groups of four non-inverting tri-state buffers.
- Each group is controlled by a separate enable input.



Example 2.5

Draw a logic circuit showing how a 74LS244 octal tristate buffer can be connected to make a data bus where one of two 4-bit numbers can be transferred to a 4-bit output.

Sol:

2.6 Integrated Circuit Logic Gates

- Integrated Circuits (ICs) contain many components in a single package.
- Several packaging options are available.
- One common package is called dual-in-line (DIP).

Key Terms

Integrated Circuit (IC) An electronic circuit having many components, such as transistors, diodes, resistors, and capacitors, in a single package.

Small Scale Integration (SSI) An integrated circuit having 12 or fewer gates in one package.

Chip An integrated circuit. Specifically, a chip of silicon on which an integrated circuit is constructed.

Medium Scale Integration (MSI) An integrated circuit having the equivalent of 12 to 100 gates in one package.

Large Scale Integration (LSI) An integrated circuit having from 100 to 10,000 equivalent gates.

Key Terms

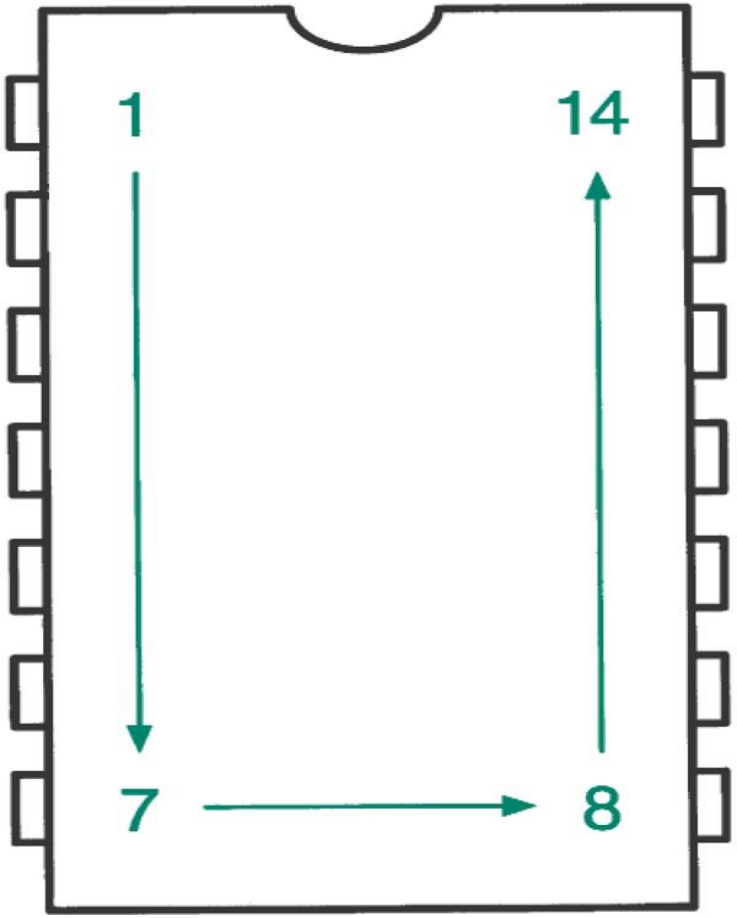
Transistor-Transistor Logic (TTL) A family of digital logic devices whose basic element is the bipolar junction transistor.

Complementary Metal-Oxide-Semiconductor (CMOS) A family of digital logic devices whose basic element is the metal-oxide-semiconductor field effect transistor (MOSFET).

Dual In-Line Package (DIP) A type of IC with two parallel rows of pins for the various circuit inputs and outputs.

Printed Circuit Board (PCB) A circuit board in which connections between components are made with lines of copper on the surfaces of the circuit board.

Integrated Circuit Package



Integrated Circuit Technology

- One common form is transistor-transistor logic, called TTL.

- The other common form is Complementary Metal-Oxide Semiconductor, called CMOS.

Part Numbers for Quad 2-Input NAND Gate

Part Number	*Logic Family*
74LS00	Low-power Schottky TTL
74ALS00	Advanced low-power Schottky TTL
74F00	FAST TTL
74HC00	High-speed CMOS
74HCT00	High-speed CMOS (TTL-compatible inputs)
74LVX00	Low-voltage CMOS
74ABT00	Advanced BiCMOS (TTL/CMOS hybrid)

Integrated Circuit Designation
IC編號

- Standard form is 74XXFF, where 74 is the logic family identifier, XX is the logic family member and FF identifies the specific logic function.

Industry-Standard Number

- SN74ALS00N:

  SN: Manufacturer (Texas Instruments)

  74: 74-series TTL

  ALS: Logic Family (Advanced Low-Power Schottky)

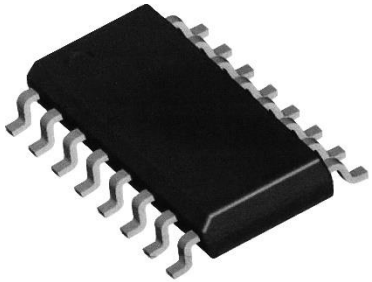
  00: Logic Function (Quad 2-Input NAND)

  N: Package (Plastic DIP)

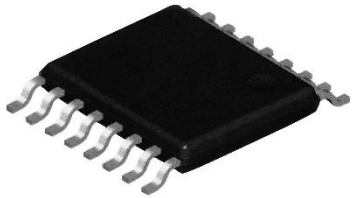
IC Package Options

- PLCC - plastic lead chip carrier
- SOIC - small outline integrated circuit
- TSSOP – thin shrink(縮小) small outline package
- QFP – quad flat pack
- DIP – dual inline package
- BGA – ball grid array

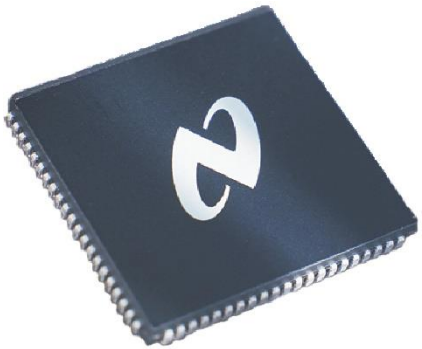
IC Package Options



SOIC



TSSOP



PLCC

d.QFP

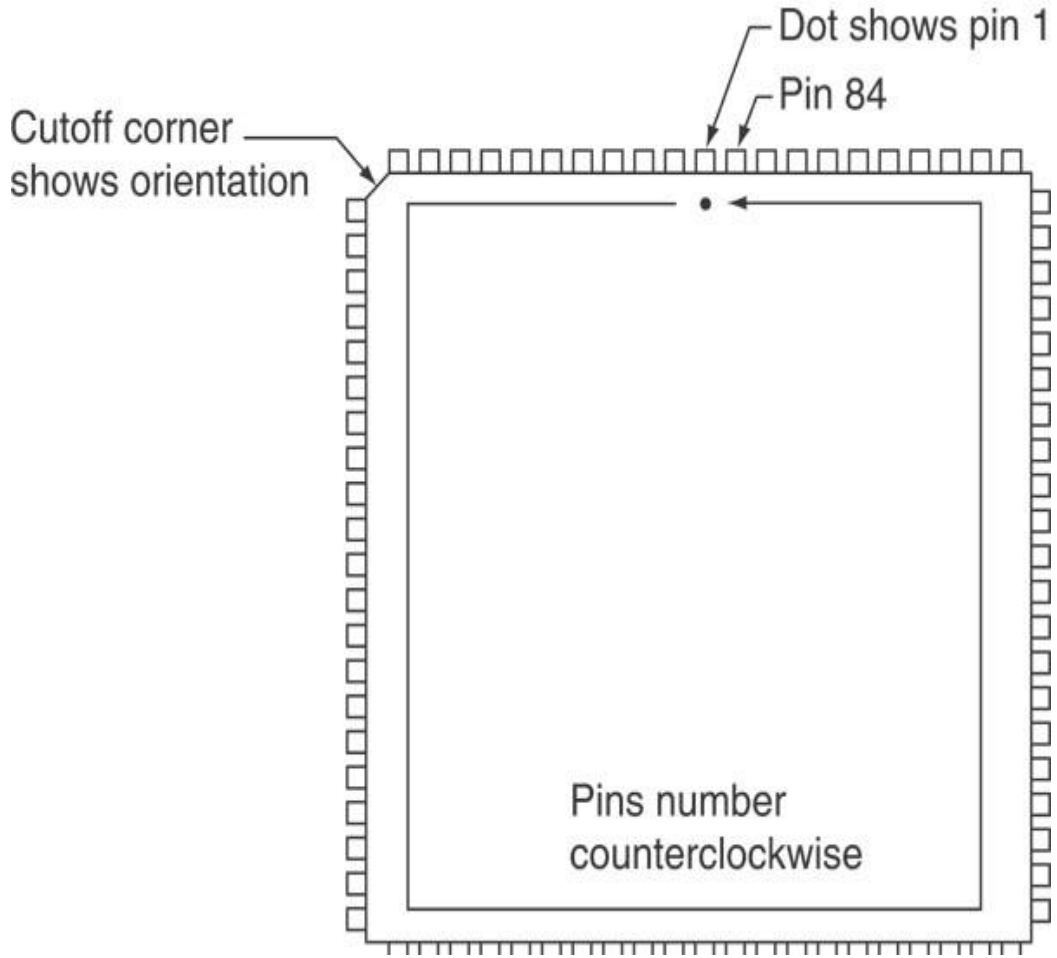
DIP

BGA

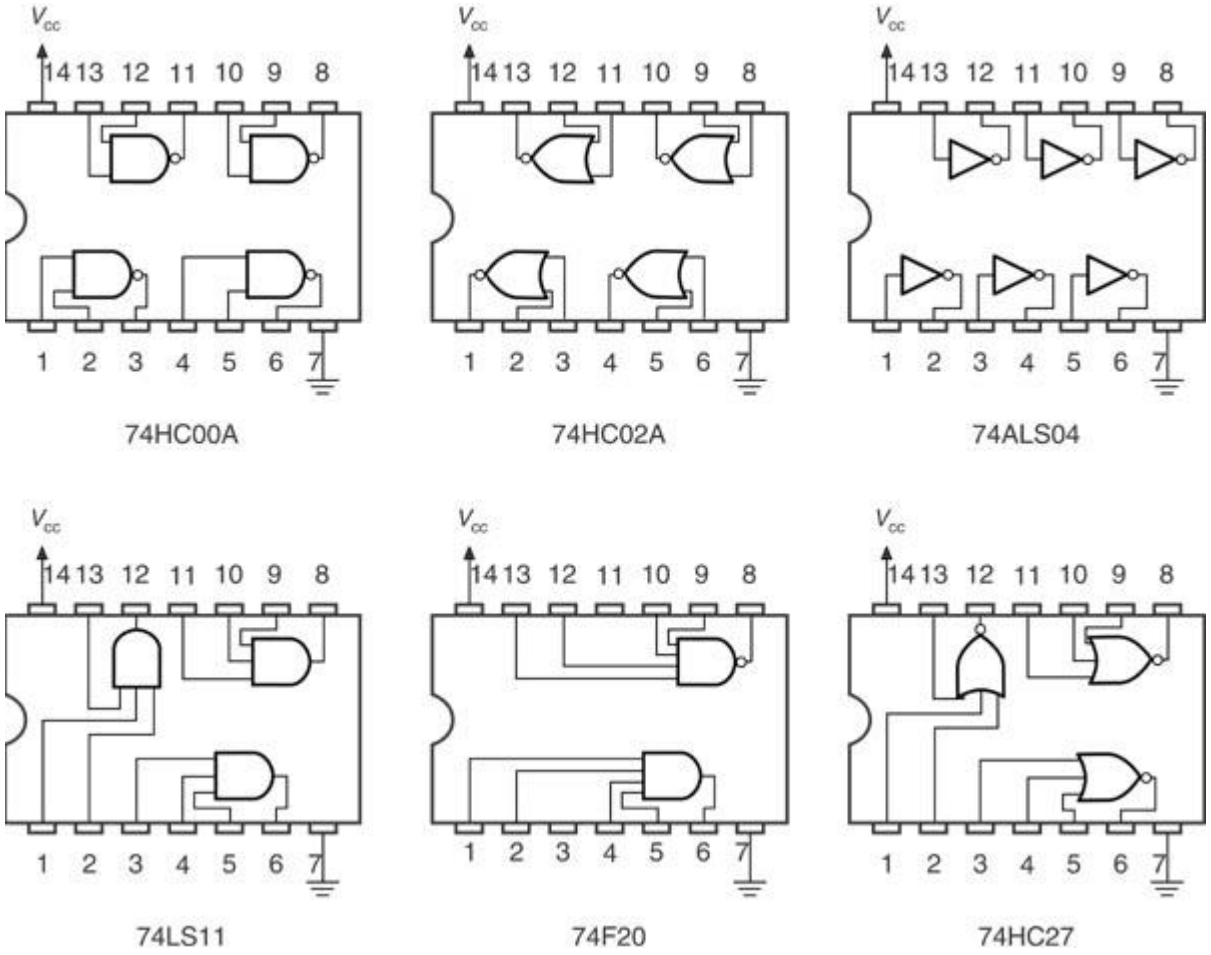
PLCC 84 Pin Packages

- Can be mounted on the surface of a circuit board or mounted in a socket.
- Pins are equally distributed on four sides.
- Pin 1 placed on the center of one of the rows, as indicated by a dot.
- Pins number counterclockwise from this point.

PLCC 84 Pin Packages



Pinouts of ICs



Homework