數位邏輯設計 Ch9 HW

注意事項：請寫出詳細計算與分析過程，不可以只寫答案!

Problems:

9.2 Figure 9.111 shows a mod-16 which controls the operation of two digital sequential circuits, labeled Circuit 1 and Circuit 2. Circuit 1 is positive edge-triggered and clocked by counter output Q_1. Circuit 2 is negative edge-triggered and clocked by Q_3. (Q_3 is the MSB output of the counter.)

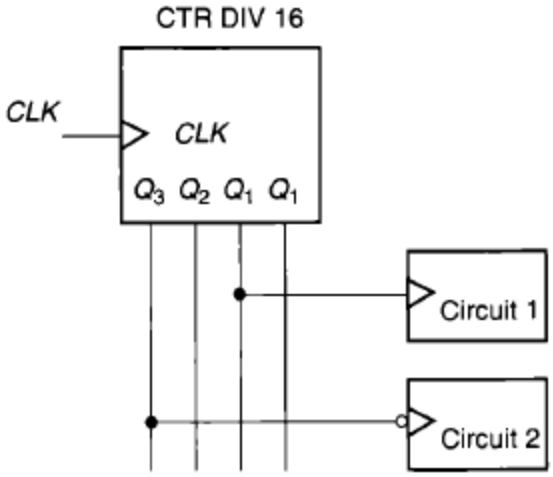

FIGURE 9.111 Problem 9.2: Mod-16 Counter Driving Two Sequential Circuits

a. Draw the timing diagram for one complete cycle of the circuit operation. Draw arrows on the active edges of the waveforms that activate Circuit 1 and Circuit 2.

b. State how many times Circuit 1 is clocked for each time that Circuit 2 is clocked.

9.11 Draw the circuit for a synchronous mod-16 UP counter made from negative edge-triggered JK flip-flops.

9.55 Complete the logic circuit shown in Figure 9.117 to make a parallel-in-serial-out shift register.

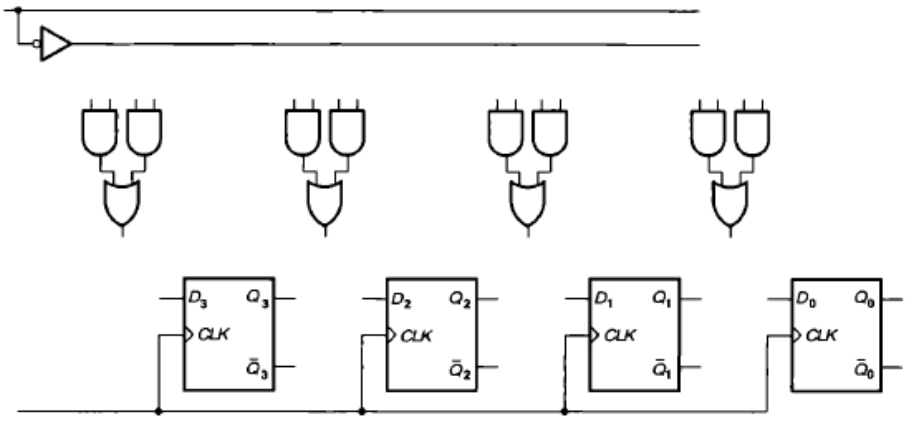

FIGURE 9.117 Problem 9.55: Logic Circuit