

Lab report (upload to iLMS before 4/7 3:30p.m.)

Your report should include the following:

- description and explanation of your work (including answers to all questions in the pre-lab)

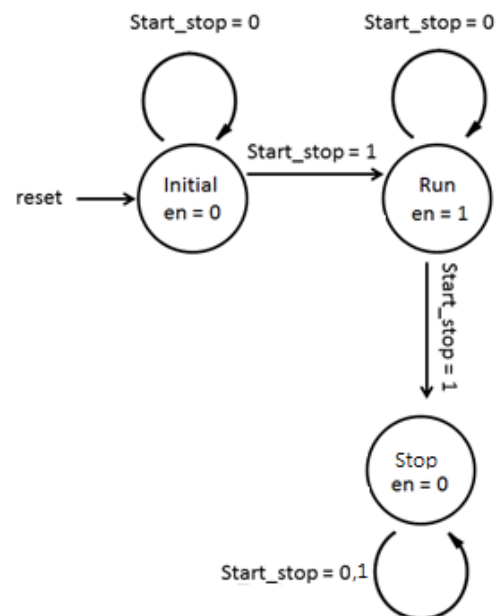
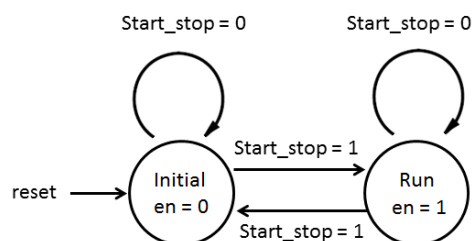
1. It is clear that we need a periodic clock source to clock the counter. What is available for this purpose on the development board? What is the clock frequency needed and how can we get the appropriate frequency?

利用 FPGA 上的 Crystal oscillator (振盪晶體)，我們可以得到 40.0MHz 的時間訊號，而我們需要每 0.1 秒改變一次的時間訊號，因此使用助教提供的 time divider 得到 10Hz 的時間訊號。

2. To implement the start/stop mechanism, we can design a control unit which produces the enable signal for the counter. Can we use the pushbutton S1 output as input to the control unit directly? Why?

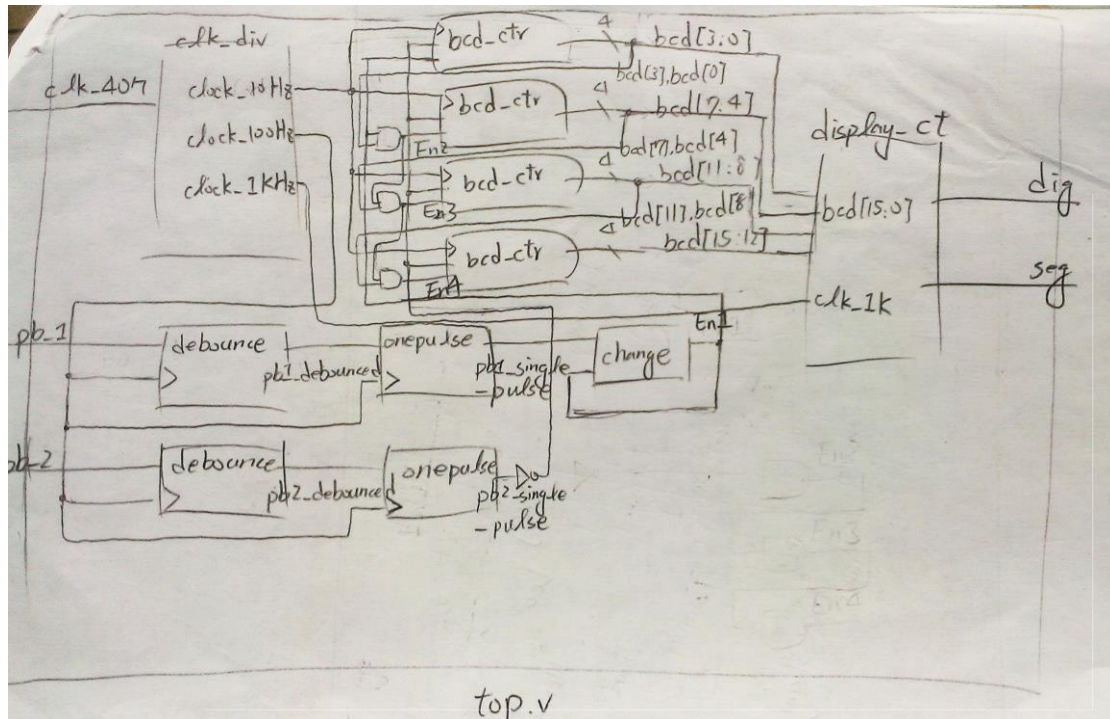
我們不能直接使用 S1 當作控制訊號，因為當按鈕按下，可能是要讓 counter 開始或繼續，也有可能是要讓他停下，意即同樣的按下訊號，會因為當下的狀態而代表不同的意涵，所以我們需要多一個 register 來做為控制訊號。

3. A sample state transition diagram for the control unit is given below. Is it a Moore machine or Mealy machine? The given diagram assumes that after stopping, it will resume if one presses the “Start/Stop” button again. Can you give an alternative state transition diagram which will ignore the Start_stop signal once it has been stopped?



這是一個 Moore machine。新的 Diagram 如右上圖所示。

4. Draw a block diagram for the complete design by re-using existing modules introduced in the class previously and defining any new module.



5. Prepare a UCF file for the input/output pin assignment.

- discussion of any issue or problem worthy of note (yes, even mistakes that you made)
運用前幾次lab製作的module在這次的lab,自己用簡單快速的方法做完之後,想說幫同學 Debug,雖然程式有一點不同,但邏輯上是相同的,不知道為什麼就是解決不了,連助教也都無法解答,這真的滿困擾的。
- optional: any extra feature you added or any suggestion
這次我堅持不修改以前已經製作好的 module,就像團隊中,別人做好的模組,我們應該調整自己的 code,而不是亂改別人已經做好的模組。
覺得自己下次可以提早看題目,構思解決方案。