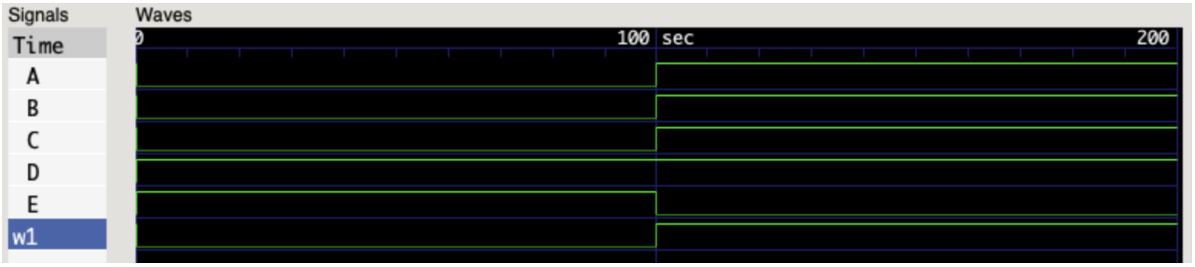
Lab 1: Writing and Testing HDL Modules of Simple Combinational Circuits

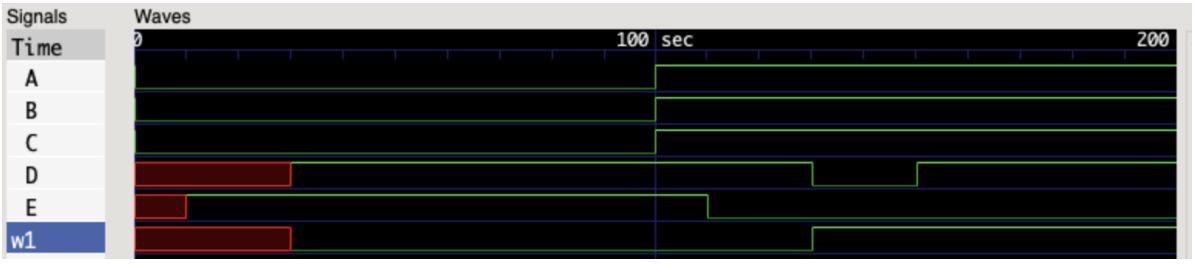
0713335 林谷翰

1. Give the waveform of the simulation result of 2A(a), including outputs *D* and *E* and internal connection *w*1, and explain the difference between the waveform of *Simple_Circuit.v* and that of *Simple_Circuit_prop_delay.v.*

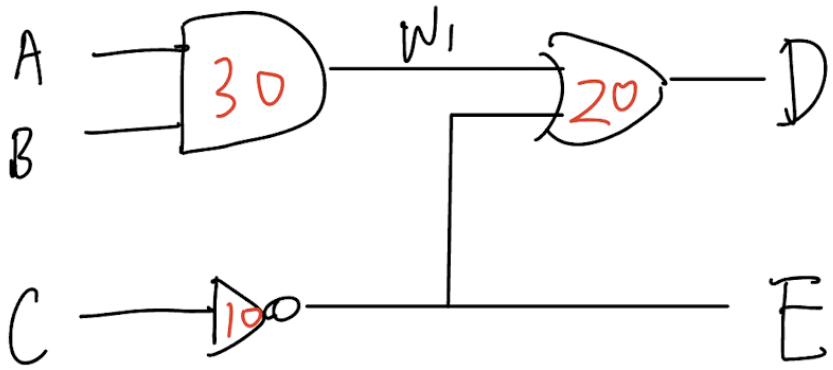
   Simple_Circuit



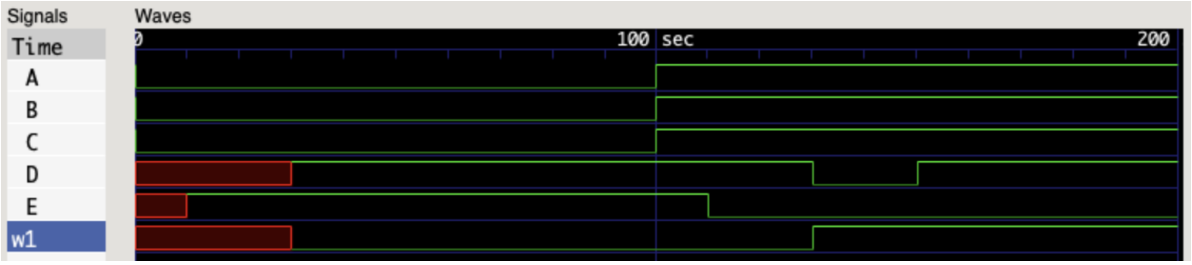
   Simple_CIrcuit_prop_delay



   Because the propagation delay is added, the change of input signal won’t immediately affect the output signal.

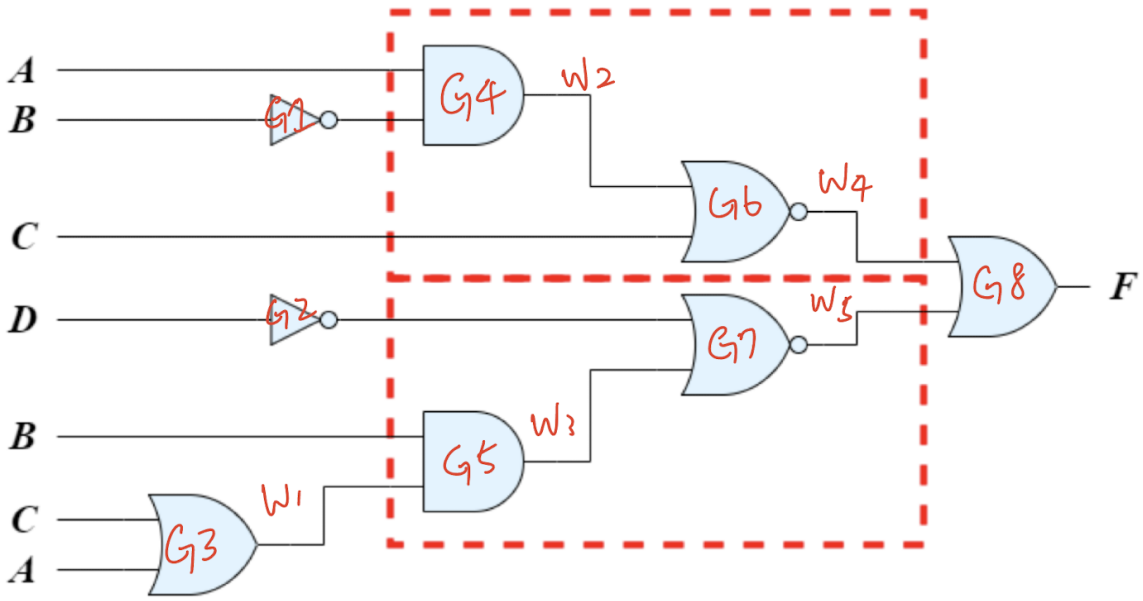


2. Give the waveform of the simulation result of 2A(b), and explain whether there is any difference between the waveforms of 2A(a) and 2A(b).

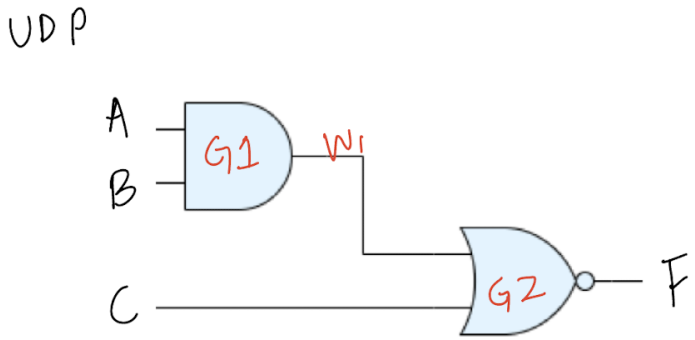


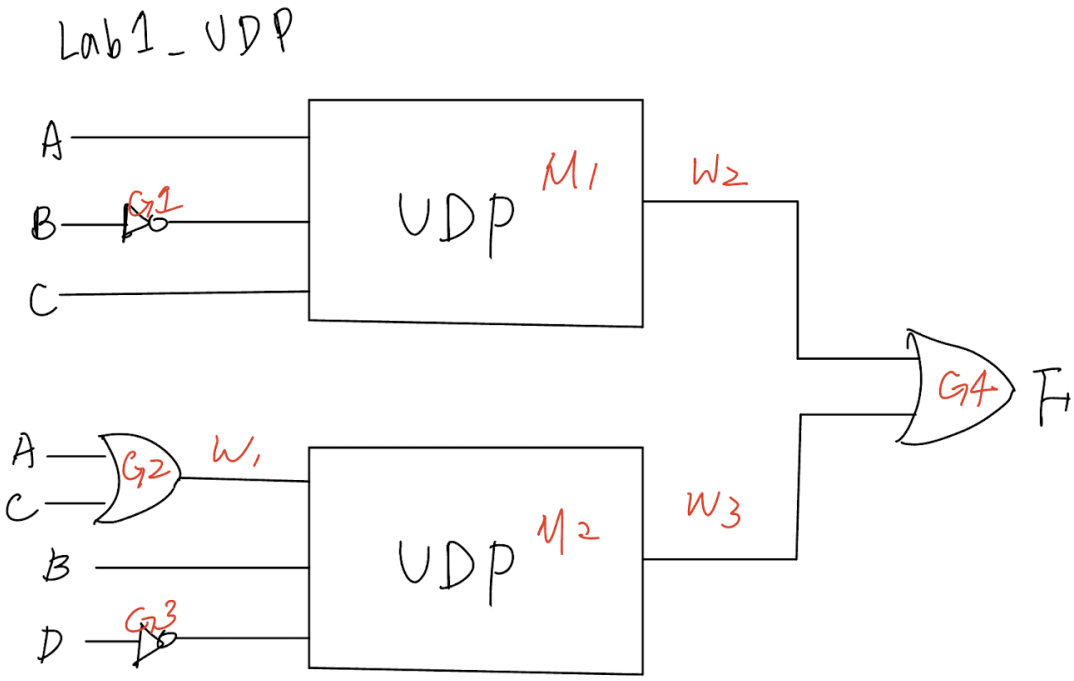
The waveform will remain same because the sequence of the gate assignment doesn't change the simulation result in Verilog.

3. Give the waveform of the simulation result in 2B(d), and explain whether the three modules are correct.

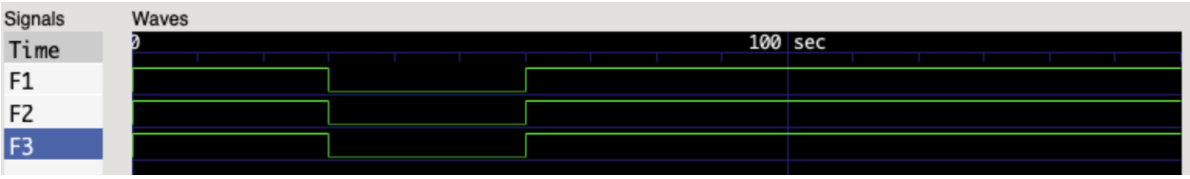


UDP





I test all possible inputs and all output signals are same for three modules.



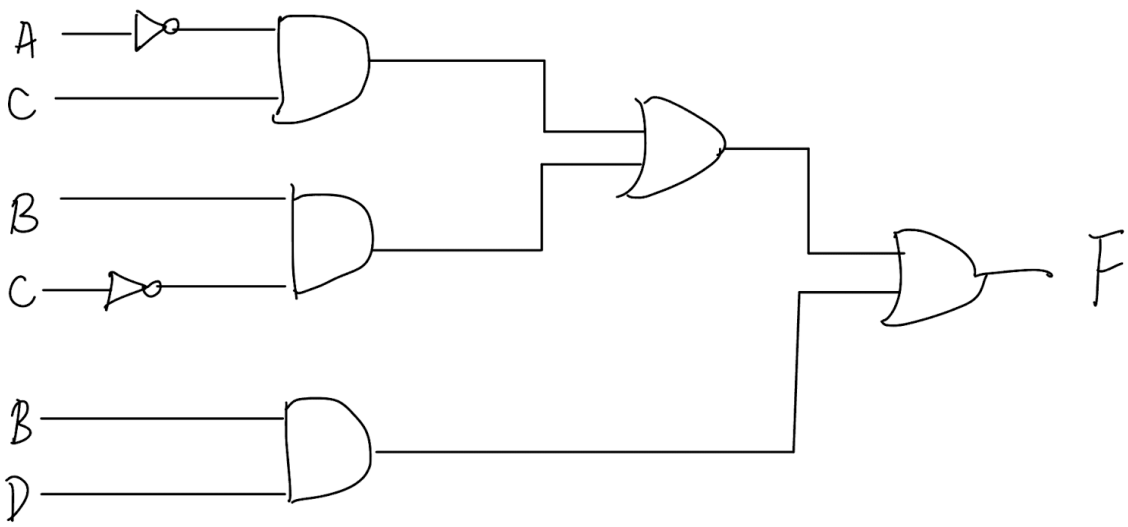

```
module  t_LAB1();
  wire  F1, F2, F3;
  reg   A, B, C, D;

  //instantiate device under test
  Lab1_gatelevel  M1(F1, A, B, C, D);
```

```
  Lab1_dataflow M2(F2, A, B, C, D);
  LAB1_UDP  M3(F3, A, B, C, D);

  //apply inputs one at a time
  initial begin
    A=1'b0; B=1'b0; C=1'b0; D=1'b0;
    #10 A=1'b0; B=1'b0; C=1'b0; D=1'b1;
    #20 A=1'b0; B=1'b0; C=1'b1; D=1'b0;
    #30 A=1'b0; B=1'b0; C=1'b1; D=1'b1;
    #40 A=1'b0; B=1'b1; C=1'b0; D=1'b0;
    #50 A=1'b0; B=1'b1; C=1'b0; D=1'b1;
    #60 A=1'b0; B=1'b1; C=1'b1; D=1'b0;
    #70 A=1'b0; B=1'b1; C=1'b1; D=1'b1;
    #80 A=1'b1; B=1'b0; C=1'b0; D=1'b0;
    #90 A=1'b1; B=1'b0; C=1'b0; D=1'b1;
    #100 A=1'b1; B=1'b0; C=1'b1; D=1'b0;
    #110 A=1'b1; B=1'b0; C=1'b1; D=1'b1;
    #120 A=1'b1; B=1'b1; C=1'b0; D=1'b0;
    #130 A=1'b1; B=1'b1; C=1'b0; D=1'b1;
    #140 A=1'b1; B=1'b1; C=1'b1; D=1'b0;
    #150 A=1'b1; B=1'b1; C=1'b1; D=1'b1;
  end
  initial #160 $finish;

  //dump the result of simulation
  initial begin
    $dumpfile("Lab1_design.vcd");
    $dumpvars;
  end
endmodule
```

4. Does the design of Figure 1 have the least gate input count for the function of the circuit? If yes, explain your reason; if not, derive the Boolean expression with least gate input count for the function, draw the logic diagram of the circuit by using AND, OR, NOT, NAND, and NOR gates, and write the gate input count of the circuit.

   No. The original GIC is 14. After simplify, the Boolean expression is :

$$F = A'C' + BC' + BD$$
$$GIC = 12$$



5. Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab.

   In this lab, I have learned the pipeline of how to designing a combinational circuit and simulate the result using Verilog and gtkwave.