Lab 5: Seven-segment display decoder

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Purpose:

1) Be able to write the truth table according to the function of logic circuit to design and be able to design the more complex block of combinational logic.
2) Be able to use Altera Quartus Software to design required logic circuit.
3) Be familiar with the VHDL language and use it to implement the logic design.
4) Be able to use ModelSim software to simulate the operation of designed circuit and thus test the correctness of designed circuit before it was physically built in hardware.
5) Download designed circuit to DE2 board and test the correctness of designed circuit on the FPGA.

Content:

1) Background: Seven-segment decoder:

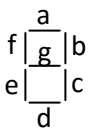


Figure 1 Seven – segment display

Each of segment is labeled a through g as shown in Figure 1, the numbers 0 ~ F are shown by lighting up the some segments of Seven-segment display as Figure 2

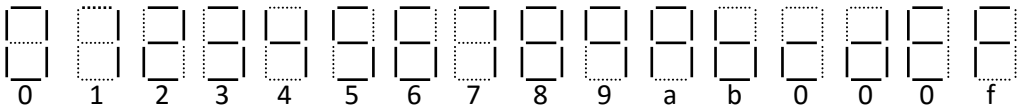


Figure 2 Seven –segment display function

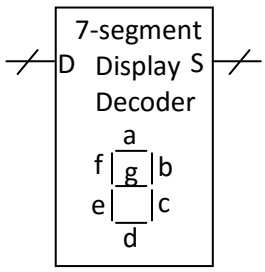


Figure 3 7–segment display decoder

We need to build a seven-segment display decoder, shown in Figure 3. The decoder has four input bits, $D_{3:0}$ (representing a hexadecimal number from 0 to F), seven output bits, $S_{a:g}$, each output bit is used to drive the corresponding segment of the display decoder to display the numbers. A segment of the display turns on when it is 0. So the output is low-asserted output or active low output.

2) Truth Table of 7-segment display decoder

The output states of the 7-segment display decoder to design corresponding to each input combination are written in following truth table.

Hexadecimal digit	Inputs				outputs							In Hex
	D_3	D_2	D_1	D_0	S_g	S_f	S_e	S_d	S_c	S_b	S_a	
0	0	0	0	0	1	0	0	0	0	0	0	40
1	0	0	0	1	1	1	1	1	0	0	1	79
2	0	0	1	0	0	1	0	0	1	0	0	24
3	0	0	1	1	0	1	1	0	0	0	0	30
4	0	1	0	0	0	0	1	1	0	0	1	19
5	0	1	0	1	0	0	1	0	0	1	0	12
6	0	1	1	0	0	0	0	0	0	1	0	2
7	0	1	1	1	1	1	1	1	0	0	0	78
8	1	0	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	1	1	0	0	0	18
A	1	0	1	0	0	0	0	1	0	0	0	8
B	1	0	1	1	0	0	0	0	0	1	1	3
C	1	1	0	0	0	1	0	0	1	1	1	27
D	1	1	0	1	0	1	0	0	0	0	1	21
E	1	1	1	0	0	0	0	0	1	1	0	6
F	1	1	1	1	0	0	0	1	1	1	0	E

Table 1 Truth Table of 7-segment display decoder

3) VHDL programming

In this lab, we program with VHDL(VHSIC Hardware Description Language) to implement the above truth table in Altera Quartus software, and hence finish the design of 7-segment display decoder. The following is the written program:

```
entity Sevensegment is

port

(

        SW: in std_logic_vector (3 downto 0);

        Hex0: out std_logic_vector (6 downto 0)

);
```

```
end entity;

architecture rtl of Sevensegment is
begin

        process(SW)
        begin
         case(SW) is
         when"0000" => Hex0 <= "1000000";
         when"0001" => Hex0 <= "1111001";
         when"0010" => Hex0 <= "0100100";
         when"0011" => Hex0 <= "0110000";
         when"0100" => Hex0 <= "0011001";
         when"0101" => Hex0 <= "0010010";
         when"0110" => Hex0 <= "0000010";
         when"0111" => Hex0 <= "1111000";
         when"1000" => Hex0 <= "0000000";
         when"1001" => Hex0 <= "0011000";
         when"1010" => Hex0 <= "0001000";
         when"1011" => Hex0 <= "0000011";
         when"1100" => Hex0 <= "0100111";
         when"1101" => Hex0 <= "0100001";
         when"1110" => Hex0 <= "0000110";
         when"1111" => Hex0 <= "0001110";
         when others => Hex0 <="0000000";
```

```
    end case;

    end process;

end rtl;
```

4) Simulation using ModelSim

The designed 7-segment display decoder using above VHDL program was simulated in ModelSim to verify its correctness

The simulation results is shown in Figure 4

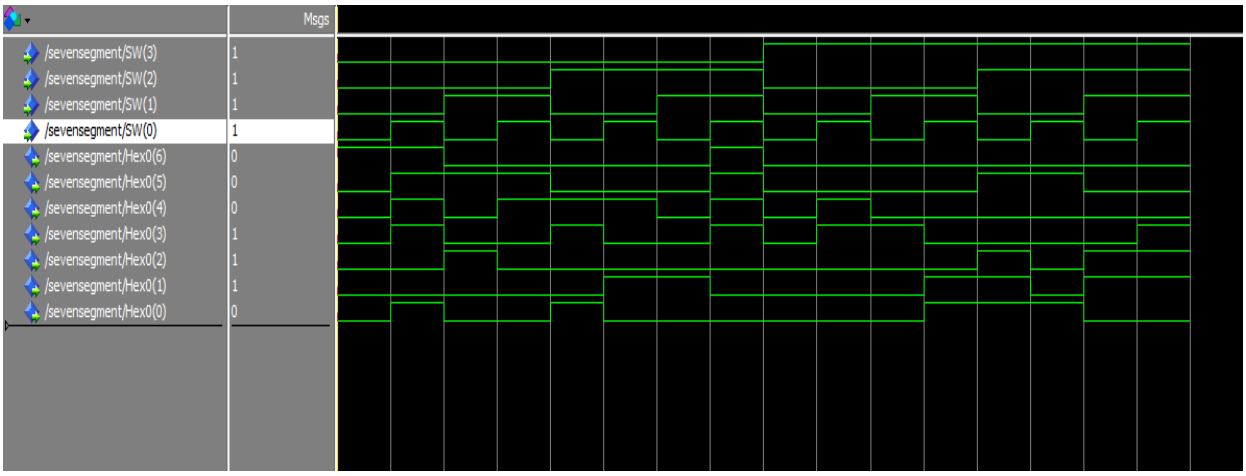
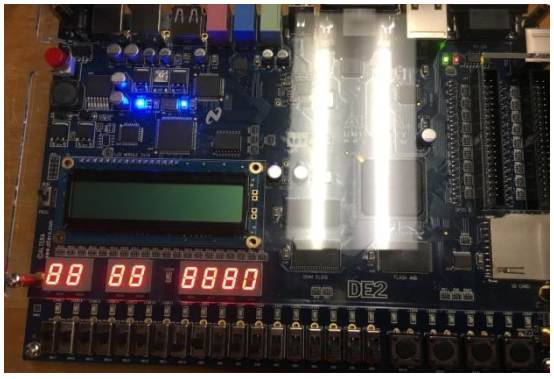


Figure 4 Simulation Results of designed 7-segment display decoder

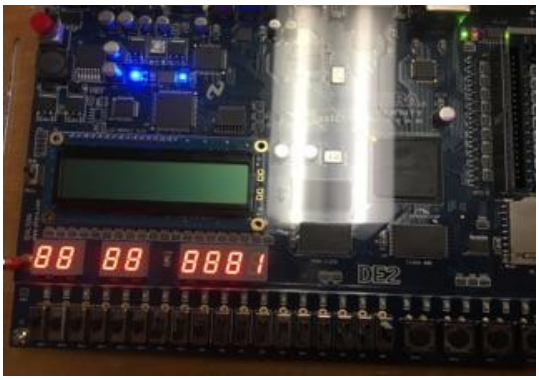
From Figure 4, it can be seen that for each combination of inputs, the outputs of designed 7-segment display decoder agree with that of truth table in Table 1. That means the designed decoder is correct.

5) Test on DE2 board

The designed circuit was downloaded to DE2 board, switches SW0-SW3 are corresponding to inputs D0-D3; the outputs of circuit are fed to HEX0 to display the results. the test results are shown in following pictures

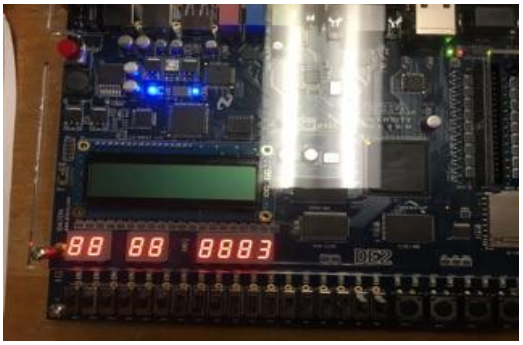


Picture 1 the output for input '0000'

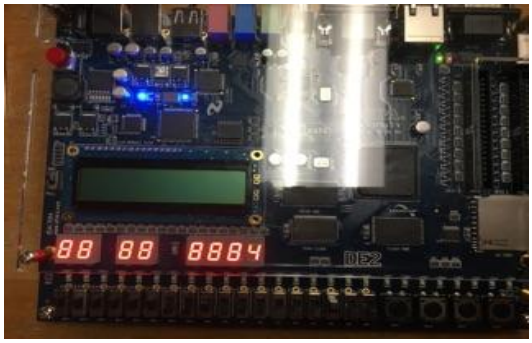


Picture 2 the output for input '0001'

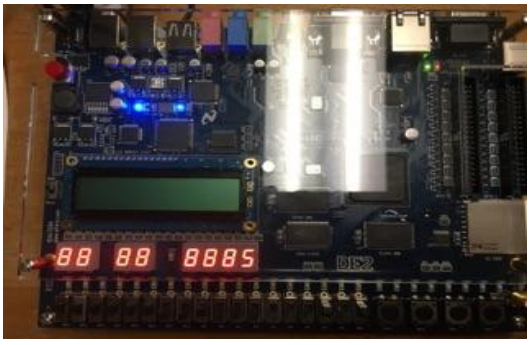
Picture 3 the output for input ‘0010’



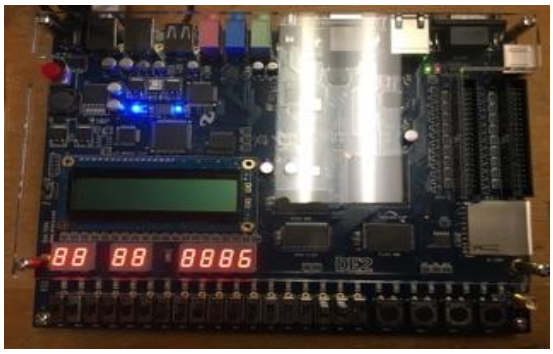
Picture 4 the output for input ‘0011’



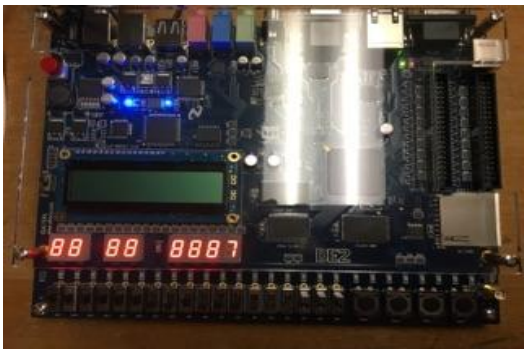
Picture 5 the output for input ‘0100’



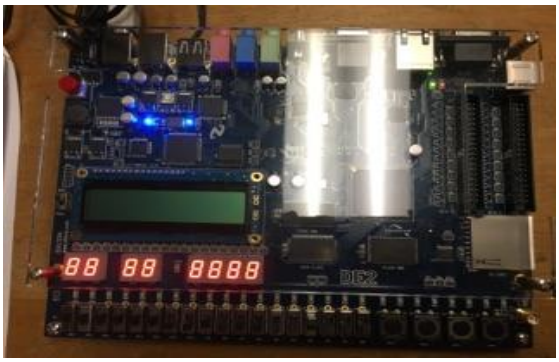
Picture 6 the output for input ‘0101’



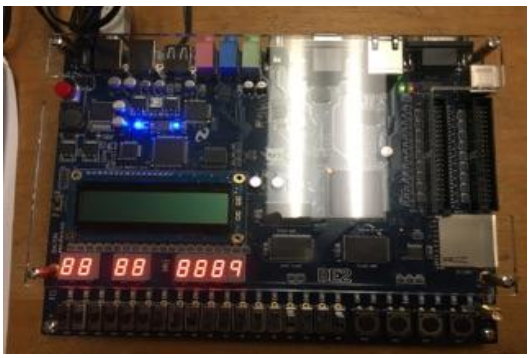
Picture 7 the output for input ‘0110’



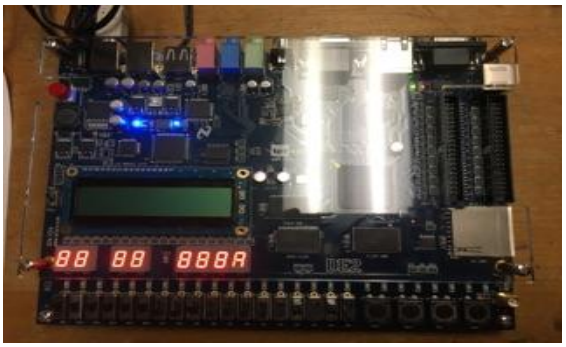
Picture 8 the output for input ‘0111’



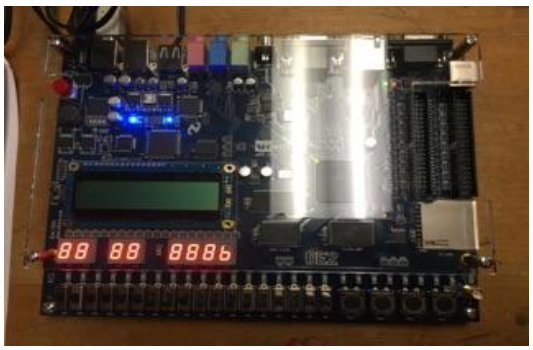
Picture 9 the output for input ‘1000’



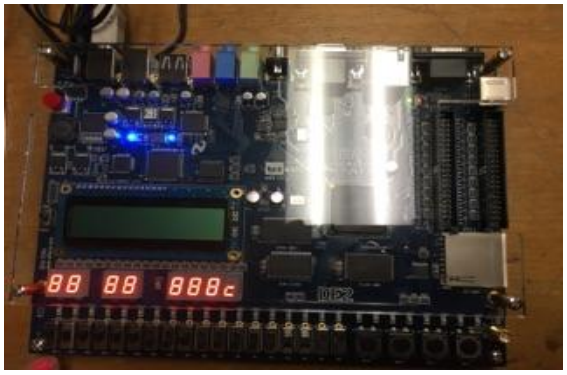
Picture 10 the output for input ‘1001’



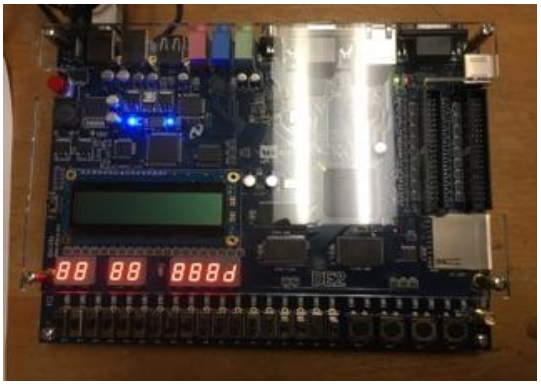
Picture 11 the output for input ‘1010’



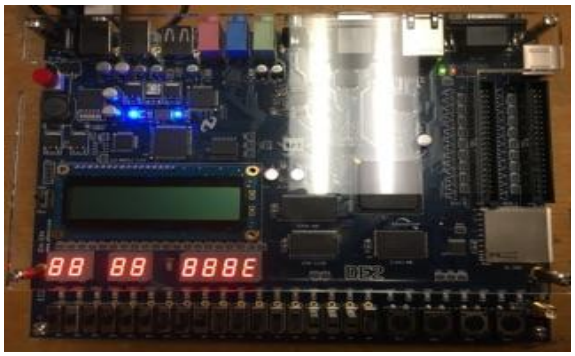
Picture 12 the output for input ‘1011’



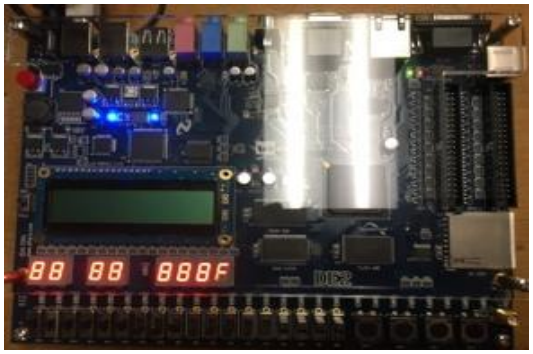
Picture 13 the output for input ‘1100’



Picture 14 the output for input ‘1101’



Picture 15 the output for input ‘1110’



Picture 16 the output for input ‘1111’

From above pictures, it can be seen that the designed circuit successfully achieved the required function of 7-segment display decoder.

3) Conclusions: (my lab partners and I used 1.5 hours to finish the Lab 5)

From the lab 5,

1) I can write the truth table according to the function of logic circuit to design and design the more complicate block of combinational logic based on truth table.
2) I can use Altera Quartus Software to design required logic circuit.
3) I become familiar with the VHDL language and use it to implement the logic design.
4) I can use ModelSim software to simulate the operation of designed circuit and thus to test the correctness of designed circuit.
5) I get to know how to download designed circuit to DE2 board and test the correctness of designed circuit on the FPGA(hard ware).

What I did in Lab 5

1)complete the truth table of 7-segment display decoder;
2)programming with VHDL language based on the truth table of 7-segment display decoder;
3)Debug the program ;
4)make simulation on designed decoder using ModelSim;
5)download the designed decoder to DE2 board to test the validity of circuit.

What my lab partner did:

1) Complete the truth table of 7-segment display decoder;
2) Programming with VHDL language together with me to implement design based on the truth table;
3) Debug the program and compile the program successfully;
4) Simulate the designed circuit using ModelSim and get simulation results;
5) Set up the DE2 board, download the designed decoder to DE2 board and check the function of designed decoder according to truth table, record the results