Lab 4: Full Adder

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Purpose:

1) Understand the binary arithmetic, digital logic and logic gates.
2) Understand the logic operation, Boolean operation, Table truth, the general Boolean operation rules, be able to use truth table and Boolean operation rules to simplify the Boolean expression and design schematic by using various logic gates.
3) Get to familiar with Altera Quartus Software and be able to use it to draw the schematic representation of the designed logic.
4) Be familiar with the ModelSim software and be able to use it to simulate the operation of circuit which has been drawn in Quartus, thus test the correctness of designed circuit before it was physically built in hardware.
5) Be familiar with DE2 Board and be able to download designed circuit onto DE2 board and test its correctness on the FPGA.

Content:

1) Boolean operation, corresponding truth table
   a. $A \cdot B$
   b. $A + B$
   c. $A \oplus B$
   d. $\overline{A}$

   Truth Table

A	B	$A \cdot B$	$A + B$	$A \oplus B$	$\overline{A}$
0	0	0	0	0	1
0	1	0	1	1	1
1	0	0	1	1	0
1	1	1	1	0	0

2) General rules of Boolean Operation
   a. $0 \cdot A = 0$
   b. $1 \cdot A = A$
   c. $A \cdot A = A$
   d. $A \cdot \overline{A} = 0$
   e. $A \cdot B = B \cdot A$
   f. $1 + A = 1$
   g. $0 + A = A$

h. A + A = A
i. $A + \overline{A} = 1$
j. A·(B·C) = (A·B)·C
k. A + B = B + A
l. A·(B+C) = A·B + A·C
m. A+(B+C) = (A+B)+C
n. $\overline{(A \cdot B)} = \overline{A} + \overline{B}$
o. $A+B \cdot C = (\overline{A} + \overline{B}) \cdot (\overline{A} + \overline{C})$
p. $\overline{(\overline{A})} = A$
q. $\overline{(A + B)} = \overline{A} \cdot \overline{B}$

3) Full adder

A full adder is a kind of circuit that can carry out the function of binary sum of its inputs. A full adder has three inputs (A, B, Cin) and two outputs (S, Cout). As shown in Figure 1, where A, B each represent 1-bit binary numbers that are being added, S represents a bit of the resulting sum.

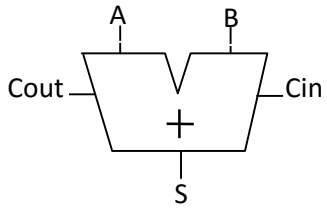

Figure 1

Cin (Carry in) and Cout (carry out) are signals when adding numbers are more than one bit long.

Design

The truth table for a full adder is given in Table 1.

Table 1

Inputs			Outputs	
Cin	A	B	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

1) For S, there is

$$S = \overline{Cin} \cdot \overline{A} \cdot B + \overline{Cin} \cdot A \cdot \overline{B} + Cin \cdot \overline{A} \cdot \overline{B} + Cin \cdot A \cdot B$$

$$S = \overline{Cin} \cdot (\overline{A} \cdot B + A \cdot \overline{B}) + Cin \cdot (\overline{A} \cdot \overline{B} + A \cdot B)$$

$$S = \overline{Cin} \cdot (\overline{A} \cdot B + A \cdot \overline{B}) + Cin \cdot (\overline{A} \cdot A + \overline{A} \cdot \overline{B} + A \cdot B + \overline{B} \cdot B)$$

$$S = \overline{Cin} \cdot (\overline{A} \cdot B + A \cdot \overline{B}) + Cin \cdot (\overline{A} \cdot (A + \overline{B}) + (A + \overline{B}) \cdot B)$$

$$S = \overline{Cin} \cdot (\overline{A} \cdot B + A \cdot \overline{B}) + Cin \cdot (A + \overline{B}) \cdot (B + \overline{A})$$

$$S = \overline{Cin} \cdot (\overline{A} \cdot B + A \cdot \overline{B}) + Cin \cdot \left(\left(\overline{\overline{A} \cdot B}\right) \cdot \left(\overline{\overline{B} \cdot A}\right)\right)$$

$$S = \overline{Cin} \cdot (\overline{A} \cdot B + A \cdot \overline{B}) + Cin \cdot (\overline{A} \cdot B + \overline{B} \cdot A)$$

$$S = \overline{Cin} \cdot (A \oplus B) + Cin \cdot (A \oplus B)$$

$$S = Cin \oplus (A \oplus B)$$

According the above simplified Boolean expression, the corresponding circuit is shown in Figure 2

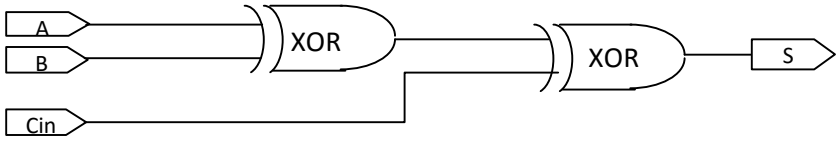

Figure 2

2) For Cout, there is

$$S = \overline{Cin} \cdot A \cdot B + Cin \cdot A \cdot \overline{B} + Cin \cdot \overline{A} \cdot B + Cin \cdot A \cdot B$$

$$S = (\overline{Cin} + Cin) \cdot A \cdot B + Cin \cdot A \cdot \overline{B} + Cin \cdot \overline{A} \cdot B + Cin \cdot A \cdot B + Cin \cdot A \cdot B$$

$$S = (\overline{Cin} + Cin) \cdot A \cdot B + Cin \cdot (\overline{A} \cdot B + A \cdot B) + Cin \cdot (A \cdot \overline{B} + A \cdot B)$$

$$S = A \cdot B + Cin \cdot B \cdot (A + \overline{A}) + Cin \cdot A \cdot (B + \overline{B})$$

$$S = A \cdot B + Cin \cdot B + Cin \cdot A$$

the above simplified Boolean expression, the corresponding circuit is shown in Figure 3

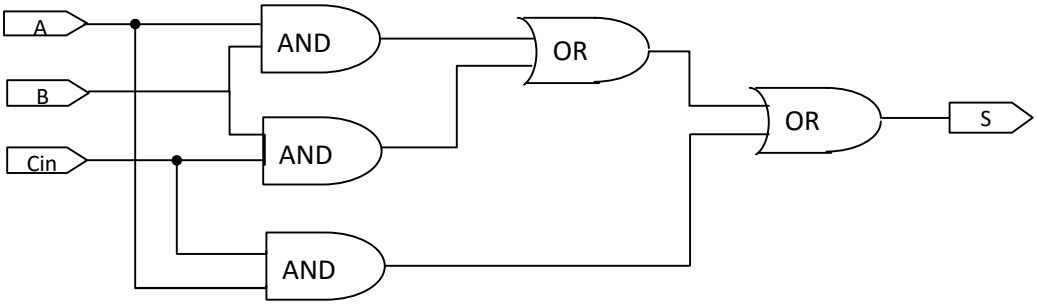

Figure 3

3) The Schematic of circuit of full adder drawn in the Altera Quartus is shown in Figure 4

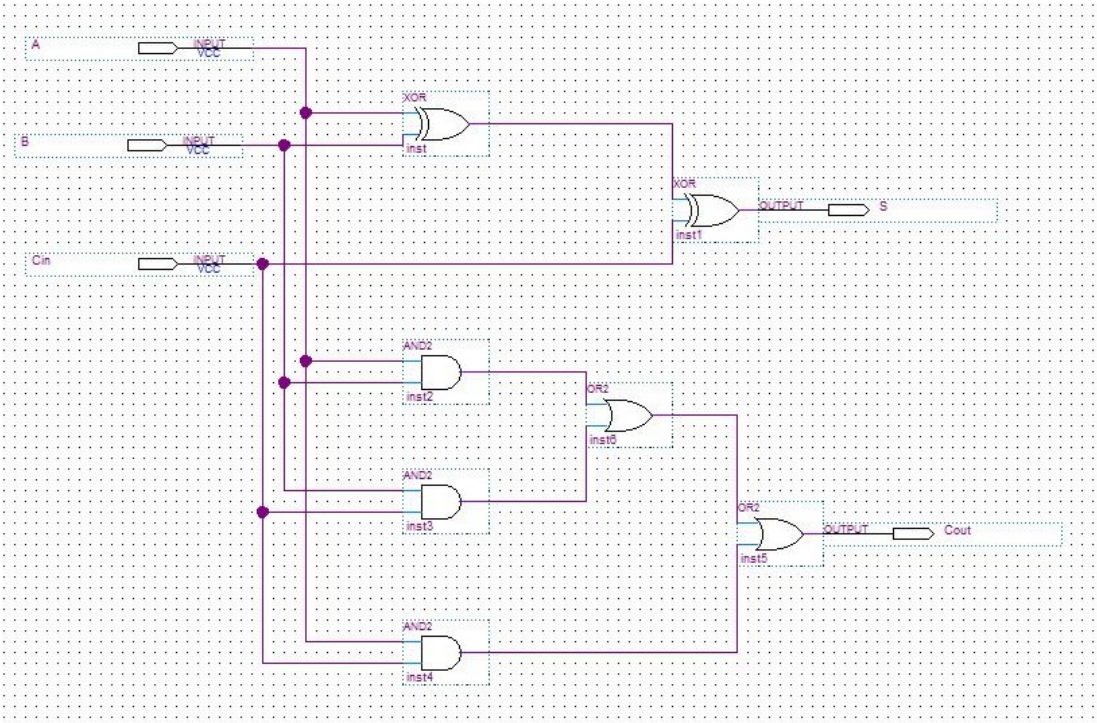

Figure 4

4) Simulation

To verify the correctness of the designed full adder, simulation is made on the schematic of design by using ModelSim, the simulation results are shown in Figure 5

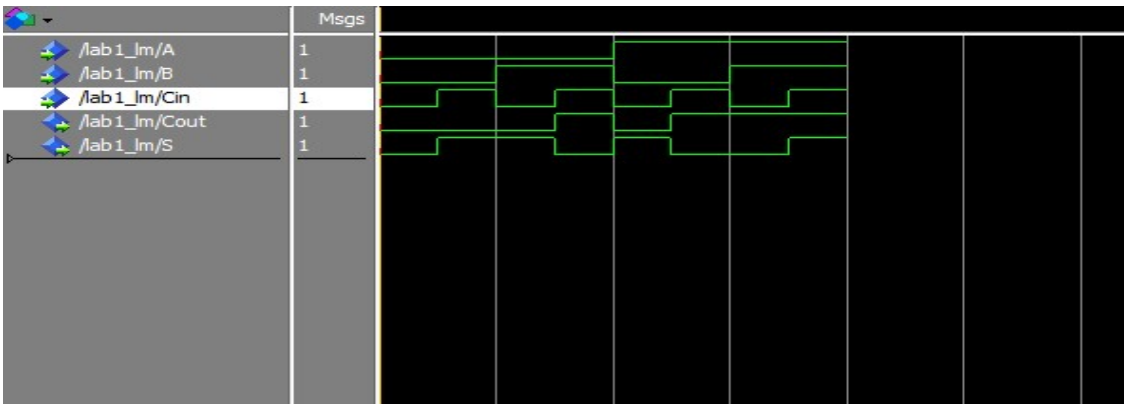

Figure 5

In the Figure 5, for different combination of states of inputs A, B, Cin, the state of outputs S, Cout are agree with the Truth Table (Table 1) , that means that the design of full adder is correct and successful.

5) DE2 board implementation
   Because there were something wrong with the assignment of inputs A, B and Cin to pin SW[0], SW[1] and SW[2], the designed full adder didn't work on DE2 board. The correctness of designed full adder, however, has been verified by the simulation with ModelSim.

Conclusions: (my lab partners and I used two hours to finish the Lab 4)

From the lab 4,

1) I understand Boolean operation and general rules of Boolean operation, understand truth table;
2) Be able to use truth table and Boolean expression to analyze the inputs and outputs of the circuit needed to design;
3) Be able to use general rules of Boolean operation to simply the Boolean expression of circuit and then use the logic gates to realize the circuit's Boolean express;
4) Be able to use Altera Quartus to draw schematic of designed full adder;
5) be able to use ModelSim to make simulate on designed full adder
6) Get familiar with DE2 board, be able to test the correctness of designed circuit using DE2 board.

What I did in Lab 2

1)complete the truth table of full adder;
2)Design the Cout schematic by using Boolean operation and truth table;
3)draw schematic of full adder using software Altera Quartus;
4)make simulation of

What my lab partner did:

1) Cooperate me with check my design and make suggestion to correct it;
2) Help me set up the Altera Quartus and ModelSim;
3) Input the states of inputs according to truth table and make simulation on outputs;
4) Set up the DE2 board, try to cooperate me to figure out the problems with testing design on DE2 board.