



# Managed Runtimes SIG August Meeting

August 24, 2021

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# RISC-V International



RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate.

We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

<https://riscv.org/risc-v-international-community-code-of-conduct/>

# Agenda



- Project updates
  - OpenJ9: Cheng (IBM)
  - OpenJDK(RV32G): Shining(PLCT)
  - WASM(WAMR): Wenyong Huang(Intel)
  - OpenJDK: Kevin(Alibaba)
- Open Discussion
  - V8: community collaboration(Xcalibyte)

# OpenJ9 Update



- Basic RISC-V code generator (OMR JIT component)
- Skeleton with Calling Convention & Inlining guards (in progress)
- Interpreter-to-JIT & JIT-to-Interpreter transitions
- Simple compiled methods (primitive)
- Non-inlined virtual calls (next steps)

# Managed Runtimes SIG: More Info



- Managed Runtimes SIG (under the Software Horizontal Committee)
  - <https://lists.riscv.org/g/sig-managed-runtimes>
  - Mailing list: [sig-managed-runtimes+subscribe@lists.riscv.org](mailto:sig-managed-runtimes+subscribe@lists.riscv.org)
  -
- GitHub
  - <https://github.com/riscv-admin-docs/Managed-Runtimes/>



# Thank You

