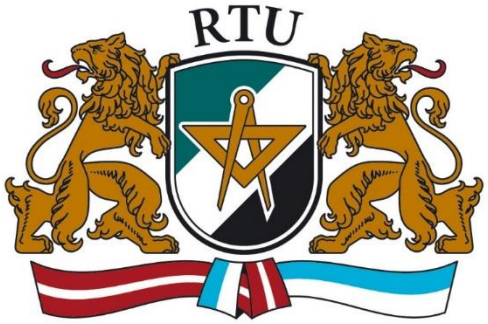

Welcome to RTR532 Functional and Logic Circuit Modelling

- Introduction, course contents
- Digital system design hierarchy
- Recap of basic digital system building blocks
- Introduction to VHDL and FPGA, digital system design flow
- Your first VHDL code

Introduction – academic staff

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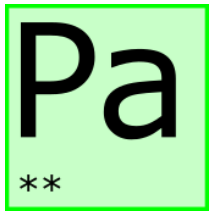
Dr.sc.ing **Gatis Valters**
Laboratory work
gatis.valters@rtu.lv

Course contents

- Functional and logical circuit modelling – 4 credits!
  - 16 lectures (8 meetings total, each 2 lectures)
  - 6 problem sets – 30% of grade
  - 3 labs – **mandatory**
  - Optional research problem – 10% of grade
  - Final project – 70 % of grade

- Design digital functionality circuits
  - Using Simulink, VHDL
  - For FPGA

Problem sets



- 30% of final grade
- Not mandatory but very recommended !
- Short submission deadline (next lecture)
- Published and submitted through Git

Laboratory works

- Lab 1 - Simulink audio compressor
- Lab 2 - FPGA counter (LED's, switches, 7seg LCD)
- Lab 3 – Signal generation and processing with FPGA

All laboratory works have to be passed by the end of May to get a final grade.

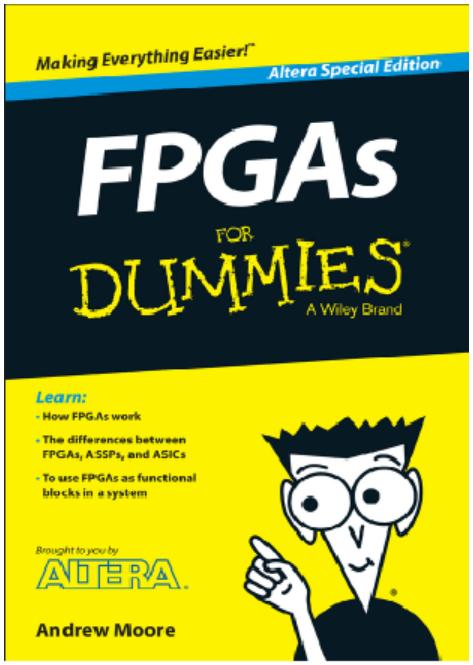
Research problem

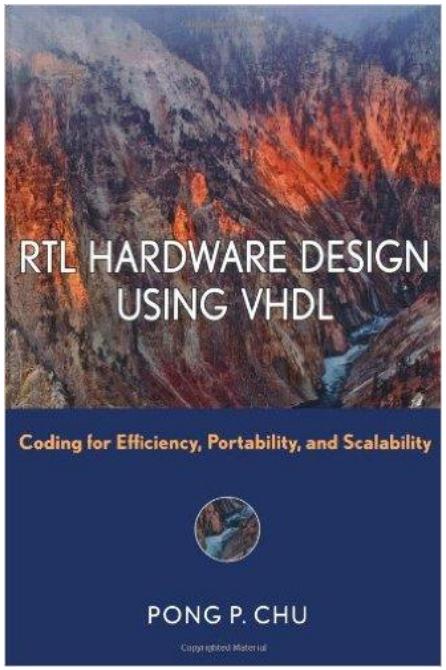
- Optional
- Select an FPGA for a given problem (work with data sheet)
- Tasks to approved till 1st March
- Result:
  - written report (<5pages)
  - presentation (10min) in May.
- 10 % of final grade

Final project

- 70 % of final grade
- Show skills for developing an FPGA project
- Defense (presentation and demo) to take place in June
- Most of the work to be done for the final project

Literature





A.Moore. **FPGAs for Dummies (Altera Special Edition)**. – New Jersey: John Wiley & Sons, 2014. – 52pp.

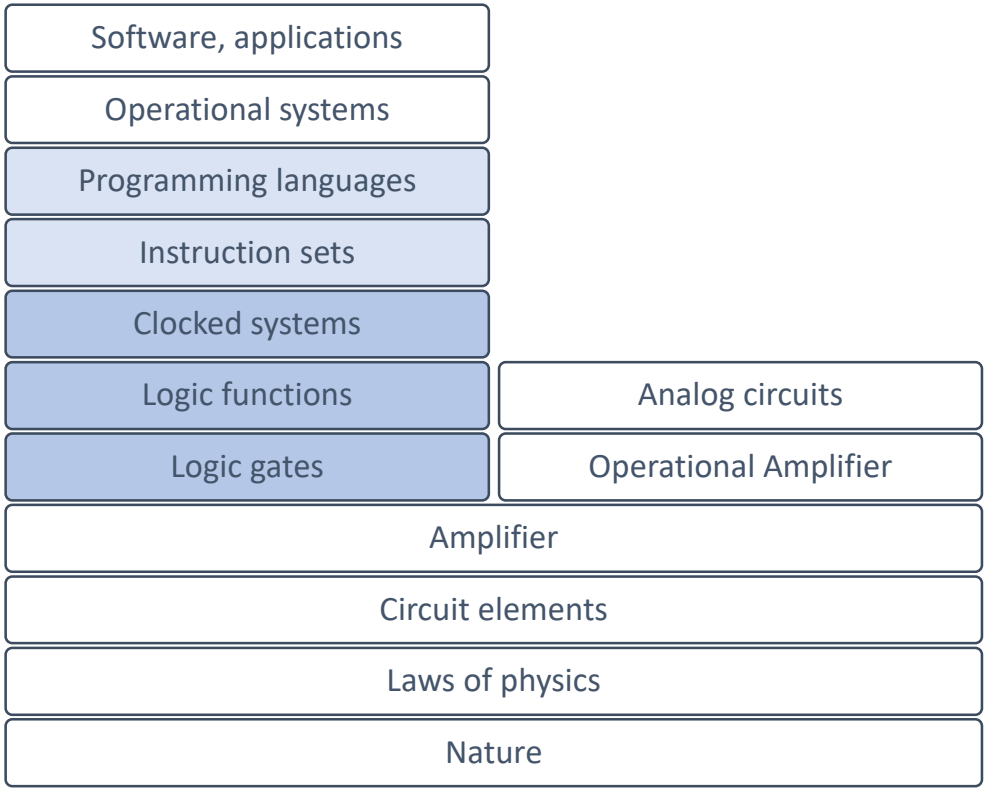
Pong P. Chu. **RTL Hardware Design Using VHDL: Coding for Efficiency, Portability and Scalability**. - Cleveland: Wiley-IEEE, 2006. – 694 pp, ISBN 978-0-471-72092-8

What you will learn?

- Model functional circuits using Matlab Simulink
- How to use VHDL to develop and simulate digital circuits (in Altera Quartus II and ModelSim)
- Develop real projects for FPGA
- How to use DSP and fixed point arithmetics

Digital System Design Hierarchy

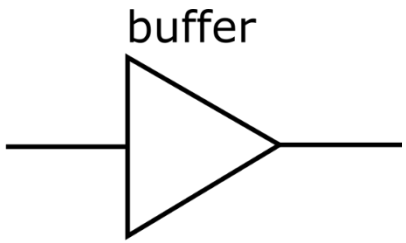
Levels of abstraction

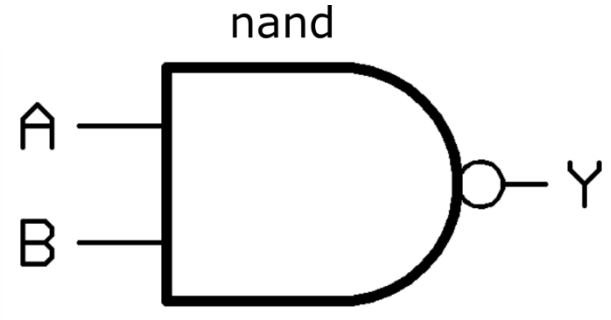


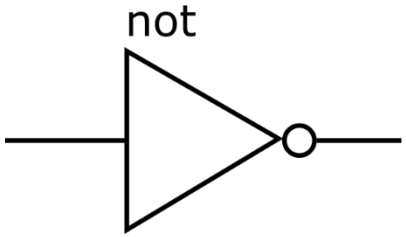
Recap of basic building blocks

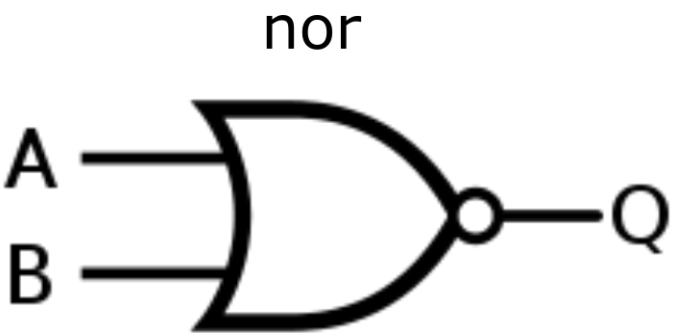
Logic gates

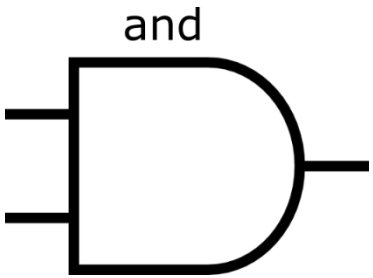
- Yes
- No
- And
- Or
- Nand
- Nor
- Xor

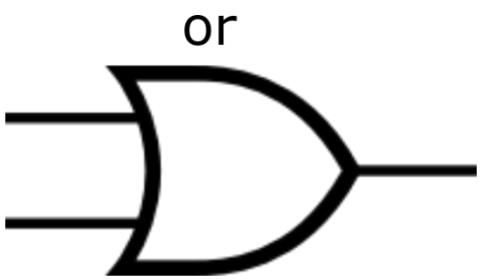


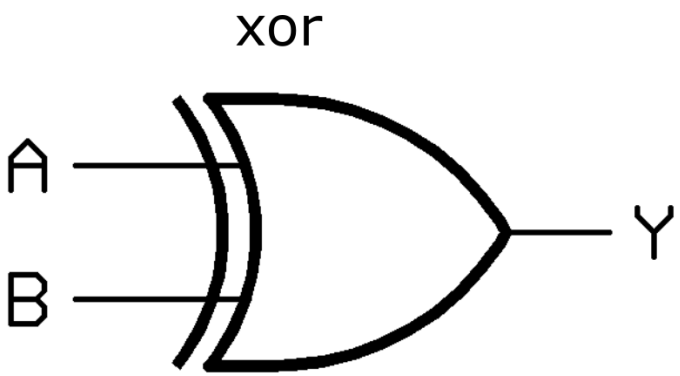








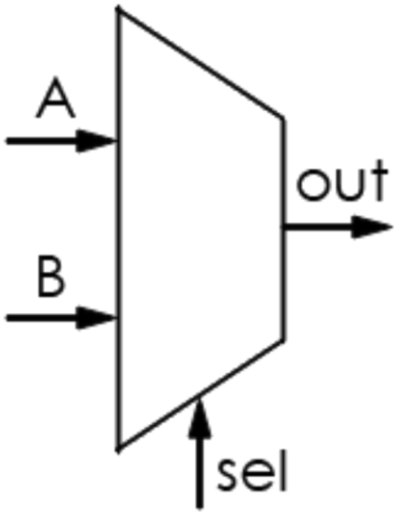




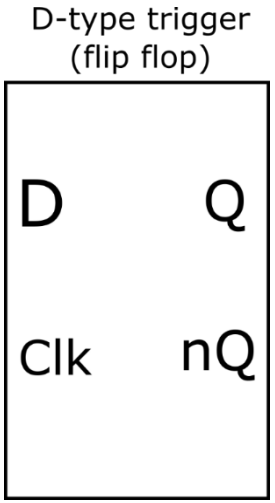
- Task – logic gate truth tables

Logic Functions

- Multiplexer (mux)



- Register (flip-flop, D-type trigger)



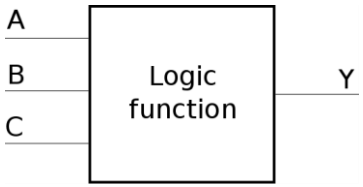
Logic Functions – Look-up Table

- Memory + mux
- Allows to implement ANY logic function (limited by number of inputs)
- https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/wp/wp-01003.pdf

- Task – logic functions truth tables

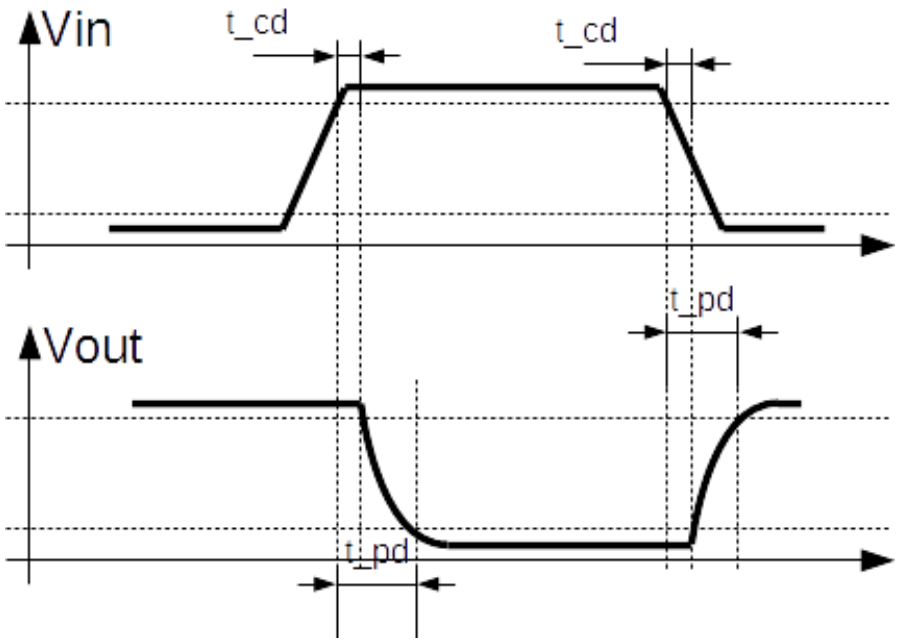
Logic Functions - Definition

- Truth table



A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

- Transient parameters
  - http://www.nileshgoel.com/wp-content/uploads/2010/02/timing-note.pdf



VHDL and FPGA

VHDL

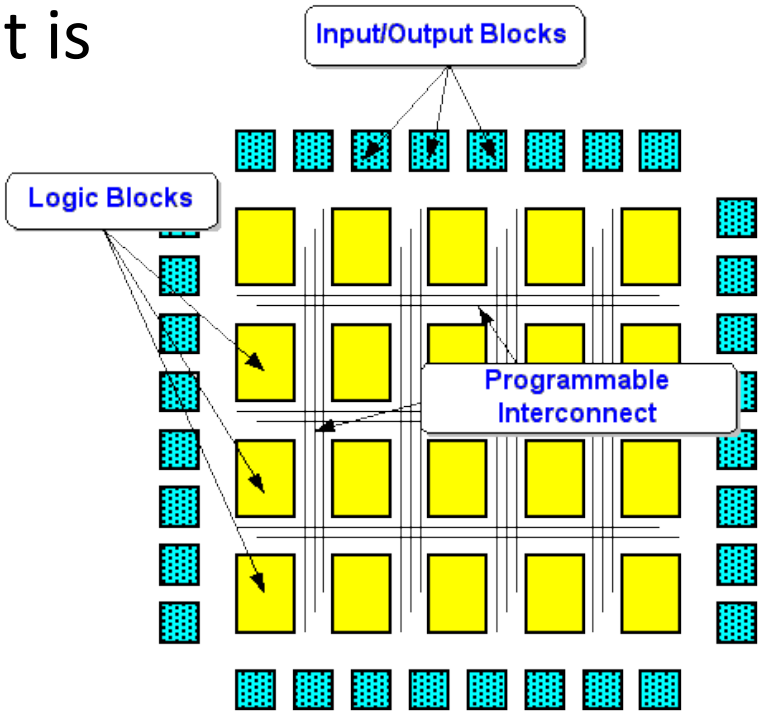
- **Very** high speed integrated circuit **hardware description language**
- Let's you describe functionality of integrated circuit
- HDLs used extensively in industry to design integrated circuits (e.g. newest Intel i7 cpu)
- Knowledge in VHDL opens lot of doors…
- http://esd.cs.ucr.edu/labs/tutorial/

Design integrated circuits with VHDL

- CPLD – complex programmable logic devices
- FPGA – field programmable gate array
- ASIC – application specified integrated circuit
- SoC – system on chip

What is an FPGA?

- Field Programmable Gate Array
- Electronic breadboard that is wired together by an automated synthesis tool
- Built-in components



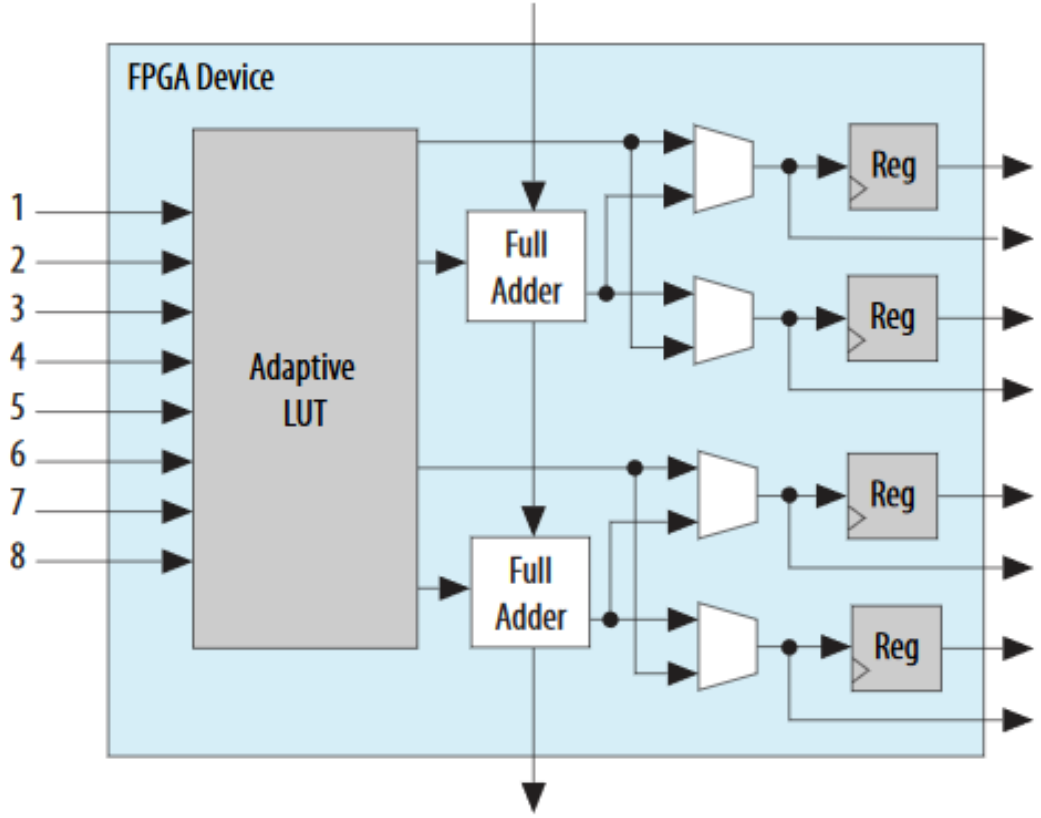
If you look inside FPGA…

You will see:

- Huge number of «Logic elements»
- Signal interconnections
- Clock routing
- Buffers to inputs/outputs
- Several specific modules (dsp, phase locked loop, serdes, othres)

Logic element

- Look up table
- Adder
- Multiplexers
- Registers (**clocked**!)



Cyclone V FPGA logic element

https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/cyclone-v/cv_5v1.pdf (page 1-12)

FPGA pros/cons

Pros:

- Implement any required digital functionality
- High speed / highly parallel
- Reconfigurable functionality
- Lot of inputs/outputs

- Cons:
  - Expensive
  - Power consumption
  - Volatile configuration
  - Development can be complex

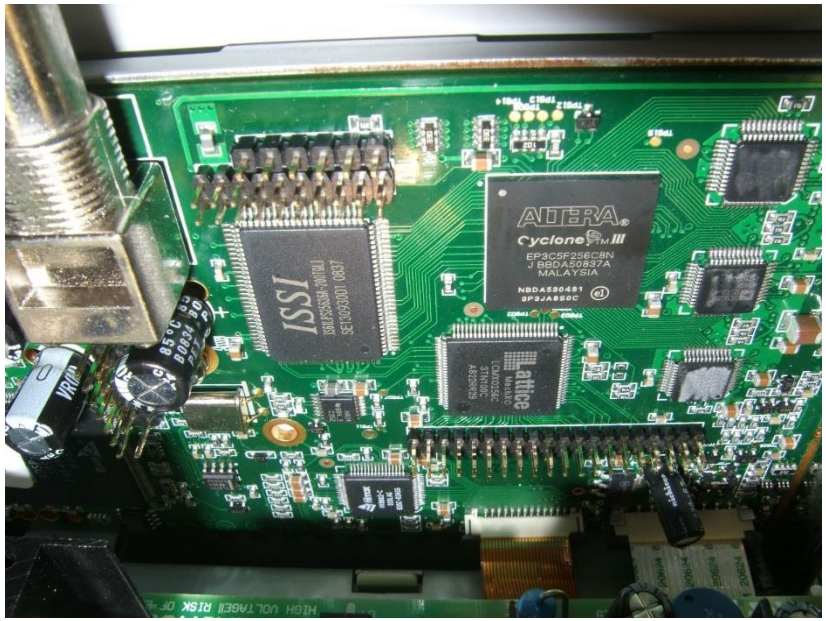
FPGA manufacturers

	Tool chain	Actual FPGA family	Soft processor	Name of basic element
Xilinx	ISE Vivado	Ultrascale, Ultrascale+, Kintex-7 Zynq	MicroBlaze	Logic Cells
Intel (Altera)	Quartus II Quartus Prime	Stratix 10 Arria 10 Cyclone V	Nios	Logic Elements

Other manufacturers – Lattice Semiconductor, Microsemi, SiliconBlue

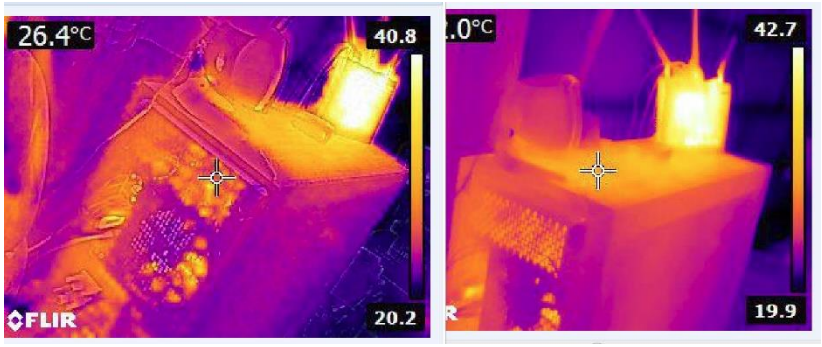
Where are FPGA's used ? Oscilloscopes

- High speed ADC interface
- High speed memory interface
- Picture from Rigol DS1052E



Where are FPGA's used ? FLIR E4

- Parallel image processing



Where are FPGA's used ? LightSpace Technologies X1405 volumetric 3D display (LV)

- DLP projection system interface
- 15+ Gbps data transfer
- Precise timing synchronization

- http://www.lightspace3d.com/

Where are FPGA's used ?
«Curiosity» Mars Scientific Laboratory

- Radiation hardened FPGA
- Remotely reconfigurable
- Used in
  - Landing craft
  - Motor control board

- http://www.xilinx.com/about/customer-innovation/aerospace-and-defense/mars-exploration-rovers.html

Where are FPGA's used in LV?

- Research
  - RTU ETF Institute of Radioelectronics
    - Xilinx 7-series
    - Altera Cyclone II, Cyclone III, Stratix, Cyclone V
  - Institute of Electronics and Computer Science
  - University of Latvia Datorikas fakultāte (undergraduate and graduate courses – digital design)
- Industry
  - SAF tehnika
    - Xilinx ZYNQ,
    - Xilinx Spartan 3e
  - Lightspace Technologies
    - Xilinx Virtex-6
    - Xilinx Spartan-6

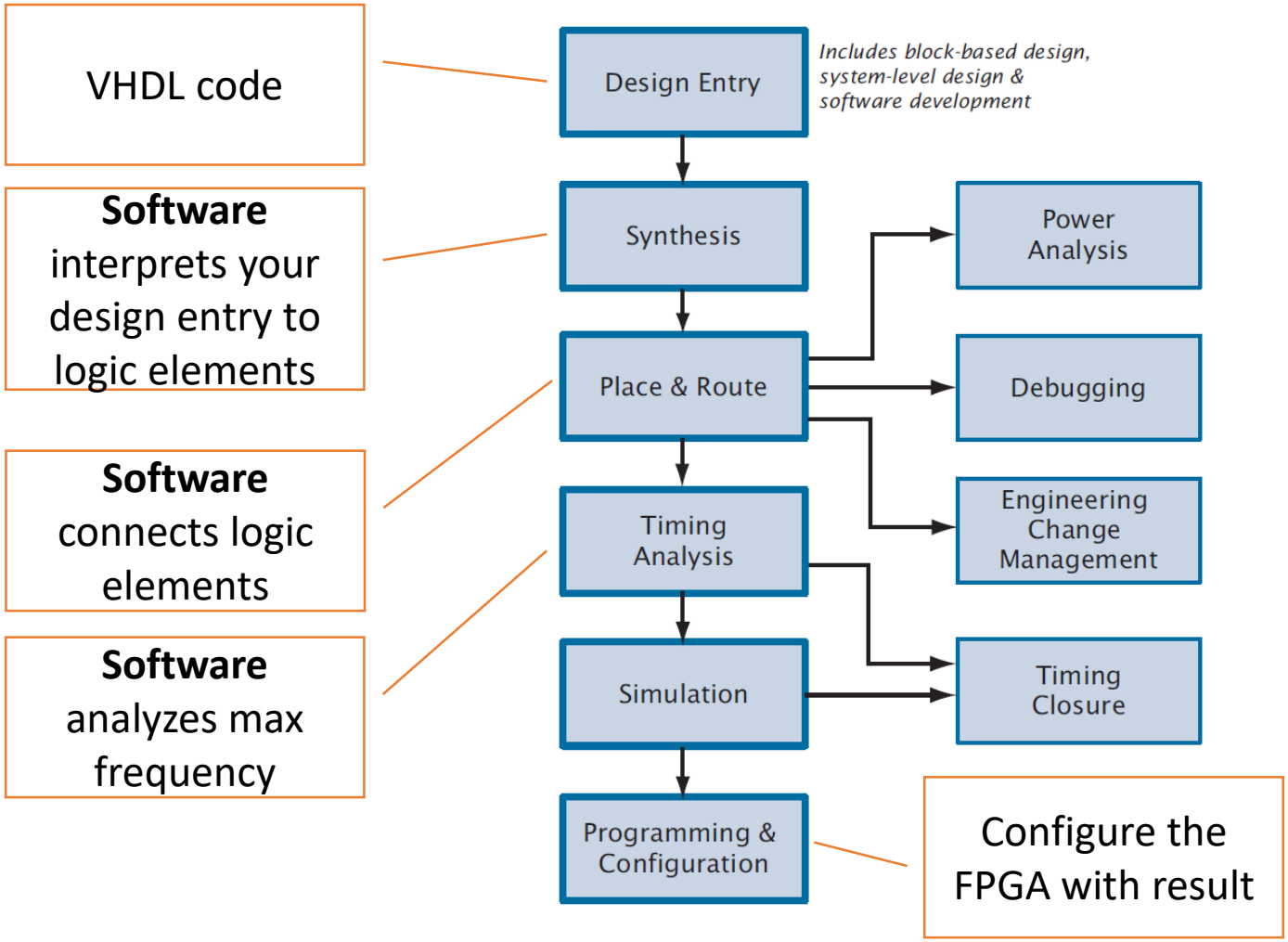
Digital system design flow

We want to somehow «tell» the design software what we want to happen

We use specific Development Tools!

- Tell the functionality by
  - Block diagrams (not used in industry)
  - Hardware description languages
- Translates your code to FPGA digital circuitry
- Simulate and verify the functionality

Digital system design flow



Synthesis

- Input
  - .vhd files
- Output
  - netlist of logic elements, to be used in Place and Route
  - Report on FPGA logic element usage (percents)

Place and Route

- Input
  - netlist of logic elements
  - .qsf settings file (which signals connect to which device i/o pins)
- Output
  - Placed and routed logic elements in FPGA
  - Final report on FPGA logic element usage (percents)

Helpful tools we will use

- Design netlist review
  - Netlist Viewer
  - Technology Map Viewer
- Simulator ModelSim
- Logic Analyzer – **SignalTap II** (on physical FPGA, sends back result through USB)
- FPGA core generators with different functionality

Your first VHDL code

Lets work together and write our first VHDL code

Enough talking, lets get down to business

Please write EMAIL you use so I can invite you to Gitlab

- Useful links
  - www.altera.com
  - www.xilinx.com
  - www.reddit.com/r/fpga
  - MIT 6.004 https://www.youtube.com/playlist?list=PLrRW1w6CGAcXbMtDFj205vALOGmiRc82-
  - MIT 6.111 http://web.mit.edu/6.111/www/f2015/index.html

Lecture Summary

- Remember from this lecture:
  - Look-up table and logic functions
  - What's inside an FPGA
  - Starting VHDL code in Quartus

To do till next lectures:

- Problem set (submit by 2018-02-21 23:59)
- Collect ideas for final project