

RTR532 2018

Problem set #4

Total value - 100 points

Submission deadline – 2018-04-11 23:59

Aim of this problem set – to practice Direct Digital Synthesis in FPGA

Starting notes

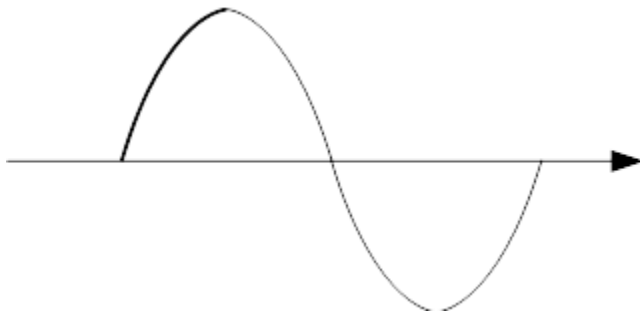
1. Copy the repo `\rtr532-2018\problem_sets\ps04\` contents to your repository (`\repo-student\problem_sets\ps04\`)
2. Remember to commit changes (of .vhd files) to your local repository, before pushing it to the master remote repository.
3. **Problem sets will be graded from your repositories.**

Task 1 – Improve L04 dds_vhdl module (80 / 100 points)

Direct digital synthesizer (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Applications of DDS include: signal generation, local oscillators in communication systems, function generators, mixers, modulators, sound synthesizers and as part of a digital phase-locked loop.

Consider the direct digital synthesis module in lecture 04 ([link](#)).

1. Replace `signal_rom_table` values with **1/4th of sinusoid period**, as shown in BOLD.



2. Set Phase Increment to 1.
3. Add 2b wide `std_logic_vector` input to the entity “control”
4. Control can be sampled (“read”) on reset or on rising edge of clock – your decision.
5. Using FSM or equivalent technique ensure the following output signal form:

control	Output signal form
00	Output fixed to zero
01	
10	
11	

NOTE – Use only the existing `signal_rom_table` (1st step) for output values. You are allowed, as required, define new signals, counters, states, etc. inside the module.

Task 2 – test the modifications (20 / 100 p)

Produce a testbench file that compiles automatically in project (add the link) for long enough time, produce required control signal stimuli to show that for each control input output signal form is as required.