CS6135 VLSI Physical Design Automation

Homework 4: Global Placement

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(2)

testcase	wirelength	runtime	status
public1	71360471	86.39	success
public2	22511175	208.49	success
public3	500884132	376.16	success

(3)

objective function : $\min \sum_{e \in E} c_e \times WL_e(x,y) + \beta \sum_b (D_b(x,y) - T_b)^2$

LSE: $r \sum_{e \in E} (\log \sum_{v \in e} \exp(x_k/r) + \log \sum_{v \in e} \exp(-x_k/r)$
$+ \log \sum_{v \in e} \exp(y_k/r) + \log \sum_{v \in e} \exp(-y_k/r)$

$D_b(x,y) = \sum_{i \in V} c_i \times \theta_x(b,i) \times \theta_y(b,i)$

Input Data

↓

random placement. set Num Iteration (1 50)

↓

for round in 0 ~ 5

beta + 3000

set size bound (width * 0.9).

set module position

Check and adjust out of core

↓

Legalization

↓

Detail Placement

(4) I found that there are total five parameters will affect the data

GlobalPlacer.cpp

`numRounds`

Increasing the number of iterations tends to reduce the wirelength, but it comes at the cost of consuming more time. The diminishing returns in the reduction of wirelength become more apparent as the number of iterations continues to rise.

`no.setStepSizeBound()`

Here we need to set the upper bound for the step size. Although I cannot see how the step size operates later, after testing, I found that a step size is not ideal that whether it is too large or too small. I believe that the step size should

generally be smaller than the target. Therefore, I have adjusted this part to be 0.9 times the size of the placement.

Examplefunction.cpp

R

A larger value of 'r' indicates a more concentrated distribution of modules. In other Log-Sum-Exp, a larger 'r' means a more confident selection of a category. Conversely, a smaller 'r' allows the model to achieve a more uniform distribution.

binNumPerEdge

If 'binNumPerEdge' is too large, it may result in bins being subdivided into excessively small parts, ineffectively to reduce wirelength within each bin significantly. If the number of bins after subdivision is too small, the final result may not be legalization.

(5)

Rank	public1	Public2	Public3
4	73804994	11105419	413161709
5	80176617	10921603	539864787
My result	71360471	22511175	500884132

My public1 is better than rank 4 and public3 is better than rank 5. When adjusting parameters, I observed that reducing both 'r' and 'binNumPerEdge' tends to result in lower wirelength, given that the configuration remains legal. Increasing the number of iterations also helps bring the placement closer to optimization. For 'StepSizeBound,' a range between 0.9 and 1.1 of the width seems to yield optimal results. Values that are too large or too small can lead to suboptimal outcomes.