Report

Your report should at least contain the following contents.

(1)

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(2) A comparison table like the following one, and an explanation of the result (The table should be built under a fixed core utilization and clock period and you should specify them in the report.)

	(congestion-driven, timing-driven)					
	(L,off)	(L,on)	(M,off)	(M,on)	(H,off)	(H,on)
slack	0.206	0.361	0.232	1.246	0.114	1.246
Total wire length(nm)	108183.56	103200.76	108212.70	102711.97	108213.64	102711.97

Result:

timing-driven on 的 total wire length 會比 off 短

timing-driven off 的 slack 會比 on 小

(3) The difference(s) between the congestion-driven placement and timing-driven placement

- timing-driven 基於時序驅動進行的 placement，大部分設計需要做 time driven 的 placement 優化。
- Congestion-driven 基於 congestion 優化的 placement，place 的過程 tool 會通過 global route 來估算 design 的繞線情況，根據估算的 congestion 來進行 placement 的優化。

timing-driven 盡量在布局階段滿足需求，減少後續時序優化工作，Congestion-driven 在布局中解決問題，提高性能，兩種方法可以依照設計需求和目標來選擇，也可以結合使用。

(4) An explanation of why we insert filler cells

- 可以提高 planarity，IC 製造的過程中可能會有不同材料厚度不均造成表面不平整，可能會影響晶片性能，經過策略性填充可以改善平面度
- 減少由 N-Well、PPlus、NPlus 造成的 DRC Error，有助於保持電源軌、VDD/VSS 連接的連續性
- 可以實現電源、接地和 N-well 的連續性，如果沒有 filler cell 可能會出現 N-well 或是 DRC Error

(5) Show your best result (including clock period, total area of chip, total wire length, slack, congestion-driven effort and timing-driven on/off setting, and their snapshots) to maintain a non-negative slack and no DRC violation.

- including clock period

```
create_clock [get_ports clk]  -name CLK  -period 1.7  -waveform {0 0.85}
```

- total area of chip

```
============================
Floorplan/Placement Information
============================
Total area of Standard cells: 8954.092 um^2
Total area of Standard cells(Subtracting Physical Cells): 8954.092 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 12768.000 um^2
Total area of Chip: 14697.883 um^2
```

- total wire length

```
============================
Wire Length Distribution
============================
Total metal1 wire length: 2938.2250 um
Total metal2 wire length: 27443.4600 um
Total metal3 wire length: 39291.7400 um
Total metal4 wire length: 17997.0600 um
Total metal5 wire length: 8592.2450 um
Total metal6 wire length: 6449.2400 um
Total wire length: 102711.9700 um
Average wire length/net: 14.3392 um
```

- congestion-driven effort and timing-driven on/off setting

congestion-driven=>High

timing-driven=>on

```
setPlaceMode -congEffort low -timingDriven 0 -clkGateAware 1 -powerDriven 0 -ignoreScan 1 -reorderScan 1 -ignoreSpare 0 -placeIOPins 1 -
moduleAwareSpare 0 -preserveRouting 1 -rmAffectedRouting 0 -checkRoute 0 -swapEEQ 0
```

- slack

```
Path 1: MET Setup Check with Pin randomize/data_out_reg_24_/CK
Endpoint:   randomize/data_out_reg_24_/D (^) checked with  leading edge of 'CLK'
Beginpoint: sequencer/round_reg_1_/Q     (^) triggered by  leading edge of 'CLK'
Path Groups: {CLK}
Analysis View: generic_view
Other End Arrival Time          0.000
- Setup                         0.086
+ Phase Shift                  10.000
= Required Time                 9.914
- Arrival Time                  8.667
= Slack Time                    1.246
```

- DRC violation

```
#-check_same_via_cell true              # bool, default=false, user setting
 *** Starting Verify DRC (MEM: 3814.3) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
**WARN: (IMPVFG-1198):  The number of CPUs requested 8 is larger than that verify_drc used 4. In Multithreading mode, the number of CPUs
verify_drc used is not larger than the number of subareas.
 Use 'setMultiCpuUsage -localCpu' to specify the less cup number if the verify area is not large.
  VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.000 0.000 61.560 60.480} 1 of 4  Thread : 1
 VERIFY DRC ..... Sub-Area: {61.560 0.000 122.360 60.480} 2 of 4  Thread : 1
 VERIFY DRC ..... Sub-Area: {0.000 60.480 61.560 120.120} 3 of 4  Thread : 1
 VERIFY DRC ..... Thread : 3 finished.
 VERIFY DRC ..... Sub-Area: {61.560 60.480 122.360 120.120} 4 of 4  Thread : 1
 VERIFY DRC ..... Thread : 1 finished.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.9  ELAPSED TIME: 1.00  MEM: 0.0M) ***
```

(6) Show the final chip layout of your best result generated by Innovus (use print-screen to save the final layout and paste on the report)