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HW #5 — Caches and Memory

due 4/12 @ 5pm

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(1) Write-through caches are usually also write-no-allocate because there isn't an advantage to bringing the data at the missed-write location because the write through policy will write to memory on subsequent writes anyway. Since write-through writes to main memory on write hits and write misses, there is no benefit to bring the block of data into the cache on write misses because it'll have to go back there anyway later.

(2) Average memory latency

$t_{avg} = t_{avgL1}$

$t_{avgL1} = t_{hitL1} + (\%\ miss_{L1} \cdot t_{missL1})$

$t_{missL1} = t_{avgL2} =$

$t_{avgL2} = t_{hitL2} = 20ns$

$t_{avg} = 3 + (.10 \cdot 20)$

$\boxed{t_{avg} = 5\ ns}$

L1 cache access latency = $t_{hitL1} = 3ns$ — $\%_{hitL1} = .90$ — $\%_{missL1} = .10$

L2 cache access latency = $t_{hitL2} = 20ns$ — $\%_{hitL1} = 1$ — $\%_{missL2} = 0$

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(3) 64-bit machine, 4GB physical memory, page = 64 KB

↳ $2^2 \cdot 2^{30}$ bytes = $\boxed{2^{32} \text{ bytes}}$

↳ $2^6 \cdot 2^{10}$ = $\boxed{2^{16} \text{ bytes}}$

(a) How many virtual pages per process?

on a 64-bit machine, each process has 2^{64} bytes of virtual memory.

$$2^{64} \text{ bytes} \times \frac{1 \text{ virtual page}}{2^{16} \text{ bytes}} = \boxed{2^{48} \text{ virtual pages}}$$

(b) How many physical pages?

4 GB physical space = 2^{32} bytes

$$2^{32} \text{ bytes} \times \frac{1 \text{ page}}{2^{16} \text{ bytes}} = \boxed{2^{16} \text{ physical pages}}$$

(c) In a translation from a virtual address to a physical address, how many bits of VPN are you mapping to how many bits of PPN?

number of virtual pages = 2^{48}

number of VPN bits = 64 - 16 = 48 bits

number of physical pages = 2^{16} pages

number of PPN bits = 16 bits

(d) How big does a PTE need to be to hold a single PPN?

PPN = 16 bits = 2 bytes

(e) How many PTEs (size above) fit on a page?

$$\frac{\text{size of page}}{\text{size of PTE}} = \frac{2^{16} \text{ bytes}}{2^{1} \text{ bytes}} = 2^{15} \text{ PTEs}$$

(f) How many pointers fit on a page?

Pointer on a 64-bit machine = 8 bytes

$$\frac{\text{size of page}}{\text{size of pointer}} = \frac{2^{16} \text{ bytes}}{2^3 \text{ bytes}} = \boxed{2^{13} \text{ pointers}}$$

(g) How big would a flat page table be?

number of pages · entry size =

$$2^{48} \cdot 2^1 \text{ bytes} = \boxed{2^{49} \text{ bytes}}$$

(h) What are the virtual page offset bits for virtual address 25012?

What are the physical page offset bits for virtual address 25012 after it has been translated?

25012_{10} = 0 ... 0 0 1 1 0 0 0 0 1 1 0 1 1 0 1 0 0

63 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Page offset = $\log_2$ (page size in bytes) =

$\log_2(2^{16}) = 16$ bits

Virtual page offset bits = 0110000110110100

physical page offset bits don't change

physical page offset bits = 0110000110110100

(i) Does a TLB miss always lead to a page fault?

Not always. If the TLB misses but the PTE can be found in the page table, then there is no page fault.