Solar Pump Controller

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1. ABSTRACT

This project uses a PSOC mixed-signal array to control a three-phase motor drive, capable of operating a submersible water pump directly from solar panels. The PSOC is responsible for 3ϕ PWM generation, signal conditioning, over-current and fault protection, temperature monitoring, constant voltage-to-frequency control, and maximizing the power from the solar array.

2. INTRODUCTION

Solar powered pumps are used in remote areas to provide ground water, where conventional power may not be readily available. As low-cost submersible pumps operate from three-phase power, the DC from the solar panel must be converted to AC using an inverter. The main components of the inverter are the control and power stages.

The PSOC is used extensively to implement the control section, reducing it to a single chip. As shown in the block diagram in Figure 1, the PSOC is connected to DIP-switch inputs for system configuration, LED status outputs, analog feedback signals from the power stage, and digital drive signals to the power stage.

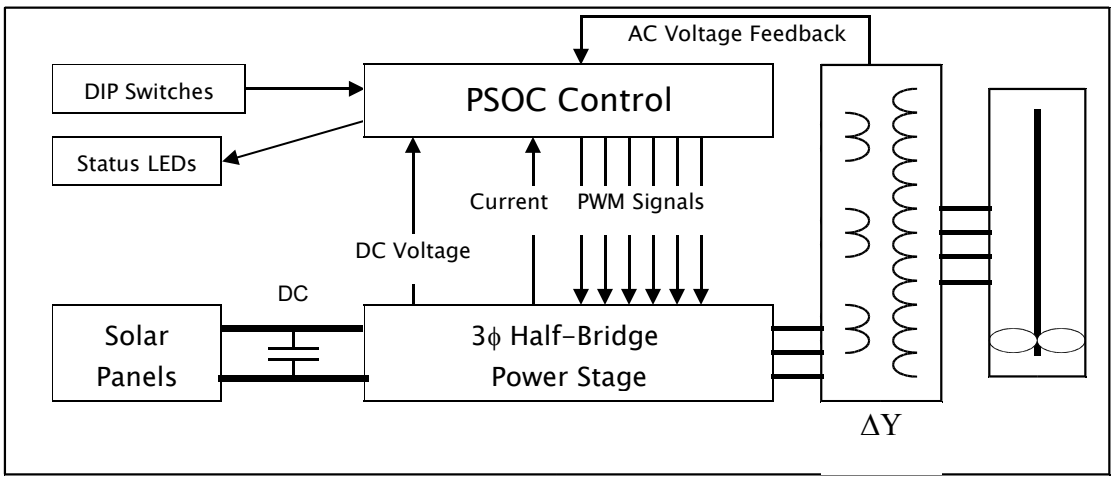

Figure 1. System Block Diagram

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The power stage consists of three-phase MOSFET/IGBT driver ICs, which are connected to an integrated three-phase MOSFET module. The topology is a hard-switched buck converter, with the solar panels connected directly to the power stage, and a three-phase delta-wye transformer responsible for generating the $230V_{nom}$ line-to-neutral voltages for the submersible pump motor.

3. DESIGN DETAIL

3.1 Resource Requirements

Device	CY8C27443
Flash	7K
Analog Inputs	8 pins
Analog Outputs	3 pins
GPIO	13 pins
CPU Utilisation @ 24 MHz	~70 %
RAM	101 bytes
Stack Space	< 16 bytes
Global Inputs	0 bus lines
Global Outputs	6 bus lines
Analog PSOC Blocks	9 blocks
Digital PSOC Blocks	8 blocks
Switching frequency	5859 Hz
Dead time	2 μs
AC Voltage Measurement Error	±8 V
DC Voltage Measurement Error	±2 V

3.2 System Architecture

The pump inverter design consists of three principle blocks: the inverter waveform generator, the analog signal acquisition, and the over-current detector. The elements that make up these blocks consist of hardware and software elements, as shown below in figure 2.

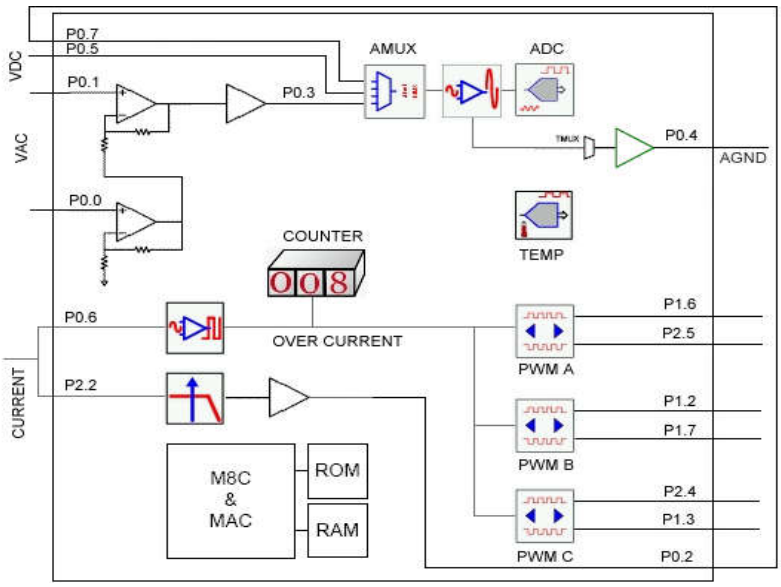

Figure 2. PSOC Internal Block Diagram

The inverter generates a three-phase composite waveform, and controls the motor of the pump using the fixed voltage-to-frequency-ratio motor control technique. This technique maintains a constant AC output voltage, which is directly proportional to the AC frequency of the inverter. Therefore, lower AC frequencies result in lower AC output voltages, maintaining a constant flux in the pump motor and maximizing its efficiency.

The output frequency is controlled to maximize the power drawn from the solar array. By increasing the output frequency, the power drawn by the pump motor also increases, thus increasing the current drawn from the solar array. As shown in figure 3, a solar panel has a non-linear relationship between output voltage and current. A maximum power operating point can be set by varying the pump frequency.

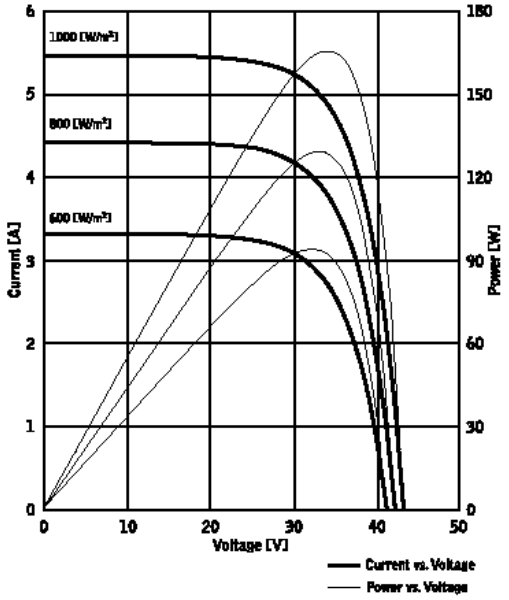

Figure 3. Voltage vs Current for a typical solar panel

The other main block is the over-current detector, which compares the instantaneous primary current to a maximum level, and kills the inverter output if this level is exceeded. If the condition persists for a period of time, the inverter is shut down completely and restarted after a predetermined period.

3.3 Hardware Architecture

3.3.1 Inverter Waveform Generator

The inverter waveform generator is responsible for directly controlling the switching action of the inverter power stage. As indicated previously in figure 1, the inverter power stage converts the DC coming from the solar array into three-phase AC, suitable for driving

the pump motor. It does this using three half-bridge MOSFET switches, one for each phase. The switches are modulated at the switching frequency, using the pulse-width modulator (PWM) blocks of the PSOC. Additionally, the internal dead-band generator is used to precisely time the break-before-make interval on the half-bridge. This delay is required to allow the switch time to turn off before the complementary switch is turned on.
Three of the PWMDB8 blocks are used, one for each phase, and the top and bottom switch are connected to phase-1 and phase-2 respectively.

3.3.2 Analog Signal Acquisition

The pump inverter monitors three analog signals; the AC voltage, the DC array voltage and a course representation of the DC current. A sigma-delta 8-bit ADC is used, operating at a sampling frequency of 11718 Hz. This uses the internal bandgap reference voltage range of 1.3±1.3V. The 1.3V analog ground is provided on the P0[4] pin, allowing it to be fed to external scaling circuitry to offset incoming signals. The input to the ADC is connected to a programmable gain amplifier (PGA) block, configured as a voltage-follower to provide a high impedance input. This amplifier is connected to a 4:1 multiplexer, which selects the input channel to the ADC.

The AC voltage signal is taken from one of the phases of the motor, and is measured from line-to-neutral. This has the nominal value of 230 V_{rms}, or 325 V_{peak}. A peak measurement value of 400 V is chosen to provide some headroom for excessive voltages. This is scaled down to the internal reference range of ±1.3V using a divider network. An additional parallel capacitor is added to provide a single-pole RC filter to provide a roll-off before the sampling frequency of the ADC. An instrumentation amplifier PSOC block is used to process the signal coming onto the IC, as it is not referenced to supply ground and requires a differential amplifier. The output from the amplifier is fed directly to the analog multiplexer via P0[3].

The DC array voltage input is referenced to supply ground, and has a maximum value of 100V. This allows for a simpler single-chain

resistive divider to be used, and it can be directly fed to the multiplexer via P0[5].

The DC current is sensed using the MOSFET drain-source voltage drop when it is turned on. As voltage drop in a MOSFET is equal to the drain-source current multiplied by the Rds-on resistance, the DC current can be inferred from this measurement. The maximum-value of the three half-bridges currents is selected using a series of parallel diodes. A switched capacitor low-pass filter PSOC block is used to pre-process the signal to reduce the switching frequency components. The signal comes into the filter on pin P2[2] and is passed out to the ADC multiplexer on P0[7].

3.3.3 Over-Current Detector

In addition to measuring the maximum DC current using the ADC, it is also monitored for excessive levels. This monitoring is done using a programmable threshold comparator block, which is directly connected to the incoming analog signal via pin P0[6]. The output from the comparator is used to disable the PWM generators using the dead-band kill function, which allows for high-speed shutdown without intervention from the main processor. The synchronous shutdown mode is used, killing the remaining switching cycle and restarting the PWM generation on the next cycle.

In addition to instantaneously shutting down the inverter waveform, the comparator output pulses are also accumulator using an 8-bit counter block. This counter is used to inform the software of a persistent over-current condition, which is flagged when it reaches its terminal count. The counter is periodically reset by the software, to prevent counting of spurious pulses.

3.3.4 Software Architecture

Figure 4 depicts the main software components of the pump inverter. The system is implemented using a combination of interrupts for handing the time critical events, a background polling algorithm for the ADC measurements, and a non-pre-emptive task scheduler, which is triggered at the voltage zero crossing of the waveform generator.

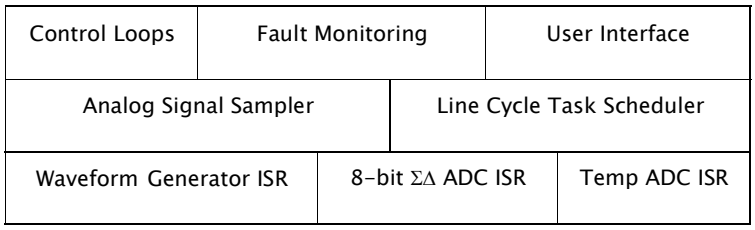

Figure 4. Software Block Diagram

3.3.5 Interrupt Processing

Interrupt service routines are used to handle the time critical events in the system. There are three main interrupt sources:

- The PSOC 8-bit sigma-delta ADC interrupt service routine. The ADC samples at a frequency of 10416 Hz. The ADC samples are intercepted and processed by the foreground thread.

- The inverter three-phase waveform generator interrupt service routine. This operates at the switching frequency of 5859 Hz, and generates a composite waveform of pre-programmed gain and frequency.

- The internal temperature sampling interrupt service routine. This uses a relatively slow 166 kHz clock to minimize the CPU loading, and is triggered once per second to infer ambient temperature of the sealed pump inverter cabinet.

3.3.6 Background Tasks

The background tasks are broadly split between the ADC sample processing and the periodic tasks, which are synchronized to the voltage zero crossing. These periodic tasks run at a variable frequency between 25 and 65 Hz.

A finite state machine is used to interleave the periodic tasks with the ADC sample processing, to minimize jitter to the measurements.

The ADC sample processing algorithm triggers whenever the ADC completes a sample, and is responsible for controlling the analog multiplexer and cycling through the AC voltage and DC voltage and current channels. The DC measurements are filtered using an accumulator, which is reset after each line cycle. The AC samples are used to compute the RMS voltage, by squaring and accumulating 16 samples per line cycle.

The finite state machine is responsible for scheduling the following tasks:

- Dividing the DC voltage and current accumulators by the number of samples taken over the previous line cycle, to give the average DC voltage and current over the previous line cycle. The integrators are also reset.

- Dividing the AC voltage accumulator by the number of samples taken, and computing the square root of the result to give the RMS voltage.

- Computing the target AC voltage based on the inverter frequency and the selected voltage-to-frequency ratio.

- Adjusting the instantaneous gain of the waveform generator to regulate the AC voltage to the target AC voltage using a feedback controller.

- Monitoring the DC voltage, and shutting the inverter down if it is less than 39 V.

- Monitoring the over-current pulse accumulator, and shutting down if an overflow has occurred. If no overflow has occurred, the pulse accumulator is reset for the following line cycle.

- Adjusting the instantaneous inverter frequency to maintain a target DC bus voltage.

- Monitoring for the dry run condition, which occurs when the DC bus voltage cannot be reduced through increasing the inverter frequency.

- Ensuring the internal IC temperature is within a safe operating range.

- Scanning the DIP configuration switches, and adjusting the system configuration accordingly.

- Controlling the status LEDs to reflect the fault monitoring status, and system operation mode.

- Restarting the system if it has shutdown due to a fault condition, and that fault no longer exists for a predetermined period of time.

- Periodically turning off the pump, and measuring the panel open-circuit voltage to determine the maximum power operating point.

3.3.7 PSOC Designer Configuration

The pump inverter only uses one primary configuration, called ‘pump’. A secondary ‘Agnd’ configuration is used to provide an overlay for the PGA block, to output the AGND voltage to an external pin via the P0[4] analog buffer.

Configuration Name	User Module Instance	User Module Base Type
Pump	ADC	DELSIG8
	AMUX4_1	AMUX4
	Amp_Vac	INSAMP
	Count_I	Counter8
	FlashTemp_1	FlashTemp
	LPF2_I	LPF2
	Limit_I	CMPPRG
	PGA_1	PGA
	PWM_PH_A	PWMDB8
	PWM_PH_B	PWMDB8
	PWM_PH_C	PWMDB8
AGnd	RefAGnd	RefMux

Table 1. PSOC Configurations and blocks used

3.3.8 PSOC Global Parameters Settings

Parameter	Setting
CPU Clock	24 MHz
VC1	9
VC2	16
VC3	SysClk1 / 16
Analog Power	SC On / Ref High
Ref Mux	Bandgap ± Bandgap
OpAmp Bias	Low
ABuf Power	Low
Supply Voltage	5.0 V
Inline MAC	Disabled
Math Optimisation	Enabled

Table 2. Global parameter settings

3.3.9 Waveform Generator

The waveform generator interrupt is responsible for generating the three-phase sinusoidal waveform for the power stage of the inverter. It does this by triggering at each terminal count of PWM-A, corresponding to the start of each switching period. The generator steps through a 360-degree lookup table containing a normalized composite sine wave, at a variable phase velocity proportional to the desired frequency, given by the formula:

Phase Velocity = N * Fl / Fs

where

N = Entries in lookup table (256)
Fs = Switching frequency (5859 Hz)
Fl = Line frequency (25-65 Hz)

A phase position variable is employed for all three PWM generators, by accessing the lookup table at offsets of 0, 120 and 240 degrees.
The sine wave values are stored in a normalized form, with the 0...127 representing 0...100%.
The sine wave values for the three phases are multiplied instantaneously by the output gain of the inverter, using the MAC unit of the PSOC. The resultant values are then loaded directly into the PWM duty cycle registers.
The output gain also has a range of 0..127, corresponding to 0...100% rated voltage output.

3.3.10 AC Voltage Regulator

The output gain of the waveform generator is controlled using a simple, closed-loop integral regulator. This regulator ensures that the AC RMS line-to-neutral voltage is maintained to the required voltage

to ensure the correct voltage-to-frequency ratio. This regulator runs every line cycle. The governing control equation is

Output gain += (Target V_{ac} – Measured V_{ac}) * I_{gain}

The Target V_{ac} is calculated based on the inverter frequency and the V/F ratio. The V/F ratio is set using the configuration DIP switches on the pump inverter. The table below shows DIP-switch combinations and the resultant V/F ratios.

Nominal Frequency	Frequency Boost	Resultant V/F Ratio (L-N)
50	0	4.6
50	+5	4.1
60	0	3.8
60	+5	3.5

Table 3. AC Frequency Regulator settings

The AC frequency of the inverter is varied to maintain a constant DC solar array voltage. This is also controlled using a simple closed-loop integral regulator, which runs every line cycle. The governing control equation is:

Frequency -= (Target V_{dc} – Measured V_{dc}) * I_{gain}

The target V_{dc} is set by the maximum power point tracking algorithm.

3.3.11 Primary Current Filter

A second-order low-pass PSOC filter block is used to filter the current signal from the power stage. This signal contains harmonics of the switching frequency, which are attenuated using a butterworth filter with its 3dB frequency set to 5kHz. This frequency also conveniently allowed the ADC clock to be reused to operate the filter block. Additional filtering is done in software, using an integrate-and-dump accumulator, which operates takes the average if 16 samples every line cycle.

3.3.12 Maximum Power Point Algorithm

The maximum power point algorithm adjusts the regulated DC bus voltage, to extract the maximum amount of power from the solar array. The maximum power for a 48V nominal array is extracted when the DC bus equals 67V, however this is quoted with a panel temperature of 25°C. The voltage typically changes by -0.32V/°C as the panel temperature rises. A simple technique to monitor the maximum power point voltage is to periodically disconnect the load, and measure the open-circuit voltage. The maximum power-point DC voltage can be extrapolated by multiplying the open-circuit voltage by 0.6-0.8. For the solar controller, a value of 0.7 is used, and the measurement is taken every 30 minutes. i.e.

Target V_{dc} = Open-circuit V_{dc} * 0.7

4. SCHEMATICS

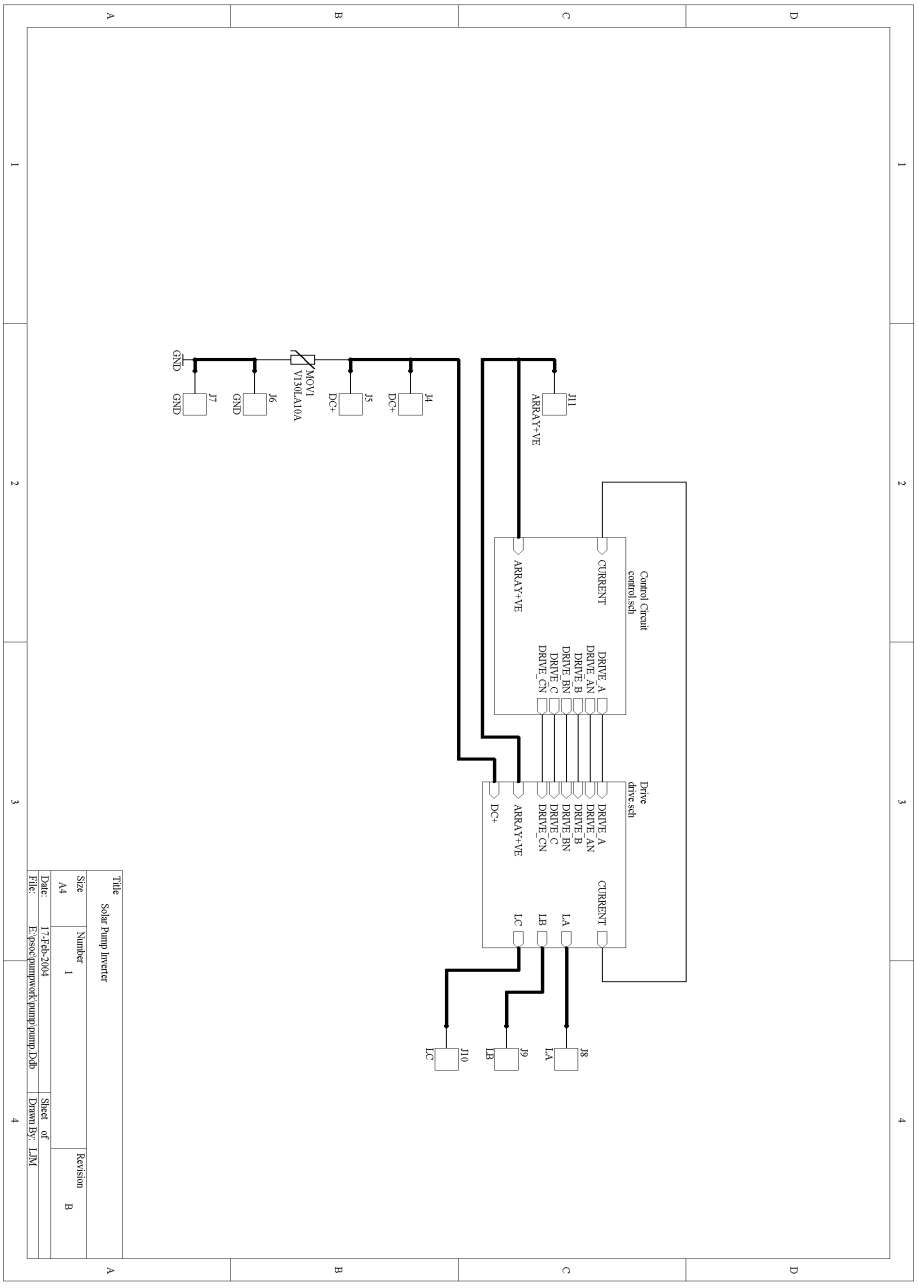

Figure 5. Top-level connection schematic

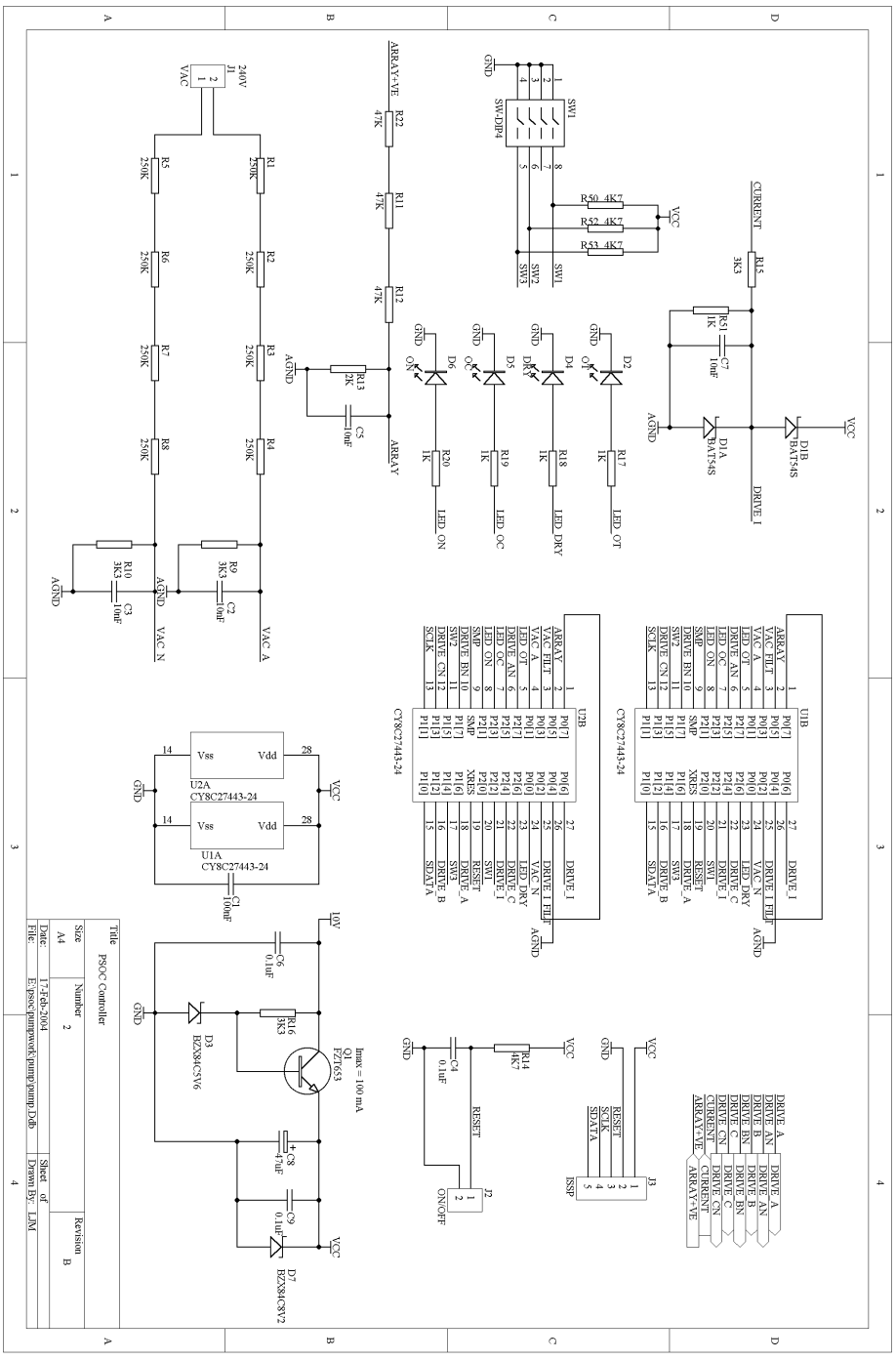

Figure 6. PSOC controller (through hole and SMD) and power supplies

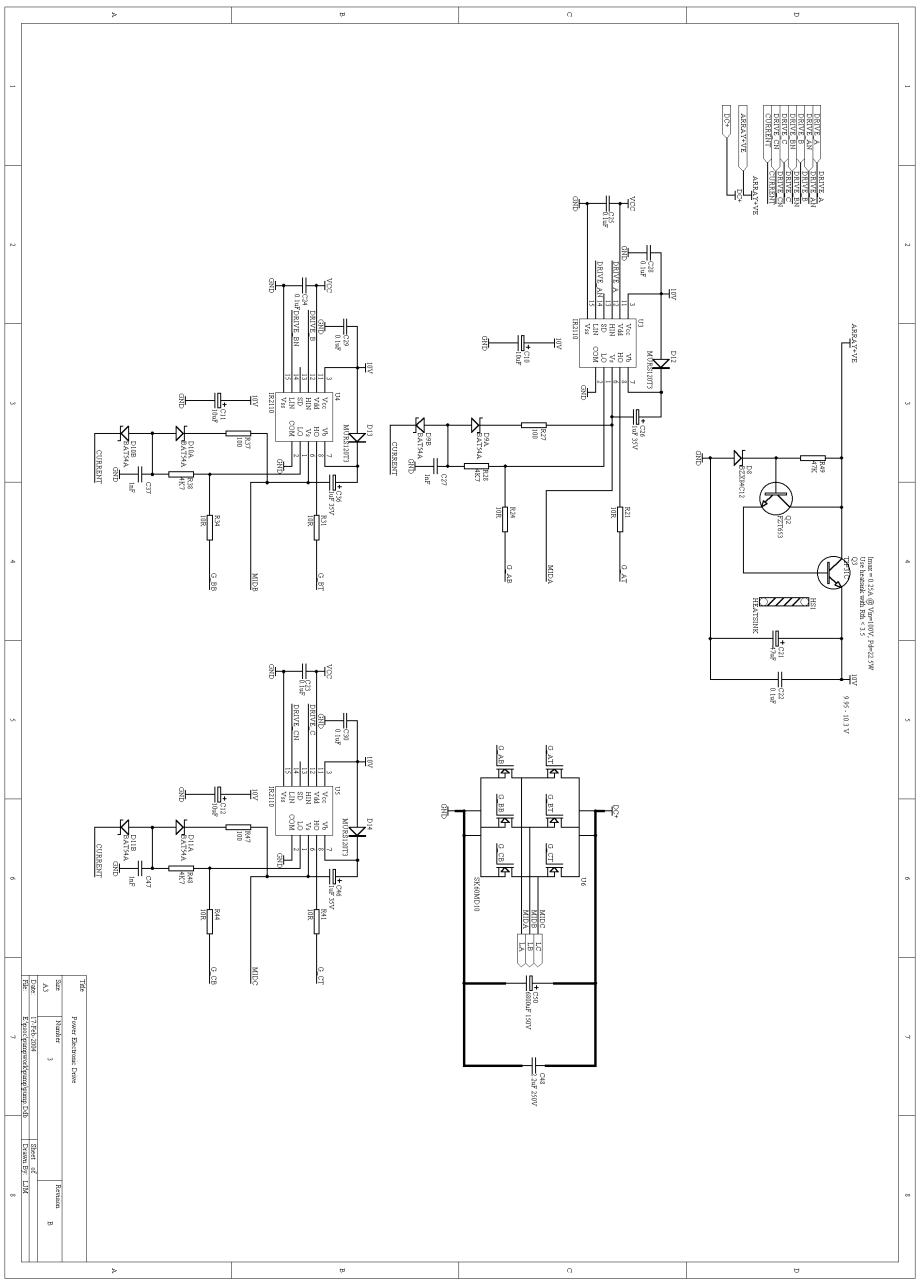

Figure 7. Power Stage

5. PHOTO

Figure 8. Prototype PCB

(Power stage left, PSOC right bottom, power-supply right top)