	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0												
1	OP SIZE	OPER	RANE)		OPER	AND	MOVE					
2	OPCODE	REG		MOD		OPER	AND	ADD, AND, CHP, SUB					
3	OPCODE	REG		OP		OPER	AND	CHK, DIVS, LEA, MULS					
4	OPCODE	REG		MOD	OP		REG	MOVEP					
5	OPCODE	REG	ОР	SIZE	OP		REG	ASL, ASR, ROL, ROR					
6	OPCODE	REG		OPC	ODE		REG	ABCD, EXG, SBCD					
7	OPCODE	REG	OP		DA [*]	TA		MOVEQ					
8	OPCODE	COUNT	OP	SIZE	OP	OP REG		ASL, ASR, ROL, ROR					
9	OPCODE	DATA	OP	SIZE OPERAND				ADDQ, SUBQ					
10	OPCODE	CONDITIO	N	OP	OPERAND			Scc					
1	OPCODE	CONDITIO		DISPLA	CEME	NT	Bcc						
12	OPCODE	CONDITIO	N	OF	CODE		REG	DBcc					
13	OPCC	SIZE	OPERAND			ADDI, CHPI, NEG, TST							
14	OP	CODE		SIZE	(OPER	AND	MOVEM					
15	C	PCODE				OPER.	AND	JMP, JSR, NBCD, PEA					
16		OPCODE				VE	CTOR	TRAP					
17		OPCOD	E			REG		EXT, LINK, SWAP, UNLINK					
18				NOP, RESET, RTS, TRAPV									
	OPCODE, OP determine instruction OPERAND determines data operated on												

OPECDE, Or determine instruction
OPERAND determines data operated on
REG selects a register
SIZE chooses byte, word, long
MOD determines if operand is source or destination, and length
COUNT, DATA are constants in the range 1-8
CONDITION specifies one of 16 possible conditions to test
DISPLACEMENT is signed offset for branches
VECTOR specifies where to trap

Fig. 5-23. Instruction formats used on the 68000 (first word only).

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDQ	0	1	0	1	Data			0	Si	Size Mode			Reg			
SUBQ	0	1	0	1	Data			1	Si	Size Mode				Reg		
s _{cc} [0	1	0	1	Condition				1	1	Mode			Reg		
DB _{cc}	0	1	0	1	Condition				1	1	0	0	1		Reg	

Fig. 5-24. Four 68000 instructions.