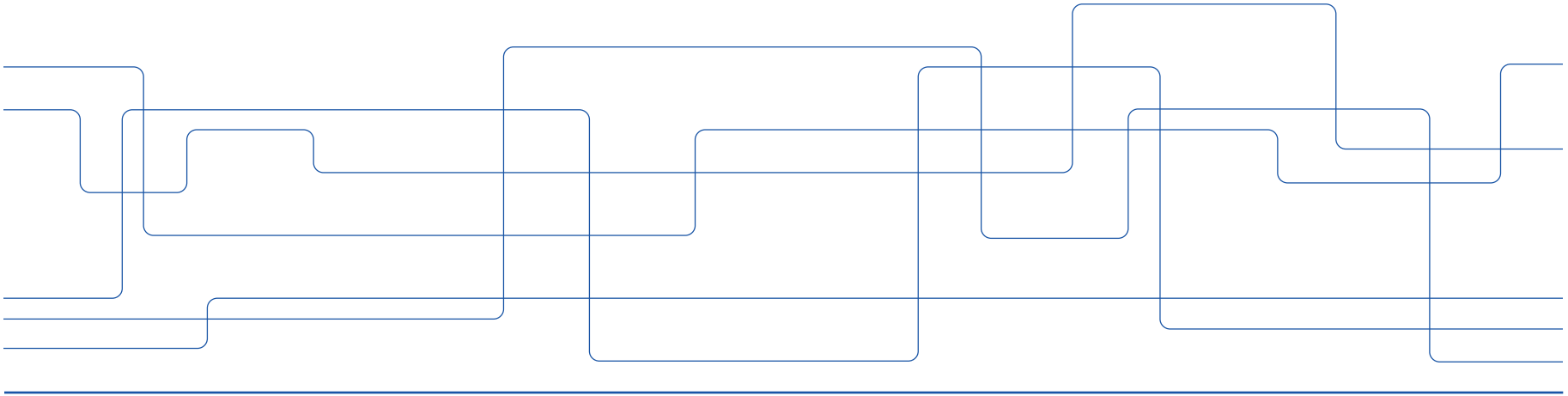
KTH ROYAL INSTITUTE OF TECHNOLOGY

Embedded Hardware Design in ASIC and FPGA

Project – Synthesis of the DRRA Fabric

Autum Semester, Period 1, 2023

Nov 23, 2023



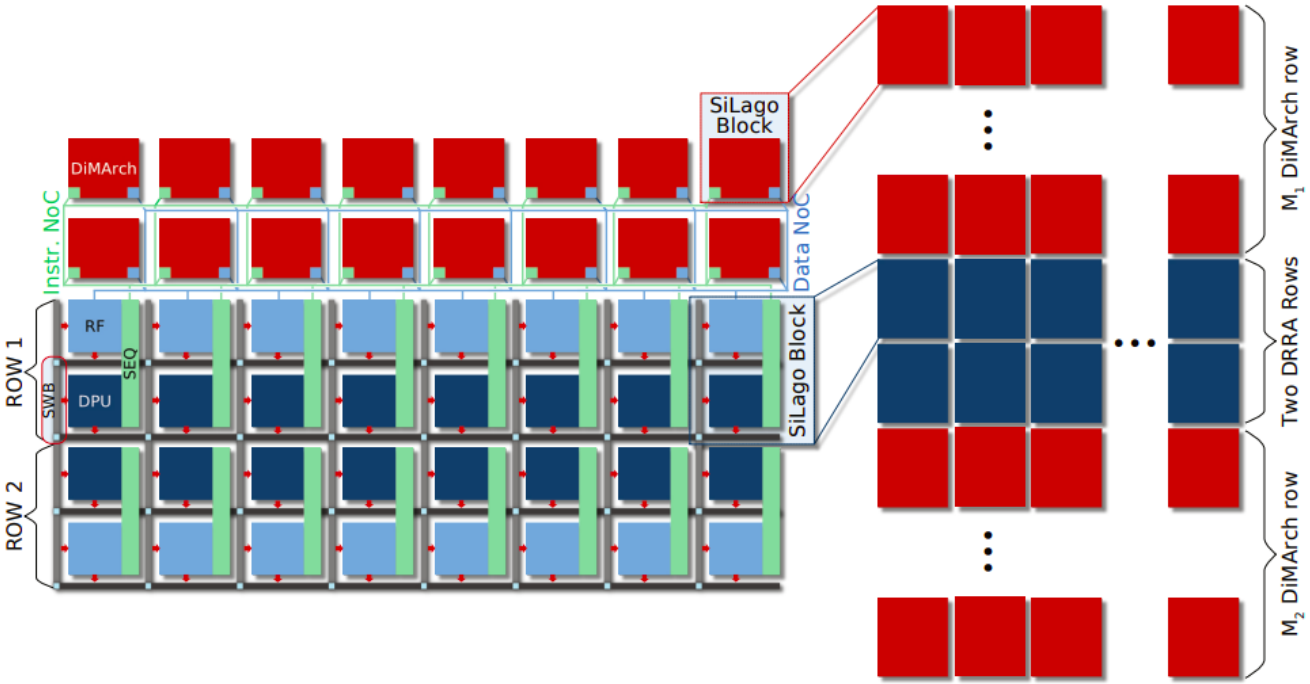
About the project

- Simulating the given design in Questasim.
- Logic synthesis of the given design.
- Physical implementation of the given design.
- Total six tasks.
- Teams of six students.
- Join a group in Canvas.

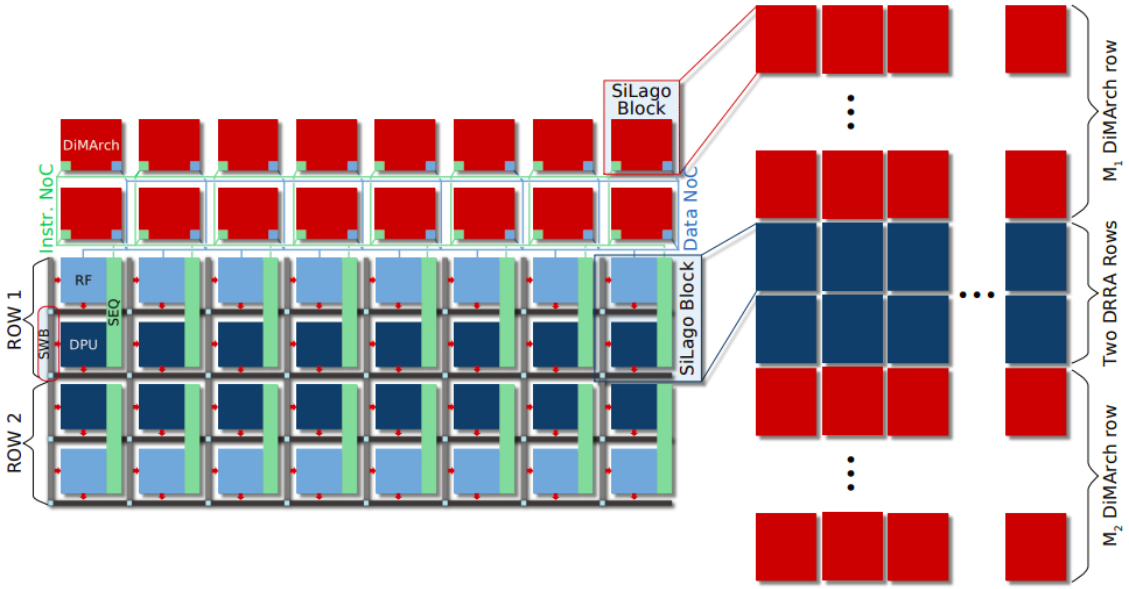
The design - DRRA and DiMArch Fabric

- DRRA stands for Dynamically Configurable Resource Array.
- DRRA serves the computational need of the design.
- DiMArch stands for Distributed Memory Architecture.
- DiMArch serves as the scratchpad memory.

DRRA and DiMArch Fabric

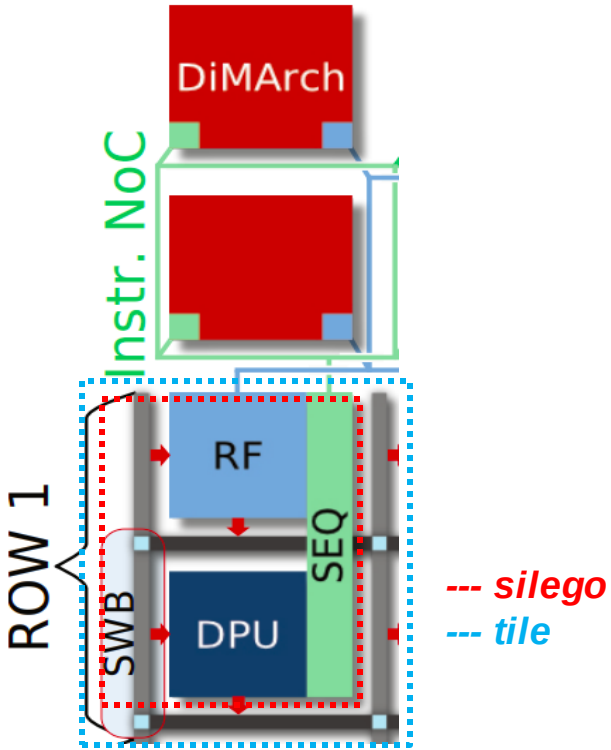


DRRA and DiMArch Fabric



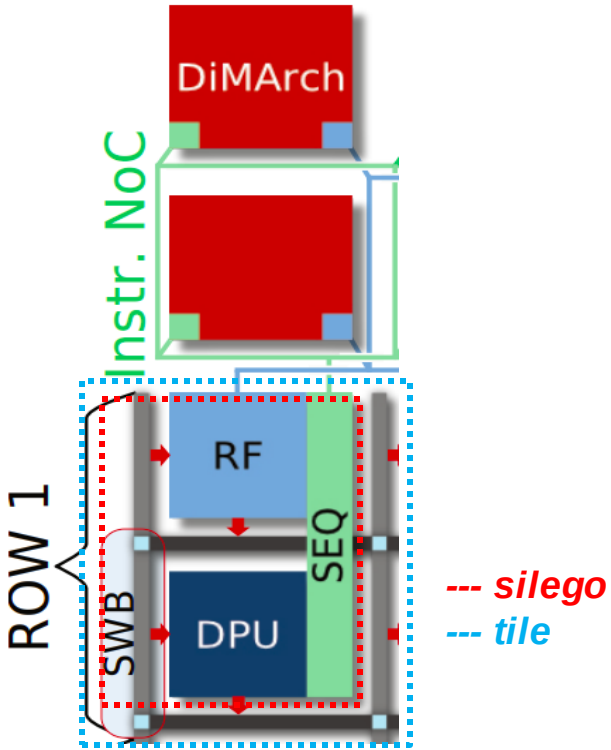
- Two rows of DRRA tiles.
- Two rows of DiMArch tiles.
- Each row has 8 tiles.

Zooming in...



- All tiles share a common module, ***silego***.
- **silego** consists of:
  - **SEQ *(Sequencer)***
    - Stores instructions.
    - Instructions configure the data path settings of each tile for data movement and computation.
  - **RF *(Register File)***
    - Bank of registers inside a tile for temp storage.
  - **DPU *(Data Processor Unit)***
    - Perform standard functions like, add, sub, mac, etc
  - **SWB *(SwitchBox)***
    - Configures the connections.

Zooming in...



- Depending on the location of each tile, ***silego*** has a tile wrapper.
- E.g, the DRRA tile in the top left corner does not have connections in the west. The tile wrapper wraps the common module silego with the connectivity associated with each tile location.
- There are six distinct DRRA tiles inside an overall ***DRRA wrapper***:
  - *DRRA_tile_top_left_corner*
  - *DRRA_tile_bot_left_corner*
  - *DRRA_tile_top_right_corner*
  - *DRRA_tile_bot_right_corner*
  - *DRRA_top*
  - *DRRA_bot*
- DiMArch follows similar design style.

A note on folder organization

- The design is available under Project/SiLagoNN in Canvas.
- Under SiLagoNN. /rtl folder contains all the design files, including hierarchy files for silego, DRRA wrapper, as well as the complete design.
- /tb contains testbench for the design.
- /syn should contain all logic synthesis related files.
- /phy should contain all physical synthesis related files.

Task 1 – Simulation of RTL design

- Goal - Demonstrate an understanding of inferring and simulating large designs.
- Testbench (available in the tb/ folder) – vector addition.
- Compile ***the complete design,*** according to the hierarchy.
- Hierarchy file to use: rtl/silagonn_hierarchy.txt
- Simulate the design.
- Check the output waveforms of DPU of the tile.
- Note: A semi-complete script with hints in comments is available with the testbench.

Task 2 – Flat logic synthesis

- Goal - Demonstrate an understanding of logic synthesis.
- Synthesise ***DRRA_wrapper*** using dc_shell. rtl/mtrf/drra_wrapper
- Hierarchy file to use: rtl/drra_wrapper_hierarchy.txt
- Since this is a big design, synthesis is slow, and it may test your patience :)
- Start with a large clock, say 50ns, and try to reduce the clock. 50ns的时候，slack36多
- The design is not perfect, please ignore warnings.
- Be careful of the errors that halt the synthesis.
- Note: A semi-complete script with hints in comments is available in /syn/scr/dc_flat.tcl. A constraints file is available under /syn.

Task 3 – Bottom-Up logic synthesis

- Goal - Demonstrate an understanding of bottom-up logic synthesis.
- Similar to Tast 2, except this time you synthesise ***DRRA_wrapper*** following a bottom-up approach using dc_shell.
- Hierarchy file to use: rtl/silego.txt
- Since silego is common to all DRRA tiles, synthesise it first so that it need not be synthesised multiple times by the tool.
- Once silego is compiled, compile all the tile wrappers, and the the complete DRRA wrapper.
- Note: A semi-complete script with hints in comments is available in /syn/scr/dc_hierarchical.tcl.

Task 4 - Flat Physical synthesis

- Goal - Demonstrate an understanding of flat physical synthesis.
- Physical synthesis of ***DRRA_wrapper*** using innovus.
- Discuss more post the physical synthesis lecture.

Task 5 - Floorplaning

- Goal - Demonstrate an understanding of floorplanning flat physical synthesis.
- Discuss more post the physical synthesis lecture.

Task 6 - Hierarchical Physical synthesis

- Goal - Demonstrate an understanding of hierarchical physical synthesis.
- Hierarchical Physical synthesis of ***DRRA_wrapper*** using innovus.
- Discuss more post the physical synthesis lecture.

Grading

Grades Tasks	A	B	C	D	E
Task 1 - RTL simulation	x	x	x	x	x
Task 2 - Flat synthesis	x	x	x	x	x
Task 3 - Bottom up synthesis	x	x	x	x	
Task 4 - Flat Physical Synthesis	x	x	x		
Task 5 - Floorplan	x	x			
Task 6 - Hierarchical Physical Synthesis	x				

- 10 min presentation for each group. All members should participate in the presentation.
- Grading is individual.
- Students are expected to have an understanding of all the tasks in the project, although they may divide the tasks individually.