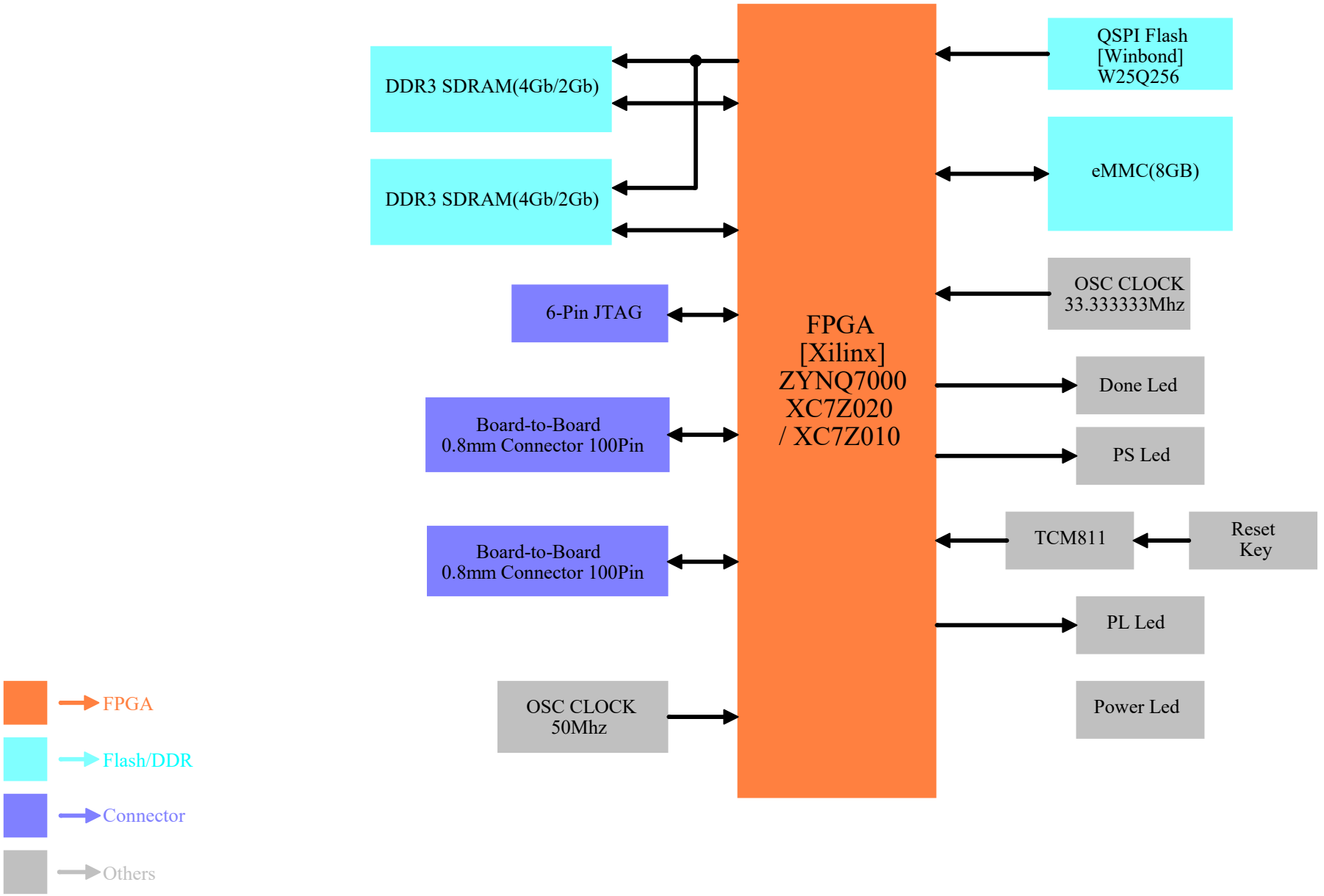

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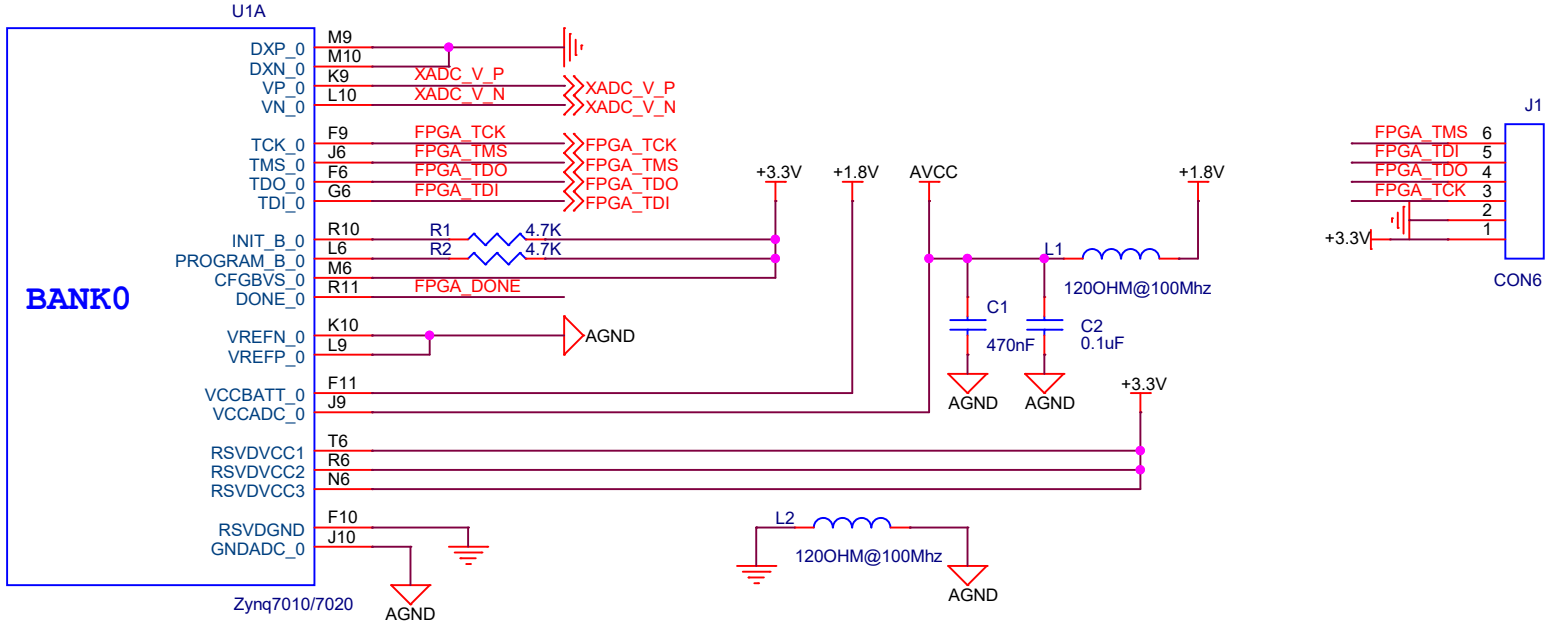
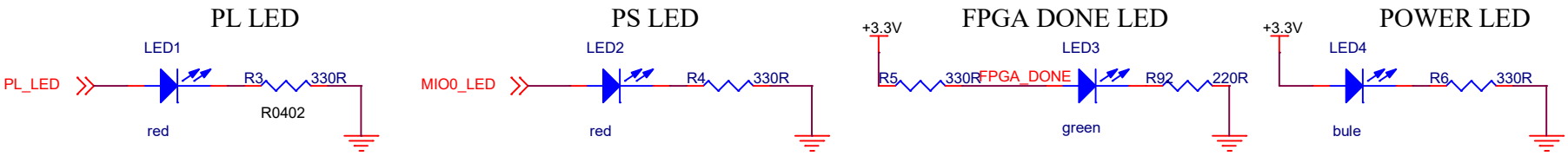
Size A4	Page Name	01_Block Diagram	Rev 1.0
Date: Monday, March 04, 2024	Sheet 1 of 11		





Design Name	ZYNQ-CORE	
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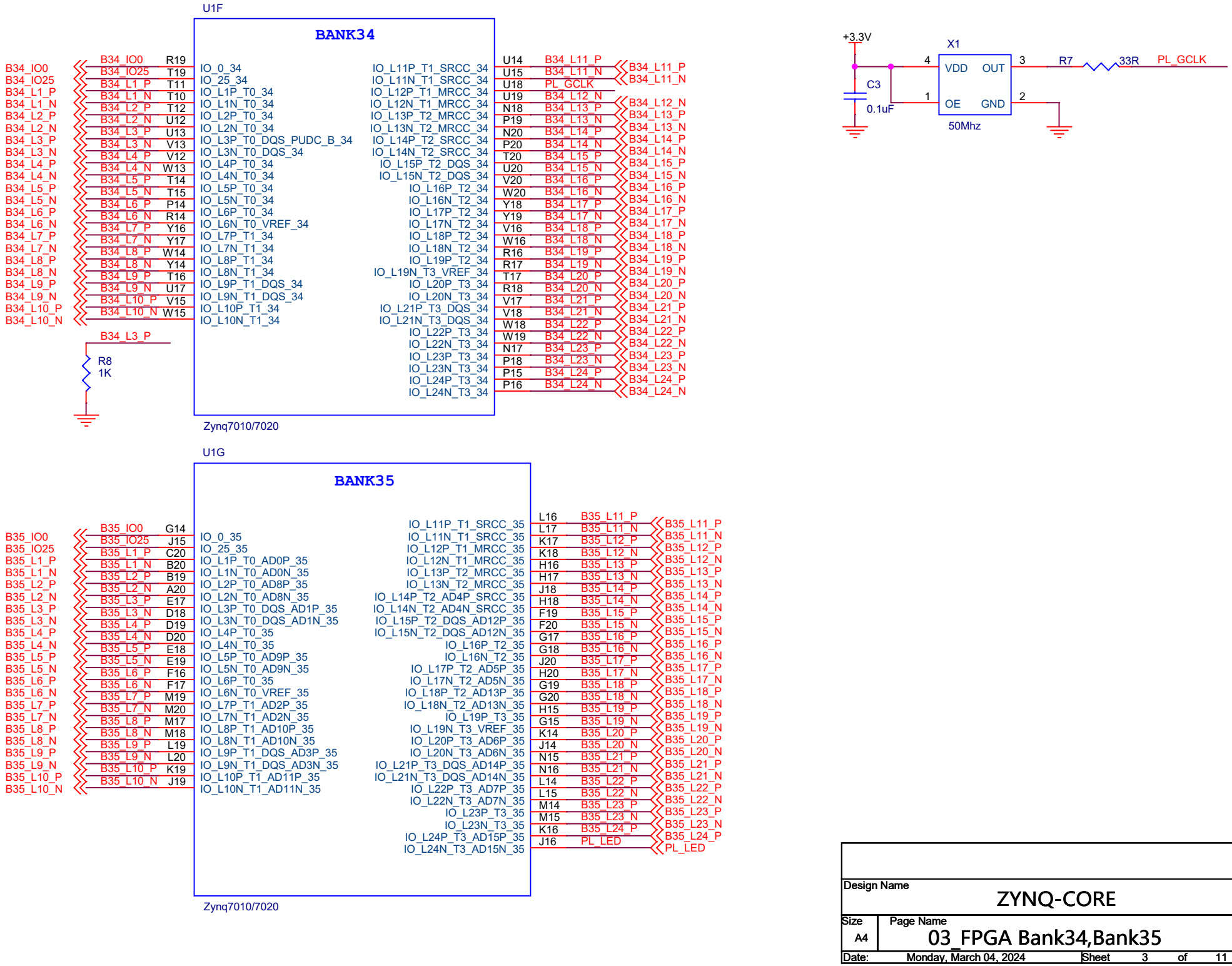
Date: Monday, March 04, 2024	Sheet 2 of 11	



Design Name	ZYNQ-CORE
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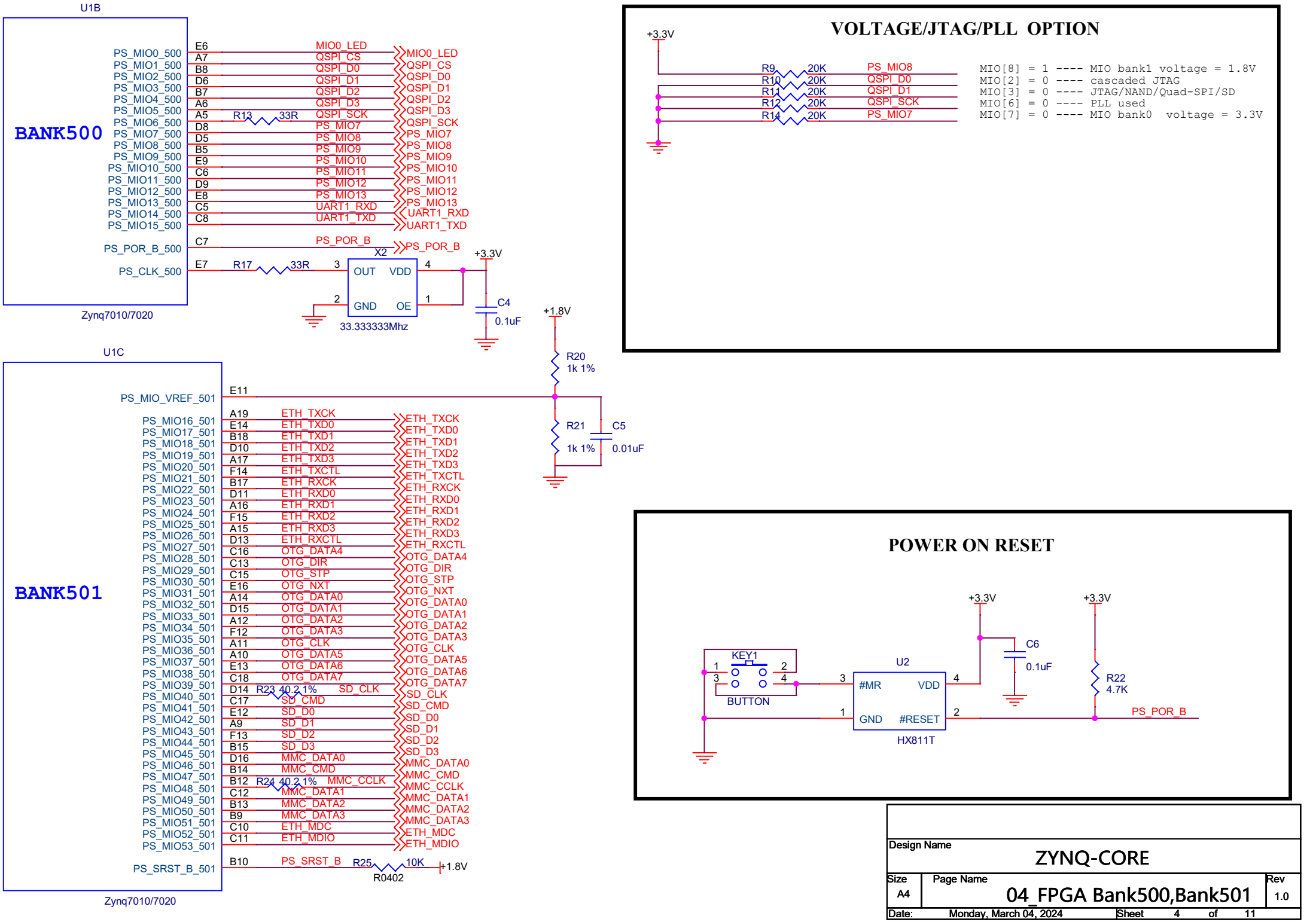
Rev: 1.0	
Date: Monday, March 04, 2024	Sheet 3 of 11


U1B
BANK500
PS_MIO0_500
PS_MIO1_500
PS_MIO2_500
PS_MIO3_500
PS_MIO4_500
PS_MIO5_500
PS_MIO6_500
PS_MIO7_500
PS_MIO8_500
PS_MIO9_500
PS_MIO10_500
PS_MIO11_500
PS_MIO12_500
PS_MIO13_500
PS_MIO14_500
PS_MIO15_500
PS_POR_B_500
PS_CLK_500
E6 MIO0_LED
A7 QSPI_CS
B8 QSPI_D0
D6 QSPI_D1
B7 QSPI_D2
A6 QSPI_D3
A5 QSPI_SCK
D8 PS_MIO7
D5 PS_MIO8
B5 PS_MIO9
E9 PS_MIO10
C6 PS_MIO11
D9 PS_MIO12
E8 PS_MIO13
C5 UART1_RXD
C8 UART1_TXD
C7 PS_POR_B
E7
R13 33R
R17 33R
X2
OUT VDD
GND OE
33.333333Mhz
+3.3V
C4 0.1uF
Zynq7010/7020
U1C
BANK501
PS_MIO_VREF_501
PS_MIO16_501
PS_MIO17_501
PS_MIO18_501
PS_MIO19_501
PS_MIO20_501
PS_MIO21_501
PS_MIO22_501
PS_MIO23_501
PS_MIO24_501
PS_MIO25_501
PS_MIO26_501
PS_MIO27_501
PS_MIO28_501
PS_MIO29_501
PS_MIO30_501
PS_MIO31_501
PS_MIO32_501
PS_MIO33_501
PS_MIO34_501
PS_MIO35_501
PS_MIO36_501
PS_MIO37_501
PS_MIO38_501
PS_MIO39_501
PS_MIO40_501
PS_MIO41_501
PS_MIO42_501
PS_MIO43_501
PS_MIO44_501
PS_MIO45_501
PS_MIO46_501
PS_MIO47_501
PS_MIO48_501
PS_MIO49_501
PS_MIO50_501
PS_MIO51_501
PS_MIO52_501
PS_MIO53_501
PS_SRST_B_501
E11
A19 ETH_TXCK
E14 ETH_TXD0
B18 ETH_TXD1
D10 ETH_TXD2
A17 ETH_TXD3
F14 ETH_TXCTL
B17 ETH_RXCK
D11 ETH_RXD0
A16 ETH_RXD1
F15 ETH_RXD2
A15 ETH_RXD3
D13 ETH_RXCTL
C16 OTG_DATA4
C13 OTG_DIR
C15 OTG_STP
E16 OTG_NXT
A14 OTG_DATA0
D15 OTG_DATA1
A12 OTG_DATA2
F12 OTG_DATA3
A11 OTG_CLK
A10 OTG_DATA5
E13 OTG_DATA6
C18 OTG_DATA7
D14 R23 40.2 1% SD_CLK
C17 SD_CMD
E12 SD_D0
A9 SD_D1
F13 SD_D2
B15 SD_D3
D16 MMC_DATA0
B14 MMC_CMD
B12 R24 40.2 1% MMC_CCLK
C12 MMC_DATA1
B13 MMC_DATA2
B9 MMC_DATA3
C10 ETH_MDC
C11 ETH_MDIO
B10 PS_SRST_B R25 10K +1.8V
R0402
+1.8V
R20 1k 1%
R21 1k 1%
C5 0.01uF
Zynq7010/7020
VOLTAGE/JTAG/PLL OPTION
+3.3V
R9 20K PS_MIO8
R10 20K QSPI_D0
R11 20K QSPI_D1
R12 20K QSPI_SCK
R14 20K PS_MIO7
MIO[8] = 1 ---- MIO bank1 voltage = 1.8V
MIO[2] = 0 ---- cascaded JTAG
MIO[3] = 0 ---- JTAG/NAND/Quad-SPI/SD
MIO[6] = 0 ---- PLL used
MIO[7] = 0 ---- MIO bank0 voltage = 3.3V
POWER ON RESET
KEY1
BUTTON
U2
#MR VDD
GND #RESET
HX811T
+3.3V
+3.3V
C6 0.1uF
R22 4.7K
PS_POR_B
Design Name
ZYNQ-CORE
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A4
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04_FPGA Bank500,Bank501
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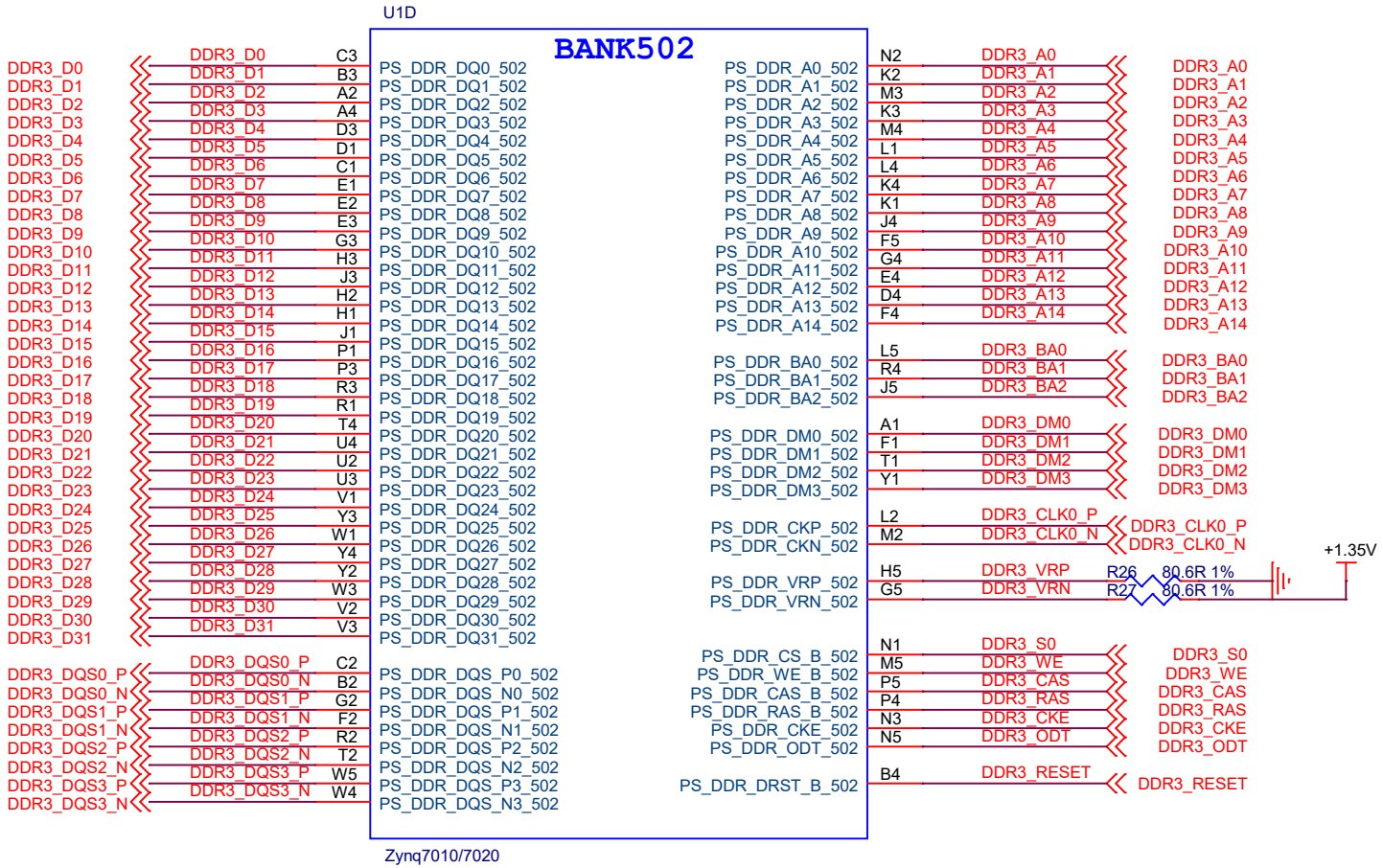

Design Name	ZYNQ-CORE	
Size A4	Page Name 05_FPGA Bank502	Rev 1.0
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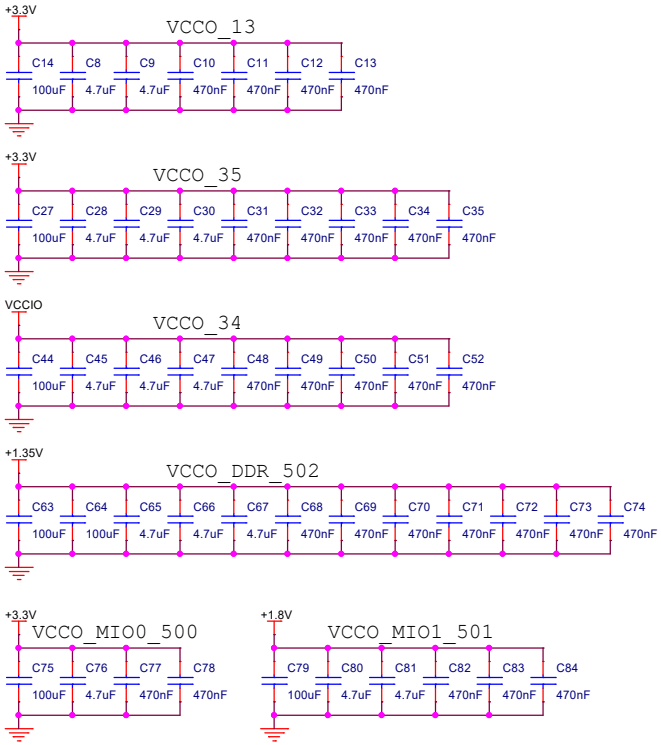

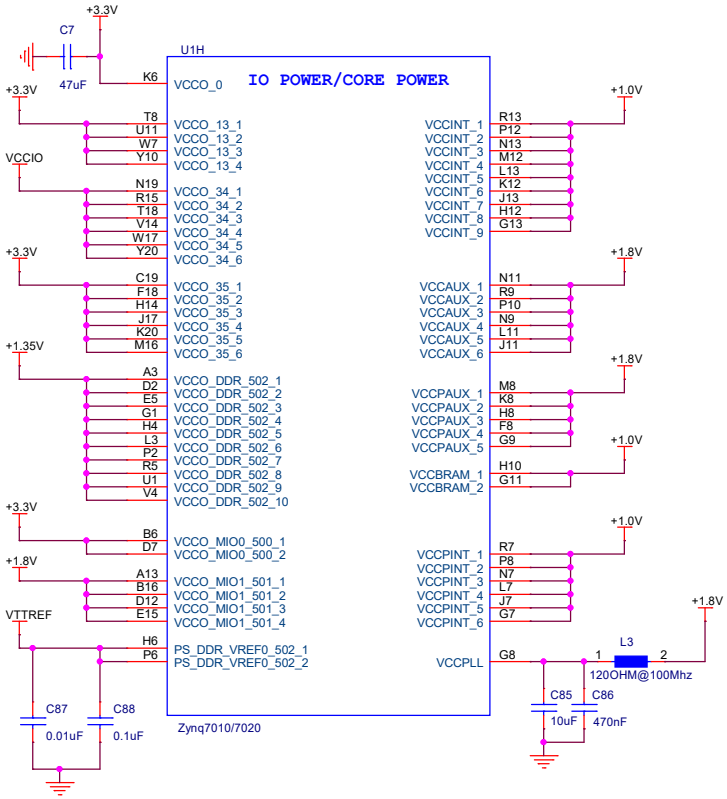

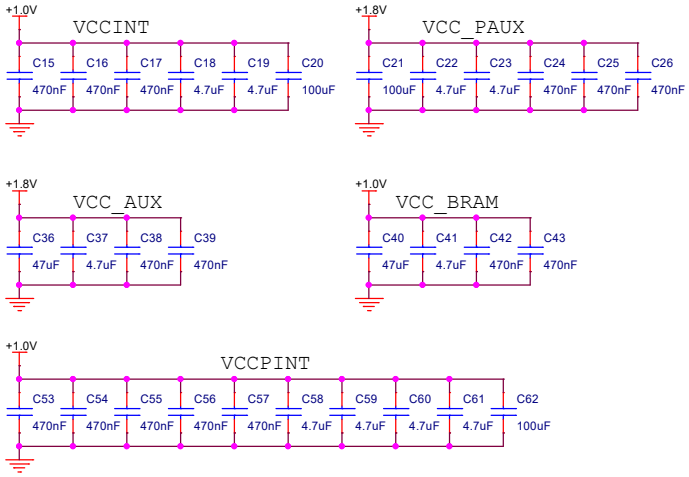

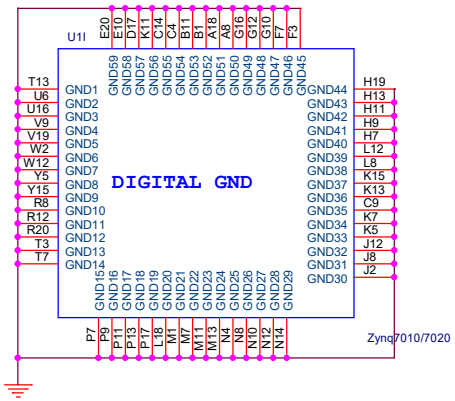

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Size A3	Page Name 07_FPGA POWER	Rev 1.0
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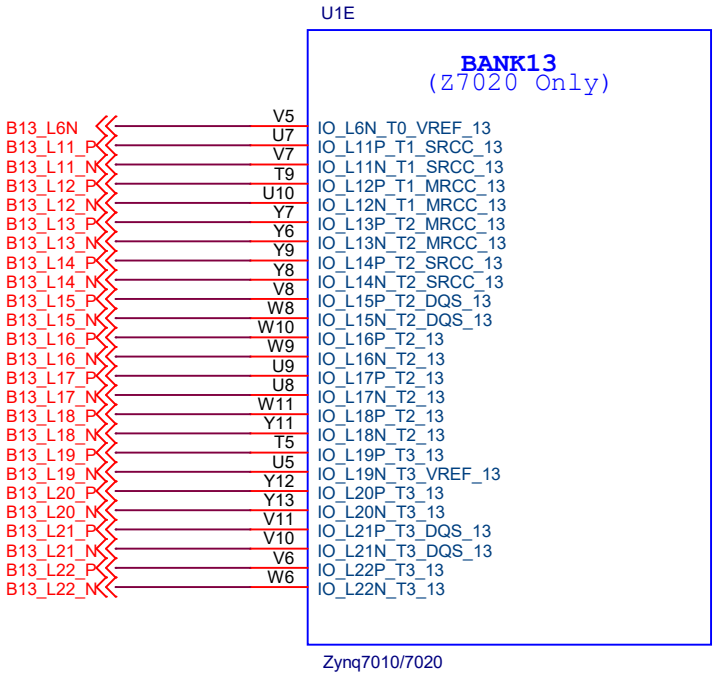

Design Name	ZYNQ-CORE	
Size: A4	Page Name: 06_FPGA Bank13	Rev: 1.0
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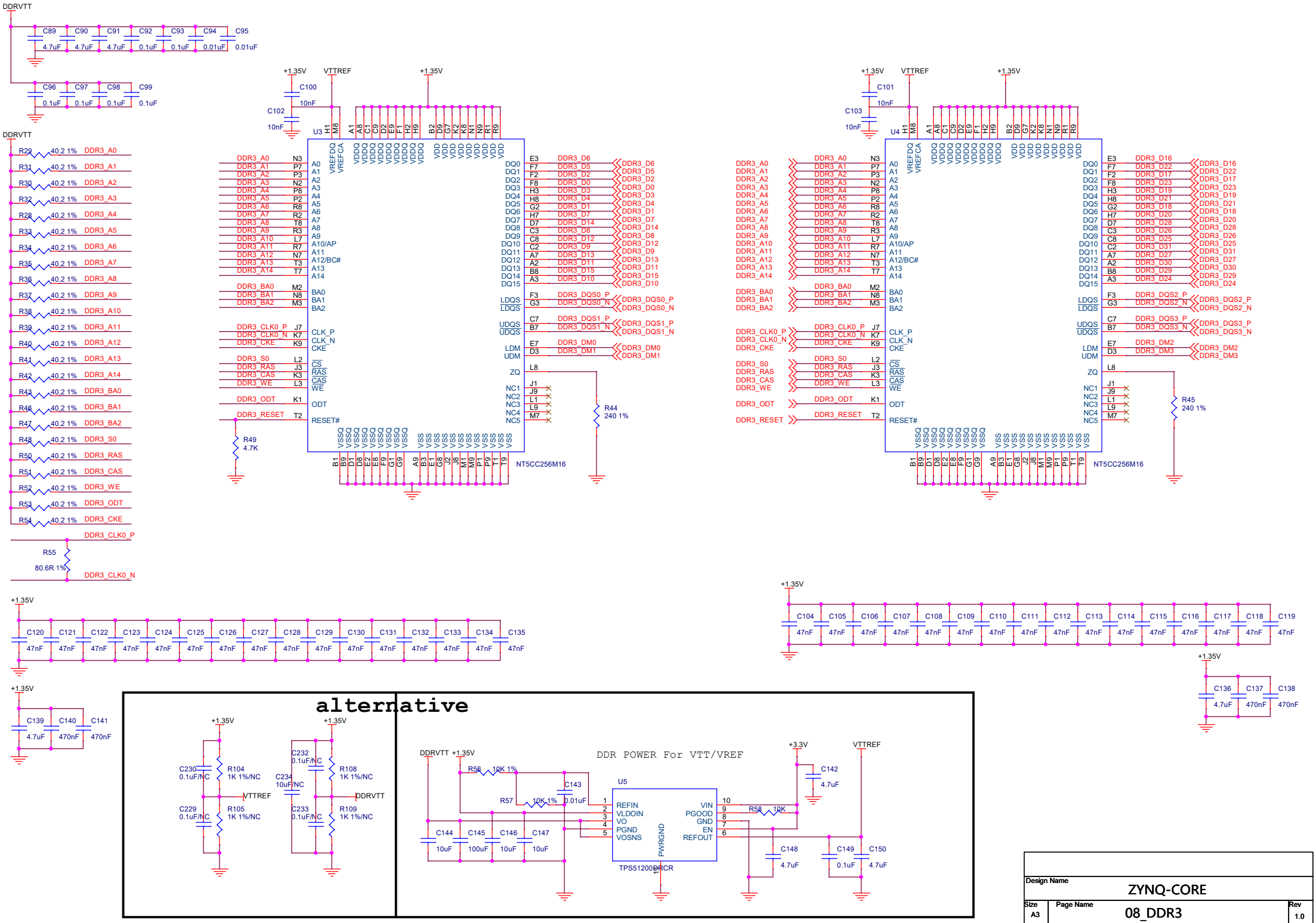

Design Name	ZYNQ-CORE	
Size A3	Page Name 08_DDR3	Rev 1.0
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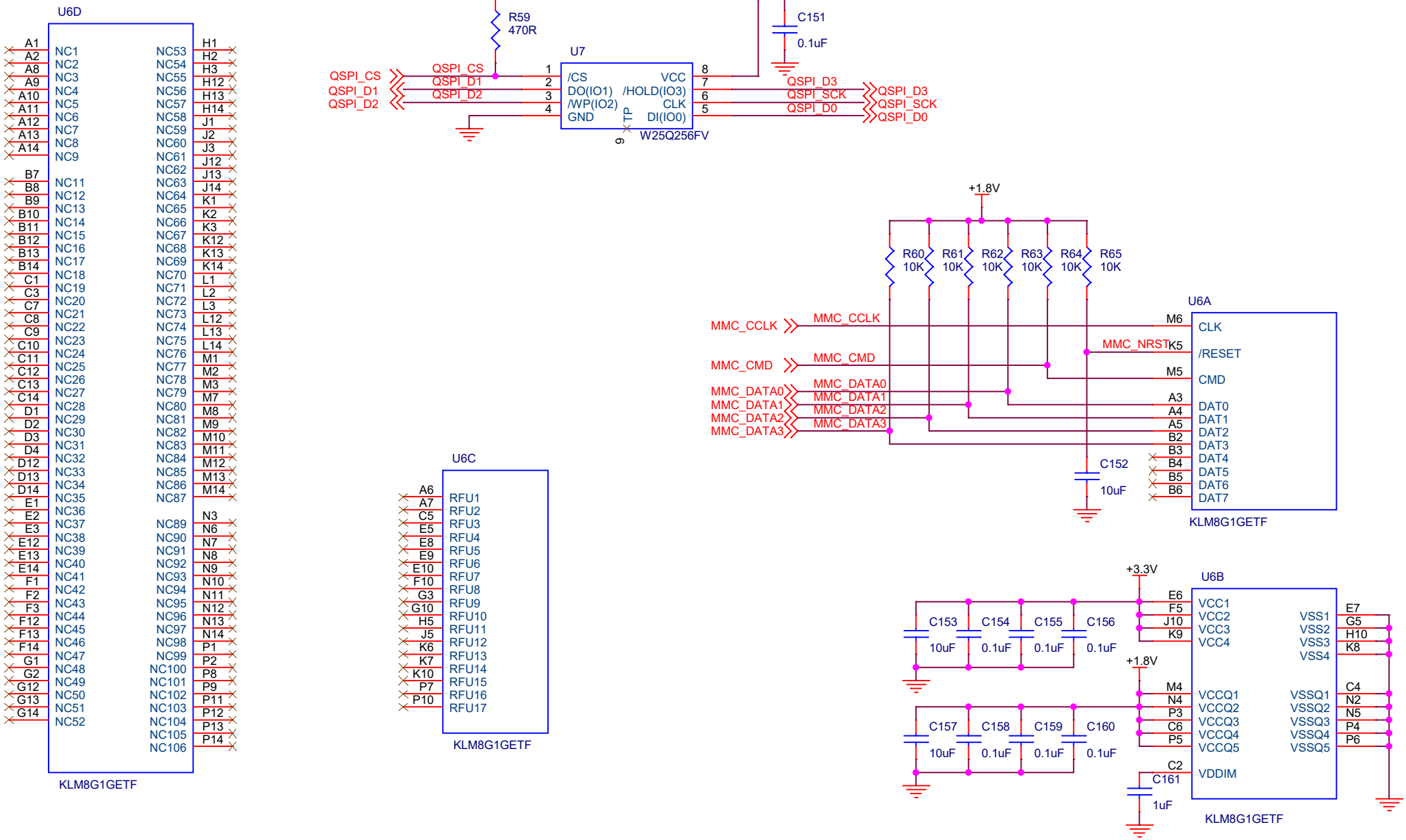

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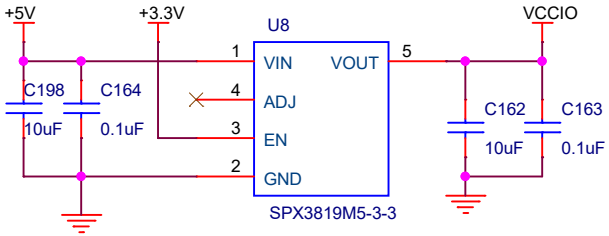
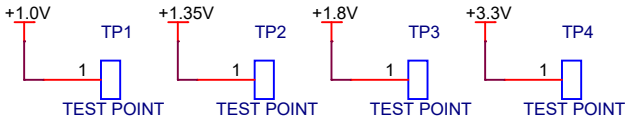
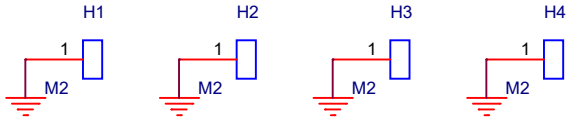
Vout=0.6*R1/R2+0.6



Power On Sequnce:
1.0V -> 1.8V -> 1.35V -> 3.3V -> VCCIO



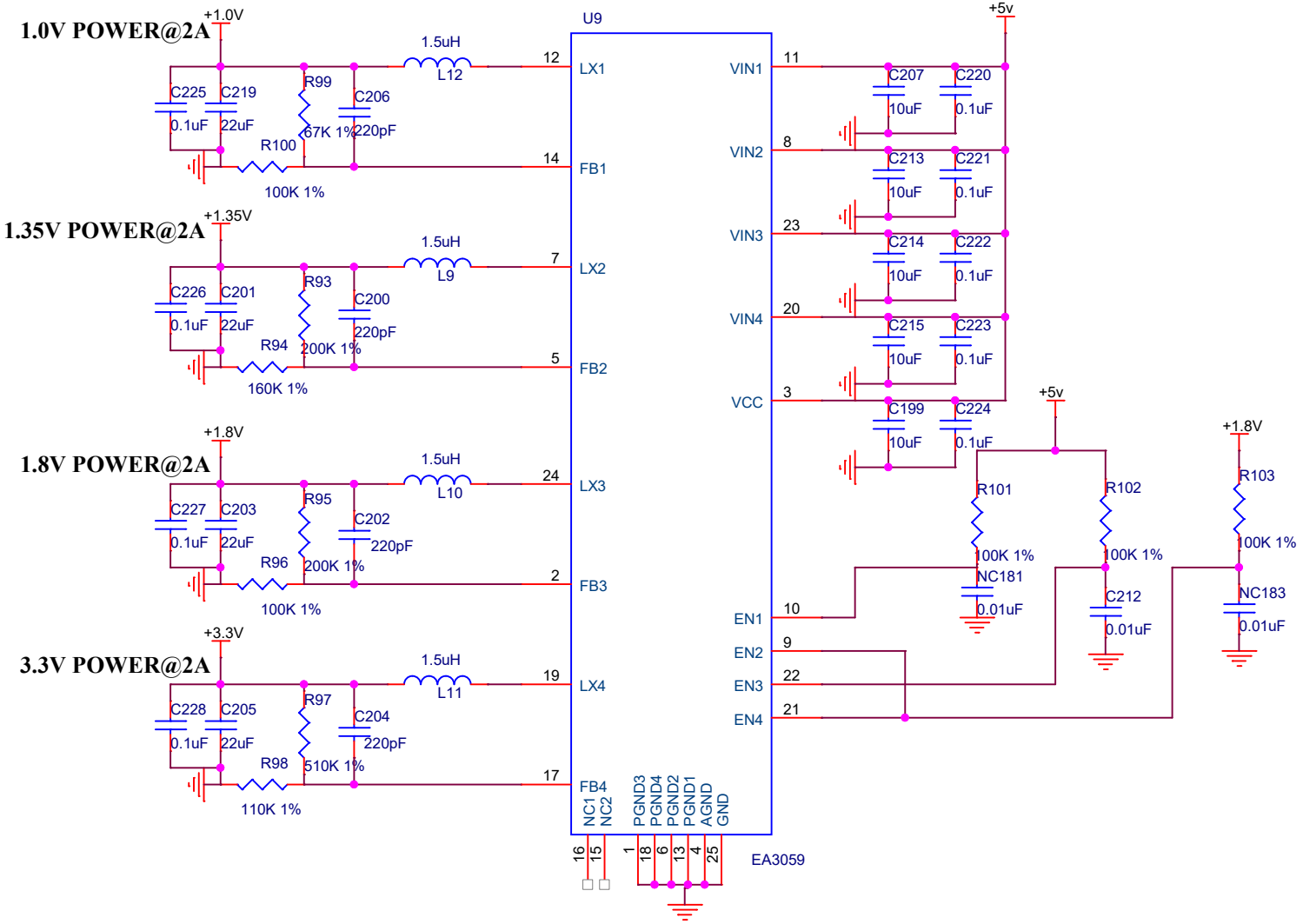


1.0V POWER@2A

1.35V POWER@2A

1.8V POWER@2A

3.3V POWER@2A



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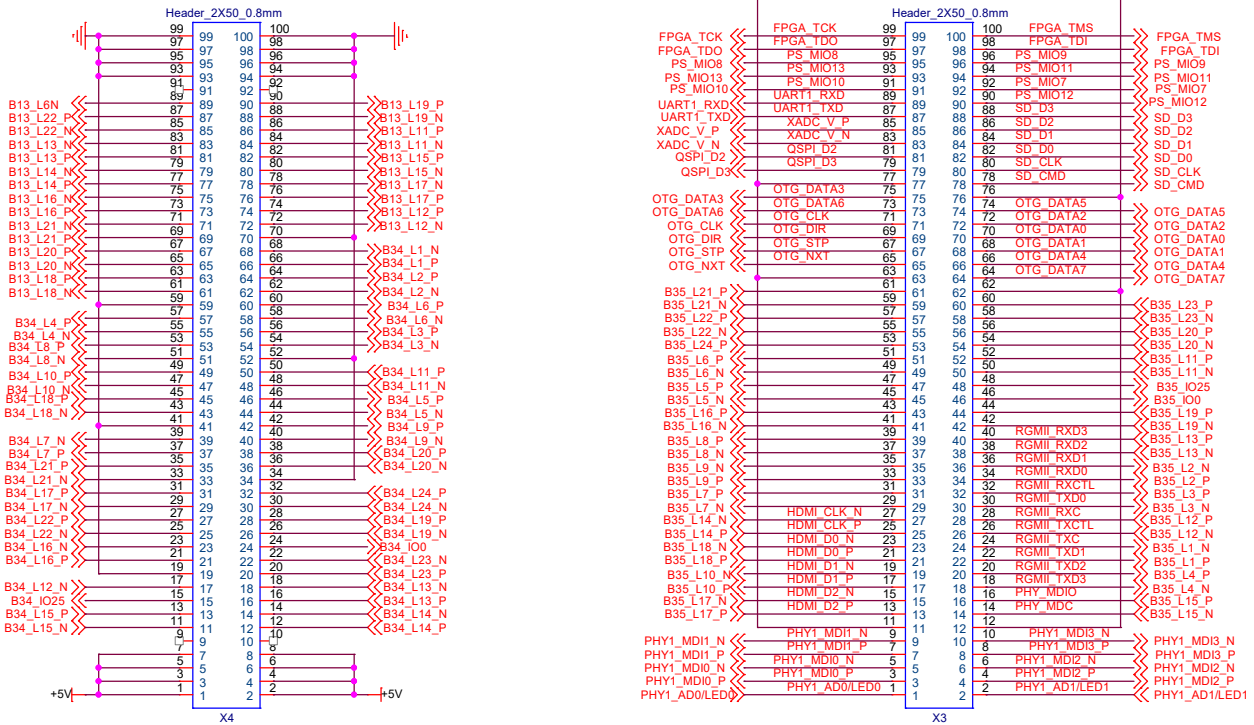

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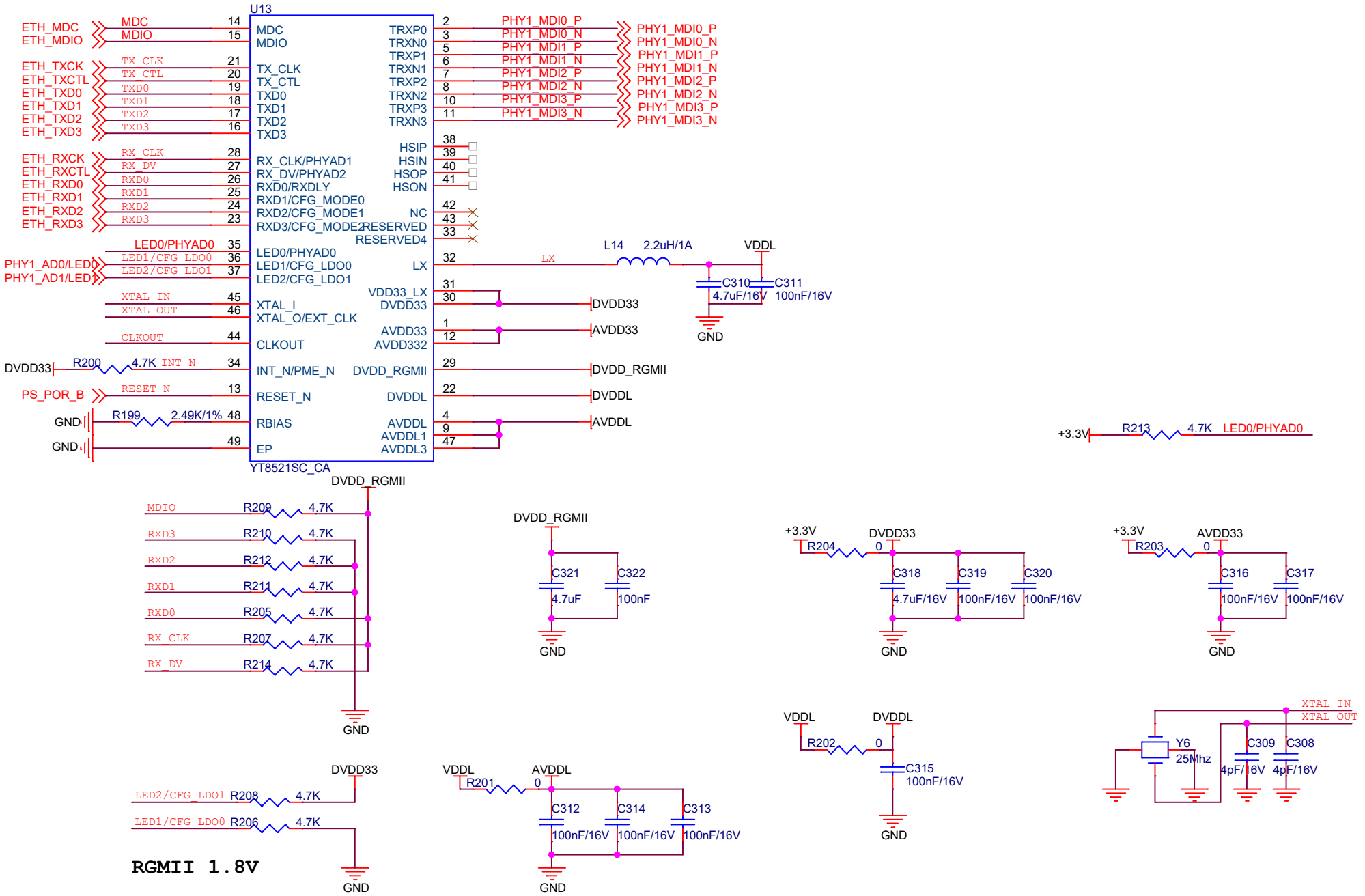

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