# Report

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1. A comparison table like the following one, and an explanation of the result

```
create clock [get ports clk]  -name CLK  -period 10  -waveform {0 5}
```

CLK –period 10 –waveform {0 5}

```
floorPlan -coreMarginsBy die -site FreePDK45_38x28_10R_NP_162NW_340 -r 1.0 0.7 4.0 4.0 4.0 4.0
```

Fixed core utilization = 0.7

| | Congestion Driven and Timing Driven table | | | | | |
|---|---|---|---|---|---|---|
| | (L, off) | (L, on) | (M, off) | (M, on) | (H, off) | (H, on) |
| Slack | 0.205 | 0.457 | 0.400 | 0.286 | 0.4 | 0.286 |
| Total wire length | 112861.7750 um | 103990.5650 um | 108667.4100 um | 103115.8600 um | 108667.4100 um | 103115.8600 um |

2. The difference(s) between the congestion-driven placement and timing-driven placement

Congestion-driven placement 目的:
讓 chip 的資源利用不會造成堵塞，但並不會著重在訊號延遲
Timing-driven placement 目的:
讓整體訊號延遲降低，但不會管 chip 位置是否造成訊號堵塞，所以必須按照設計目的來決定哪一個 placement 佔的比例比較重。

簡而言之，如果著重在 timing-driven placement，會有較好的 timing dealy，但會造成 routing problem 和 timing violation 在壅塞區域(chip)

反之，可以減少 congestion 的問題，進而分散 logical cell，但可能會無法達到想要的 timing delay

3. An explanation of why we insert filler cells

如果不放入填料，晶片會是不平整的，而現代晶片通常都是好幾層相疊，所以需要填料將中空的部分進行填充，除此之外，根據網路上的資料，填料是可以增加整個晶片的承受壓力，有利於增加其強健性。

4. Show your best result (including clock period, total area of chip, total wire length, slack, congestion-driven effort and timing-driven on/off setting, and their snapshots) to maintain a non-negative slack and no DRC violation.

Clock period:

```
set sdc_version 2.0

set_units -time ns -resistance MOhm -capacitance fF -voltage V -current mA
create_clock [get_ports clk]  -name CLK  -period 8  -waveform {0 4}
```

Total area of chip

```
Total area of Chip: 13787.525 um^2
```

Total wire length

```
Total wire length: 106909.2700 um
```

Slack time

```
= Slack Time                    0.111
```

Congestion-driven and timing-driven setting

```
setPlaceMode -congEffort auto -timingDriven 1 -clkGateAware 1 -powerDriven 0 -ignoreScan 1 -reorderScan 1 -ignoreSpare 0 -placeIOPins 1 -moduleAwareSpare 0
-preserveRouting 1 -rmAffectedRouting 0 -checkRoute 0 -swapEEQ 0
```

從我的 apr.tcl file 中的結果

Congestion-dirven placement 是選取 auto，timing-driven placement 則是選擇開啟。

```
floorPlan -coreMarginsBy die -site FreePDK45_38x28_10R_NP_162NW_340 -r 1.0 0.75 4.0 4.0 4.0 4.0
```

Core utilization = 0.75

經過幾次測試後，得出最好的結果為 0.75。

Check the DRC

```
-check_same_via_cell true             # bool, default=false, user setting
 *** Starting Verify DRC (MEM: 2996.5) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
**WARN: (IMPVFG-1198):  The number of CPUs requested 8 is larger than that verify_drc used 4. In Multithreading mode, the number of CPUs verify_drc used is no
t larger than the number of subareas.
 Use 'setMultiCpuUsage -localCpu' to specify the less cup number if the verify area is not large.
  VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.000 0.000 60.480 58.320} 1 of 4  Thread : 3
 VERIFY DRC ..... Sub-Area: {60.480 0.000 118.940 58.320} 2 of 4  Thread : 3
 VERIFY DRC ..... Sub-Area: {0.000 58.320 60.480 115.920} 3 of 4  Thread : 3
 VERIFY DRC ..... Thread : 1 finished.
 VERIFY DRC ..... Thread : 0 finished.
 VERIFY DRC ..... Sub-Area: {60.480 58.320 118.940 115.920} 4 of 4  Thread : 3
 VERIFY DRC ..... Thread : 3 finished.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:01.0  ELAPSED TIME: 1.00  MEM: 288.1M) ***
```

No violation

最後的 layout 會放在問題五

5. Show the final chip layout of your best result generated by Innovus (use print screen to save the final layout and paste on the report)