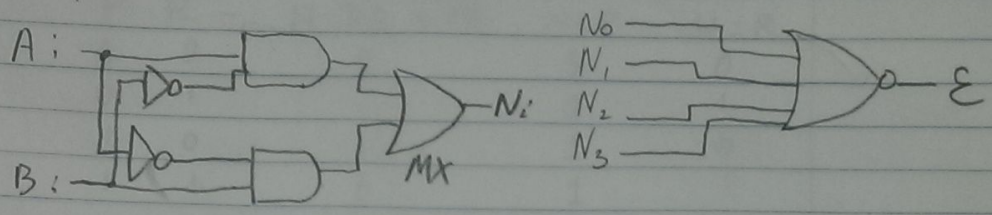
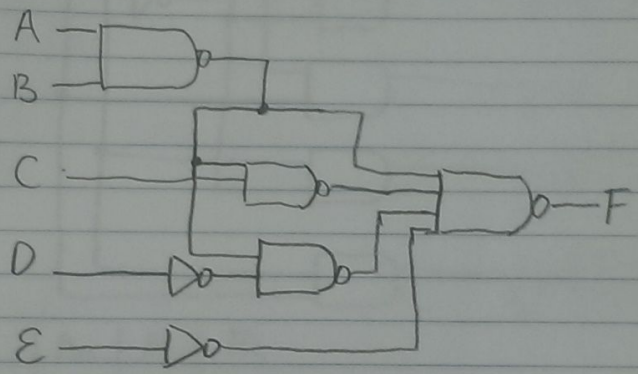
Chapter 3 Examples.

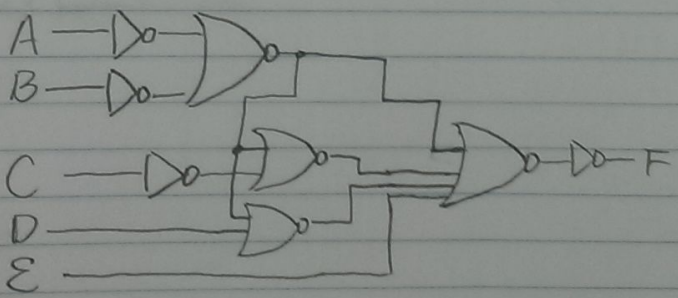
Example 3-1



Example 3-2 Implementation with NAND Gate

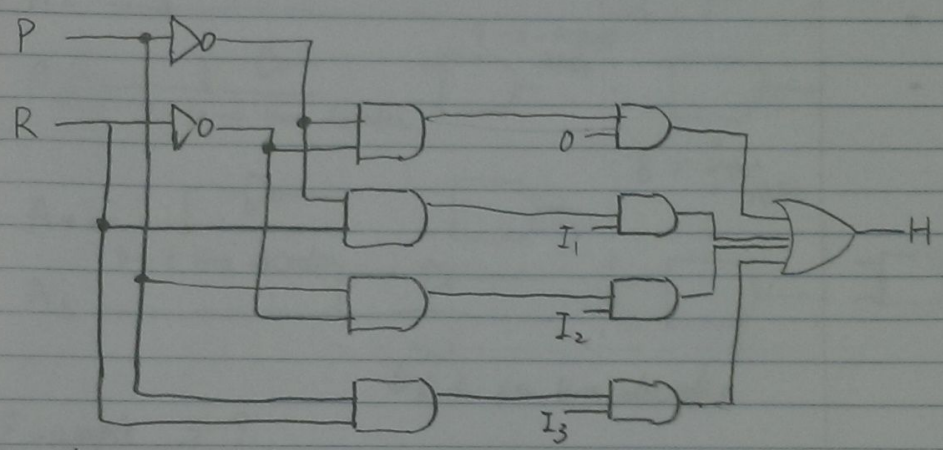


Example 3-3 Implementation with NOR Gates



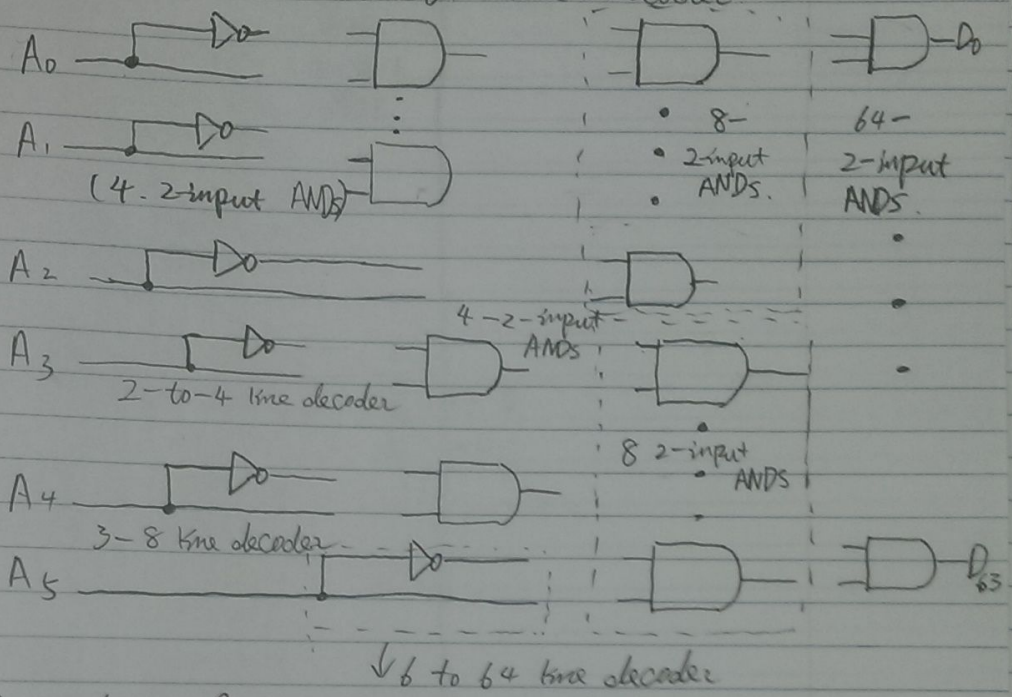
Example 3-4 Value Fixing

Mode		M_0	M_1	M_2
P	R	$H = \bar{P}R + P\bar{R}$	$H = P$	$H = R$
0	0	0	0	0
0	1	1	0	1
1	0	1	1	0
1	1	0	1	1

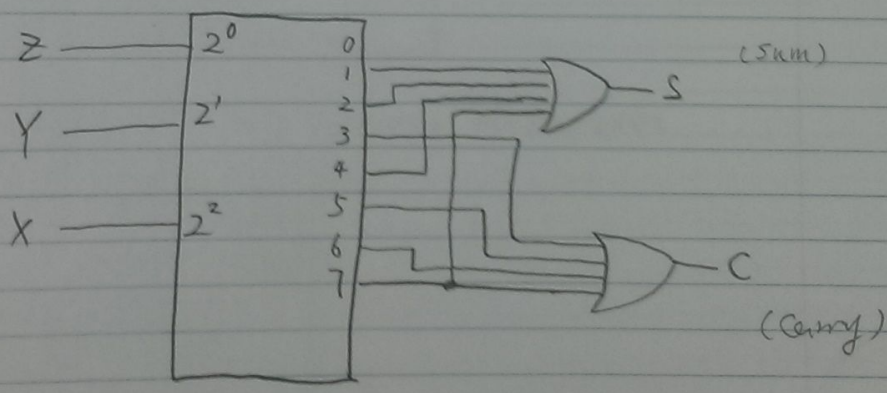


	M_0	M_1	M_2
I_1	1	0	1
I_2	1	1	0
I_3	0	1	1

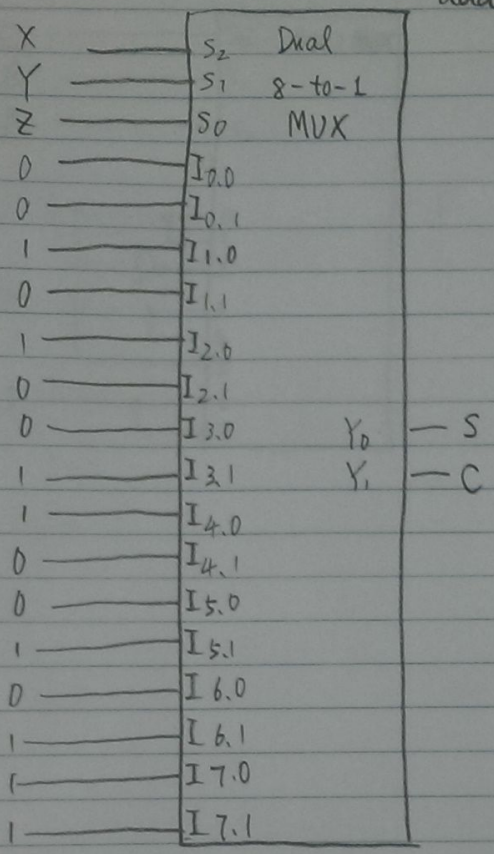
Example 3-6 6-to-64-line Decoder



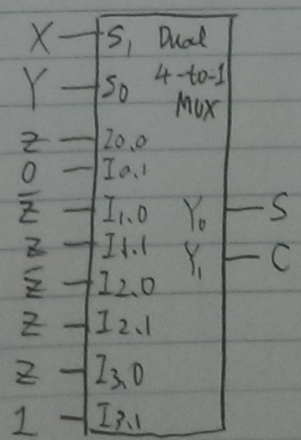
Example 3-9



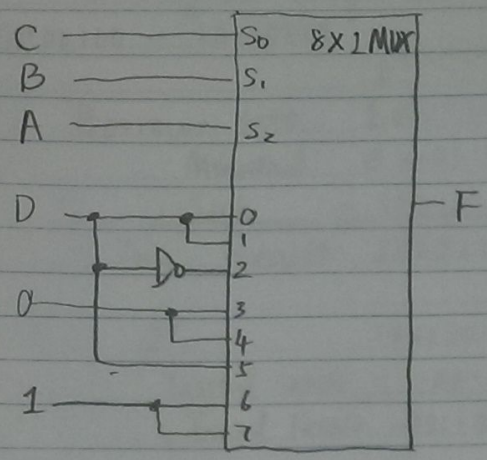
Example 3-15 multiplexer Implementation of binary adder Bit



Example 3-16 Alternative multiplexer



Example 3-17 Multiplexer Implementation of 4-variable Function



Example 3-19 Unsigned Binary Subtraction by 2s complement subtract

01100100 − 10010110

borrowed ↓

Borrows into 100111100

Minuend 01100100

Sub −10010110

Int Result 11001110

2^8 100000000

− Initial result −11001110

Final Result −00110010

Example 3-21

+6	00000110	−6	11111010	+6	00000110	−6	
+13	00001101	+13	00001101	−13	11110011	−13	
+19	00010011	+7	00000111	−7	11111001	−19	

11111010
11110011
11101101

Example 3-22 Signed binary sub using 2's complement

−6	11111010	11111010	+6	00000110	
−(−3)	−11110011	+00001101	−(−13)	−11110011	
+7		00000111	+19		

00000110
+ 00001101
00010011