HW #10 Summary of chapter 10.

10 - Pipelined Datapath

By breaking up the delay path with register, the pipelined Datapath reduced the clock period and increased the clock frequency.

However, the term "pipeline" does not provide the best analogy for the corresponding datapath structure. The production line is a better analogy.

We compare the pipelined and nonpipelined as car wash in single station and mult-stations. The single station car wash frequency is the inverse of the latency time, the mult-station car wash the frequency is three times the inverse of latency time.
Thus, the processing rate of pipelined datapath with n stages is n times the nonpipelined datapath.

The data in pipeline is in discrete steps rather than continuous. The time provided for each stage is same, registers are placed between stages.

The registers provide temporary storage as pipelined platforms.

10-2. Pipelined Control.

We need an instruction for the pipelined datapath as data pass through each stage. We add additional registers serve to pass along the instruction information, just like the order sheet pass through in the car wash example.

There're four stages added here: the If, DOF, EX, WB stages. The location of the pipelined platforms has balanced of the delays, so that the delays per stage are no more than 1.0 ns.

10-3 Reduced instruction set computer

The RISC is a reduced instruction set architecture. The size of the programmer-accessible register file is comparatively large in the RISC because of the load/store instruction set architecture. In real pipelines, it requires more than one clock cycle to execute the stores and loads. A program counter is also provided in addition of the register file.

The only operations that can access memory are Load and Store. A significant number of immediate instructions help to reduce later memory accesses and speed up execution when constant are employed.

Four addressing modes in the RISC are: register, register indirect, immediate and relative, the mode is specified by the operation code.

The RISC have software and hardware two solutions to deal with data hazards: Data-hazard stall and data forwarding.

10-4 The complex instruction set

CISC are the complex instruction set to implement using a single cycle computer or a single pass through pipeline. The microprogrammed control is choosen to work with the multiple instruction here, the develop and operation of the microprogram is characterized as CISC ISA.

The modifications of RISC ISA are: new format of branch instruction, register partition, adding condition code.

To support the modifications of ISA, datapath and the control unit are also required to make several changes.

10-5 method on Design.

The following methods are used for advanced CPU design: multiple unit organized as a pipeline-parallel structure, superpipelines and superscalar architecture.

With the limitation of one instruction per clock circle in all of those methods, it is desirable to maximize the clock rate by minimizing pipeline stage.

MIMD and symmetric on-chip core multiprocessors are developed for general purpose applications and digital media applications.