Chapter 7 Summary

7-1 Definition of Memory

Memory is a collection of cells capable of storing binary information. Information from an input device is placed in memory so that it can be used in processing. Output information are placed in memory as well so it can be sent to output device.

two types of memory are used in various Computer: RAM (Random access memory)
ROM (Read-only memory)

7-2 Random-Access Memory.

For random memory, the access taking the same time regardless of the location. In Contrast, serial memory takes different length of time to access memory in different locations.

Binary information stored in memory as word (group of bits) A group of 8 bits is called byte.

The wire input cause binary data to be transferred into memory, the Read input cause binary data to be transferred out of memory.

Write and Read are the two operations that RAM can perform. Write transfer a new word to memory to store. Read transfers a copy of stored word out of memory.

7-3 SRAM Integrated Circuit.

The static memory circuit consist of RAM chips and addition logic. The circuitry is made up if decoders to select the word to be read or write.

7-4 Array of SRAM ICs

If the memory unit needed is larger than the capacity of one chip, then the integrated-circuit RAM chips can be combined in an array to form the required size of memory.

An increas in the number of words requires the increasing of address length. An increase in the number of bits per word does not require we increase the length of address.

7-5 DRAM

The dynamic RAM provides high storage capacity at low cost, it is similar to SRAM in many ways but the electronic design of DRAM is more complicate than the SRAM.

7-6 DRAM types

Many new types of DRAM are on market now, they are based on the basic DRAM principle but have they own unique way of memory access approach.

7-7

The DRAM Controller performs Controling and accessing of DRAM arrays.

Summary of chapter 11

11 - 1 Computer I/O

The input and output device provide a way to connect Computer CPU with the outside environment. All different kind of I/O devices need to correspond differently in order to interconnect with them. (with Computer).

11-2 Sample Peripherals

The three most used peripherals are : keyboard, Hard drive and the liquid Crystal display screen.

A scan matrix is lying beneath keys that is used. A microcontroller is programmed to periodically scan all intersections in the matrix by manipulating the control inputs of a decoder and multiplexer.

The hard driver stores information serially on a non movable disk. Each platter of hard driver is magnetizable on one or both surface. One or more read/write heads on each surface.

The liquid crystal display screen is the primary output device that help us comunicate with our computers. The basic picture element of the screen is pixels which has sets of subpixels that correspond to the Red, Green and Blue those three basic colors. The molecules inside liquid Crystal rotated when voltage signals come in and display colors in each pixels.

11-3 I/O interface

Interface units interface between the bus from CPU and the peripheral devices. In addition to communicating with the I/O devices, the CPU of a computer must communicate with the memory unit through an address and data bus.

Two methods are used in order to communicate with I/O devices: memory-mapped I/O and the isolated I/O configuration.

11-4 Serial Communication

The transfer of data between two units may be parallel or serial. The parallel transmission is faster because signal lines operate parallel. The serial transmission is slower but cheaper and only need one conduct.

A half-duplex transmission system is capable of transmitting in both directions but only one direction a time.

A full-duplex can send and received data simultaneously from both direction.

The serial transmission of data can be synchronous or asynchronous. Synchronous signals are transmitted periodically, in contrast, the asynchronous transmission does not keep the clock frequency, the clock frequencies in each unit are different.

11-5 Modes of transfer

The data transfer to and from peripherals are handled in three ways:

1. Data transfer under program control
2. Interrupt-initiated data transfer
3. Direct memory access transfer

11-6 priority interrupt

When the system needs to decide which device to service first, priority interrupt occurs. A priority interrupt system establishes a priority over the various interrupt sources to determine which interrupt request to service first when two or more are pending simultaneously.

High speed devices are given high priority, low speed devices receive lowest priority.

The interrupt can be made hardware or software. Polling is not required when the interrupt decision are made by hardware priority unit.

The Daisy Chain method of establishing priority consists of a serial connection of all devices that request an interrupt. High priority devices are put in front of chain.

The parallel hardware interrupt uses a register with bit to determine the priority. The position of bits in the register affect the priority of devices.

11-7 Direct Memory Access (DMA)

The DMA release the CPU from the I/O operation and let the devices manage memory bus directly.

In this transfer technique, the DMA Controller access and control the memory temporary.

An address register, a word-count and a set of address lines are required for DMA Controller along with usual circuits that communicate with I/O device and CPU.

DMA transfer is very useful in many applications.