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Rockchip RV1106G EVB User Guide

(Fuzhou Hardware Development Center)

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	Approver:	
	Date:	

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Preface

Overview

This guide mainly introduces the basic functions and hardware features, multi-function hardware configuration, and software debugging operation methods of RV1106G EVB. It aims to help debuggers use RV1106G EVB be faster and more accurately, and be familiar with RV1106G chip development and application solutions.

Product version

The product versions corresponding to this document are as follows:

Product name	Product version
RV1106G EVB	RV1106G_EVB1_V11 20220402SQJ
SC530AI camera modules	RV1103_RV1106_EVB_Extboard_SENSOR_SC500AI_V10 20220112GXL
Camera modules conversion card	RV1103_RV1106_EVB_Extboard_SENSOR_40P_TO_24P_V10 20220112GXL

Intended Audience

This guide is mainly intended for:

- Hardware development engineers
- Layout engineers
- Technical support engineers
- Test engineers

Revision History

This revision history recorded description of each version, and any updates of previous versions are included in the latest one.

Version No.	Author	Revision Date	Revision Description	Remark
V1.0	Linus.Lin		First release (correspond to CN V1.1)	

Contents

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1. System overview

1.1. RV1106G chip introduction

RV1106 is a highly integrated vision processor SoC, especially for AI related application.

It is based on single-core ARM Cortex-A7 32-bit core which integrates NEON and FPU. There is a 32KB I-cache and 32KB D-cache and 128KB unified L2 cache. The build-in NPU supports INT4/INT8/INT16 hybrid operation and computing power is up to 0.5TOPs. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RV1106 introduces a new generation totally hardware-based maximum 5-Megapixel ISP (Image Signal Processor). It implements a lot of algorithm accelerators, such as HDR, 3A, LSC, 3DNR, 2DNR, sharpening, dehaze, gamma correction and so on. Cooperating with two MIPI CSI (or LVDS) and one DVP (BT.601/BT.656/BT.1120) interface, users can build a system that receives video data from multiple camera sensors simultaneous.

1.2. RV1106G chip diagram

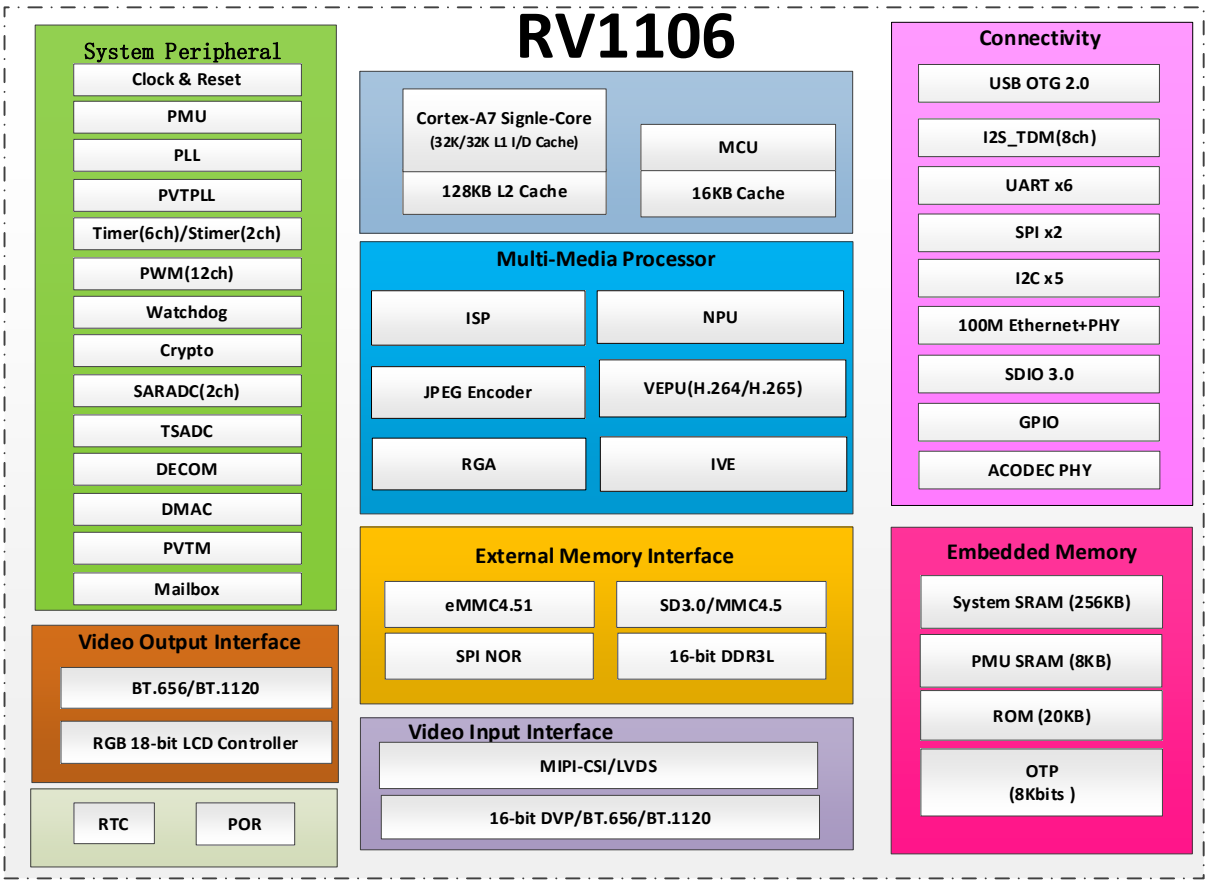

Figure 1-1 RV1106G chip diagram

1.3. System introduction

1.3.1. System diagram

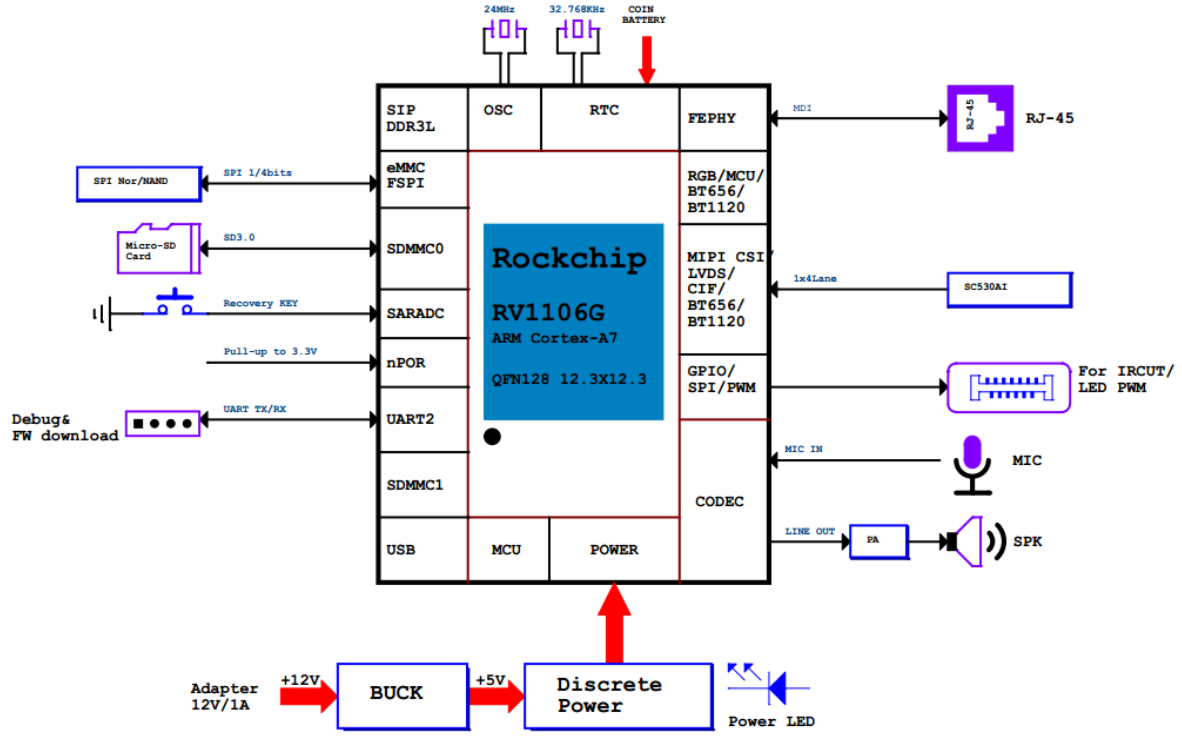

Figure 1-2 RV1106G application sample

1.3.2. Function overview

The RV1106G EVB provides the following functions:

- Power: DC 12V adapter power interface.
- Video input interface: supports 1x3Lane/2xLane MIPI, 8-16bit CIF, BT656 and BT1120 and others input methods. It supports multiple-camera input and peripherals input and others functions through the supporting expansion board.
- Video output interface: supports RGB 16bit/18bit, RGB 8bit, MCU, BT656 and BT1120 and others output methods. It supports multiple screen display function through the supporting expansion board.
- GPIO interface: supports GPIO input and output. Through the supporting expansion board, it can realize the motor drive, light plate drive, light sensing input and other functions.
- Internet interface: supports 1xRJ45 10/100 Ethernet.
- Audio interface: supports speaker output, single MIC record and single Line in.
- Wi-Fi: supports SDIO WIFI
- UART Debug: for user check debug LOG. It supports TYPEC AND Micro-B USB interface.
- JTAG: JTAG debug interface.
- System Key: include RESET, UPDATE, KEY1/RECOVER, KEY2.

- RTC: Support real-time clock, and it can be powered by the development board or button battery (CR1220-3V).

1.3.3. Function modules distribution

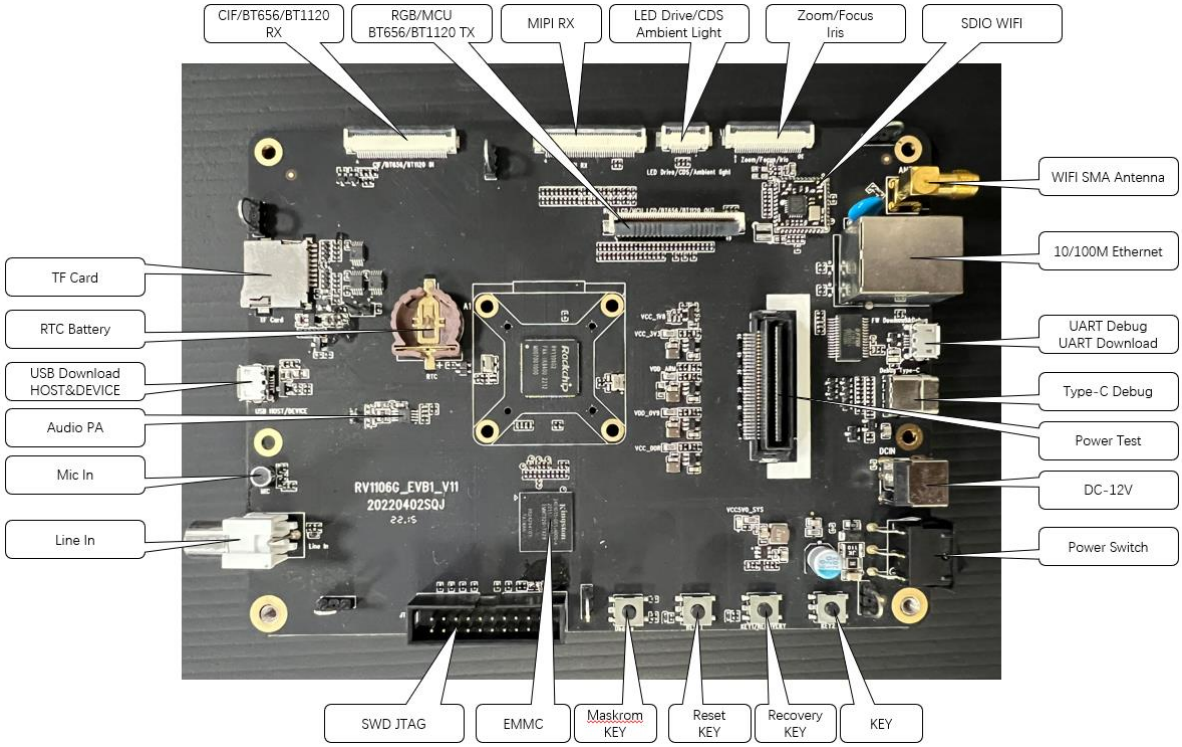

Figure 1-3 RV1106G EVB function interface distribution (front)

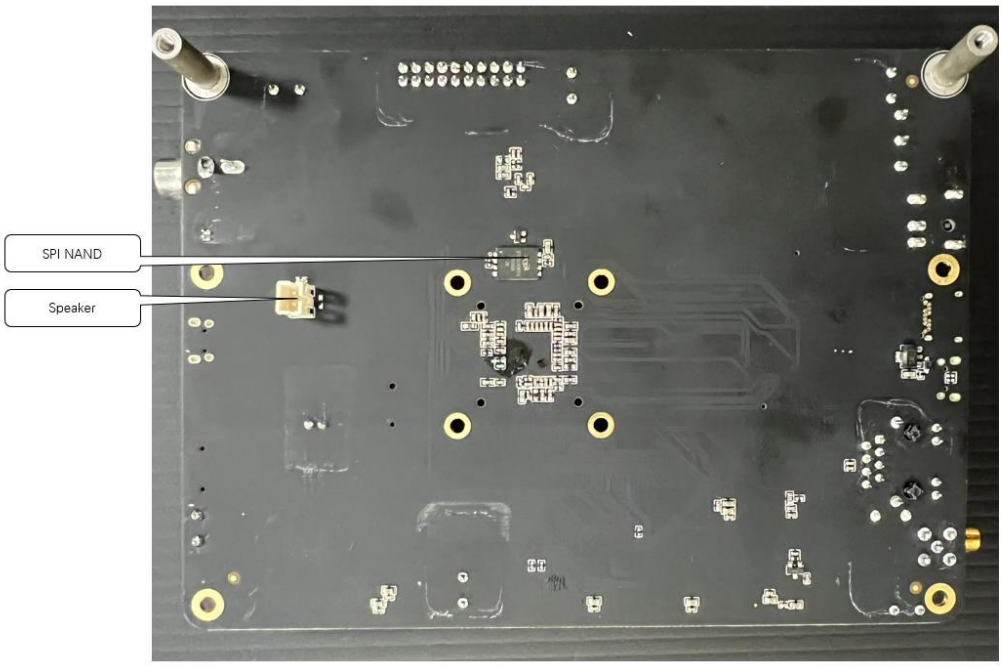

Figure 1-4 RV1106G EVB function interface distribution (back)

1.4. Modules

RV1106G EVB suite contains the following items:

- RV1106G EVB
- Power adapter. Specification: input 100V AC~240V AC, 50Hz, output 12V DC, 3A
- SC530AI single-camera module
- An antenna with 2.4G single-frequency SMA male head interface

1.5. Power on and off

- Power on

Powered by DC 12V, and turn on the power switch. When serial port output information means the firmware started successful.

- Power off

Turn off the power switch.

1.6. Firmware Download and Upgrade

RV1106G EVB supports USB, UART, TYTP, Micro-SD and others firmware updates method.

1.6.1. Driver Installation

The driver needs to be installed before the EVB driver is upgraded. The following describes the driver installation process under Windows system.

Find **DriverAssitant_v5.12** in the provided tool folder, and click **DriverInstall.exe** to pop up the following interface. Click "Install Driver" and wait for the prompt to install the driver successfully. If the old driver has been installed, please click "Uninstall Driver " and reinstall the driver.

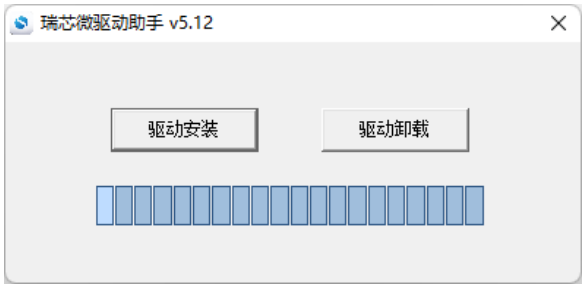

Figure 1-5 Drive Assistant installation screen

1.6.2. USB update mode

The specific steps are as follows:

1) Connect the USB HOST/DEVICE of Micro-B to the computer, press and hold the Update key on the mainboard.
2) Turn on the 12V power key. If it has been powered on, press the reset key.

3) After the programming tool shows that “a MASKROM device is found”, release the key.
4) Right-click the "Set Firmware Directory", then select the path where image is located, and click “OK”.
5) The update tool will automatically load the corresponding image file in the firmware directory. If the file name is not a standard name, click the ellipsis after the path to manually select the file.
6) Click Execute to enter the upgrade state. The right side of the tool is the progress display bar, which displays the download progress and verification status.

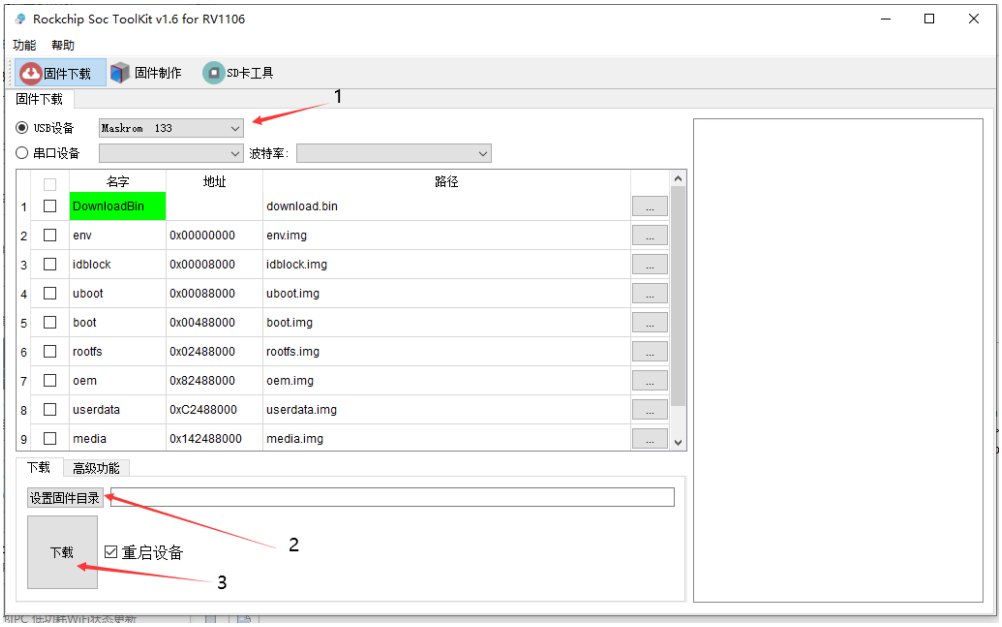

Figure 1-6 USB update method diagram

1.6.3. UART Update method

The specific steps are as follows:

1) Connect the USB HOST/DEVICE of Micro-B to the computer, press and hold the Update key on the mainboard.
2) Turn on the 12V power key. If it has been powered on, press the reset key.
3) After the programming tool shows that “a COM device is found”, release the key. Set the baud rate for the serial port. The value can be 115200 or 1500000.
4) Right-click the "Set Firmware Directory", then select the path where image is located, and click “OK”.
5) The update tool will automatically load the corresponding image file in the firmware directory. If the file name is not a standard name, click the ellipsis after the path to manually select the file.
6) Click Execute to enter the upgrade state. The right side of the tool is the progress display bar, which displays the download progress and verification status.

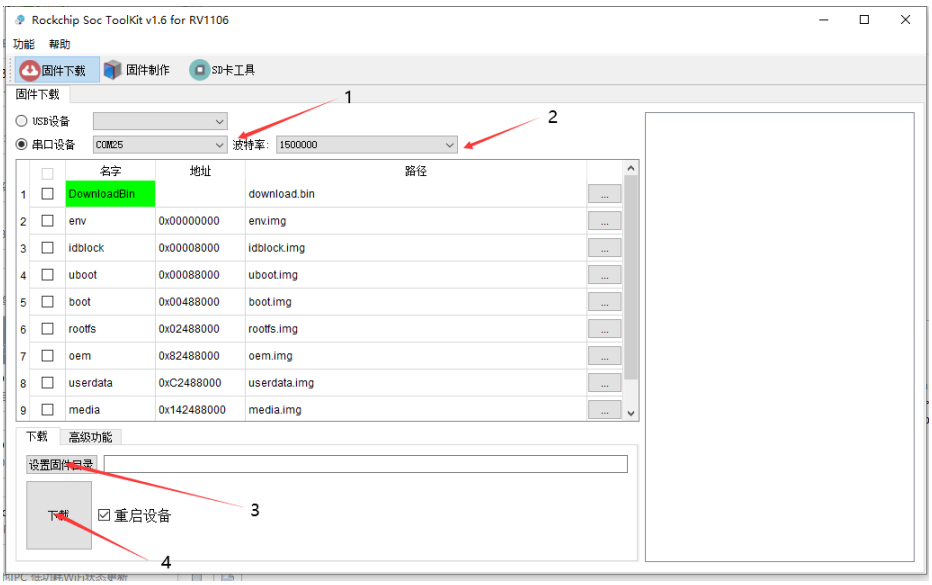

Figure 1-7 USB update method diagram

1.6.4. TFTP Update method

TFTP upgrade files will be compiled with the firmware in the "<sdk>/output/image/" directory. The file is named tftp_update.txt. The use method is as follows:

- Config the TFTP servers

TFTPD64 download address: https://pjo2.github.io/tftpd64

Note:

1) Use TFTPD64 software need to comply with relevant open source protocols.
2) All legal risks and other consequences that the TFTPD64 may bring is borne by the user.

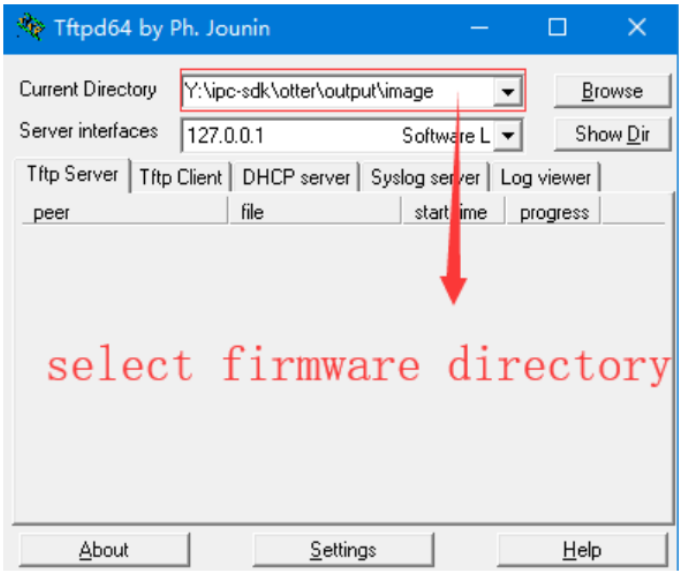

Figure 1-8 TFTP update mode

- Put the update file TFTP_UPDATEXT and all suffixes named .img in the directory specified by the server (Note: SLC NAND does not support the following firmware to update the idBLock partition.)
- Set the IP address on the U-Boot terminal (the IP address in the follow figure is for reference only. Please set it by yourself according to the actual scene to ensure that the client and the server are in the same network segment.)

```
=> setenv ipaddr 192.168.1.111
=> setenv serverip 192.168.1.100
=> saveenv
Saving Environment to envf...
=>
```

Figure 1-9 Setting the IP address on the U-Boot terminal

- Run “tftp_update” on the U-Boot terminal

```
=>  tftp_update
ethernet@ffc40000 Waiting for PHY auto negotiation to complete. done
Using ethernet@ffc40000 device
TFTP from server 192.168.1.100; our IP address is 192.168.1.111
Filename 'tftp_update.txt'.
Load address: 0x3be24c00
Loading: *•#
     203.1 KiB/s
done
Bytes transferred = 1250 (4e2 hex)
...
```

Figure 1-10 running the upgrade command on the U-Boot terminal

1.7. Serial Debugging

Connect the USB Debug of Micro-B debugging interface to the computer, and get the current port COM number in the device manager of the PC end.

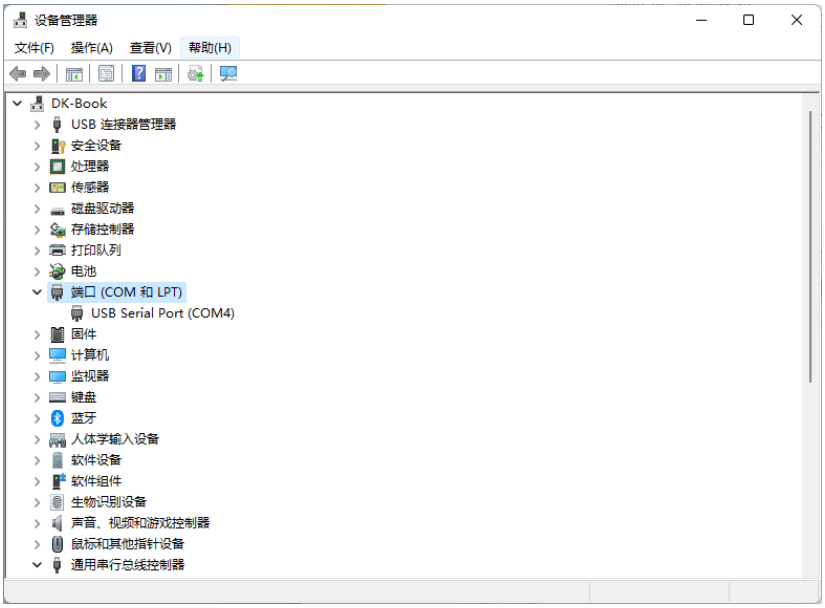

Figure 1-11 Get the Current Port COM Number

Open the serial port tool, under the "Quick Connect" interface, first select the serial port, then select the corresponding serial port number, change the baud rate to 115200, and close the flow control, Finally, click the "Open" button to enter the serial port debugging interface.

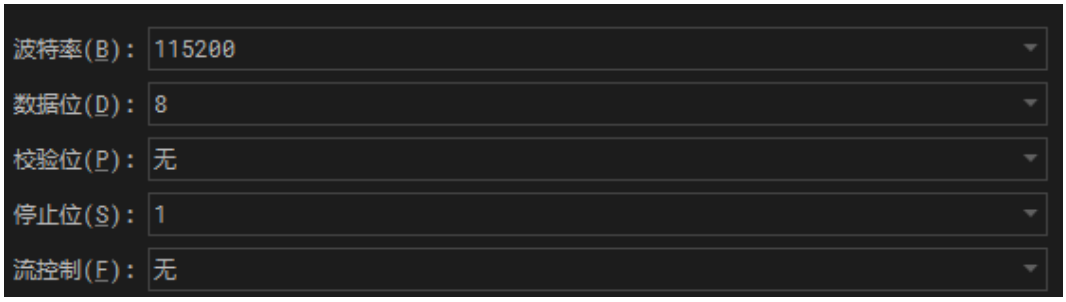

Figure 1-12 Serial Port Tool Configuration Interface

2. Hardware Introduction

2.1. The Pictures

Figure 2-1 RV1106G EVB

2.2. Power Block Diagram

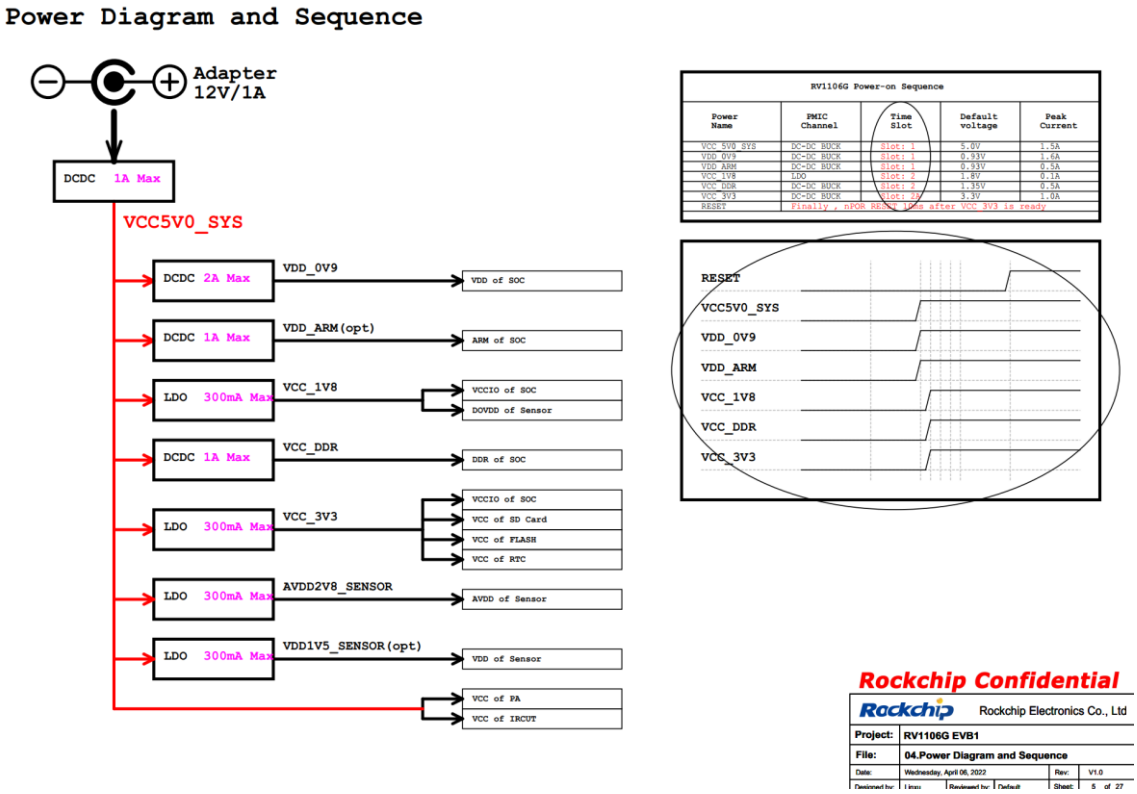

Figure 2-2 RV1106G EVB Block diagram

2.3. Extension Connector Information

The model of development board connector for the expansion board is as follows:

U4600 and U4700 are 0.15mm pins, and a horizontal single -row 40pin connector with a spacing of 0.5mm, the size is as follows:

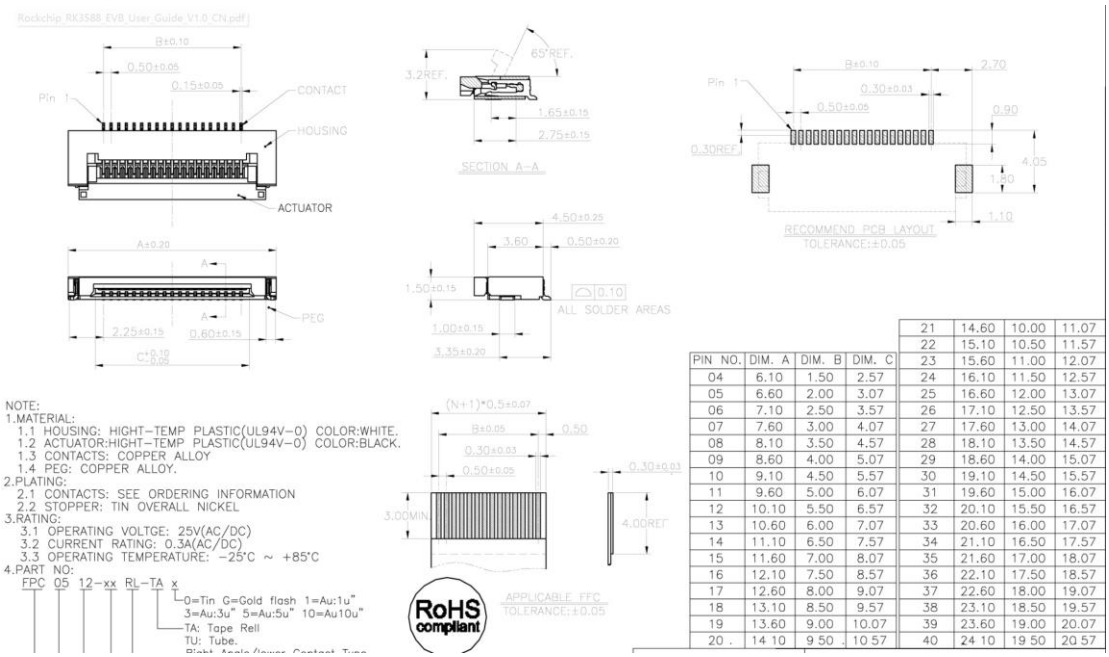

Figure 2-3 RV1106G EVB extension board connector

2.4. Reference Diagram

The reference diagram and PCB design information corresponding to the EVB are as follows:

- Schematic: RV1106G_EVB1_V11_20220401LX.DSN
- PCB: RV1106G_EVB1_V11_20220402SQJ.pcb

The reference diagram and PCB design information corresponding to the SC3336/SC4336 Camera module (used for 3M/4M camera debug) are as follows:

- Schematic: RV1103_RV1106_EVB_Exboard_SENSOR_SC3336_4336_V11_20220208.DSN
- PCB: RV1103_RV1106_EVB_Exboard_SENSOR_SC3336_4336_V11_20220208GXL.brd

The reference diagram and PCB design information corresponding to the SC500/530AI Camera module (used for 5M camera debug) are as follows:

- Schematic: RV1103_RV1106_EVB_Exboard_SENSOR_SC500AI_V11_20220418.DSN
- PCB: RV1103_RV1106_EVB_EXBOARD_SENSOR_SC500AI_V11_20220418GXL.brd

The reference diagram and PCB design information corresponding to the Camera conversion card (used for connecter EVB and modules) are as follows:

- Schematic: RV1103_RV1106_EVB_Exboard_SENSOR_40p_to_24p_V10_20220111.DSN
- PCB: RV1103_RV1106_EVB_EXBOARD_SENSOR_40P_TO_24P_V10_20220112GXL.brd

The reference diagram and PCB design information corresponding to the extension board of CVBS TO BT656 (used for BT656 input) are as follows:

- Schematic: RV1103_RV1106_EVB_Extboard_CVBS_to_BT656_V10_20220223LX.DSN
- PCB: RV1103_RV1106_EVB_Extboard_CVBS_to_BT656_V10_20220223KYY.pcb

The reference diagram and PCB design information corresponding to the binocular camera extension board (used for binocular camera debug) are as follows:

- Schematic: RV1103_RV1106_EVB_Exboard_SENSOR_Dual_mipi_V10_20220120.DSN
- PCB: RV1103_RV1106_EVB_Exboard_SENSOR_Dual_mipi_V10_20220211LXF.pcb

The reference diagram and PCB design information corresponding to the extension board of TF to UART (used for debug) are as follows:

- Schematic: RV1103_RV1106_EVB_Extboard_TF2JTAG_V10_20220323.DSN
- PCB: RV1103_RV1106_EVB_Extboard_TF2JTAG_V10_20220324LXF.pcb

3. Module Brief

3.1. Power Input

The power adapter inputs 12V/3A power, after passing the front-end buck converter power supply, the system power VCC5V0_SYS is obtained, and then the system voltage is provided to other PMIC, and 5 different voltages are output for system use.

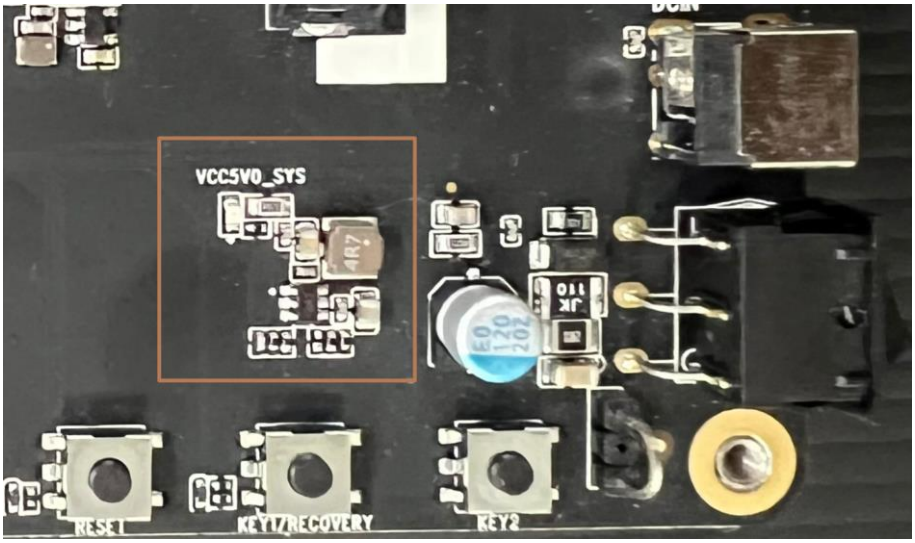

Figure 3-1 RV1106G EVB power input

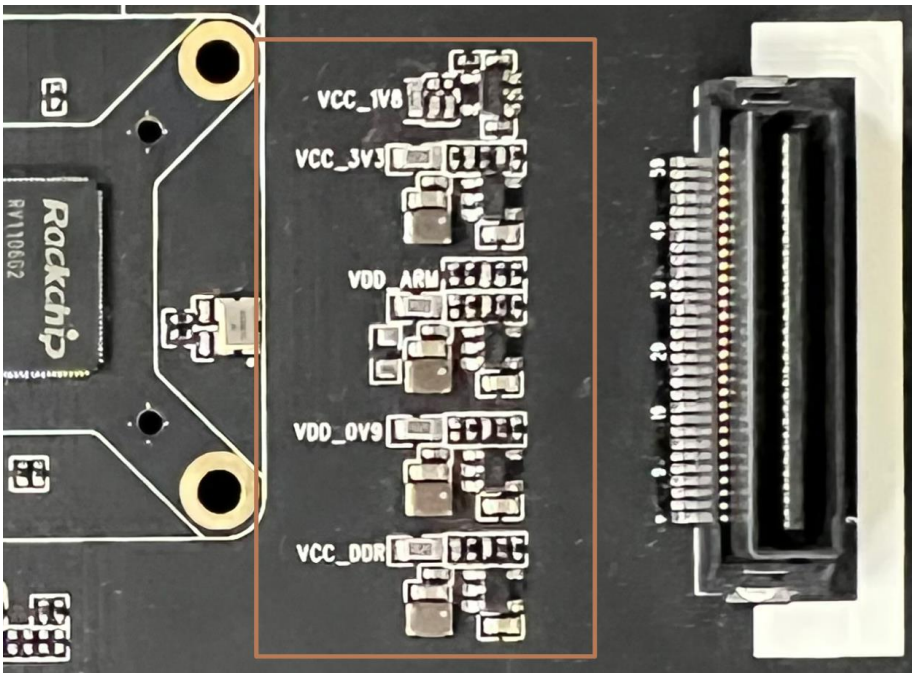

Figure 3-2 RV1106G EVB power output

3.2. Memory

There are two memory on the RV1106G EVB, which are SPI Flash and eMMC Flash, and the default is SPI Flash.

If you need to use EMMC Flash, please note that the Flash power supply configuration in Figure 3-3 needs to be modified to 1.8V. The EMMC signal selection resistance in Figure 3-4 needs to be pasted and disconnected the SPI Flash signal selection resistance.

- SPI Flash: The type on the development board is SPI Flash, and the capacity by default is 1GB.
- EMMC: The EMMC Flash device is reserved for the development board.

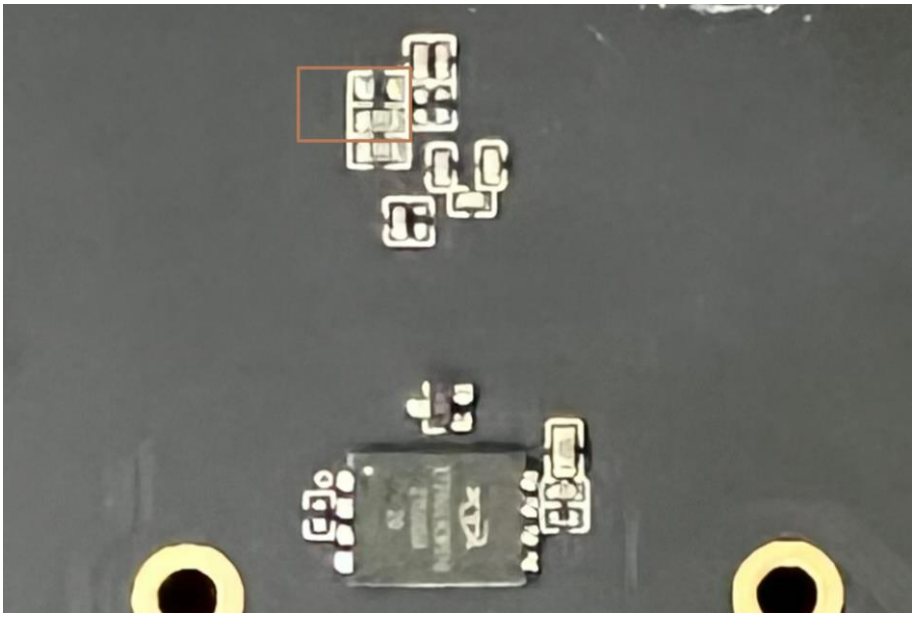

Figure 3-3 RV1106G EVB SPI FLASH

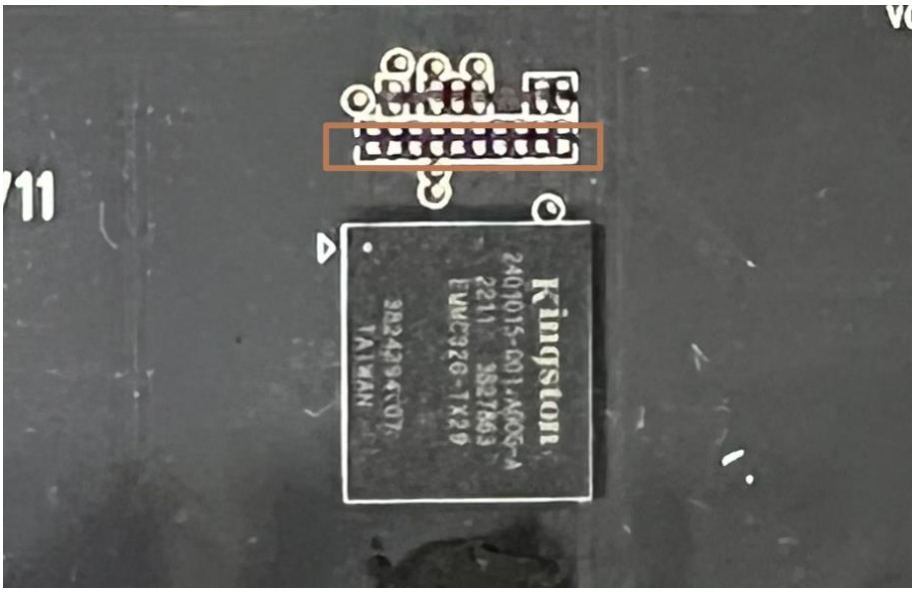

Figure 3-4 RV1106G EVB EMMC FLASH

The key position of EVB into MASKROM programming:

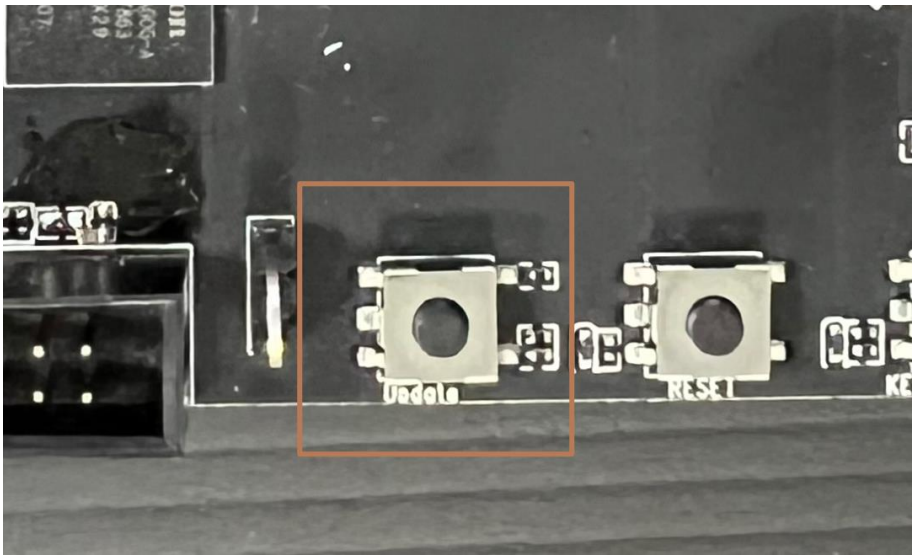

Figure 3-5 Key Position of EVB into MASKROM Programming

3.3. RTC

The RV1106G EVB uses the chip's own RTC, which can be powered by the development board (under power supply) or the CR1220-3V button battery (under the power of power) through the electrical selection circuit to ensure that accurate real-time clocks can be continuously provided.

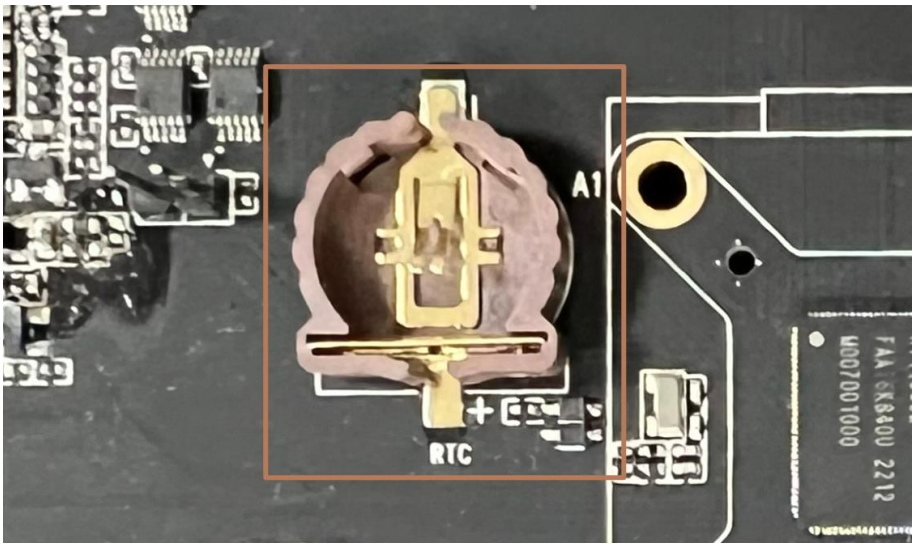

Figure 3-6 RV1106G EVB RTC battery holder

3.4. Keys

The development board uses SARADC_IN0(KEY1) and SARADC_IN1(KEY2) as the RECOVER detection port, supports 10-bit resolution. The KEY1/RECOVERY key is used to enter programming mode; KEY2 keys can be configured for other purposes; RESET button used to reset the hardware.

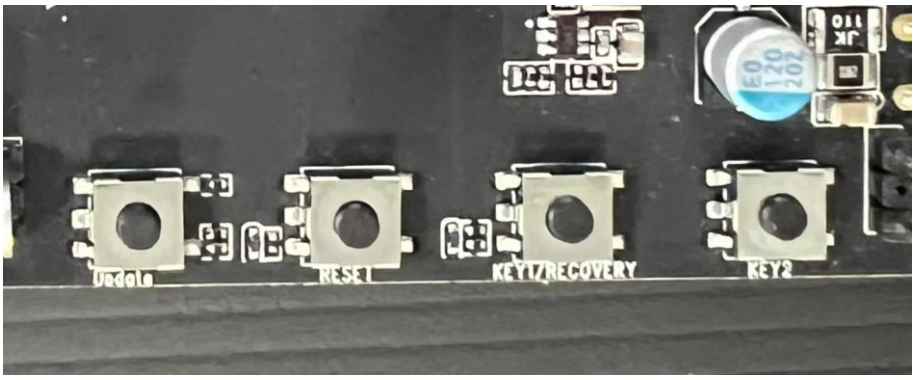

Figure 3-7 keys position

3.5. Ethernet Port

The development board supports RJ45, which can provide 10/100M Ethernet connection function.

- Compatible with IEEE802.3 standard, supports full-duplex and half-duplex operation, support cross detection and self-adaptation.
- Support 10/100M rate.
- The interface adopts the combination of RJ45 interface with isolation transformer and indicator light.

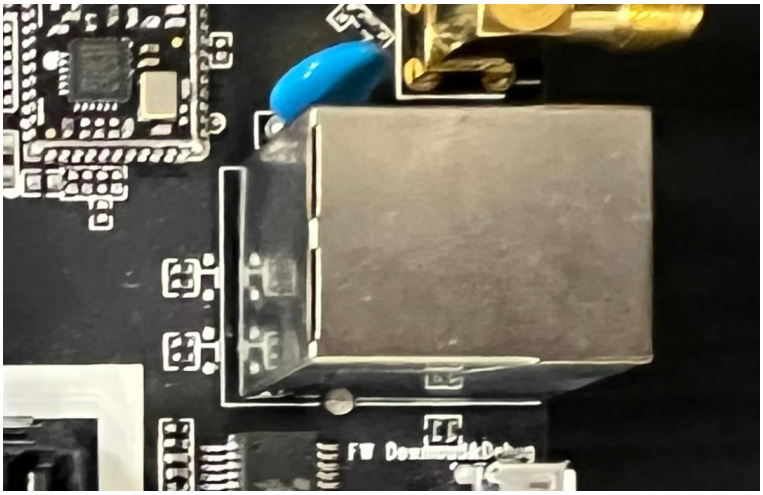

Figure 3-8 RV1106G EVB Ethernet port

3.6. WIFI interface

EVB adopts the Fn-Link single WIFI module.

- Based on the RTL8189FTV chip
- Supports 1x1WIFI(2.4G， 802.11 b/g/n), and 1 external SMA interface antennas.
- Powered by 3.3V, supporting SDIO2.0 and SDIO3.0 modes.

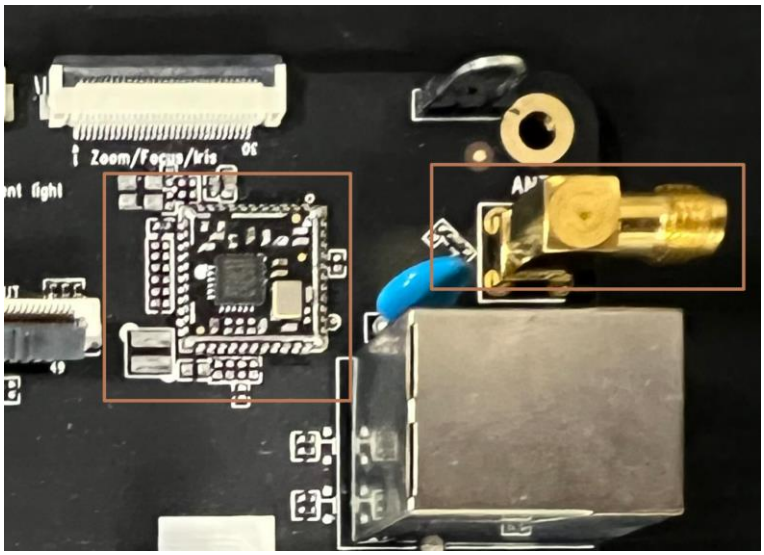

Figure 3-9 RV1106G EVB WIFI

3.7. UART debug interface

The development board supports the Micro USB debug interface. If use the Type-C interface to debug, the R9337/R9338 resistance on the back of the interface is needed.

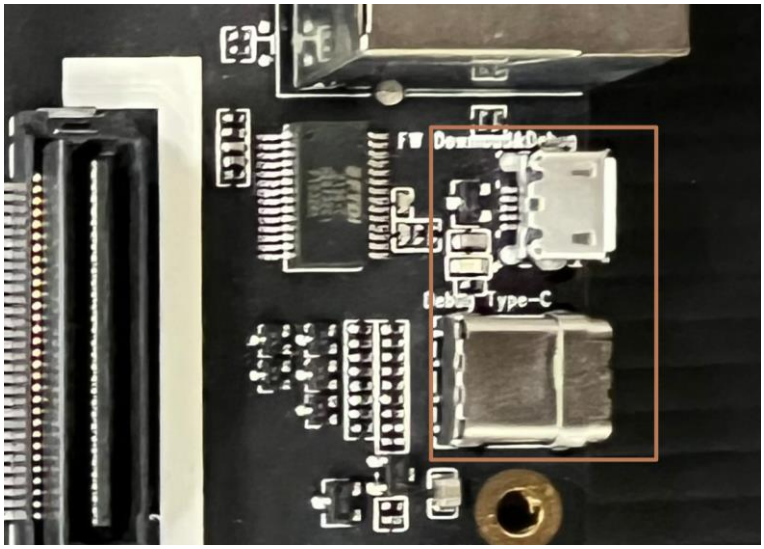

Figure 3-10 RV1106G EVB UART debug interface

3.8. JTAG debug interface

The development board reserves 1xJTAG interface. RV1106G's JTAG interface and SDMMC interface are reused, so the interface is used as a JTAG debug port when no TF card. If the TF card is inserted, it will be forced to switch to the TF card mode. The JTAG mode will be available.

The JTAG connector supports ARM/HPMCU/LPMCU JTAG and switches through a pin and jump cap: As shown in Figure 3-11. When J9305 is suspended, the JTAG connection seat is the LPMCU debug mode. After the jumper jumping cap is connected to the jump cap, the JTAG connection seat is ARM/HPMCU debugging mode.

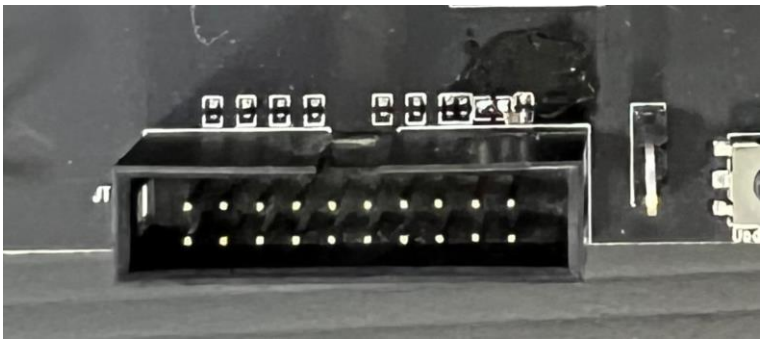

Figure 3-11 RV1106G EVB JTAG connector

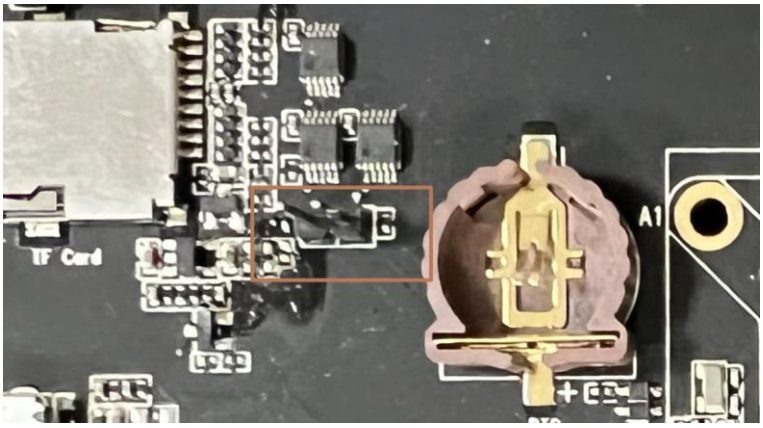

Figure 3-12 RV1106G EVB JTAG mode switch pin

3.9. MIPI input interface

The MIPI input interface adopts a horizontal 40pin connector with a spacing of 0.5mm (see Section 2.3 for specifications), supporting dual MIPI input.

- Support IRCUT switching circuit, and control the module in day or night mode
- Supports 1x4lane and 2x2lane input modes
- MCLK1 and FSYNC signals are reserved on the module, which can be extended for binocular applications as required

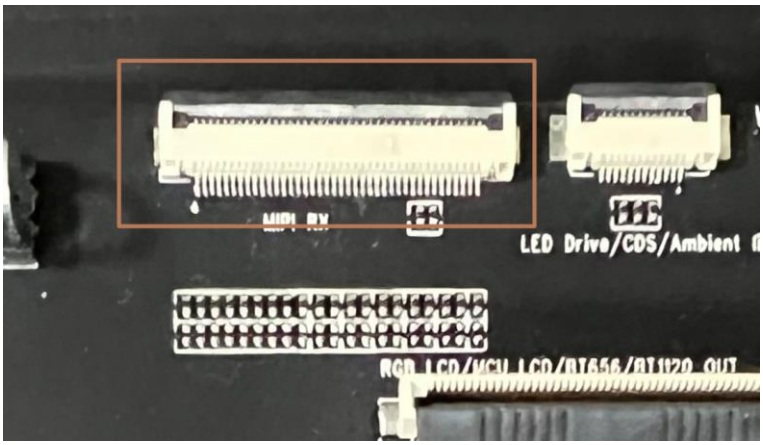

Figure 3-13 RV1106G EVB MIPI input interface

The MIPI RX interface signal sequence is as follows:

No.	Signal	IO level	No.	Signal	IO level
1	GND		21	MIPI_PDN0	1.8V
2	LVDS/MIPI_D0N		22	MIPI_PWREN0	3.3V
3	LVDS/MIPI_D0P		23	I2C_SCL/SPI_CLK	1.8V
4	GND		24	I2C_SDA/SPI_MOSI	1.8V
5	LVDS/MIPI_D1N		25	FSYNC_IN/SPI_MISO	1.8V
6	LVDS/MIPI_D1P		26	GND/SPI_CSN	
7	GND		27	GND	
8	LVDS/MIPI_CLK0N		28	5V0	
9	LVDS/MIPI_CLK0P		29	5V0	
10	GND		30	5V0	
11	LVDS/MIPI_D2N		31	GND	
12	LVDS/MIPI_D2P		32	IRCUT_A	3.3V
13	GND		33	IRCUT_B	3.3V
14	LVDS/MIPI_D3N		34	MIPI_RST1	1.8V
15	LVDS/MIPI_D3P		35	GND	
16	GND		36	MIPI_MCLK1	1.8V
17	MIPI_CLK0	1.8V	37	GND	
18	GND		38	LVDS/MIPI_CLK1N	
19	1V8_OUT	1.8V	39	LVDS/MIPI_CLK1P	
20	MIPI_RST0	1.8V	40	GND	

3.10. CIF/BT656/BT1120 input interface

CIF/BT656/BT1120 input interface adopts horizontal 40pin connector with spacing of 0.5mm (see Section 2.3 for specifications), supporting one of three inputs.

- Supports a maximum of 16bit CIF input.

- Support BT656/BT1120 input
- The MIPI signal and CIF/BT656/BT1120 signal share the same IO group. Therefore, the CIF input interface and MIPI input interface can only input one at the same time.

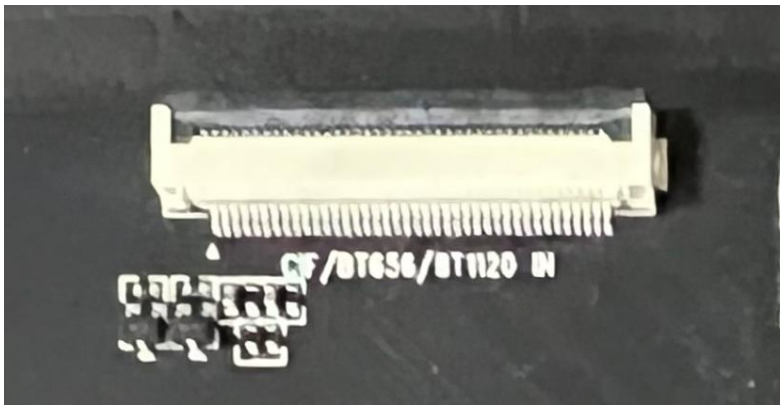

Figure 3-14 RV1106G EVB CIF/BT656/BT1120 input interface

The CIF/BT656/BT1120 interface signal sequence is as follows:

No.	Signal	IO level	No.	Signal	IO level
1	CIF_PDN1	1.8V	21	CIF_D3/BT1120_D3	1.8V
2	GND		22	CIF_D4/BT1120_D4	1.8V
3	CIF_SDA	1.8V	23	CIF_D1/BT1120_D1	1.8V
4	CIF_AVDD		24	CIF_D0/BT1120_D0	1.8V
5	CIF_SCL	1.8V	25	GND	
6	CIF_RESET	1.8V	26	CIF_D10/BT1120_D10/ BT656_D2	1.8V
7	CIF_VSYNC	1.8V	27	CIF_D11/BT1120_D11/ BT656_D3	1.8V
8	CIF_PDN0	1.8V	28	VCC5V0_SYS	
9	CIF_HREF	1.8V	29	VCC5V0_SYS	
10	CIF_DVDD		30	VCC5V0_STS	
11	CIF_DOVDD		31	GND	
12	CIF_D9/BT1120_D9/ BT656_D1	1.8V	32	VCC3V3_SYS	
13	CIF_CLKOUT	1.8V	33	GPIO	
14	CIF_D8/BT1120_D8/ BT656_D0	1.8V	34	FLASH_TRIGOUT	
15	GND		35	PRELIGHT_TRIGOUT	
16	CIF_D7/BT1120_D7	1.8V	36	CIF_D12/BT1120_D12/ BT656_D4	1.8V

No.	Signal	IO level	No.	Signal	IO level
17	CIF_CLKIN/ BT1120_CLKIN/ BT656_CLKIN	1.8V	37	CIF_D13/BT1120_D13/ BT656_D5	1.8V
18	CIF_D6/BT1120_D6	1.8V	38	CIF_D14/BT1120_D14/ BT656_D6	1.8V
19	CIF_D2/BT1120_D2	1.8V	39	CIF_D15/BT1120_D15/ BT656_D7	1.8V
20	CIF_D5/BT1120_D5	1.8V	40	GN	

3.11. LED interface

The LED interface is a horizontal 12pin connector with a spacing of 0.5mm (see Section 2.3 for specifications) for controlling the light panel display, photoresistor input, and ambient light detection input.

- Supports white light and infrared complementary light output.

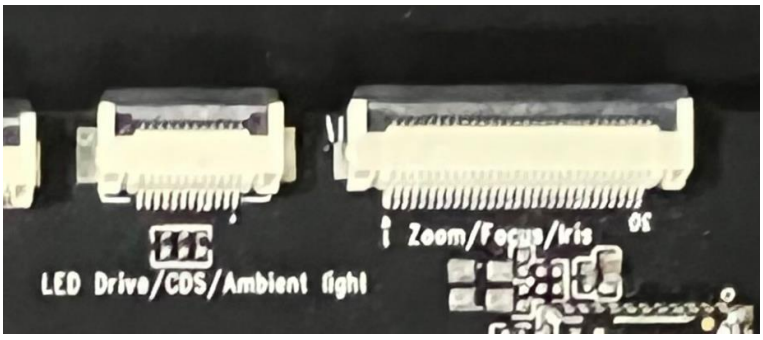

Figure 3-15 RV1106G EVB LED interface

The LED interface signal sequence is as follows:

No.	Signal	IO level	No.	Signal	IO level
1	VCC5V0_SYS		7	LED_PWM_WHITE	3.3V
2	VCC5V0_SYS		8	CDS_IN	1.8V
3	VCC5V0_SYS		9	SENSOR_INT	1.8V
4	GND		10	GND	
5	GND		11	MIPI_I2C_SDA	1.8V
6	LED_PWM_IR	3.3V	12	MIPI_I2C_SCL	1.8V

3.12. Display Output interface

The RGB/BT656/BT1120 display interface adopts a horizontal 50-pin connector with a spacing of 0.5mm (see Section 2.3 for specifications), supporting one of three outputs. Because the display signal and SDIO/PWM signal share the same group of IO, only one output can be selected at the same time, and the default output is SDIO/PWM. If the display interface is required, adjust the configuration resistance shown

in Figure 3-16.

- Supports up to 18bit RGB output.
- Supports the output of BT656/BT1120

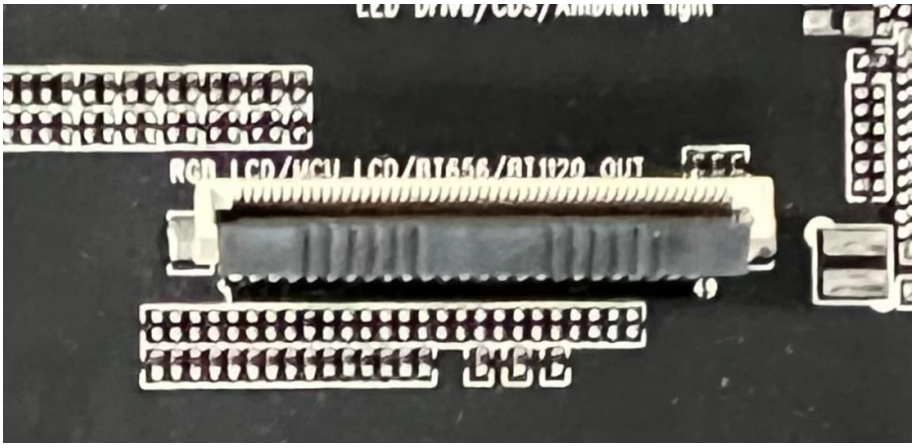

Figure 3-16 RV1106G EVB display output interface

The RGB/BT656/BT1120 display interface signal sequence is as follows:

No.	Signal	IO level	No.	Signal	IO level
1	GND		26	LCDC_D19/BT656_D19	3.3V
2	LCDC_D0/BT656_D0	3.3V	27	LCDC_D20/BT656_D20	3.3V
3	LCDC_D1/BT656_D1	3.3V	28	GND	
4	LCDC_D2/BT656_D2	3.3V	29	LCDC_D21/BT656_D21	3.3V
5	LCDC_D3/BT656_D3	3.3V	30	LCDC_HSYNC/ BT1120_D13	3.3V
6	LCDC_D4/BT656_D4	3.3V	31	LCDC_VSYNC/ BT1120_D14	3.3V
7	LCDC_D5/BT656_D5	3.3V	32	LCDC_DEN/BT1120_D15	3.3V
8	LCDC_D6/BT656_D6	3.3V	33	LCDC_D22	3.3V
9	LCDC_D7/BT656_D7	3.3V	34	LCDC_D23	3.3V
10	GND		35	GND	
11	LCDC_CLK/BT656_CLK	3.3V	36	PWM/LCD_INT	3.3V
12	GND		37	GPIO1/I2C_SCL	3.3V
13	LCDC_D8/BT656_D8	3.3V	38	GPIO2/I2C_SDA	3.3V
14	LCDC_D9/BT656_D9	3.3V	39	GPIO3/SPI_CSN/LCD_RST	3.3V
15	LCDC_D10/BT656_D10	3.3V	40	GPIO4/SPI_MISO/ LCD_PWREN	3.3V
16	LCDC_D11/BT656_D11	3.3V	41	GPIO5/SPI_MOSI	3.3V
17	LCDC_D12/BT656_D12	3.3V	42	GPIO6/SPI_CLK	3.3V
18	GND		43	GND	

No.	Signal	IO level	No.	Signal	IO level
19	LCDC_D13/BT656_D13	3.3V	44	GND	
20	GND		45	VCC3V3_SYS	
21	LCDC_D14/BT656_D14	3.3V	46	GND	
22	LCDC_D15/BT656_D15	3.3V	47	VCC1V8_SYS	
23	LCDC_D16/BT656_D16	3.3V	48	GND	
24	LCDC_D17/BT656_D17	3.3V	49	VCC5V0_SYS	
25	LCDC_D18/BT656_D18	3.3V	50	VCC5V0_SYS	

3.13. USB2.0 interface

The EVB board supports 1xUSB2.0 OTG. The interface is a standard Micro-B port, which is convenient for user to programming and debugging

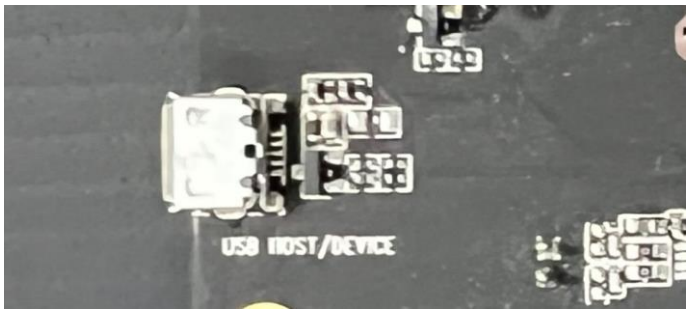

Figure 3-17 RV1106G EVB USB2.0 interface

3.14. TF card

The EVB board supports a TF card interface, and supports SDMMC2.0 and SDMMC3.0 modes.

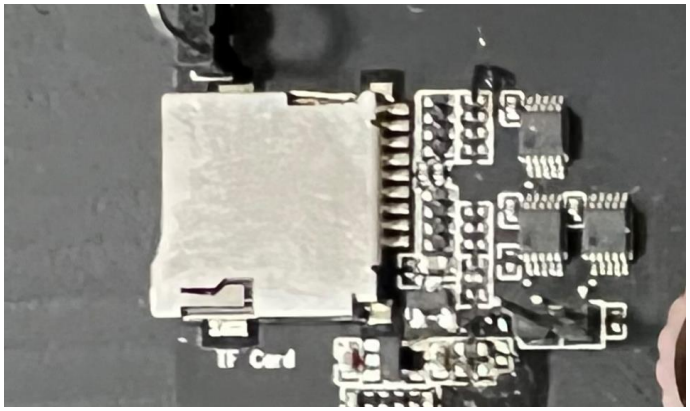

Figure 3-18 RV1106G EVB TF cart interface

3.15. Audio interface

The EVB board supports two audio inputs, one for differential mic input, the other for line in input, and the input amplitude shall not exceed 3.3V.

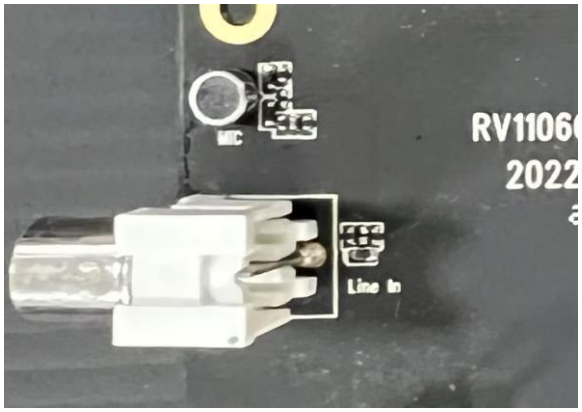

Figure 3-19 RV1106G EVB audio interface

3.16. Audio output

One Speaker interface is reserved on the EVB board, which supports a maximum output power of 3W (10% THD, 4ohm speaker).

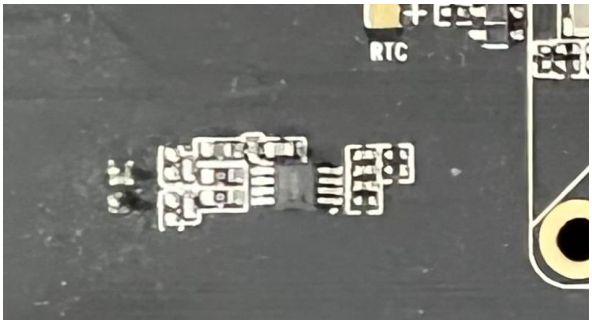

Figure 3-20 RV1106G EVB Power amplifier chip

Figure 3-21 RV1106G EVB speaker connector

3.17. Power test interface

The EVB board has reserved a power test interface for power consumption test.

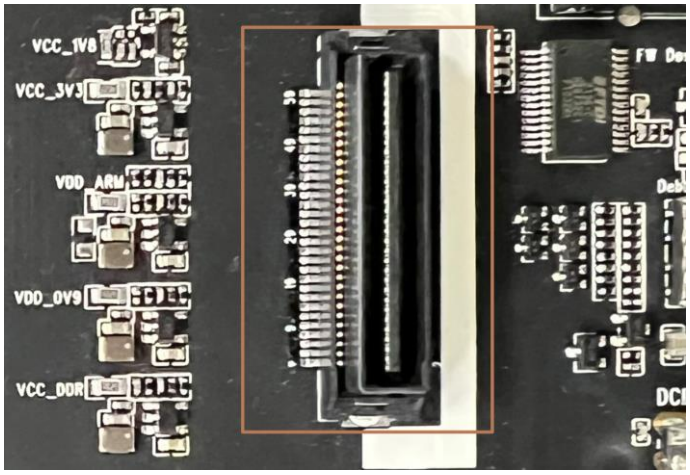

Figure 3-22 RV1106G EVB power test interface

4. Precautions

RV1106G EVB is suitable for laboratory or engineering environment, please read the following precautions before operation:

- Under no circumstances can the screen interface and expansion board be hot-swapped.
- Before unpacking and installing the development board, take necessary anti-static measures to avoid electrostatic discharge (ESD) damage to the development board hardware.
- When holding the development board, please hold the edge of the development board, and do not touch the exposed metal parts of the development board, so as to avoid damage to the components of the development board caused by static electricity.
- Please place the development board on a dry surface to keep them away from heat sources, electromagnetic interference sources and radiation sources, electromagnetic radiation sensitive equipment (such as medical equipment), etc.