Demo Board For RV1106

RV1106G AI IPC V1.3

Reference Design Main Functions Introduction	
Power	4 DCDC + 4 LDO (or 3 DCDC + 4 LDO)
RAM	SPI FLASH
Interface	SDMMC/SDIO/MIPI_CSI/LVDS_RX/VI_CIF/ VI_BT656/VI_BT1120/I2S/USB/ADC

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Project:	RV1106G AI IPC				
File:	00.Cover Page				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	1 of 20

Index and Notes

Catalogue

Note

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Generate Bill of Materials

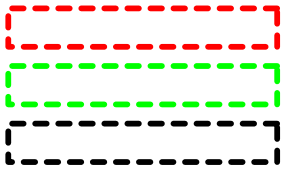
Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Graphic Description



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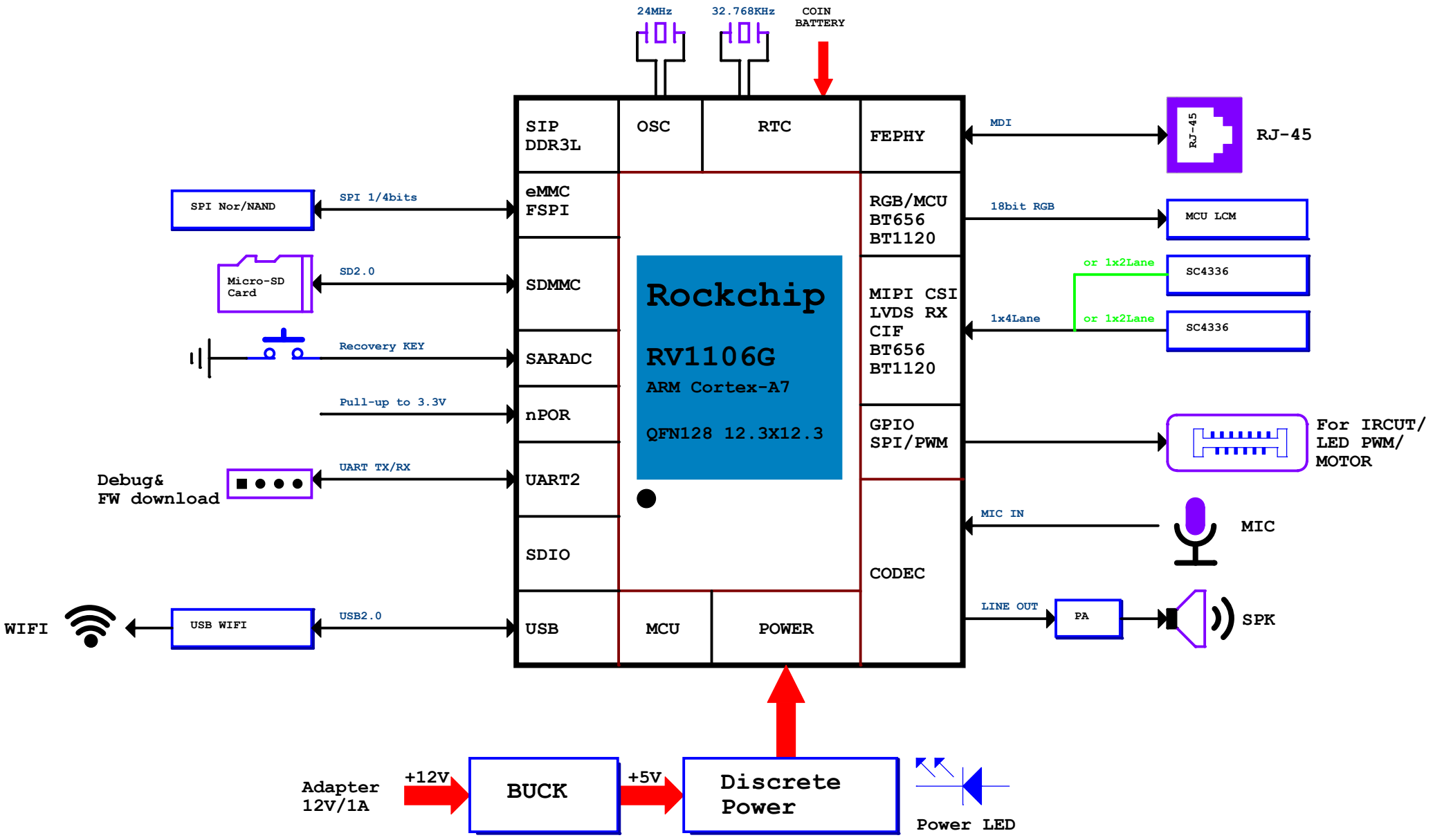
Project:	RV1106G AI IPC				
File:	01.Index and Notes				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	2 of 20

Revision History

Version	Date	Author	Change Note	Approved
V1.0	2022.04.21	Linxu	First edition;	
V1.1	2022.05.27	Linxu	1.Update RV1106G symbol; 2.Change netname of SDMMC0 to SDMMC; 3.Change C1000 to 4.7uF. 4.Change R2005 to 47K. 5.Change DOVDD1V8 to DOVDD_1V8. 6.Add R1006 and connect R8100 to CODEC_AVSS 7.Swap R8100/R8101 and C8101/C8102.	
V1.2	2022.11.14	Linxu	1.Change R1110 to 1K and C1114 to 10nF; 2.Add R1111/R1112; 2.Add FB1001;	
V1.3	2023.11.10	Linxu	1.Add ED6000 / ED6001. 2.Add USB WIFI / Motor Drive / MCU LCM circuit. 3.Add VO / VI / Power Description. 4.Add IRCUT U9901. 5.Delete AVDD1V5_SENSOR Power circuit. 6.Delete TP1202 / TP1203. 7.Change R8204 to 4.7uF, L4700 to L0402. 8.Modify SC530AI to 2xSC4336 for dual-camera. 9.Change R1106 / R1108 to 510R.	

Block Diagram



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Project:	RV1106G AI IPC				
File:	03.Block Diagram				
Date:	Friday, November 10, 2023			Rev:	V1.3
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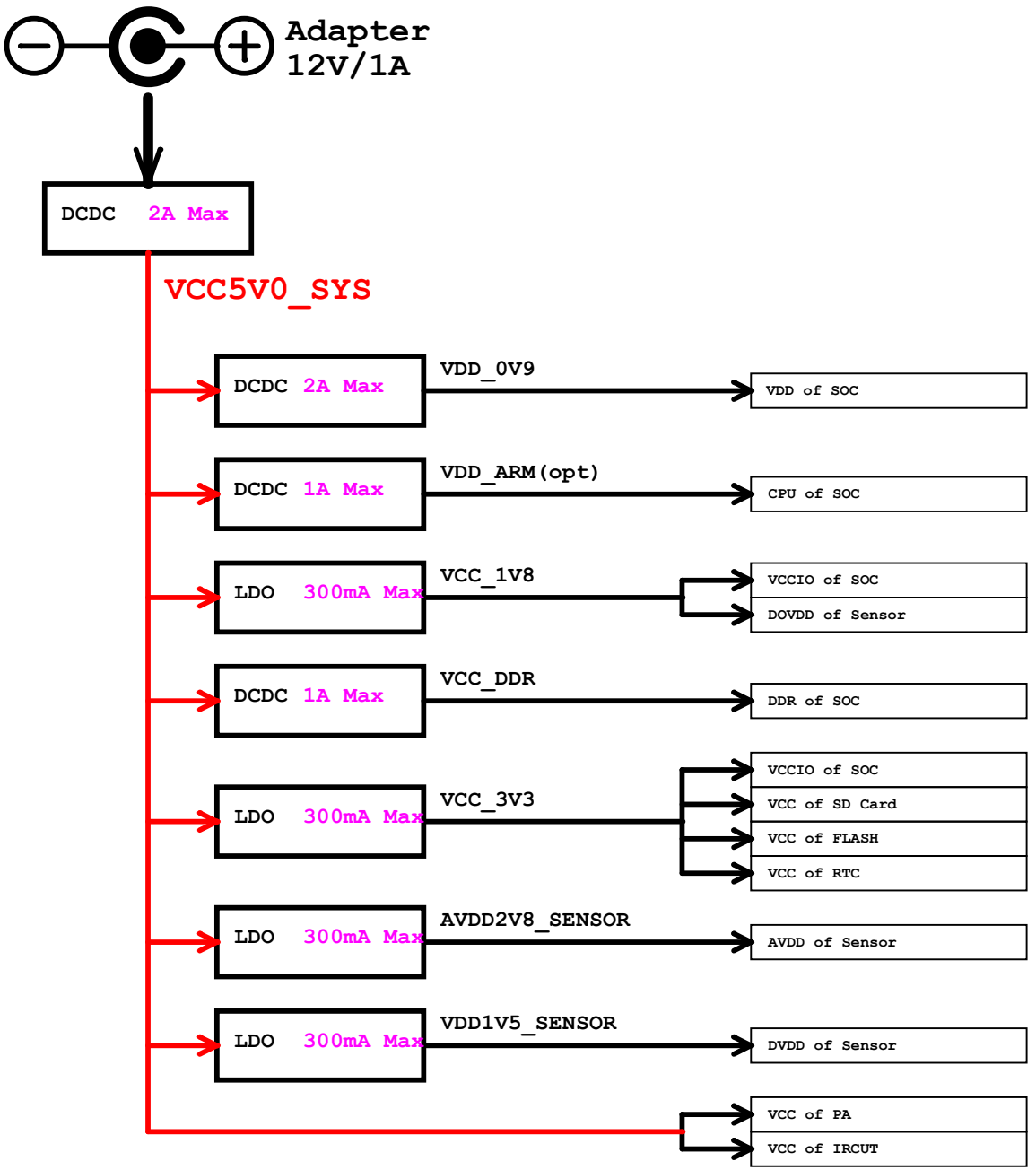
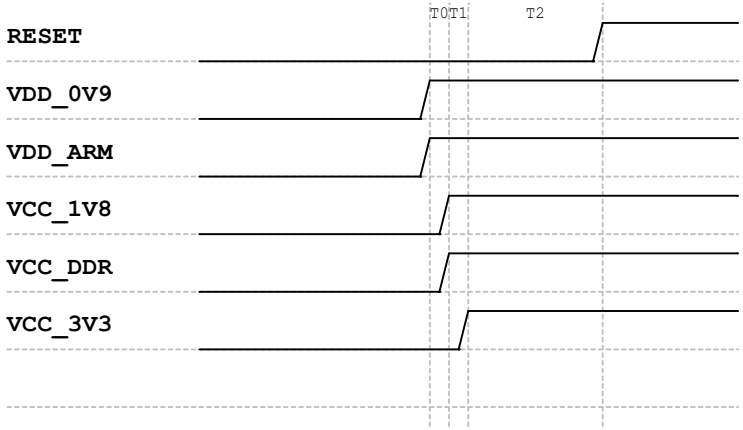
Power Diagram and Sequence



Power-on Sequence

Power Name	PMIC Channel	Time Slot	Default voltage	Peak Current
VCC5V0_SYS	DC-DC BUCK		5.0V	1.5A
VDD_0V9	DC-DC BUCK	Slot: 1	0.88V	1.6A
VDD_ARM	DC-DC BUCK	Slot: 1	0.90V	0.5A
VCC_1V8	LDO	Slot: 2	1.80V	0.1A
VCC_DDR	DC-DC BUCK	Slot: 2	1.35V	0.5A
VCC_3V3	LDO	Slot: 3	3.30V	0.2A
RESET	Finally , nPOR RESET 10ms after VCC_3V3 is ready			

Note:
T0、T1 > 1ms
T2 = 10ms (Internal)
Trise > 100us



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Project:	RV1106G AI IPC				
File:	04.Power Diagram and Sequence				
Date:	Friday, November 10, 2023			Rev:	V1.3
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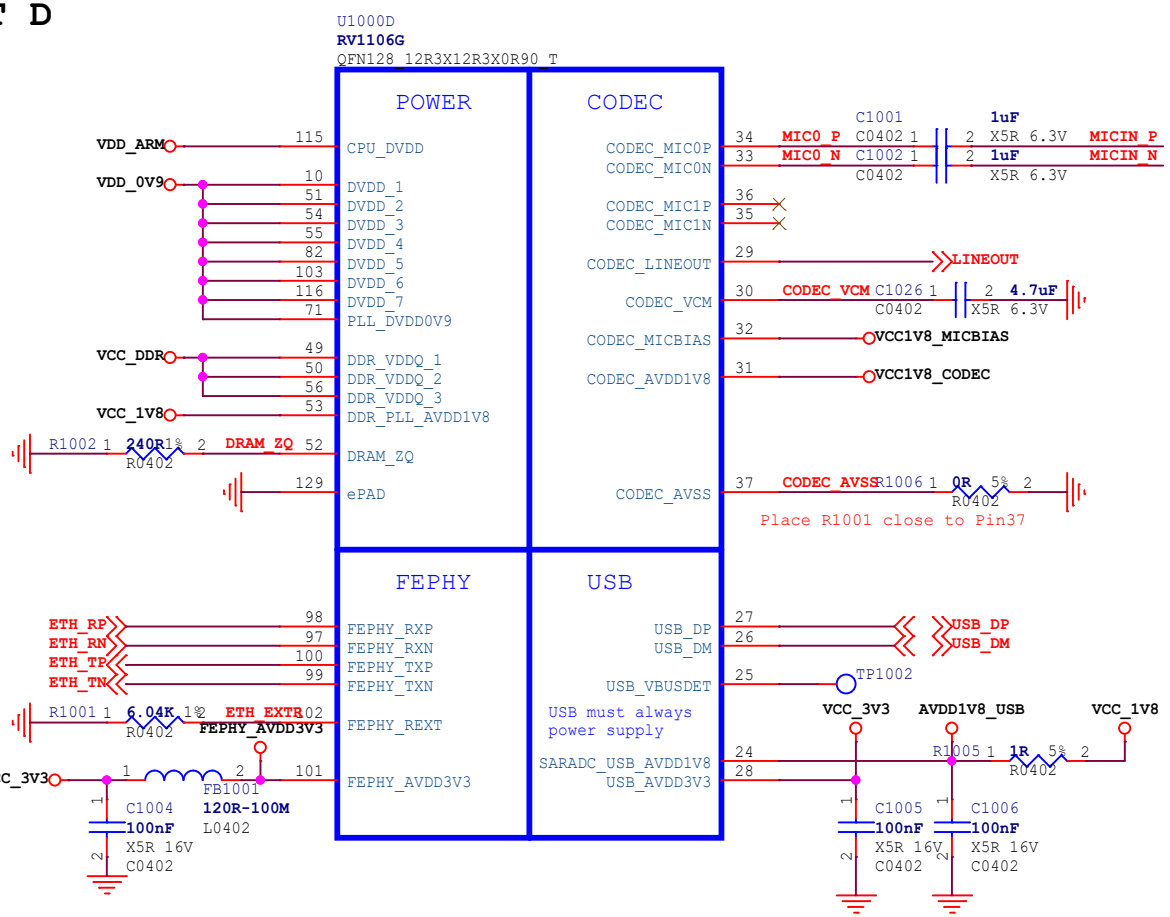
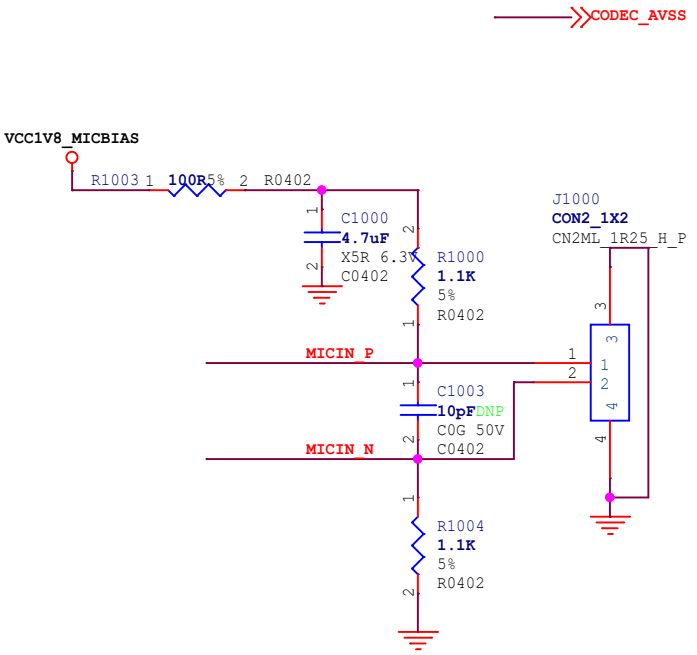
IO Power Domain Map

IO Domain	IO Group	Support of IO Voltage		Default Actual assigned IO Domain Voltage			Remark
		1.8V	3.3V	Net Name of Power Supply	Power Source	Voltage	
PMU	Group GPIO0_A		✓	VCC_3V3		3.3V	
VCCIO1	Group GPIO1_AB		✓	VCC_3V3		3.3V	
VCCIO2	Group GPIO4_C	✓		VCC_1V8		1.8V	
VCCIO3	Group GPIO4_AB	✓	✓	VCCIO_FLASH		1.8/3.3V	
VCCIO4	Group GPIO3_A	✓	✓	VCCIO_SD		1.8/3.3V	
VCCIO5	Group GPIO2_AB	✓	✓	VCC_3V3		3.3V	
VCCIO6	Group GPIO1_CD	✓	✓	VCC_3V3		3.3V	
VCCIO7	Group GPIO3_BCD	✓		VCC_1V8		1.8V	

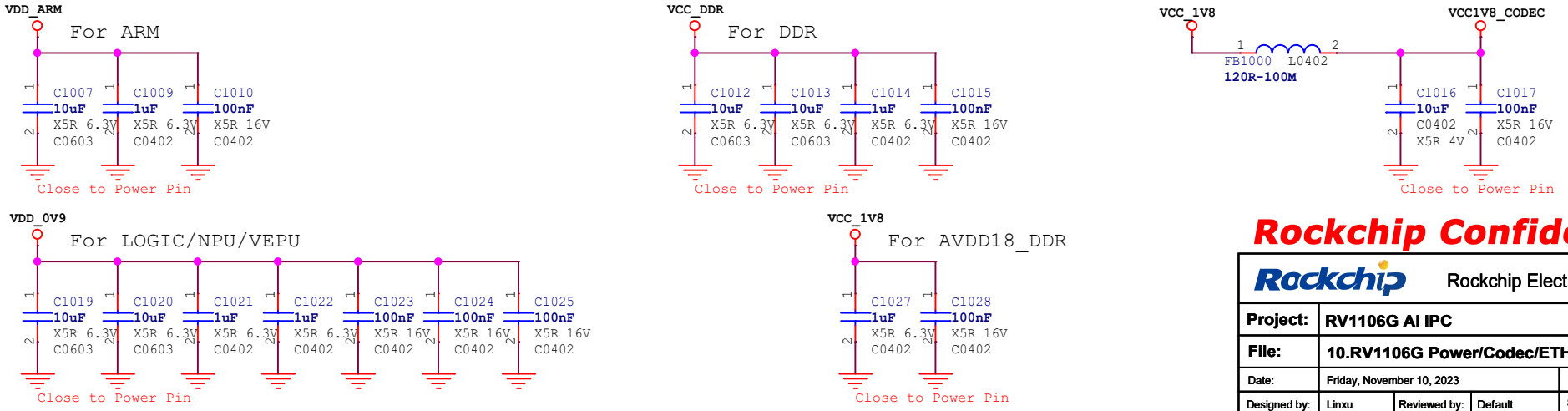
PART D



MIC IN



POWER



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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RV1106G AI IPC				
File:	10.RV1106G Power/Codec/ETH/USB				
Date:	Friday, November 10, 2023			Rev:	V1.3
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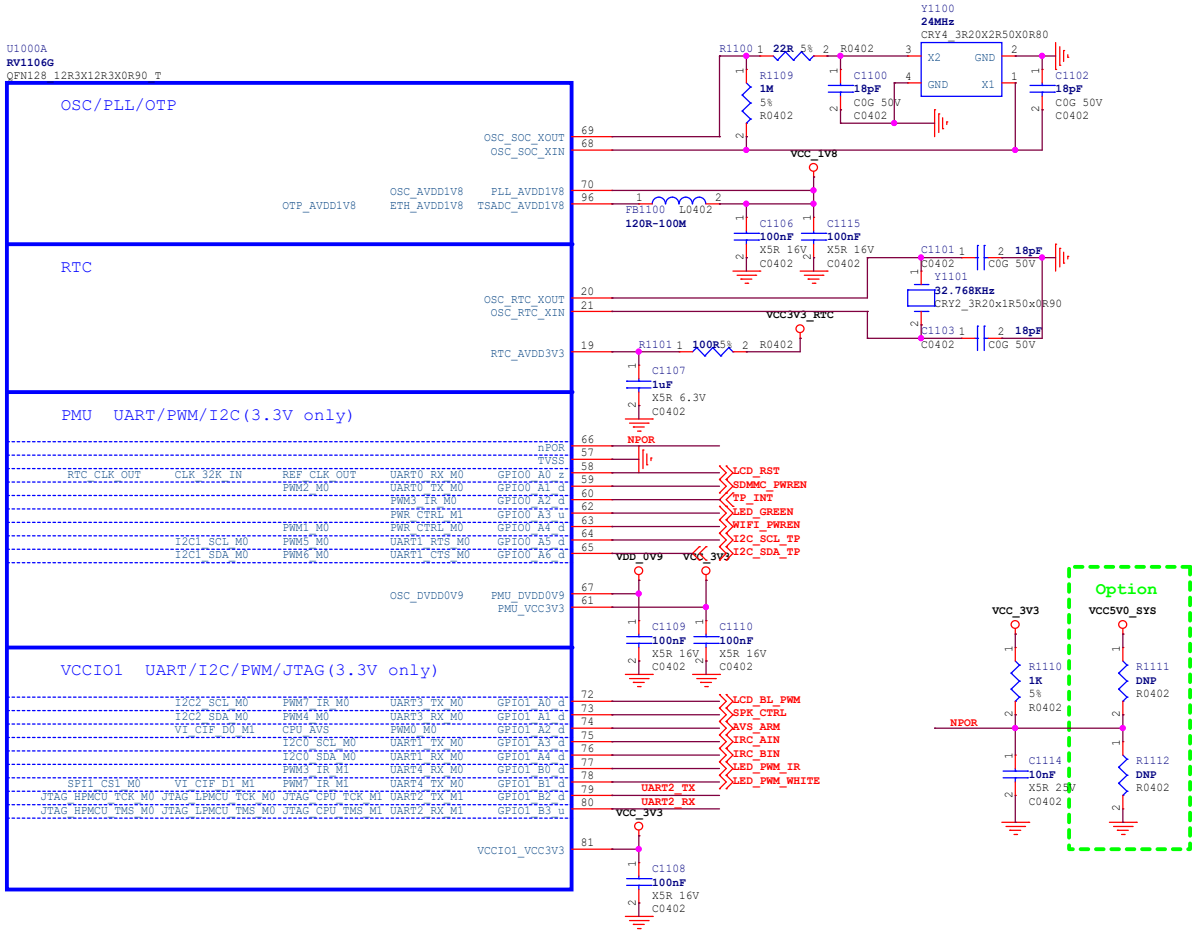
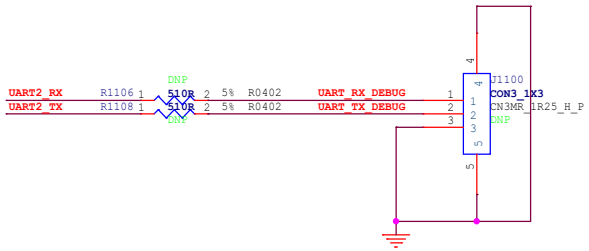
PART A



UART



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Project:	RV1106G AI IPC				
File:	11.RV1106G OSC/RTC/PMU/VCCIO				
Date:	Friday, November 10, 2023			Rev:	V1.3
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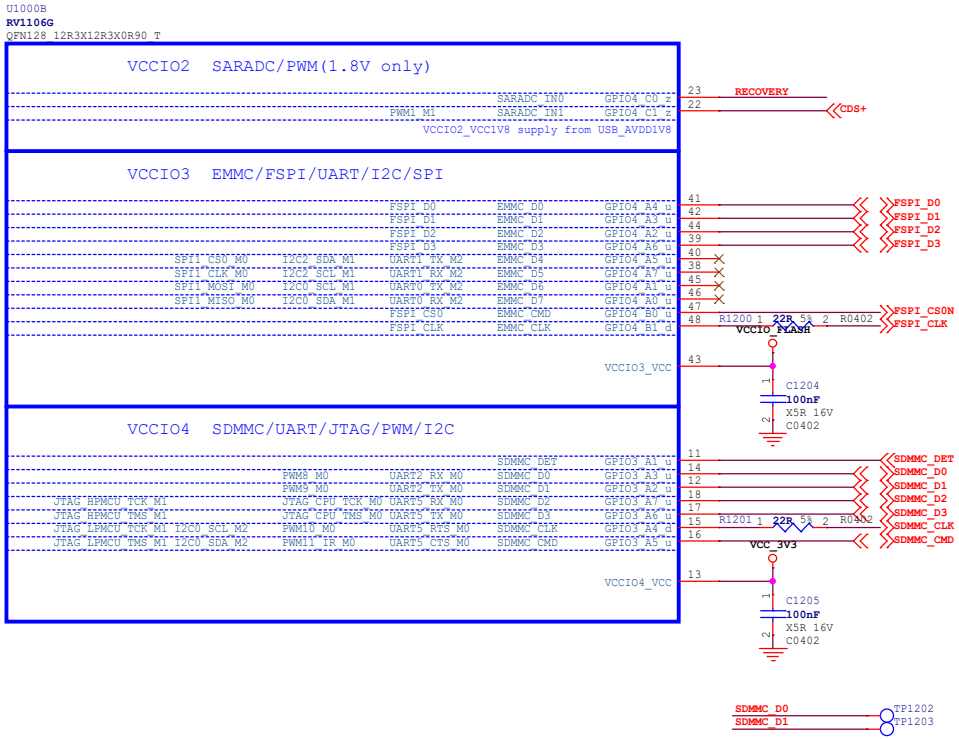
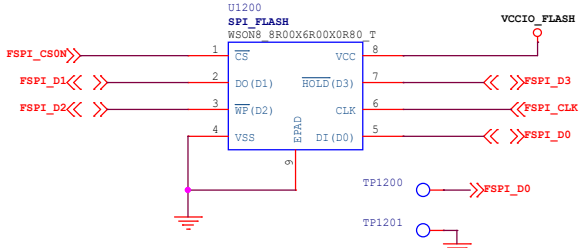
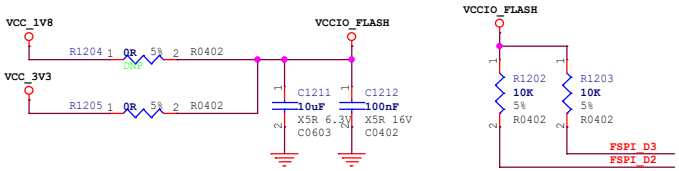
PART B



SPI Flash

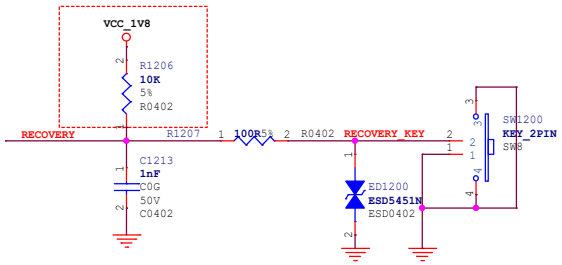
NOTE:
Refer to the latest AVL for parts selection.





RECOVERY Key

Note:
SARADC_IN0 must always be pulled-up.



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Project:	RV1106G AI IPC				
File:	12.RV1106G ADC/FLASH/SDMMC				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	9 of 20

PART C

U1000C
RV1106G
QFN128_12R3X12R3X0R90_T

VCCIO5 SDIO/I2S/VO_LCDC/UART/PWM/I2C

	I2C4_SCL_M0	UART1_RTS_M1	VO_LCDC_D9	I2S0_LRCK	SDIO_D0_M0	GPIO2_A1_d	110 MOTOR1_D1
	I2C4_SDA_M0	UART1_CTS_M1	VO_LCDC_D8	I2S0_SCLK	SDIO_D1_M0	GPIO2_A0_d	109 MOTOR1_D2
		UART1_RX_M1	VO_LCDC_D13	I2S0_SDI0	SDIO_D2_M0	GPIO2_A5_d	114 MOTOR1_D3
		UART1_TX_M1	VO_LCDC_D12	I2S0_SDO0	SDIO_D3_M0	GPIO2_A4_d	113 MOTOR1_D4
			VO_LCDC_D10	I2S0_MCLK	SDIO_CLK_M0	GPIO2_A2_d	111 MOTOR2_D1
			VO_LCDC_D11	I2S0_SDO3_SDI1	SDIO_CMD_M0	GPIO2_A3_d	112 MOTOR2_D2
FLASH_TRIGOUT	I2C3_SCL_M0	PWM2_M1	VO_LCDC_D14	I2S0_SDO2_SDI2	UART0_RTS_M1	GPIO2_A6_d	107 MOTOR2_D3
PRELIGHT_TRIGOUT	I2C3_SDA_M0	PWM4_M1	VO_LCDC_D15	I2S0_SDO1_SDI3	UART0_CTS_M1	GPIO2_A7_d	106 MOTOR2_D4
		PWM5_M1	VO_LCDC_D16	I2C1_SCL_M1	UART0_RX_M1	GPIO2_B0_d	105
		PWM6_M1	VO_LCDC_D17	I2C1_SDA_M1	UART0_TX_M1	GPIO2_B1_d	104

VCCIO5_VCC 108 — VCC_3V3 — C1302 100nF X5R 16V C0402

VCCIO6 VO_LCDC/VI_CIF/PWM/UART/I2C/SDIO/SPI/AUD_DSM/VI_BT656

VI_BT656_D0_M1		SDIO_D1_M1	SPI0_CS0_M0	PWM2_M2	VI_CIF_D2_M1	VO_LCDC_D7	GPIO1_C0_d 95 LCD_D7
VI_BT656_D1_M1		SDIO_D0_M1	SPI0_CLK_M0	PWM4_M2	VI_CIF_D3_M1	VO_LCDC_D6	GPIO1_C1_d 94 LCD_D6
VI_BT656_D2_M1	I2C4_SCL_M1	SDIO_CLK_M1	SPI0_MOSI_M0	PWM5_M2	VI_CIF_D4_M1	VO_LCDC_D5	GPIO1_C2_d 93 LCD_D5
VI_BT656_D3_M1	I2C4_SDA_M1	SDIO_CMD_M1	SPI0_MISO_M0	PWM6_M2	VI_CIF_D5_M1	VO_LCDC_D4	GPIO1_C3_d 92 LCD_D4
VI_BT656_D4_M1		SDIO_D3_M1	UART4_RX_M1	PWM8_M1	VI_CIF_D6_M1	VO_LCDC_D3	GPIO1_C4_d 91 LCD_D3
VI_BT656_D5_M1		SDIO_D2_M1	UART4_TX_M1	PWM9_M1	VI_CIF_D7_M1	VO_LCDC_D2	GPIO1_C5_d 90 LCD_D2
VI_BT656_D6_M1			UART4_RTS_M1	PWM10_M1	VI_CIF_D8_M1	VO_LCDC_D1	GPIO1_C6_d 83 LCD_D1
VI_BT656_D7_M1			UART4_CTS_M1	PWM11_IR_M1	VI_CIF_D9_M1	VO_LCDC_D0	GPIO1_C7_d 84 LCD_D0
VI_BT656_CLK_M1		UART3_TX_M1	UART5_RTS_M1	PWM3_IR_M2	VI_CIF_CLKI_M1	VO_LCDC_DEN	GPIO1_D0_d 89 LCD_RDN
		UART3_RX_M1	UART5_CTS_M1	PWM10_M2	VI_CIF_HREF_M1	VO_LCDC_HSYNC	GPIO1_D1_d 87 LCD_WRN
SPI0_CSI_M0	I2C3_SDA_M1	AUD_DSM_P	UART5_RX_M1	PWM0_M1	VI_CIF_VSYNC_M1	VO_LCDC_VSYNC	GPIO1_D2_d 86 LCD_CSN
	I2C3_SCL_M1	AUD_DSM_N	UART5_TX_M1	PWM11_IR_M2	VI_CIF_CLKO_M1	VO_LCDC_CLK	GPIO1_D3_d 85 LCD_RS

R1305 1 22R 5% 2 R0402

VCCIO6_VCC 88 — VCC_3V3 — C1301 100nF X5R 16V C0402

VCCIO7 VI_CIF/MIPI_CSI/LVDS_RX/UART/I2C/VI_BT1120/VI_BT656 (1.8V only,some for input only)

		VI_BT1120_D0	LVDS_RX_D3N	MIPI_CSI_RX_D3N	VI_CIF_D0_M0	GPIO3_B0_d	117 MIPI_LVDS_D3N
		VI_BT1120_D1	LVDS_RX_D3P	MIPI_CSI_RX_D3P	VI_CIF_D1_M0	GPIO3_B1_d	118 MIPI_LVDS_D3P
		VI_BT1120_D2	LVDS_RX_CLK1N	MIPI_CSI_RX_CLK1N	VI_CIF_D2_M0	GPIO3_B2_d	119 MIPI_LVDS_CLK1N
		VI_BT1120_D3	LVDS_RX_CLK1P	MIPI_CSI_RX_CLK1P	VI_CIF_D3_M0	GPIO3_B3_d	120 MIPI_LVDS_CLK1P
		VI_BT1120_D4	LVDS_RX_D2N	MIPI_CSI_RX_D2N	VI_CIF_D4_M0	GPIO3_B4_d	121 MIPI_LVDS_D2N
		VI_BT1120_D5	LVDS_RX_D2P	MIPI_CSI_RX_D2P	VI_CIF_D5_M0	GPIO3_B5_d	122 MIPI_LVDS_D2P
		VI_BT1120_D6	LVDS_RX_D1N	MIPI_CSI_RX_D1N	VI_CIF_D6_M0	GPIO3_B6_d	123 MIPI_LVDS_D1N
		VI_BT1120_D7	LVDS_RX_D1P	MIPI_CSI_RX_D1P	VI_CIF_D7_M0	GPIO3_B7_d	124 MIPI_LVDS_D1P
	VI_BT656_D0_M0	VI_BT1120_D8	LVDS_RX_CLK0N	MIPI_CSI_RX_CLK0N	VI_CIF_D8_M0	GPIO3_C0_d	125 MIPI_LVDS_CLK0N
	VI_BT656_D1_M0	VI_BT1120_D9	LVDS_RX_CLK0P	MIPI_CSI_RX_CLK0P	VI_CIF_D9_M0	GPIO3_C1_d	126 MIPI_LVDS_CLK0P
	VI_BT656_CLK_M0	VI_BT1120_CLK	LVDS_RX_D0N	MIPI_CSI_RX_D0N	VI_CIF_CLKI_M0	GPIO3_C2_d	127 MIPI_LVDS_D0N
			LVDS_RX_D0P	MIPI_CSI_RX_D0P	VI_CIF_HREF_M0	GPIO3_C3_d	128 MIPI_LVDS_D0P
			MIPI_CLK0_OUT		VI_CIF_CLKO_M0	GPIO3_C4_d	2 MIPI_LVDS_MCLK0
					VI_CIF_VSYNC_M0	GPIO3_C5_d	3 MIPI_LVDS_RST0
	VI_BT656_D2_M0	VI_BT1120_D10	PWM7_IR_M2	MIPI_CLK1_OUT	VI_CIF_D10	GPIO3_C6_d	4 MIPI_LVDS_MCLK1
	VI_BT656_D3_M0	VI_BT1120_D11	UART5_TX_M2	I2C4_SCL_M2	VI_CIF_D11	GPIO3_C7_d	5
	VI_BT656_D4_M0	VI_BT1120_D12	UART5_RX_M2	I2C4_SDA_M2	VI_CIF_D12	GPIO3_D0_d	7 MIPI_I2C_SCL
	VI_BT656_D5_M0	VI_BT1120_D13	UART5_RTS_M2	I2C3_SCL_M2	VI_CIF_D13	GPIO3_D1_d	6 MIPI_I2C_SDA
	VI_BT656_D6_M0	VI_BT1120_D14	UART5_CTS_M2	I2C3_SDA_M2	VI_CIF_D14	GPIO3_D2_d	8
	VI_BT656_D7_M0	VI_BT1120_D15		PWM1_M2	VI_CIF_D15	GPIO3_D3_d	9 MIPI_LVDS_RST1

R1302 1 22R 5% 2 R0402
R1304 1 22R 5% 2 R0402

MIPI_AVDD1V8 VCCIO7_VCC1V8 1 — MIPI_CSI_AVDD_1V8 R1303 1 1R 5% 2 R0402 — VCC_1V8 — C1300 100nF X5R 16V C0402

Mode	MCU	4-SPI 8bit interface II
VO_LCDC_D7	LCD_D7	SPI_CS (LCD_CS)
VO_LCDC_D6	LCD_D6	SPI_CLK (LCD_SCL)
VO_LCDC_D5	LCD_D5	SPI_MOSI(LCD_SDI/SDA)
VO_LCDC_D4	LCD_D4	SPI_MISO(LCD_SDO)
VO_LCDC_D3	LCD_D3	SPI_DCX (LCD_DCX)
VO_LCDC_D2	LCD_D2	--
VO_LCDC_D1	LCD_D1	--
VO_LCDC_D0	LCD_D0	--
VO_LCDC_DEN	LCD_RDN	--
VO_LCDC_HSYNC	LCD_WRN	--
VO_LCDC_VSYNC	LCD_CSN	--
VO_LCDC_CLK	LCD_RS	--

Mode	MIPI 1*4 lane	MIPI 2*2 lane
MIPI/LVDS_D0P	MIPI/LVDS_D0P	MIPI/LVDS0_D0P
MIPI/LVDS_D0N	MIPI/LVDS_D0N	MIPI/LVDS0_D0N
MIPI/LVDS_CLK0P	MIPI/LVDS_CLKP	MIPI/LVDS0_CLKP
MIPI/LVDS_CLK0N	MIPI/LVDS_CLKN	MIPI/LVDS0_CLKN
MIPI/LVDS_D1P	MIPI/LVDS_D1P	MIPI/LVDS0_D1P
MIPI/LVDS_D1N	MIPI/LVDS_D1N	MIPI/LVDS0_D1N
MIPI/LVDS_D2P	MIPI/LVDS_D2P	MIPI/LVDS1_D0P
MIPI/LVDS_D2N	MIPI/LVDS_D2N	MIPI/LVDS1_D0N
MIPI/LVDS_CLK1P	--	MIPI/LVDS1_CLKP
MIPI/LVDS_CLK1N	--	MIPI/LVDS1_CLKN
MIPI/LVDS_D3P	MIPI/LVDS_D3P	MIPI/LVDS1_D1P
MIPI/LVDS_D3N	MIPI/LVDS_D3N	MIPI/LVDS1_D1N

*Support 1x4lane or 2*2lane MIPI/LVDS input*

VCC_1V8
R1300 4.7K 5% R0402
R1301 4.7K 5% R0402
MIPI_I2C_SCL
MIPI_I2C_SDA

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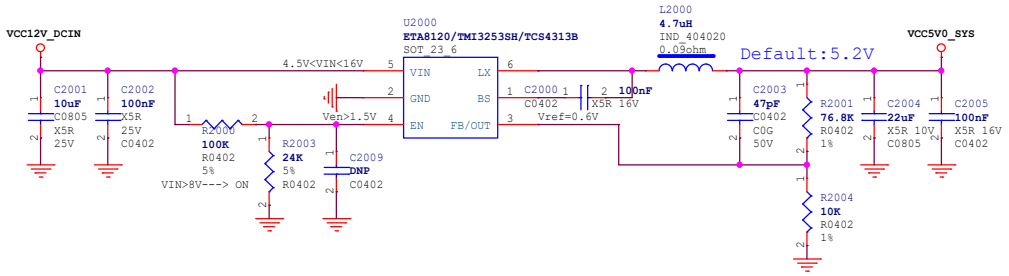
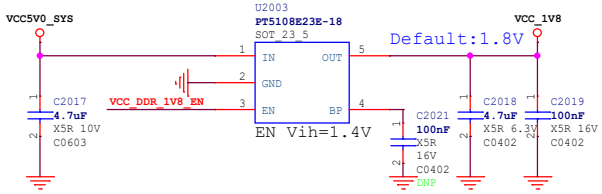
Rockchip Electronics Co., Ltd					
Project:	RV1106G AI IPC				
File:	13.RV1106G SDIO/LCD/VICAP/MIPI				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	10 of 20

12V--->VCC5V0_SYS

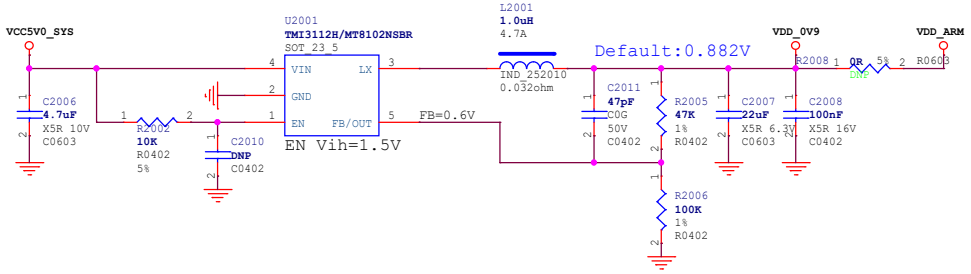


VCC5V0_SYS--->VCC_1V8
Setp 2

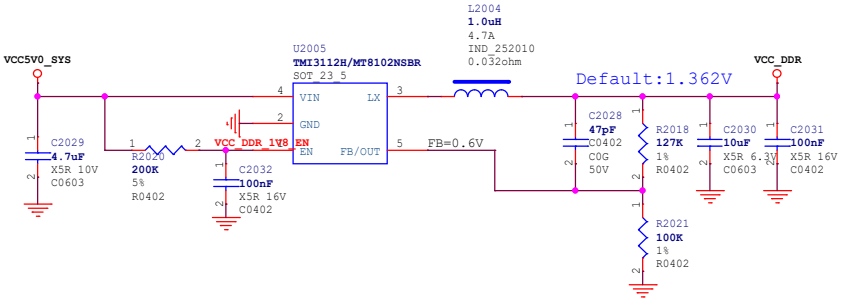


VCC5V0_SYS--->VDD_0V9
Setp 1

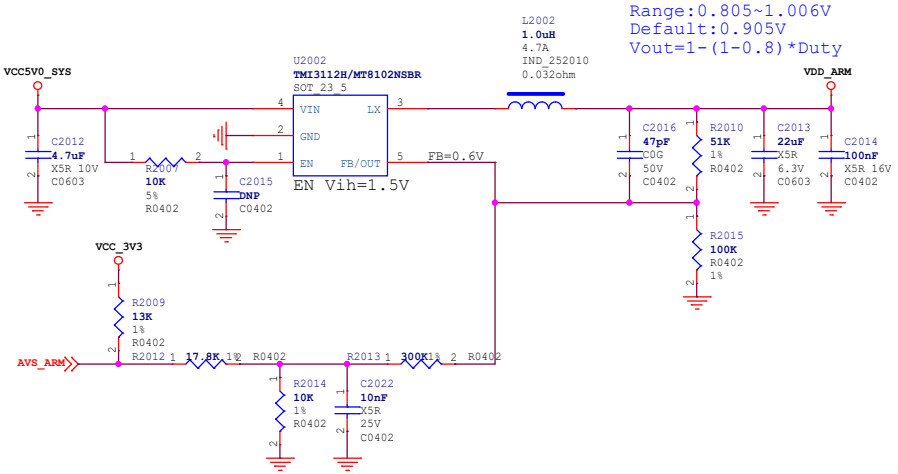
Note:
需要用到高算力的RV1106G3产品，VDD_0V9需要定频0.95V。
此时不建议VDD_ARM与VDD_0V9合并供电，易造成功耗增加。



VCC5V0_SYS--->VCC_DDR
Setp 2

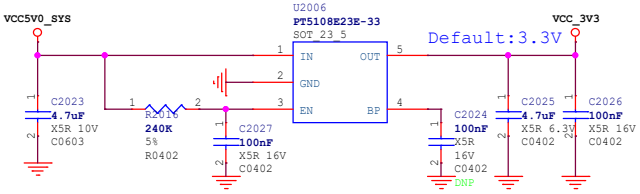


VCC5V0_SYS--->VDD_ARM
Setp 1

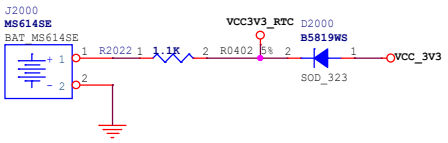


Option:
1.双目融合以及AI-ISP产品，对CPU需求较高的，VDD_ARM必须可调压，所以需要独立供电。
2.双目拼接及通用IPC产品，对CPU需求不高的，VDD_ARM可以与VDD_0V9合并供电，降低成本。

VCC5V0_SYS--->VCC_3V3
Setp 3



RTC Power



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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RV1106G AI IPC				
File:	20.Power-System				
Date:	Friday, November 10, 2023			Rev:	V1.3
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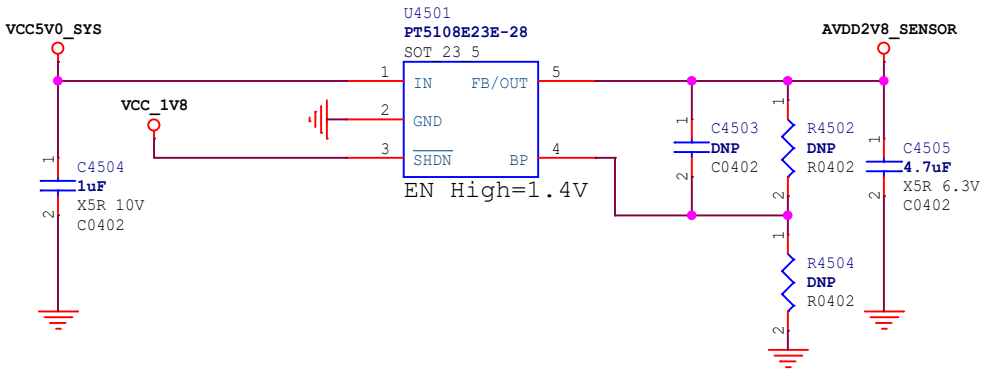
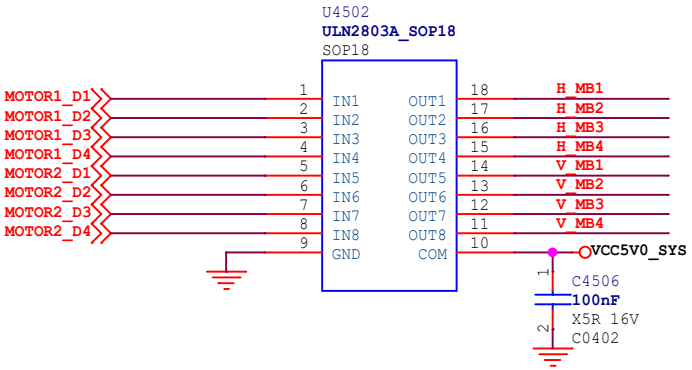
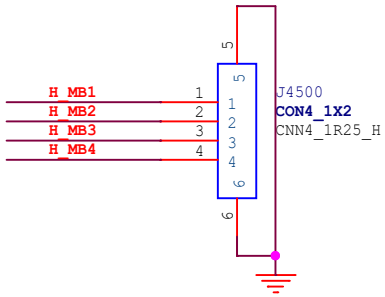
VCC5V0_SYS--->AVDD2V8_SENSOR

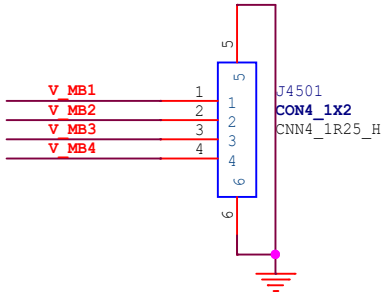


Note:
Default power-on timing:
All three power on at the same time.
Or DOVDD(VCC_1V8)-->DVDD(VCC_1V5)-->AVDD(VCC_2V8)

Motor







Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RV1106G AI IPC				
File:	45.VI-Camera Power				
Date:	Friday, November 10, 2023			Rev:	V1.3
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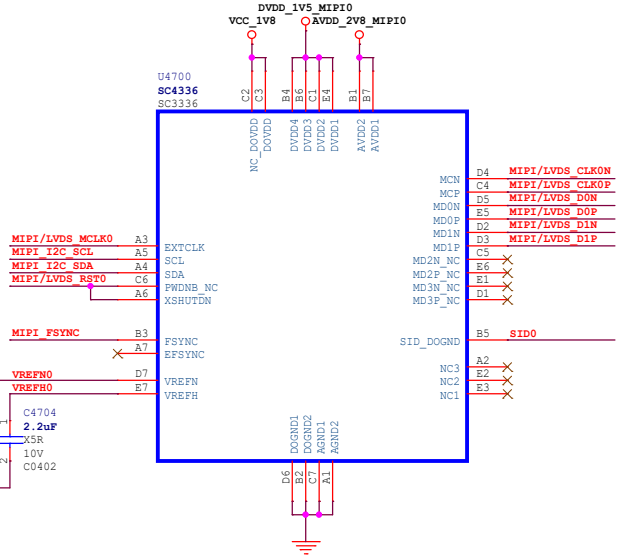
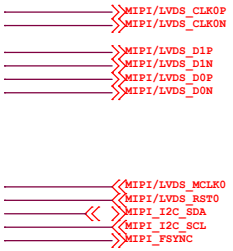
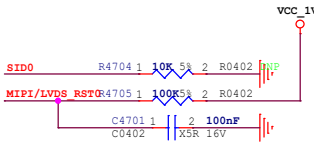
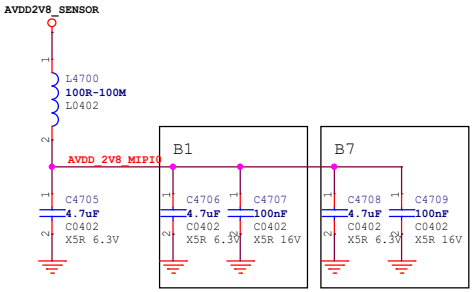
Sensor0 : Master



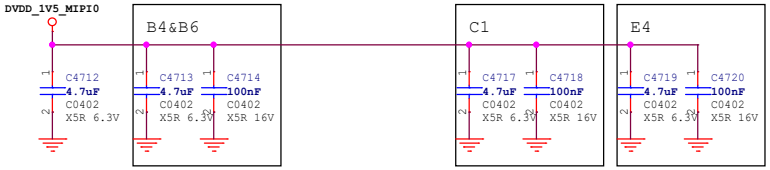


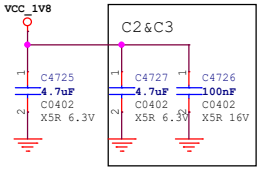


SID(7-bit I2C Device ID)
1:7h32
0:7h30(default)



Note:
The built-in LDO power supply is used by default





Rockchip	Rockchip Electronics Co., Ltd				
Project:	RV1106G AI IPC				
File:	47.VI-Camera Master				
Date:	Monday, December 25, 2023			Rev:	V1.3
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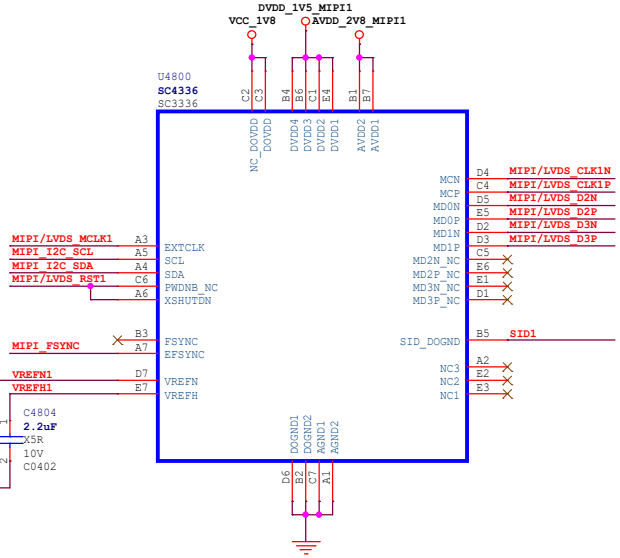
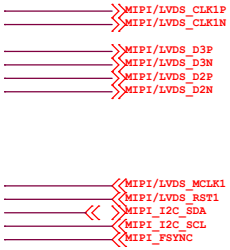
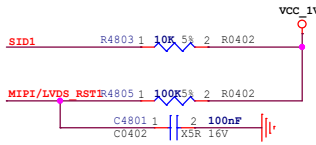
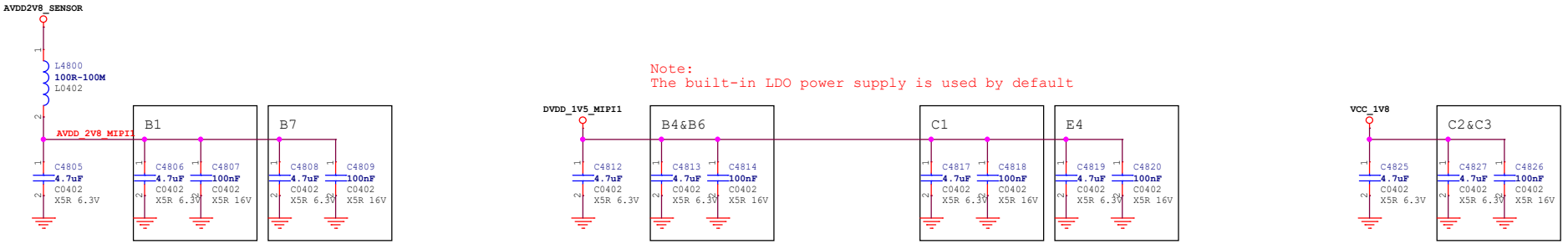
Sensor1 : Slave







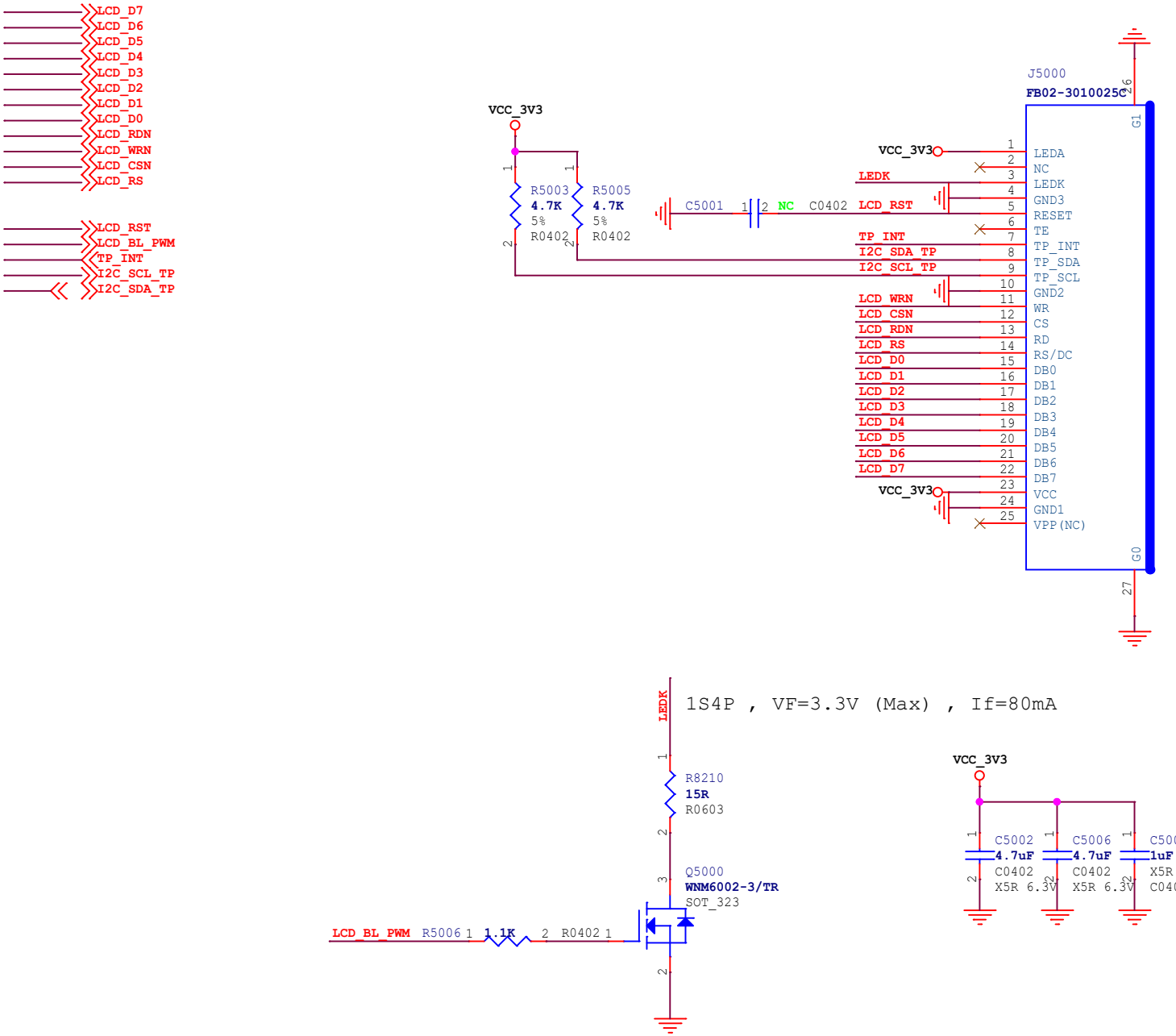
SID(7-bit I2C Device ID)
1:7h32(default)
0:7h30



Note:
The built-in LDO power supply is used by default

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RV1106G AI IPC				
File:	48.VI-Camera Slave				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	14 of 20

Panel and TP



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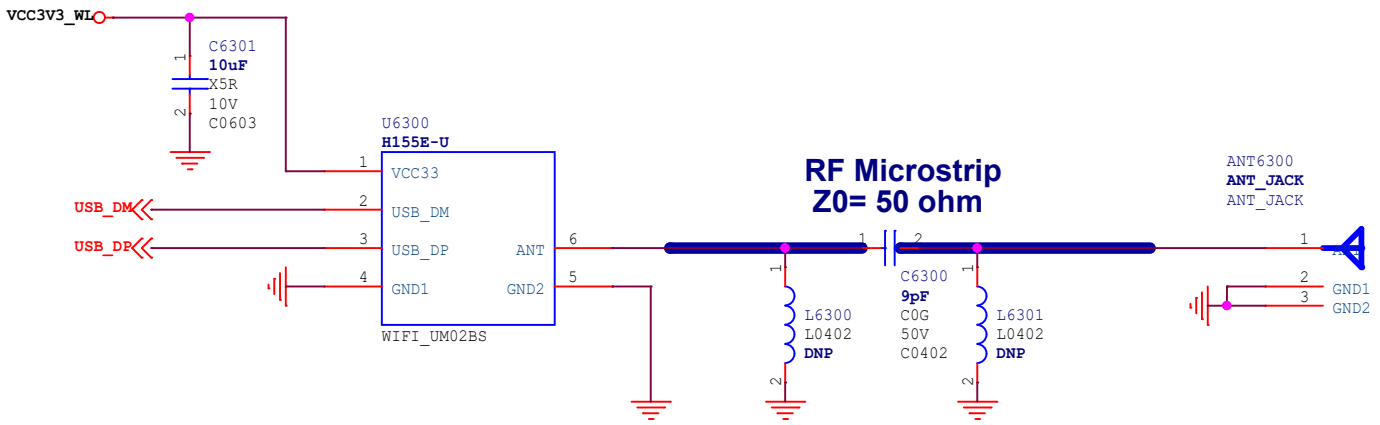
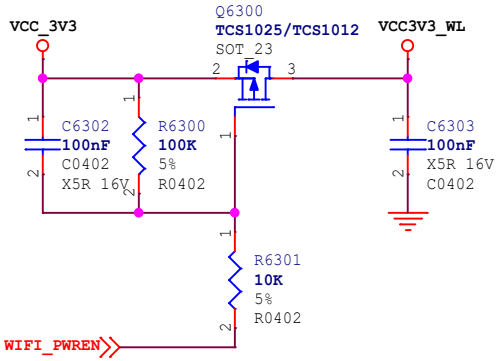
Rockchip Electronics Co., Ltd					
Project:	RV1106G AI IPC				
File:	50.VO-MCU Panel				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	15 of 20

USB WIFI Module





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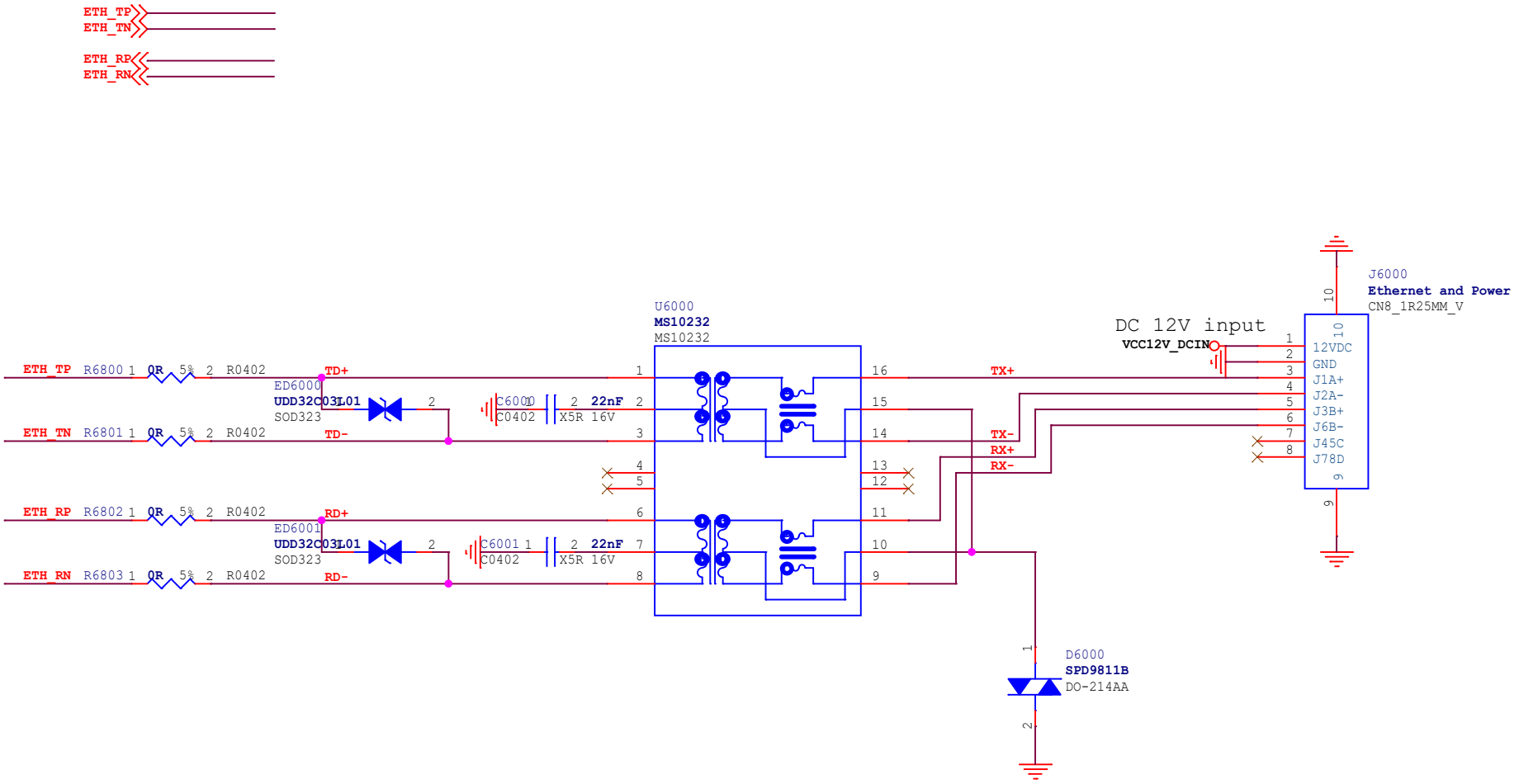
Rockchip Electronics Co., Ltd					
Project:	RV1106G AI IPC				
File:	63.WIFI-USB				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	16 of 20

Ethernet



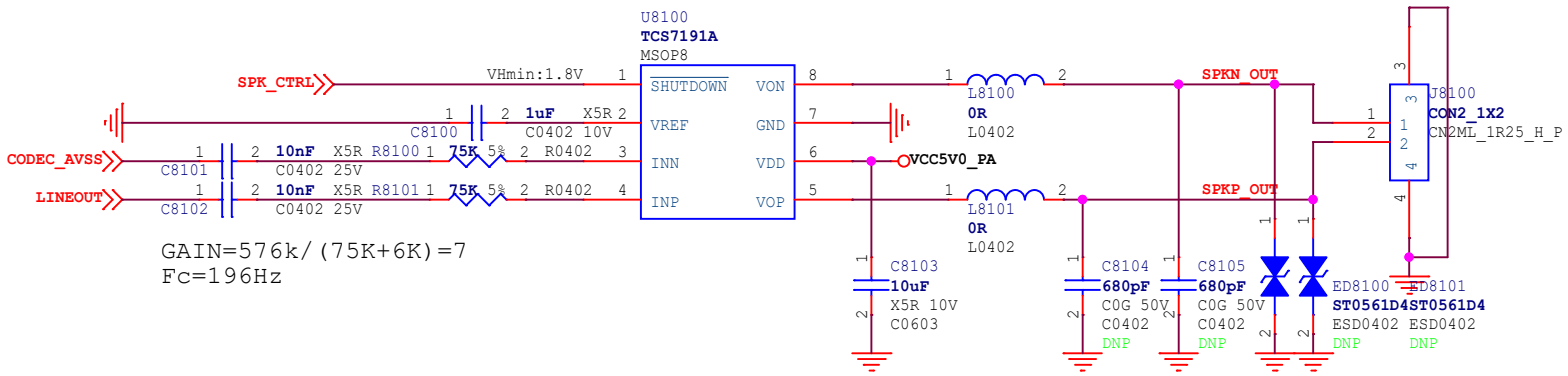
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RV1106G AI IPC				
File:	68.Ethernet-FEPHY_Embed				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	17 of 20

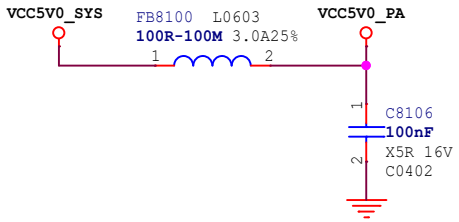
Speaker Out

NOTE:If there is no EMI problem, the ferrite beads can be replaced by 0ohm resistors;

NOTE:CODEC_AVSS and LINEOUT are routed according to the difference rule;



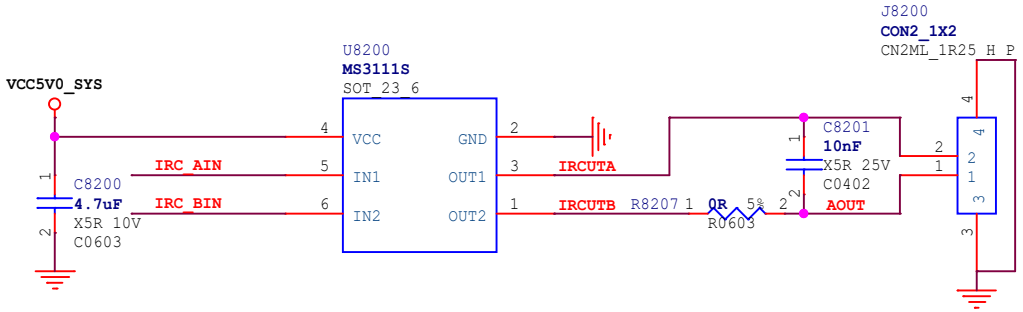
Speaker power



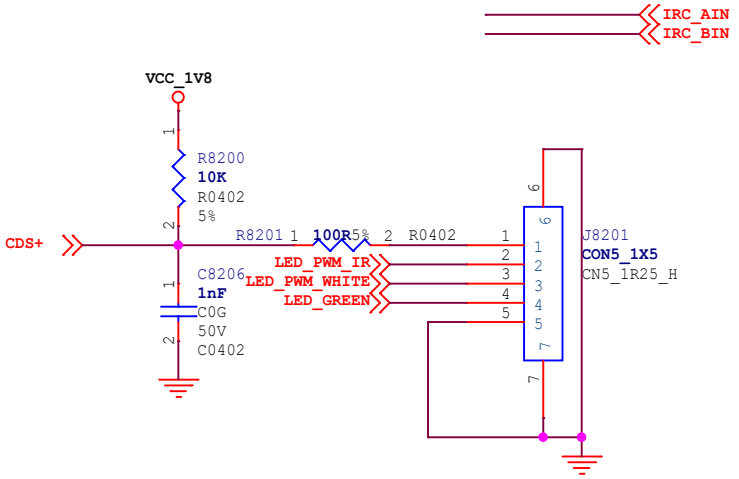
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RV1106G AI IPC				
File:	70.Audio Port				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	18 of 20

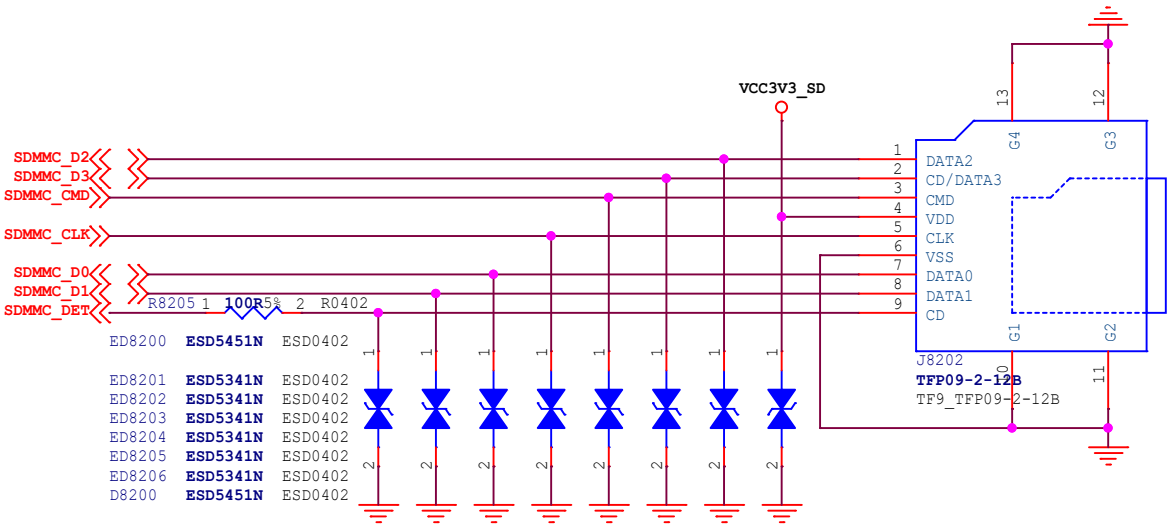
IR-CUT Drive



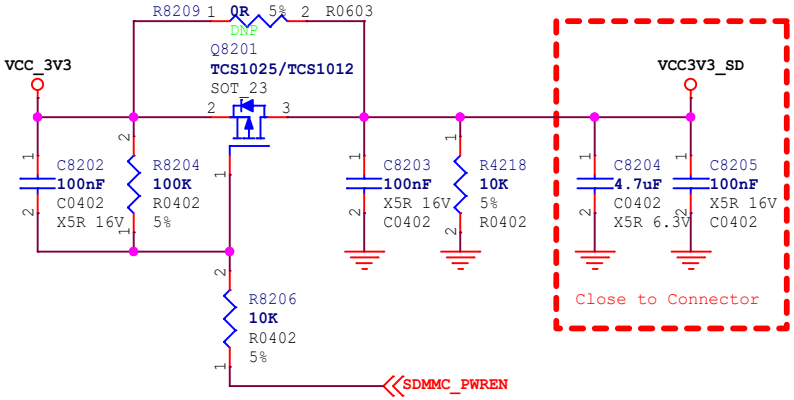
CDS&LED



Micro-SD Card



Card Power

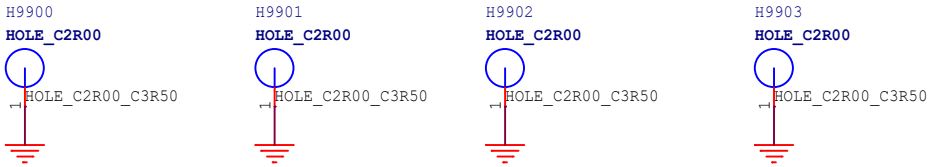


SDMMC0_PWREN=L VCC3V3_SD=3.3V(Default)
SDMMC0_PWREN=H VCC3V3_SD=0V

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RV1106G AI IPC				
File:	82.Micro-SD Card/IRCUT/CDS				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	19 of 20

HOLE



LENS

MARK

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RV1106G AI IPC				
File:	99.MARK/HOLE				
Date:	Friday, November 10, 2023			Rev:	V1.3
Designed by:	Linxu	Reviewed by:	Default	Sheet:	20 of 20