


# RV1106G\_COREDLOC\_SL\_V1.2\_20220924

Reference Design Main Functions Introduction	
Power	
RAM	SPI FLASH
Interface	SDMMC/SDIO/MIPI_CSI/VICAP/I2S/USB/ADC

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Project:	RV1106G_CoreDloc_SL		
File:	00.Cover Page		
Date:	Saturday, September 24, 2022		Rev: V1.2
Designed by:	LLS	Reviewed by: Default	Sheet: 1 of 20

Catalogue	
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Page02	01.Index and Notes
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# Index and Notes

## Note

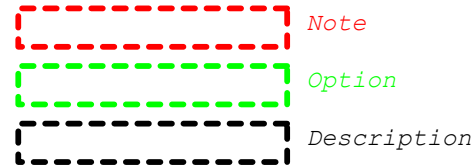
NOTE 1:  
Component parameter description  
1. DNP stands for component not mounted temporarily  
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:  
Please use our recommended components to avoid too many changes.  
For more informations about the second source,please refer to our AVL.

## Generate Bill of Materials

Header:  
`Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption`  
Combined property string:  
`{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}`

## Graphic Description



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Rockchip Rockchip Electronics Co., Ltd

Project:	RV1106G_CoreDloc_SL			
File:	01.Index and Notes			
Date:	Saturday, September 24, 2022		Rev:	V1.2
Designed by:	LLS	Reviewed by:	Default	Sheet: 2 of 20

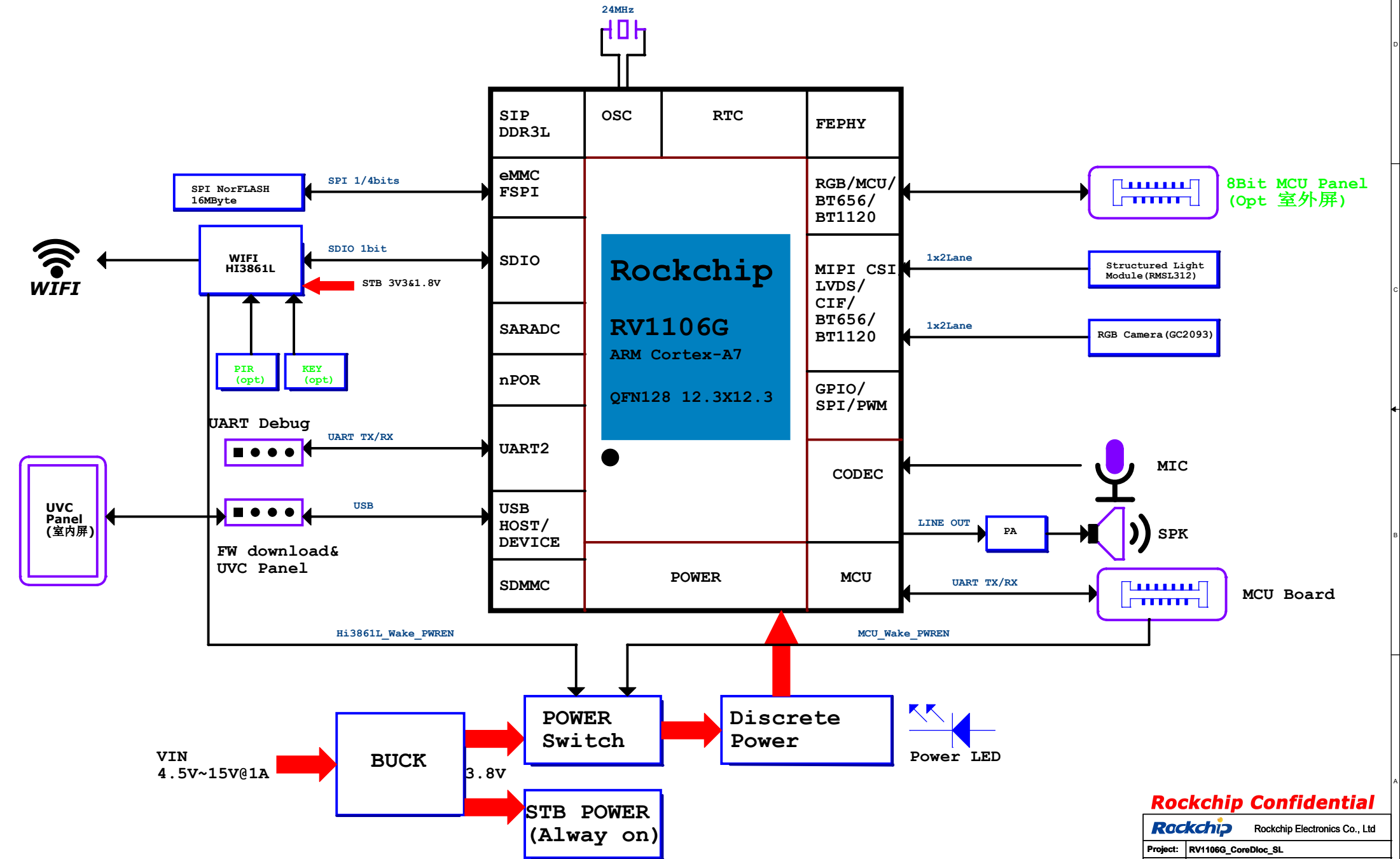
# Revision History

Version	Date	Author	Change Note	Approved
V1.0	2022.4.29	LLS	First edition.	
V1.1	2022.7.27	LLS	Refer to <RV1106_COREDLOC_SL_V11_20220727_SCH_Modify_Notes.pdf>	
V1.2	2022.9.24	LLS	Refer to <RV1106_COREDLOC_SL_V12_20220924_SCH_Modify_Notes.pdf>	


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Project:	RV1106G_CoreDloc_SL		
File:	02.Revision History		
Date:	Saturday, September 24, 2022		Rev: V1.2
Designed by:	LLS	Reviewed by:	Default
		Sheet:	3 of 20

Block Diagram



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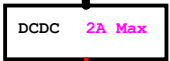


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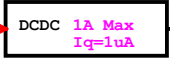
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File:	03.Block Diagram				
Date:	Saturday, September 24, 2022			Rev:	V1.2
Designed by:	LLS	Reviewed by:	Default	Sheet:	4 of 20

Power Diagram and Sequence

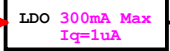
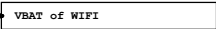
VCCSYS\_IN (4.5V~15V@1A)



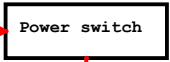
VCC3V8\_SYS



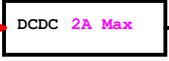
VCC3V3\_STB



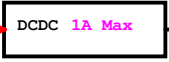
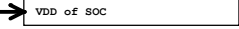
VCC1V8\_STB



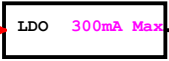
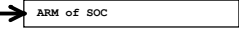
VCC\_SYS\_S0



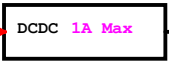
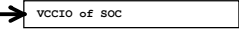
VDD\_0V9



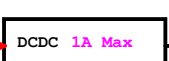
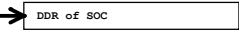
VDD\_ARM



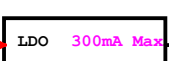
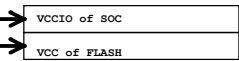
VCC\_1V8



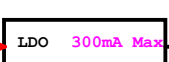
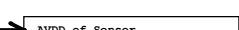
VCC\_DDR



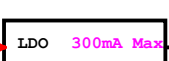
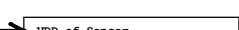
VCC\_3V3



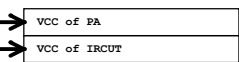
AVDD2V8\_SENSOR



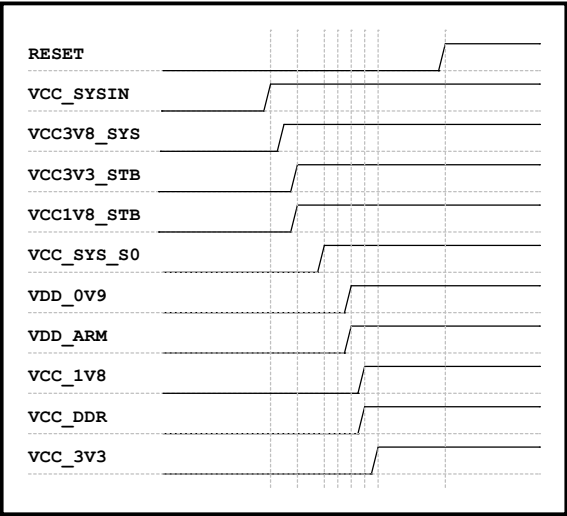
VDD1V2\_SENSOR



VDD1V8\_SENSOR



RV1106G Power-on Sequence				
Power Name	PMIC Channel	Time Slot	Default voltage	Peak Current
VCC3V8_SYS	DC-DC BUCK	Slot: 1	3.8V	1.5A
VCC3V3_STB	DC-DC BUCK	Slot: 2	3.3V	1.0A
VCC1V8_STB	LDO	Slot: 2	1.8V	0.3A
VCC_SYS_S0	SWITCH	Slot: 3	3.8V	1.5A
VDD_0V9	DC-DC BUCK	Slot: 4	0.88V	1.6A
VDD_ARM	DC-DC BUCK	Slot: 4	0.805V~1.006V	0.5A
VCC_1V8	LDO	Slot: 5	1.8V	0.1A
VCC_DDR	DC-DC BUCK	Slot: 5	1.35V	0.5A
VCC_3V3	LDO	Slot: 6	3.3V	0.2A
RESET	Finally , nPOR RESET 10ms after VCC_3V3 is ready			



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Project: RV1106G\_CoreDloc\_SL

File: 04.Power Diagram and Sequence

Date: Saturday, September 24, 2022 Rev: V1.2

Designed by: LLS Reviewed by: Default Sheet: 5 of 20


I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Write/Read Address	Note
I2C3	I2C3_SCL_M2 I2C3_SDA_M2	VCCIO7	I2C3_SCL_M2_DLOC I2C3_SDA_M2_DLOC	1.8V	RK803		write address 0xC6 read address 0xC7	
					IR Camera(SC035)		write address 0x60 read address 0x61	
					built-in EEPROM GT24C512-2ZLI-TR		write address 0xA0; read address 0xA1	
I2C4	I2C4_SCL_M2 I2C4_SDA_M2	VCCIO7	I2C3_SCL_M2_RGB I2C3_SDA_M2_RGB	1.8V	RGB Camera(GC2093)		write address 0x6E; read address 0x6F	
					EEPROM		write address 0xA0; read address 0xA1	

# IO Power Domain Map

IO Domain	IO Group	Support of IO Voltage		Default Actual assigned IO Domain Voltage			Remark
		1.8V	3.3V	Net Name of Power Supply	Power Source	Voltage	
PMUIO	Group GPIO0_A		✓	VCC_3V3		3.3V	
VCCIO1	Group GPIO1_AB		✓	VCC_3V3		3.3V	
VCCIO2	Group GPIO4_C	✓		VCC_1V8		1.8V	
VCCIO3	Group GPIO4_AB	✓	✓	VCCIO_FLASH		1.8/3.3V	
VCCIO4	Group GPIO3_A	✓	✓	VCC_1V8		1.8/3.3V	
VCCIO5	Group GPIO2_AB	✓	✓	VCC_1V8		3.3V	
VCCIO6	Group GPIO1_CD	✓	✓	VCC_3V3		3.3V	
VCCIO7	Group GPIO3_BCD	✓		VCC_1V8		1.8V	

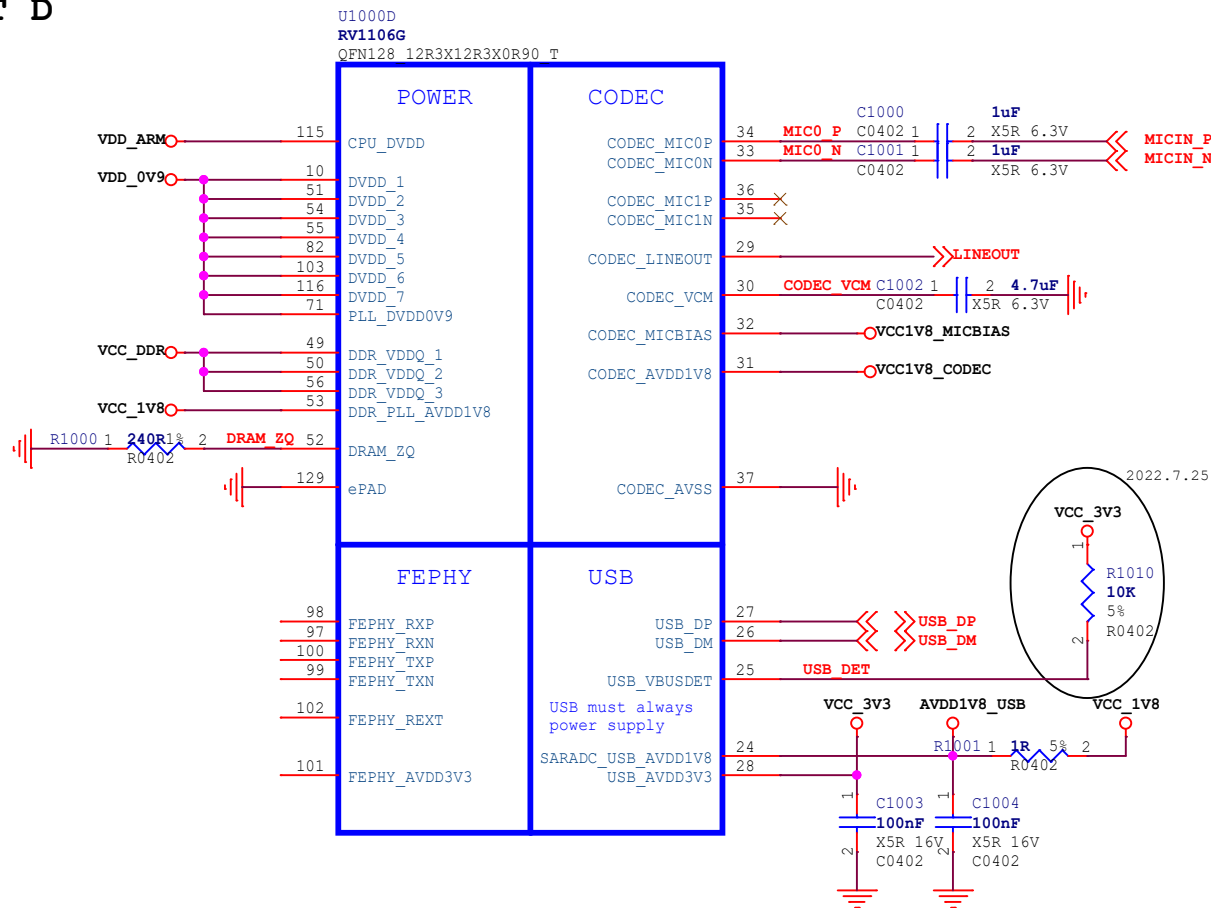
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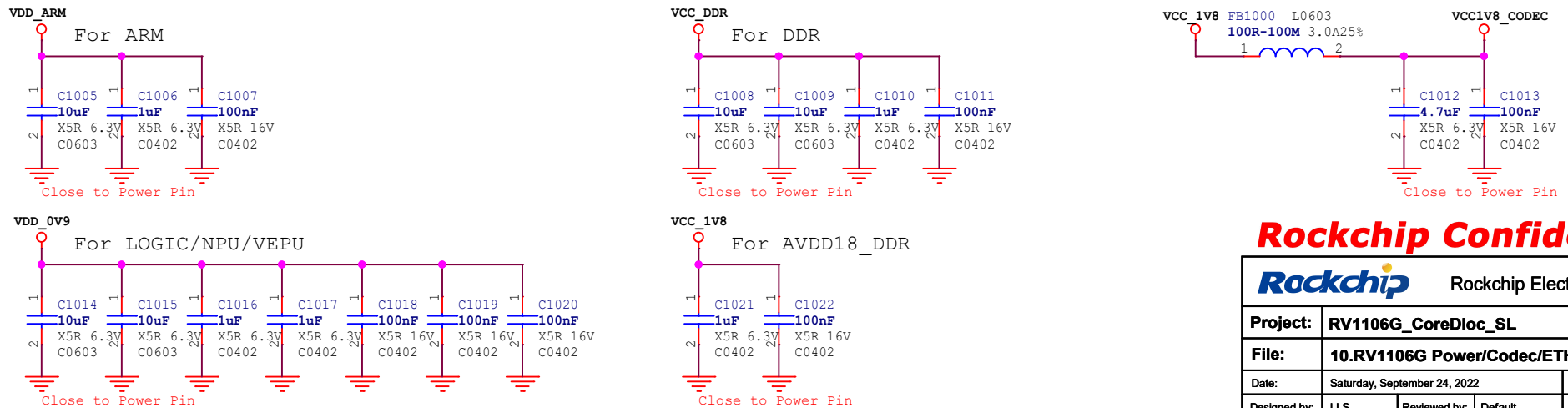
Rockchip Electronics Co., Ltd

Project:	RV1106G_CoreDloc_SL				
File:	06.IO Power Domain Map				
Date:	Saturday, September 24, 2022			Rev:	V1.2
Designed by:	LLS	Reviewed by:	Default	Sheet:	6 of 20


# PART D



## POWER



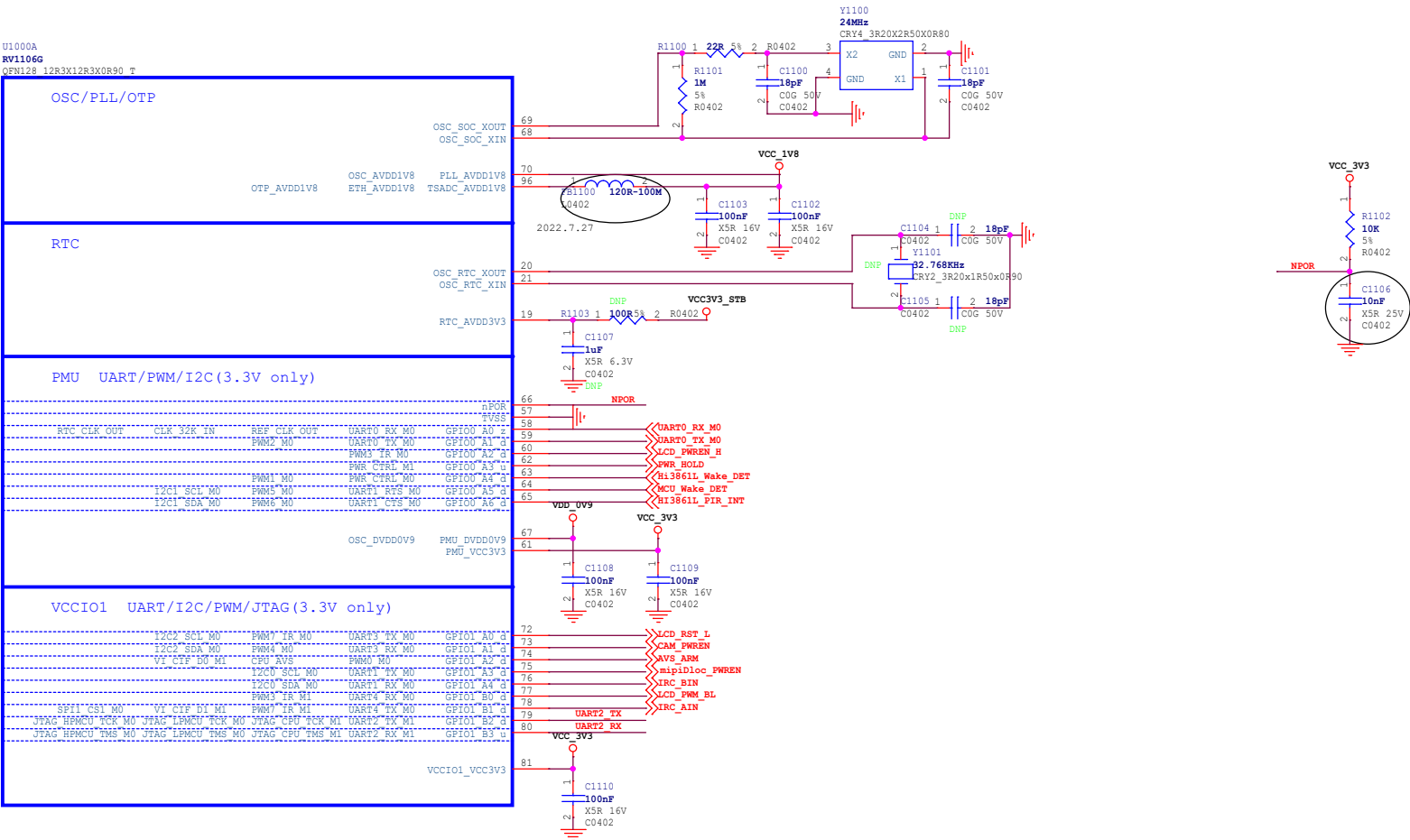
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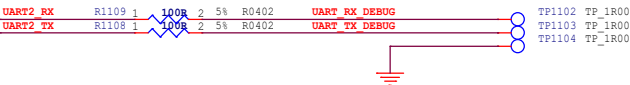
Rockchip Electronics Co., Ltd

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File:	10.RV1106G Power/Codec/ETH/USB						
Date:	Saturday, September 24, 2022				Rev:	V1.2	
Designed by:	LLS	Reviewed by:	Default		Sheet:	7 of 20	

PART A



UART Debug



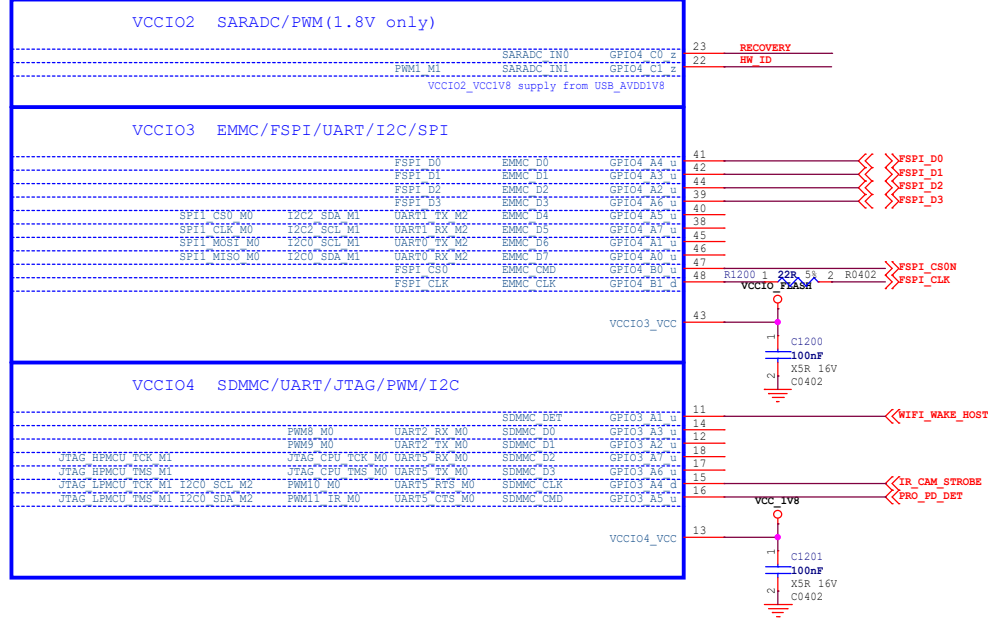
Rockchip Confidential

Rackchip Rockchip Electronics Co., Ltd

Project:	RV1106G_CoreDioC_SL		
File:	11.RV1106G_OSC/RTC/PMU/VCCIO		
Date:	Saturday, September 24, 2022	Rev:	V1.2
Designed by:	LLS	Reviewed by:	Default
Sheet:	8	of	20

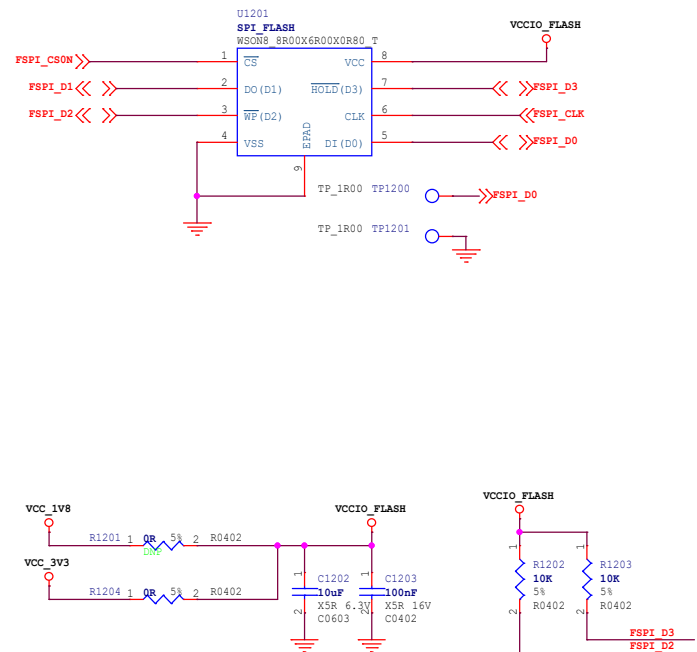
PART B

U1000B  
RV1106G  
OFN128 12R3X12R3X0R90 T

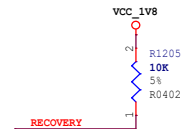


SPI Flash

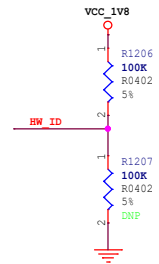
NOTE:  
Refer to the latest AVL for parts selection.



RECOVERY Key



HW_ID	Rup (R1206)	Rdown (R1207)	ADC
Demo-v1.0	DNP	100K	0
Demo-v1.2	100K	DNP	1023

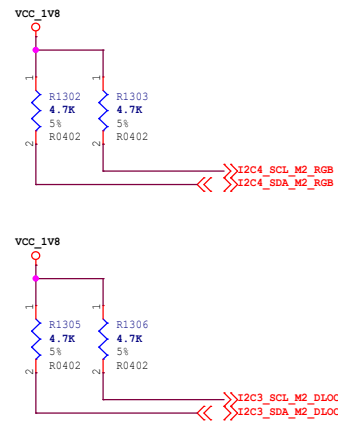
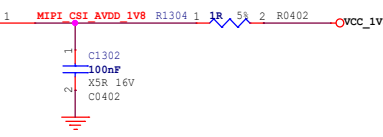
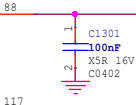
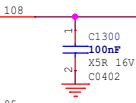
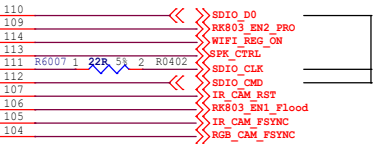
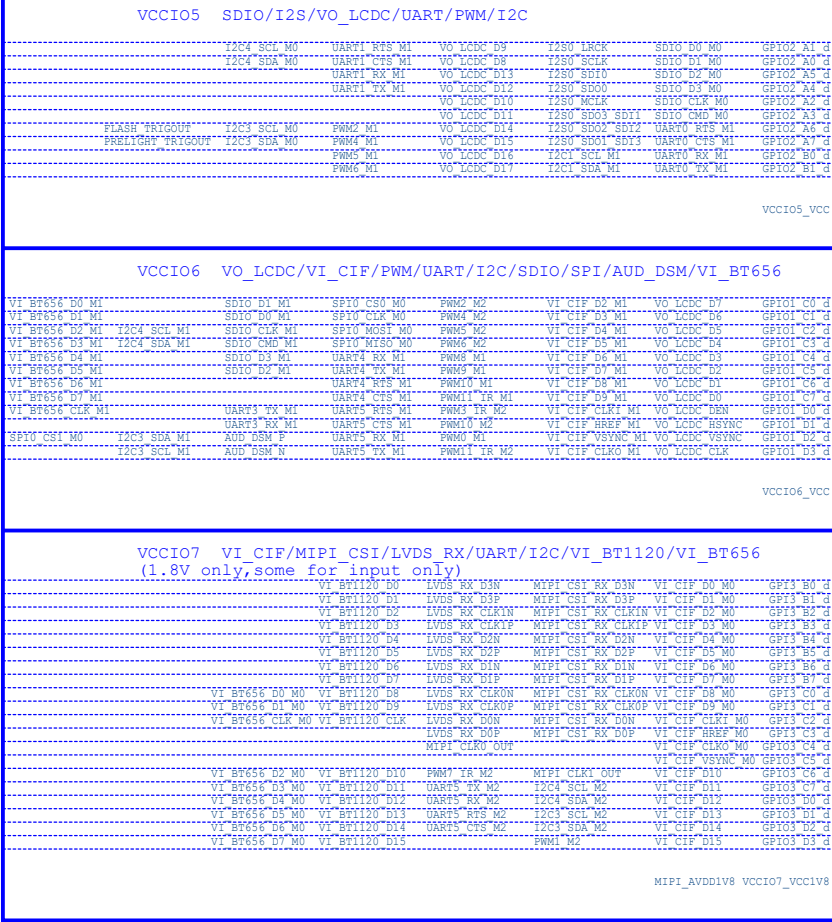


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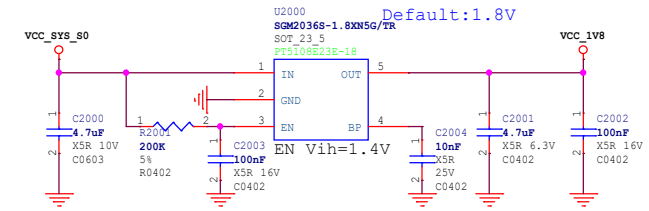
Rockchip Electronics Co., Ltd

Project:	RV1106G_CoreDloc_SL
File:	12.RV1106G_ADC/FLASH/SDMMC
Date:	Saturday, September 24, 2022
Designed by:	LLS
Reviewed by:	Default
Rev:	V1.2
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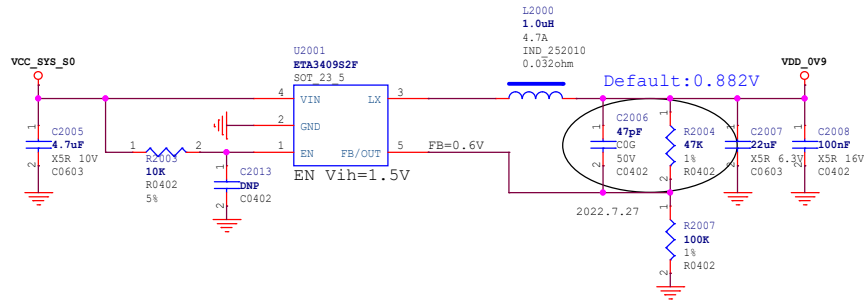
U1000C  
RV1106G  
QFN128 12R3X12R3X0R90 T



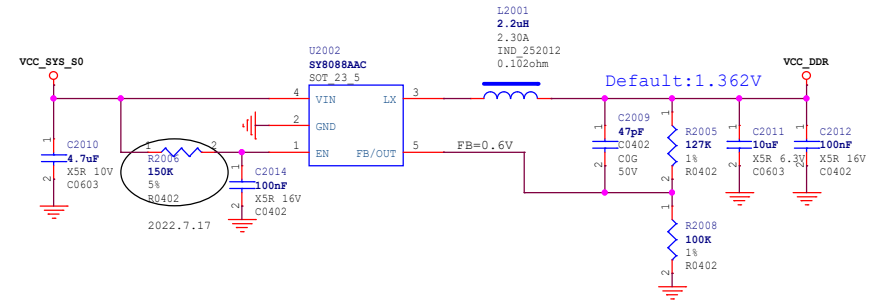
# VCC5V0\_SYS--->VCC\_1V8 Setp 2



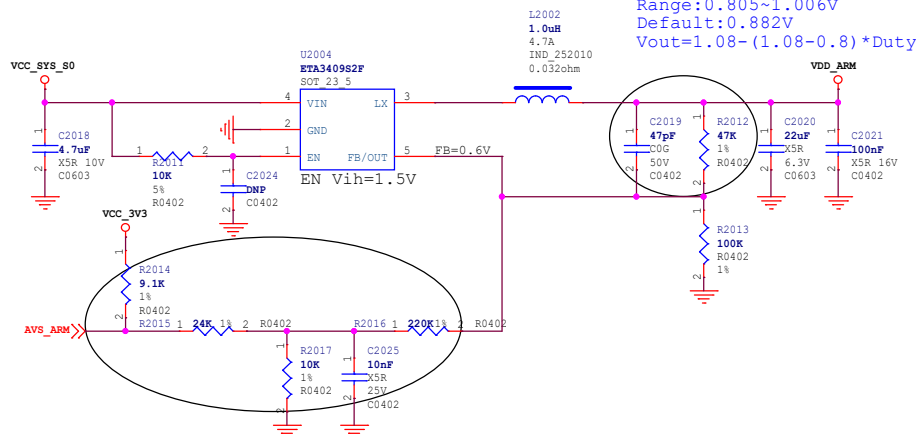
# VCC5V0\_SYS--->VDD\_0V9 Setp 1



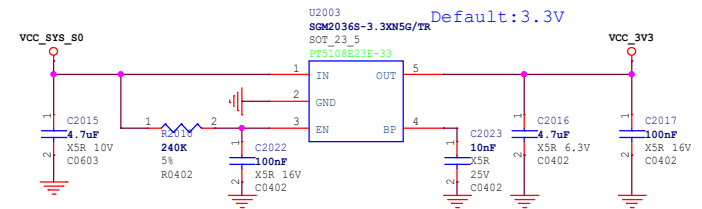
# VCC5V0\_SYS--->VCC\_DDR Setp 2



# VCC5V0\_SYS--->VDD\_ARM Setp 1



# VCC5V0\_SYS--->VCC\_3V3 Setp 3



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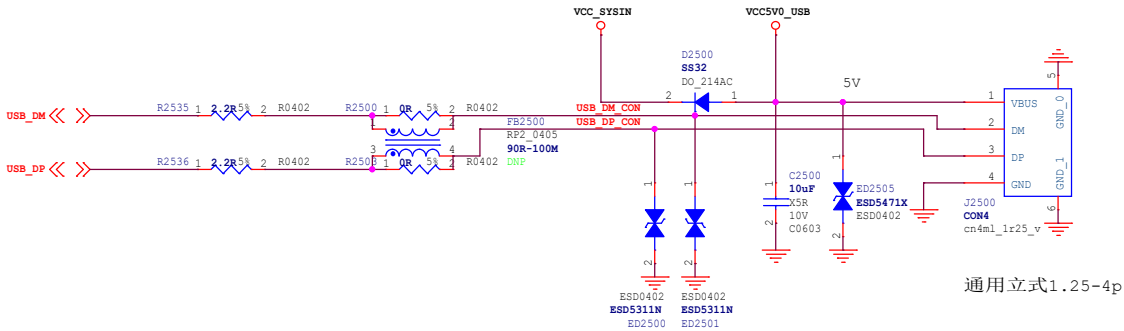
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File: 20.Power-System

Date: Saturday, September 24, 2022 Rev: V1.2

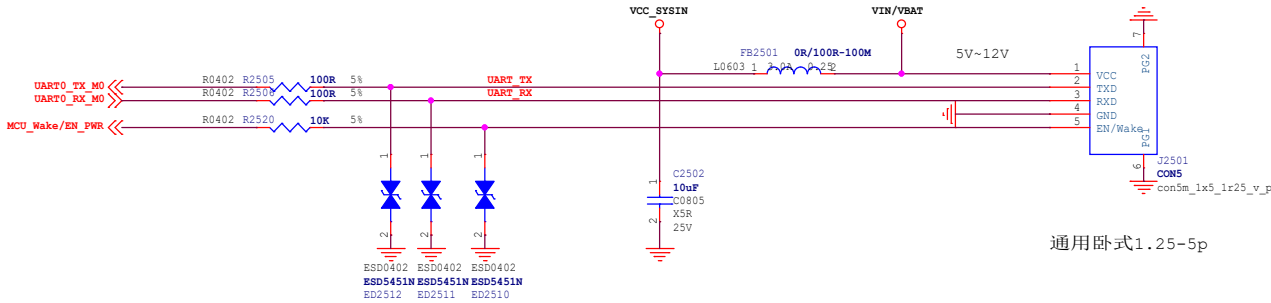
Designed by: LLS Reviewed by: Default Sheet: 11 of 20

USB for Download Firmware & UVC panel



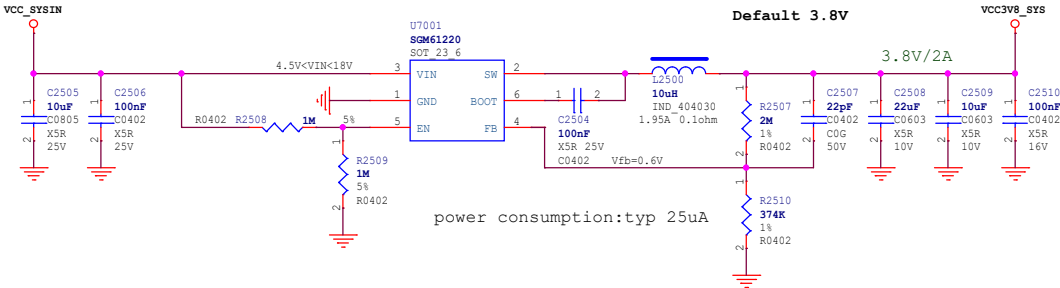
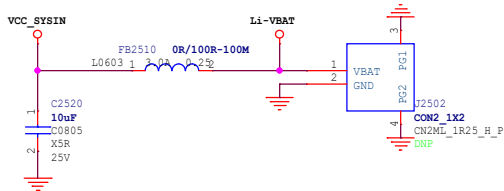
通用立式1.25-4p

UART\_CON Connect MCU Board



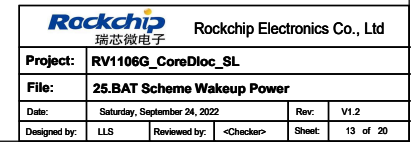
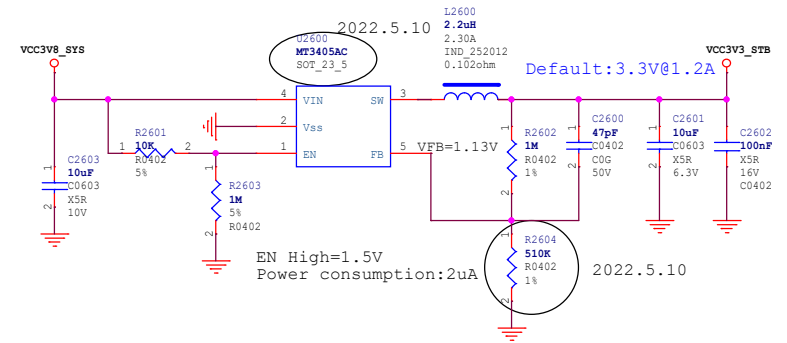
通用卧式1.25-5p

LI-BAT VIN(Optional)

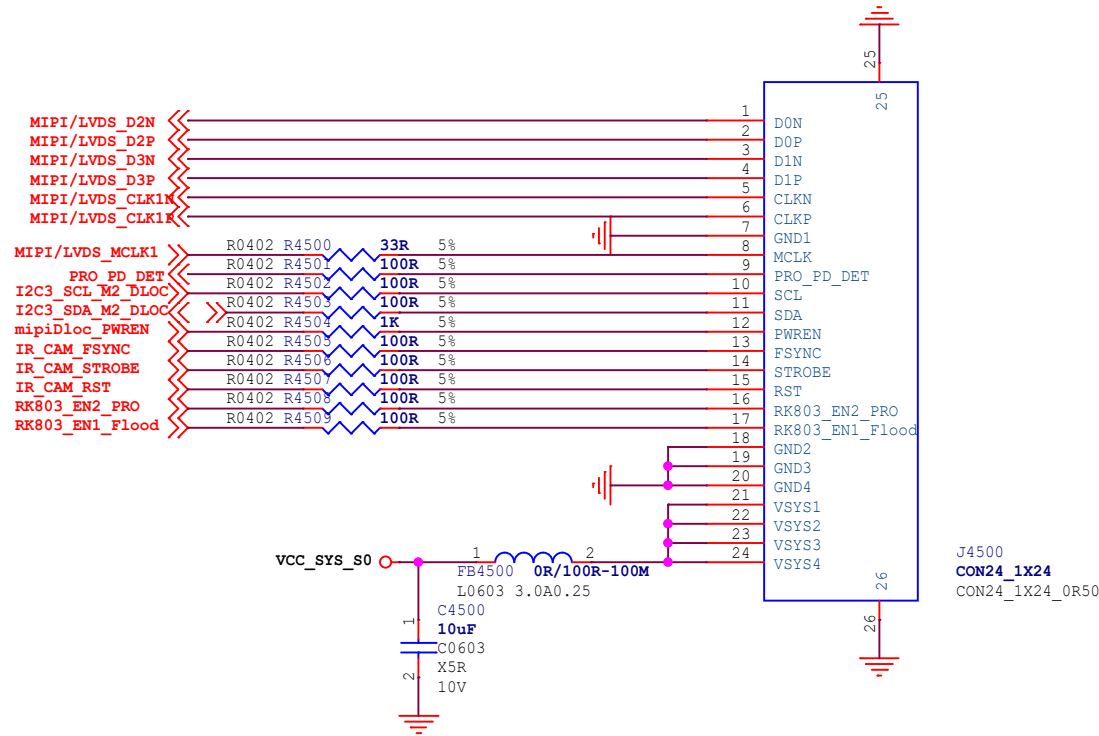


VCC\_SYSIN=4.5V~15V ---2cell 7.4V Battery&6/8节干电池


## Standby Power (Always on)



# MIPI Structured Light Module (RMSL312)



通用0.5mm间距24PIN下接座



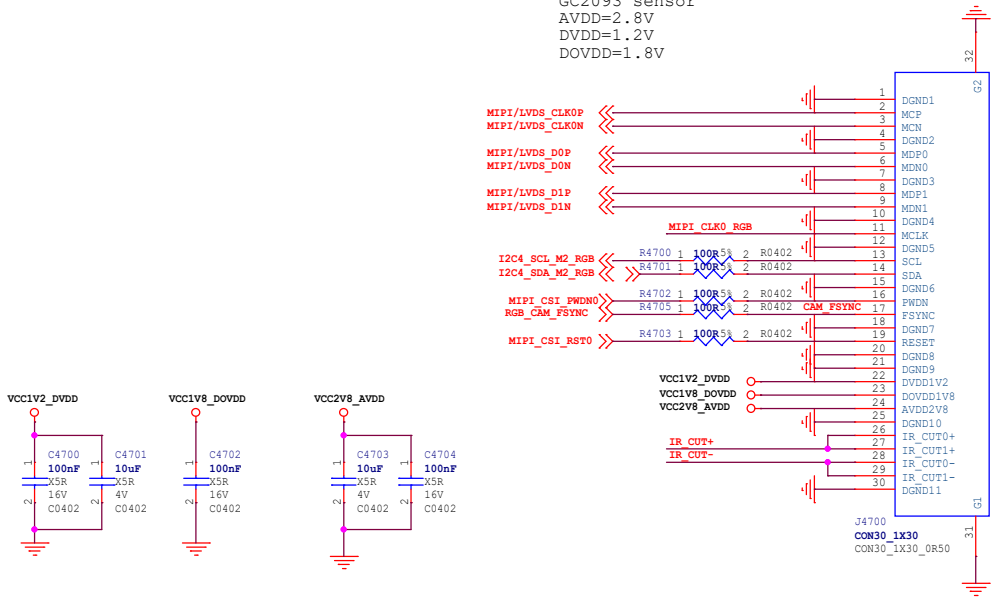
瑞芯微电子

Fuzhou Rockchip Electronics

Project:	RV1106G_CoreDloc_SL		
File:	45.VI-MIPI_SL_Module-RMSL312		
Date:	Saturday, September 24, 2022	Rev:	V1.2
Designed by:		Sheet:	14 of 20

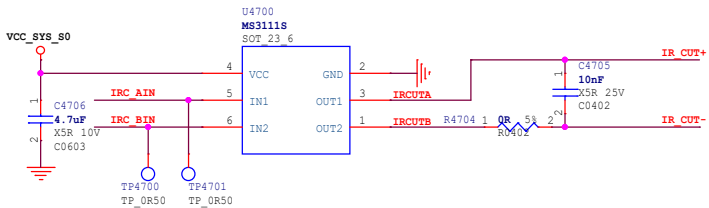
RGB Camera

GC2093 sensor  
AVDD=2.8V  
DVDD=1.2V  
DOVDD=1.8V



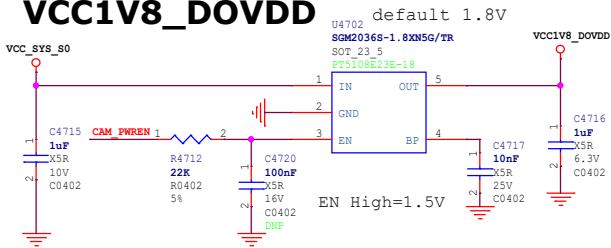
通用0.5mm间距30PIN下接座

IR-CUT Drive

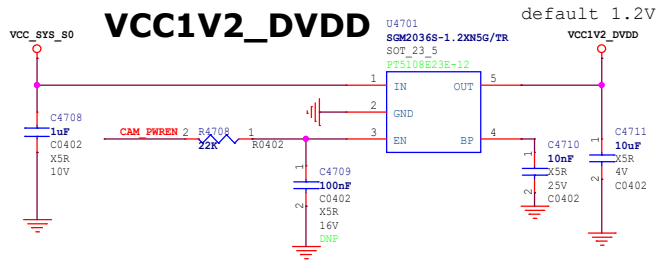


Power for Camera

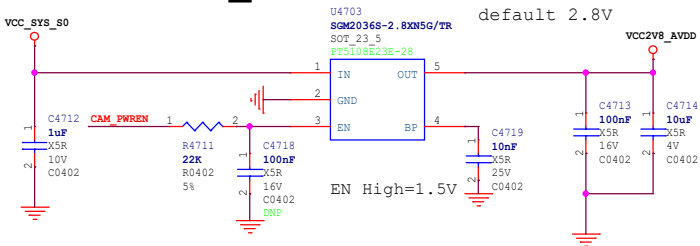
VCC1V8\_DOVDD



VCC1V2\_DVDD

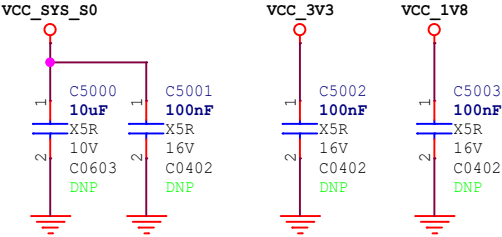
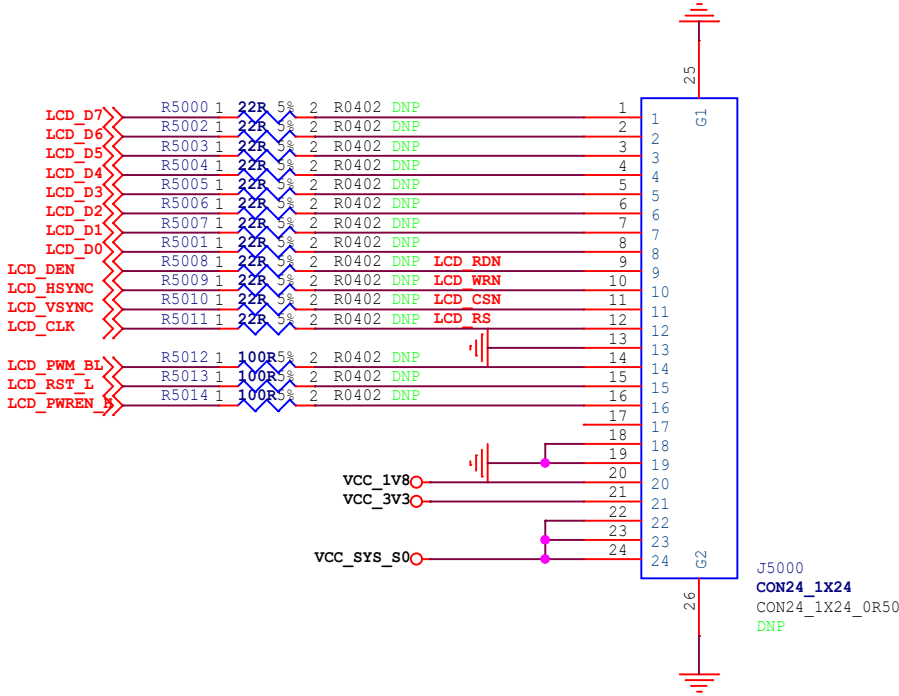


VCC2V8\_AVDD



50.VO-8Bit MCU Panel(Optional)

预留门锁室外屏（8bit MCU Panel）

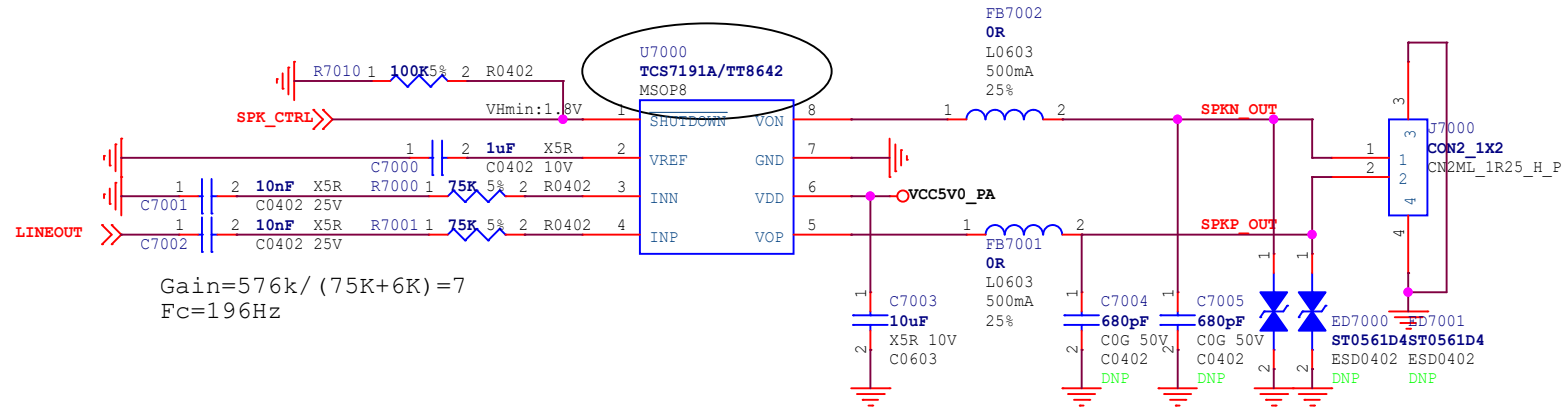


	mcu	BT656	RGB serial
Mode	8bit	8bit	3x8/4x8
LCD_D0	D0	D0	D0
LCD_D1	D1	D1	D1
LCD_D2	D2	D2	D2
LCD_D3	D3	D3	D3
LCD_D4	D4	D4	D4
LCD_D5	D5	D5	D5
LCD_D6	D6	D6	D6
LCD_D7	D7	D7	D7
LCD_DEN	RDN	--	DEN
LCD_HSYNC	WRN	--	HSYNC
LCD_VSYNC	CSN	--	VSYNC
LCD_DCLK	RS	DCLK	DCLK

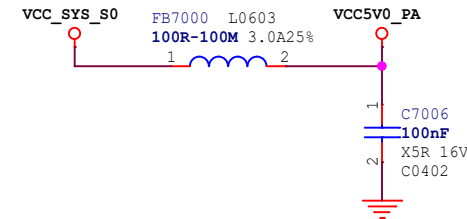
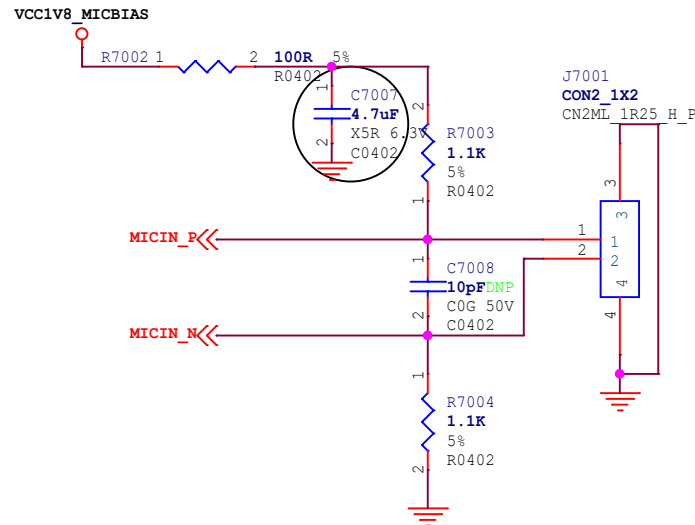


## Speaker Out


NOTE: If there is no EMI problem, the ferrite beads can be replaced by 0ohm resistors;



## MIC IN



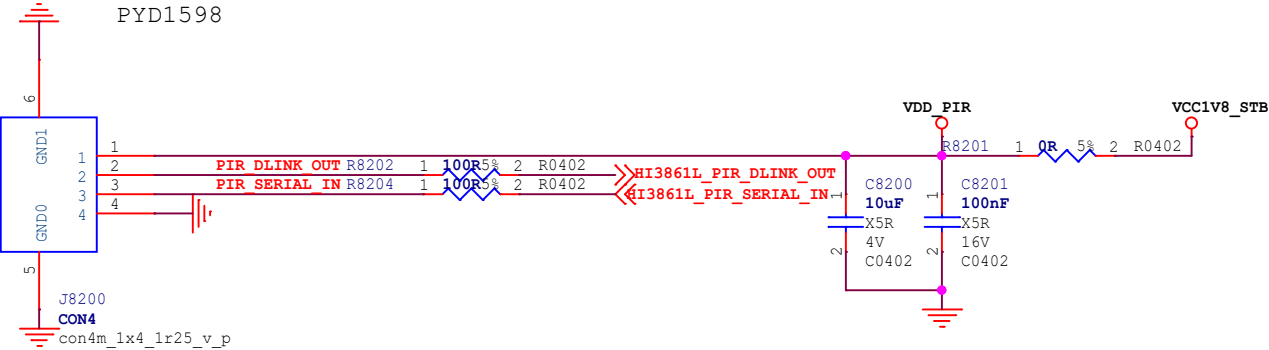
**Rockchip Confidential**



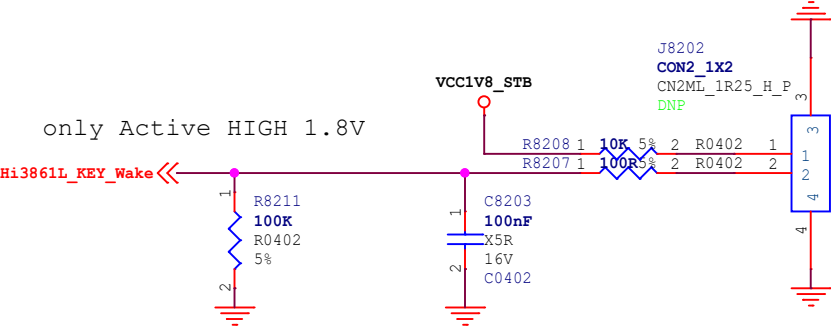
Rockchip Electronics Co., Ltd

Project:	RV1106G_CoreDloc_SL		
File:	70.Audio Port		
Date:	Saturday, September 24, 2022		Rev: V1.2
Designed by:	LLS	Reviewed by:	Default
		Sheet:	18 of 20


# PIR board



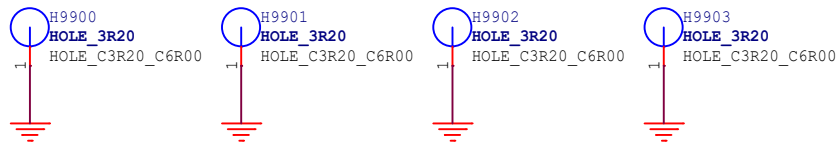
# Wake Key/Function Key (option)



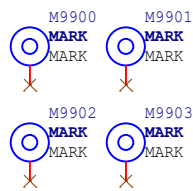
Rockchip Confidential

		Rockchip Electronics Co., Ltd	
Project:	RV1106G_CoreDloc_SL		
File:	82.PIR/Wake KEY(Optional)		
Date:	Saturday, September 24, 2022		Rev: V1.2
Designed by:	LLS	Reviewed by: Default	Sheet: 19 of 20


HOLE



MARK



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Rockchip Electronics Co., Ltd

Project:	RV1106G_CoreDloc_SL				
File:	99.MARK/HOLE				
Date:	Saturday, September 24, 2022			Rev:	V1.2
Designed by:	LLS	Reviewed by:	Default	Sheet:	20 of 20