Department of **C**omputer **E**ngineering	Subject : IT4272E - Computer System Class :……ICT-K59…… Fullname :…… Student Index:…….	Exam ID
	*Duration: **60 minutes*** *Date: 27/12/2016* *Allow student to use paper documents* *Each question has a correct option. Not decrease mark for wrong answer* *Should write the choice into Answer Part, others are illegal.*	

ANSWER PART

Question	1	2	3	4	5	6	7	8	9	10
Answer										

QUESTIONAIRE

Question 1. Which kind of memory below is the fastest?
1) DRAM 2) HDD 3) Cache 4) USB Drive

Question 2. How many 32-bit integers can be stored in a 16-byte cache line of 4 Mi-Byte cache?
1) 2 2) 4 3) 1 Mi 4) 2 Mi

Question 3. A 4-way cache has the total of 1024 line. How many lines in a cache set?
1) 256 2) 64 3) 8 4) 4

Question 4. Page Table stored the number 27 in an entry at the index of 12 (row index). Which do these number mean?
1) Virtual Page number is 27
2) Virtual Page number is 12
3) Physical Page number is 27
4) Physical Address of Byte is 12

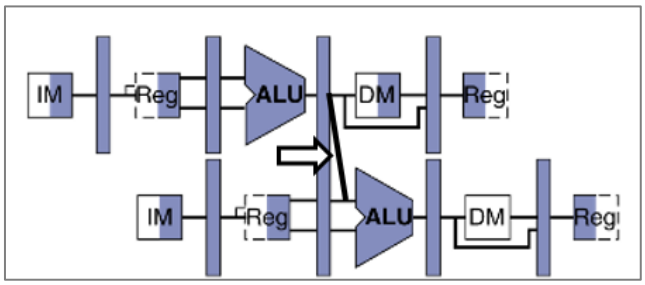
Question 5. A hard disk has the MTTF of 3 years, and the MTTR of 1 day. Calculate the MTBF of this hard disk? (1 year has 365 days)
1) 1096 2) 4096 3) 366 4) 1094

Question 6. A big data process has 20% workload cannot run in parallel. How many processors need to make the system 41 times faster?
1) 51 2) 50 3) 41 4) 40

Question 7. Which memory type is used to store software instructions?
1) Cache L1-I
2) Cache L1-D
3) Cache L1-D, RAM
4) Cache L1-I, RAM

Question 8. The mechanism in which CPU delegates another device to control transferring data directly to or from memory. What is the mechanism's name?
1) Interrupt
2) Polling
3) DMA
4) Virtual Memory

Question 9. The data path (bold line) in the diagram below resolves a hazard between 2 consecutive instructions. Choice the correct case?



1) lw $1,$2,$3
add $4,$1,$3

2) add $1, $2, $3
sw $4, 8($1)

3) sw $1, 8($2)
add $4, $1, $2

4) sub $1, $2, $3
add $2, $2, $3

Question 10. Stages latencies as following:

IF	ID	EX	MEM	WB
200 ps	170 ps	220 ps	210 ps	150 ps

What is the total latency of an **lw** instruction in a pipelined processor?
1) 800 ps
2) 950 ps
3) 1100 ps
4) 190 ps

Question 11. For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index (Line)	Offset
31 - 10	9 – 5	4 - 0

1) What is the cache line's size (in byte)?
2) How many entries (line) does the cache have?
3) Starting from power on, the following byte-addressed cache references are recorded.

Address (in Hex)	0	4	10	84	E8	A0	400	1E	8C

Calculate the line index of above addresses?
4) What is the hit ratio with above addresses?

Question 12. These are technical specifications of the hard disk Toshiba Travelstar 5K1000

- Average Seek Time: 1 ms
- Rotational Speed: 5400 rpm
- Controller Overhead: 5.5 ms
- Transfer Rate: 125 MiByte/s
- Sector Size: 1024 Byte

1) Calculate the average time to read or write a sector.
2) How many sectors need to store a 100-MiByte movie?
3) After defragmentation, all sector positions of that movie are continuous on disk, sector by sector. The disk can works in burn-mode, sequential read with max-speed (seeking one-time, transferring all sectors). How long to transfer the movie?

Answers for Question 11, 12

Answer 1. Cache > DRAM > HDD > USB Drive
Answer 2. 16 / (32/8) = 4 bytes
Answer 3. N-way cache, each set has N lines.
Answer 4. With Page Table, row index is the virtual page number, and the value of row is the physical page number
Answer 5. MTBF = MTTF + MTTR = 365 * 3+ 1 = 366 day.
Availability = MTTF / (MTTF + MTTR) = 365/366
Answer 6. Speedup(N) = N – S(N-1) = N(1-S) + S
41 = N(1-20%) + 20%
➔ N = (41- 0.2)/0.8 = 51
Answer 7.
Answer 8.
Answer 9.
Answer 10. Max(200 ps, 170 ps, 220 ps, 210 ps, 150 ps) * Count(200 ps, 170 ps, 220 ps, 210 ps, 150 ps)=220 x 5ps

Answer 11.
1) Line Size = $2^{\text{<length of offset>}} = 2^5 = 32$ Byte
2) Line Num = $2^{\text{<length of index>}} = 2^5 = 32$ Line
3) Table

Address	Address in	Line		Tag	Hit/Miss
0	… 0000 0000 0000	0		0	Miss
4	… 0000 0000 0100	0		0	Hit
10	… 0000 0001 0000	0		0	Hit
84	… 0000 1000 0100	4		0	Miss
E8	… 0000 1110 1000	7		0	Miss
A0	… 0000 1010 0000	5		0	Miss
400	… 0100 0000 0000	0		1	Miss
1E	… 0000 0001 1110	0		0	Miss
8C	… 0000 1000 1100	4		0	Hit

4) Hit Ratio = 3/9 = 1/3 = 33%

Answer 12.
1) <Average Time> = <Average Seek Time>
+ 30 / <RPM>
+ <Controller Overhead>
+ <Sector Size>/<Transfer Rate>
= 1 ms
+ 30 / 5400 s
+
+ 1024 / 125.2^{20} s
= 1 ms
+ 5.555 ms
+ 5.5 ms
+ 0.016 ms
= 12.055 ms + 0.007 = 12.061
2) <Sector Quantity> = <Movie Size> / < Sector Size> = 100 x 2^{20} / 1024 = 102400 (sectors)
3) <Time> = 1 ms
+ 5.555 ms
+ 5.5 ms
+ 100 MiByte/ 125. MiByte/s
= 12.055 + 800 ms = 812.055 ms