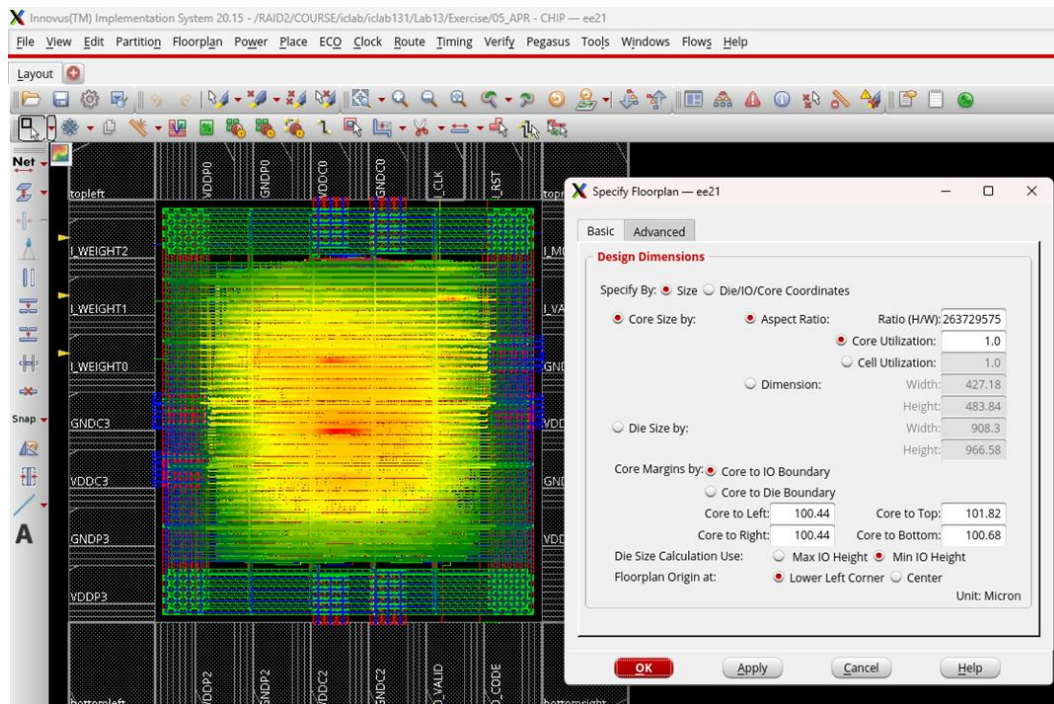
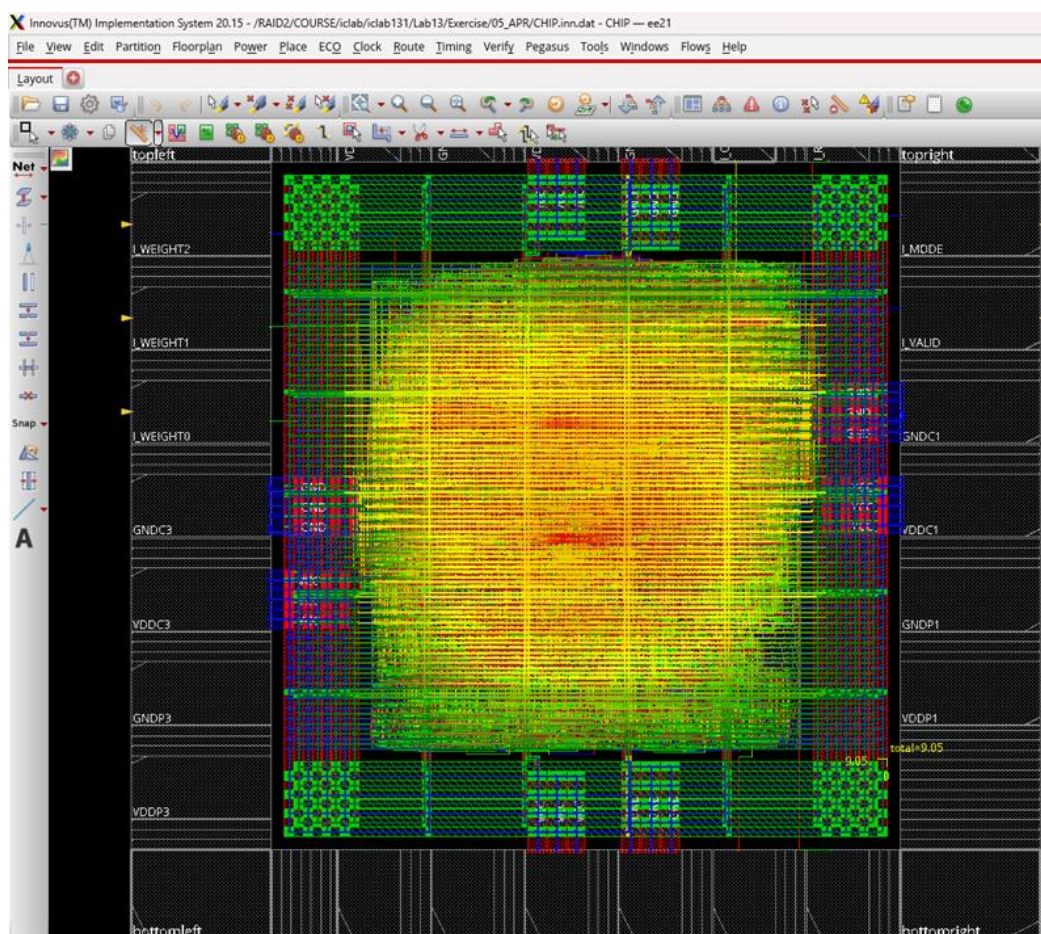


Report

1. Core to IO boundary :



2. Core Ring :



3. Post-Route setup time analysis :

Terminal Sessions View Xserver Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

ee21.ee.ncnu.edu.tw (iclab131)

131fab131Exercise05_APRpower.log

Name Size

stdcells.d 3

techonly.d 211

.top.power.db 721

cellIDMap 32

CHP.rpt 1

power.db 3.2

power.db.cnstr.td 1

static_default_ground_rail.pt... 3

static_default_power_rail.pt... 3

static_GND.ptbav 205

static_VCC.ptbav 205

stdcells.report 164

stdcells.summary 19

techonly.report 146

techonly.summary 14

voltage_power.ptfiles 1

Remote monitoring

Follow terminal folder

```
VERIFY DRC ..... Sub-Area: {0.000 725.760 230.400 966.580} 13 of 16
VERIFY DRC ..... Sub-Area: 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {230.400 725.760 460.800 966.580} 14 of 16
VERIFY DRC ..... Sub-Area: 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {460.800 725.760 691.200 966.580} 15 of 16
VERIFY DRC ..... Sub-Area: 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {691.200 725.760 900.300 966.580} 16 of 16
VERIFY DRC ..... Sub-Area: 16 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.2 ELAPSED TIME: 1.00 MEM: 57.0M) ***

Innovus I> *** timeDesign #1 [begin] : totSession cpu/real = 0:02:09.2/0:14:28.7 (0.1), mem = 3070.9M
Reset EDS DB
Ignoring AAE DB Resetting ...
Extraction called for design 'CHIP' of instances=12083 and nets=8866 using extraction engine 'postRoute' at effort level 'high'.
Integrated DRC (IQuantus) Extraction in Multi-Corner mode called for design 'CHIP'. Number of corners is 1.
No changed net or region found. No need to perform incremental extraction.

-----
timeDesign Summary
-----

Setup views included:
av_func_mode_max

-----
Setup mode | all | reg2reg | default |
-----
WNS (ns): | 0.572 | 0.572 | 1.987 |
TNS (ns): | 0.000 | 0.000 | 0.000 |
Violating Paths: | 0 | 0 | 0 |
All Paths: | 371 | 281 | 370 |
-----

-----
DRVs | Real | Total |
-----
Nr nets(terms) | Nr nets(terms) |
-----
max_cap | 0 (0) | 0.000 | 0 (0) |
max_fanout | 0 (0) | 0.000 | 0 (0) |
max_length | 0 (0) | 0 | 0 (0) |
-----

Density: 89.040%
(127.632% with Fillers)
Total number of glitch violations: 0
Reported timing to dir timingReports
Total CPU time: 1.14 sec
Total Real time: 4.0 sec
Total Memory Usage: 3116.71875 Mbytes
Reset AAE Options
*** timeDesign #1 [finish] : cpu/real = 0:00:01.1/0:00:03.1 (0.4), totSession cpu/real = 0:02:10.3/0:14:31.8 (0.1), mem = 3116.7M
Innovus I>
```

4. Post-Route hold time analysis :

Terminal Sessions View Xserver Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

ee21.ee.ncnu.edu.tw (iclab131)

131fab131Exercise05_APRpower.log

Name Size

stdcells.d 3

techonly.d 211

.top.power.db 721

cellIDMap 32

CHP.rpt 1

power.db 3.2

power.db.cnstr.td 1

static_default_ground_rail.pt... 3

static_default_power_rail.pt... 3

static_GND.ptbav 205

static_VCC.ptbav 205

stdcells.report 164

stdcells.summary 19

techonly.report 146

techonly.summary 14

voltage_power.ptfiles 1

Remote monitoring

Follow terminal folder

```
# Design Name: CHIP
# Design Mode: 180nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: SPEF/RCDB
# Signoff Settings: SI On

*****
AAE INFO: 1 threads acquired from CTE.
Start delay calculation (fullDC) (1 T). (MEM=3087.93)
*** Calculating scaling factor for lib_min libraries using the default operating condition of each library.
Total number of fetched objects 8887
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 8866, 100.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=3147.23 CPU=0:00:02.2 REAL=0:00:02.0)
End delay calculation (fullDC). (MEM=3147.23 CPU=0:00:02.4 REAL=0:00:02.0)
Loading CTE timing window with TwFlowType 0...(CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 3147.2M)
Add other clocks and setupCteToAAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 3147.2M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=3113.35)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 8887.
Total number of fetched objects 8887
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 8866, 0.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=3152.51 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=3152.51 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:02.9 real=0:00:03.0 totSessionCpu=0:02:23 mem=3152.5M)

-----
timeDesign Summary
-----

Hold views included:
av_func_mode_min

-----
Hold mode | all | reg2reg | default |
-----
WNS (ns): | 0.233 | 0.233 | 9.793 |
TNS (ns): | 0.000 | 0.000 | 0.000 |
Violating Paths: | 0 | 0 | 0 |
All Paths: | 371 | 281 | 370 |
-----

Density: 89.040%
(127.632% with Fillers)
Reported timing to dir timingReports
Total CPU time: 3.59 sec
Total Real time: 4.0 sec
Total Memory Usage: 3082.777344 Mbytes
Reset AAE Options
*** timeDesign #3 [finish] : cpu/real = 0:00:03.6/0:00:03.9 (0.9), totSession cpu/real = 0:02:22.8/0:16:20.3 (0.1), mem = 3082.8M
Innovus I>
```


5. DRC result :

```

ee21.ee.nctu.edu.tw (iclab131)
Terminal Sessions View Xserver Tools Games Settings Macros Help

Quick connect...

131/Lab131/Exercise05_APR/power_top...

Name Size
stdcells.d 3
techonly.d 211
top.power.db 722
cellIDMap 3
CHIP.rpt 3
power.db 3
power.db.cnstr.td 1
static_default_ground_rail.pti... 3
static_default_power_rail.pti... 3
static_GND.ptiavg 205
static_VCC.ptiavg 205
stdcells.report 164
stdcells.summary 19
techonly.report 146
techonly.summary 14
volts_power.ptfiles 1

Remote monitoring
Follow terminal folder

**MARN: (EMS-27): Message (IMPCTE-291) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.
innovus 1> set_power_rail_display -plot none
innovus 1> set_power_rail_display -plot ir
innovus 1>
innovus 1>
innovus 1> #check_ndr_spacing auto # enums={true false auto}, default=auto, user setting
#report CHIP.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 3544.9) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 230.400 241.920} 1 of 16
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {230.400 0.000 460.800 241.920} 2 of 16
VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {460.800 0.000 691.200 241.920} 3 of 16
VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {691.200 0.000 908.300 241.920} 4 of 16
VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {908.300 0.000 1139.400 241.920} 5 of 16
VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1139.400 0.000 1370.500 241.920} 6 of 16
VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1370.500 0.000 1601.600 241.920} 7 of 16
VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1601.600 0.000 1832.700 241.920} 8 of 16
VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1832.700 0.000 2063.800 241.920} 9 of 16
VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2063.800 0.000 2294.900 241.920} 10 of 16
VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2294.900 0.000 2526.000 241.920} 11 of 16
VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2526.000 0.000 2757.100 241.920} 12 of 16
VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2757.100 0.000 2988.200 241.920} 13 of 16
VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2988.200 0.000 3219.300 241.920} 14 of 16
VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3219.300 0.000 3450.400 241.920} 15 of 16
VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3450.400 0.000 3681.500 241.920} 16 of 16
VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.2 ELAPSED TIME: 1.00 MEM: 57.0M) ***
innovus 1>

```

6. LVS result :

```

ee21.ee.nctu.edu.tw (iclab131)
Terminal Sessions View Xserver Tools Games Settings Macros Help

Quick connect...

131/Lab131/Exercise05_APR/power_top...

Name Size
stdcells.d 3
techonly.d 211
top.power.db 722
cellIDMap 3
CHIP.rpt 3
power.db 3
power.db.cnstr.td 1
static_default_ground_rail.pti... 3
static_default_power_rail.pti... 3
static_GND.ptiavg 205
static_VCC.ptiavg 205
stdcells.report 164
stdcells.summary 19
techonly.report 146
techonly.summary 14
volts_power.ptfiles 1

Remote monitoring
Follow terminal folder

Total number of fetched objects 8887
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 8866, 0.0 percent of the nets selected for S
I analysis
End delay calculation. (MEM=3152.51 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (FullDC). (MEM=3152.51 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:02.9 real=0:00:03.0 totSessionCpu=0:02:23 mem=3152.5M)

-----
timeDesign Summary
-----
Hold views included:
av_func_mode_mtn

+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns): | 0.233 | 0.233 | 9.793 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 371 | 281 | 370 |
+-----+-----+-----+-----+

Density: 89.040%
(127.632% with Fillers)

Reported timing to dir/timingReports
Total CPU time: 3.59 sec
Total Real time: 4.0 sec
Total Memory Usage: 3082.777344 Mbytes
Reset AAE Options
*** timeDesign #3 [finish] : cpu/real = 0:00:03.6/0:00:03.9 (0.9), totSession cpu/real = 0:02:22.8/0:16:20.3 (0.1), mem = 3082.8M
innovus 1> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Dec 22 21:37:07 2023

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (908.3000, 966.5800)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 21:37:07 **** Processed 5000 nets.

Begin Summary
Found no problems or warnings.
End Summary

End Time: Fri Dec 22 21:37:07 2023
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.3 MEM: 0.000M)
innovus 1>

```

7. Post Layout simulation result :

```
ee21.ee.nctu.edu.tw (iclab131)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
/RAID2/COURSE/iclab/iclab131/Lab13/Exe
Name Size
Lab13_iclab131
00_tar 1
01_submit 1
02_check 1
Lab13_iclab131.tar.gz 2 3
Lab13_iclab131_1st_demo.ta... 2 3

Remote monitoring
Follow terminal folder

PASS PATTERN NO.1957
PASS PATTERN NO.1958
PASS PATTERN NO.1959
PASS PATTERN NO.1960
PASS PATTERN NO.1961
PASS PATTERN NO.1962
PASS PATTERN NO.1963
PASS PATTERN NO.1964
PASS PATTERN NO.1965
PASS PATTERN NO.1966
PASS PATTERN NO.1967
PASS PATTERN NO.1968
PASS PATTERN NO.1969
PASS PATTERN NO.1970
PASS PATTERN NO.1971
PASS PATTERN NO.1972
PASS PATTERN NO.1973
PASS PATTERN NO.1974
PASS PATTERN NO.1975
PASS PATTERN NO.1976
PASS PATTERN NO.1977
PASS PATTERN NO.1978
PASS PATTERN NO.1979
PASS PATTERN NO.1980
PASS PATTERN NO.1981
PASS PATTERN NO.1982
PASS PATTERN NO.1983
PASS PATTERN NO.1984
PASS PATTERN NO.1985
PASS PATTERN NO.1986
PASS PATTERN NO.1987
PASS PATTERN NO.1988
PASS PATTERN NO.1989
PASS PATTERN NO.1990
PASS PATTERN NO.1991
PASS PATTERN NO.1992
PASS PATTERN NO.1993
PASS PATTERN NO.1994
PASS PATTERN NO.1995
PASS PATTERN NO.1996
PASS PATTERN NO.1997
PASS PATTERN NO.1998
PASS PATTERN NO.1999

-----
Congratulations!
You have passed all patterns!
Your execution cycles = 32000 cycles
Your clock period = 20.0 ns
Total Latency = 640000.0 ns
-----
$finish called from file "PATTERN.v", line 36.
$finish at simulation time 1819630000
VCS Simulation Report
Time: 1819630000 ps
CPU Time: 27.440 seconds; Data structure size: 2.2Mb
Fri Dec 22 21:39:32 2023
CPU time: 27.498 seconds in simulation
21:39 iclab131@ee21[~/Lab13/Exercise/06_POST]$
```

8. Power result :

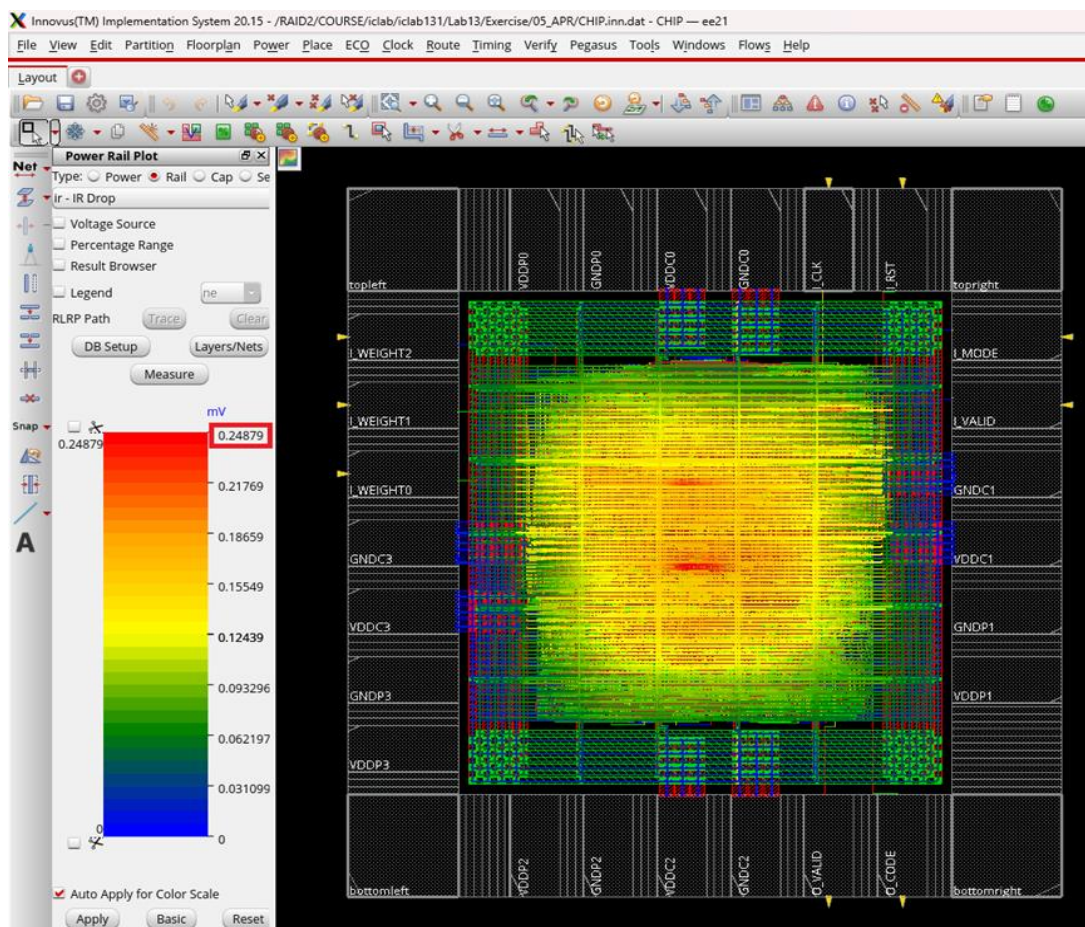
```
ee21.ee.nctu.edu.tw (iclab131)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
/RAID2/COURSE/iclab/iclab131/Lab13/Exe
Name
.cadence
Celtic
CHIP_inn.dat
CHIP_floorplan.inn.dat
CHIP_nanoRoute.inn.dat
CHIP_placement.inn.dat
CHIP_poewrplan.inn.dat
CHIP_postCTS.inn.dat
CHIP_postRoute.inn.dat
CHIP_preCTS.inn.dat
cmd
D8S
extLogDir
layermap
LEF
LIB
RC
timingReports
work
.qor_metric.tcl
00_combine

** WARN: (VOLTUS_POWER-2152): Instance GNDP3 (GNDI00) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance VDDC0 (VCCCKD) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance GNDK0 (GNDKD) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance VDDC1 (VCCCKD) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance GNDK1 (GNDKD) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance VDDC2 (VCCCKD) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance GNDK2 (GNDKD) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance VDDC3 (VCCCKD) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance GNDK3 (GNDKD) has no static power.
*

Total Power
-----
Total Internal Power: 1.41023821 50.4216%
Total Switching Power: 1.37790253 49.2655%
Total Leakage Power: 0.00875329 0.3130%
Total Power: 2.79689403
-----
```


9. IR Drop Results :



我把Core Utilization 設為 0.7 且 Core 的長寬都設為100，並盡量把Core power pad 盡量放在每個edge的正中間，讓core裡每個點到Core power pad 的距離都不會太遠，而這樣實作之後最大值大概落在 0.25 mV 。