

Homework 4: Edge-Based Line Average interpolation

NAME		林恆霈					
Student ID		E94081050					
Simulation Result							
Functional simulation	Pass	Gate-level simulation	Pass	Clock width	26 ns	Gate-level simulation time	51309 ns
<pre>YOSYS 3.7.7 run -saa ----- START!!! Simulation Start ----- --S U M M A R Y-- ----- Congratulations! Result image data are generated successfully! The result is PASS!!! ----- ** Note: \$finish : C:/IC_homework/hw4/testfixture.v(176) Time: 51298 ns Iteration: 0 Instance: /TB_ELA ----- 1</pre>				<pre># Congratulations! # # Result image data are generated successfully! # # The result is PASS!!! #----- # ** Note: \$finish : C:/IC_homework/hw4/testfixture.v(176) # Time: 51309705 ps Iteration: 0 Instance: /TB_ELA # 1 # Break in Module TB_ELA at C:/IC_homework/hw4/testfixture.v(176) -----</pre>			
Synthesis Result							
Total logic elements				221			
Total memory bit				0			
Embedded multiplier 9-bit element				0			
Flow Summary							
Flow Status				Successful - Sun May 15 16:26:19 2022			
Quartus II 64-Bit Version				13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition			
Revision Name				ELA			
Top-level Entity Name				ELA			
Family				Cyclone II			
Device				EP2K10K10-10C8			
Timing Models				Final			
Total logic elements				221 / 68,416 (< 1 %)			
Total combinational functions				203 / 68,416 (< 1 %)			
Dedicated logic registers				97 / 68,416 (< 1 %)			
Total registers				97			
Total pins				39 / 622 (6 %)			
Total virtual pins				0			
Total memory bits				0 / 1,152,000 (0 %)			
Embedded Multiplier 9-bit elements				0 / 300 (0 %)			
Total PLLs				0 / 4 (0 %)			
Description of your design							

首先在存取資料方面，我先把所有灰階值的資料都存到目標記憶體裡，再利用右的取值方法讓我只需要讀取兩個值就可以重新計算出新的值(最右邊的上下各兩個值往左平移，再讀取左邊兩個新的值即可)。

而在計算方面，我利用五個暫存器(data[4:0])與data_rd，來存當下所需要比較用組合電路算出所需的D1, D2, D3之值，最後再用一個連續的if來比較D1, D2, D3之大小與data_wr。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*