

2022 Digital IC Design Homework 2

| | | | | | |
|--|-----------|---------|------|---------|------|
| NAME | 林恆霈 | | | | |
| Student ID | E94081050 | | | | |
| Functional Simulation Result | | | | | |
| Stage 1 | Pass | Stage 2 | Pass | Stage 3 | Pass |
| Stage 1 | | | | | |
| <div>(your simulation result)</div> <pre># ----- Start ----- # -- Simulation Start -- # ----- # --stage1 simulation-- # # Setting1: PASS # # Setting2: PASS # # Setting3: PASS # # Setting4: PASS # # Setting5: PASS # # Setting6: PASS # # Setting7: PASS # # Setting8: PASS # # Setting9: PASS # # Setting10: PASS #</pre> | | | | | |
| Stage 2 | | | | | |
| <div>(your simulation result)</div> <pre># # --stage2 simulation-- # # Setting11: PASS # # Setting12: PASS # # Setting13: PASS # # Setting14: PASS # # Setting15: PASS # # Setting16: PASS # # Setting17: PASS # # Setting18: PASS # # Setting19: PASS # # Setting20: PASS #</pre> | | | | | |
| Stage 3 | | | | | |

```
# --stage3 simulation--
# Setting21: PASS
# Setting22: PASS
# Setting23: PASS
# Setting24: PASS
# Setting25: PASS
# Setting26: PASS
# Setting27: PASS
# Setting28: PASS
# Setting29: PASS
# Setting30: PASS
#
# =====
# -- Simulation finish, ALL PASS --
# =====
** Note: sfinish : C:/DC_homework/hw2/TLS_tb.av(205)
# Time: 97650 ns Iteration: 1 Instance: /testfixture

Ln: 205 Col: 0 READ Project: hw2 Now: 97,650 ns Delta: 1 smc
```

(your simulation result)

Description of your design

用兩個 register(current_state , next_state)來記錄目前以及接下來的狀態，並用兩個乾淨的組合電路(next state combination , output logic combination)來得到正確的輸出，在 output logic combination 中當 current_state 為

1. green 就把 Gout 拉為 high 。
2. yellow 就把 Yout 拉為 high 。
3. red 就把 Rout 拉為 high 。

在 next state combination 中當 current_state 為

1. green 就把 next_state 設為 yellow 。
2. yellow 就把 next_state 設為 red 。
3. red 就把 next_state 設為 green 。

再利用一個循序電路來判斷紅綠燈狀態的變換，例：當 counter 計數到了該燈號的 duration 時就切換成下一個訊號、當 set 訊號來時就把 current_state 強制換成 green、當 jump 訊號來時就把 current_state 強制換成 red、當 stop 訊號來時就維持 current_state 與 counter 數值等等。