ELEC 4700 Assignment-4

Circuit Modelling

Linh Lam

101095109

1. Using the code from the assignment 3 with fixed bottled neck value 1.5^{-7} m, the voltage sweep from 0.1 V to 10 V gives:

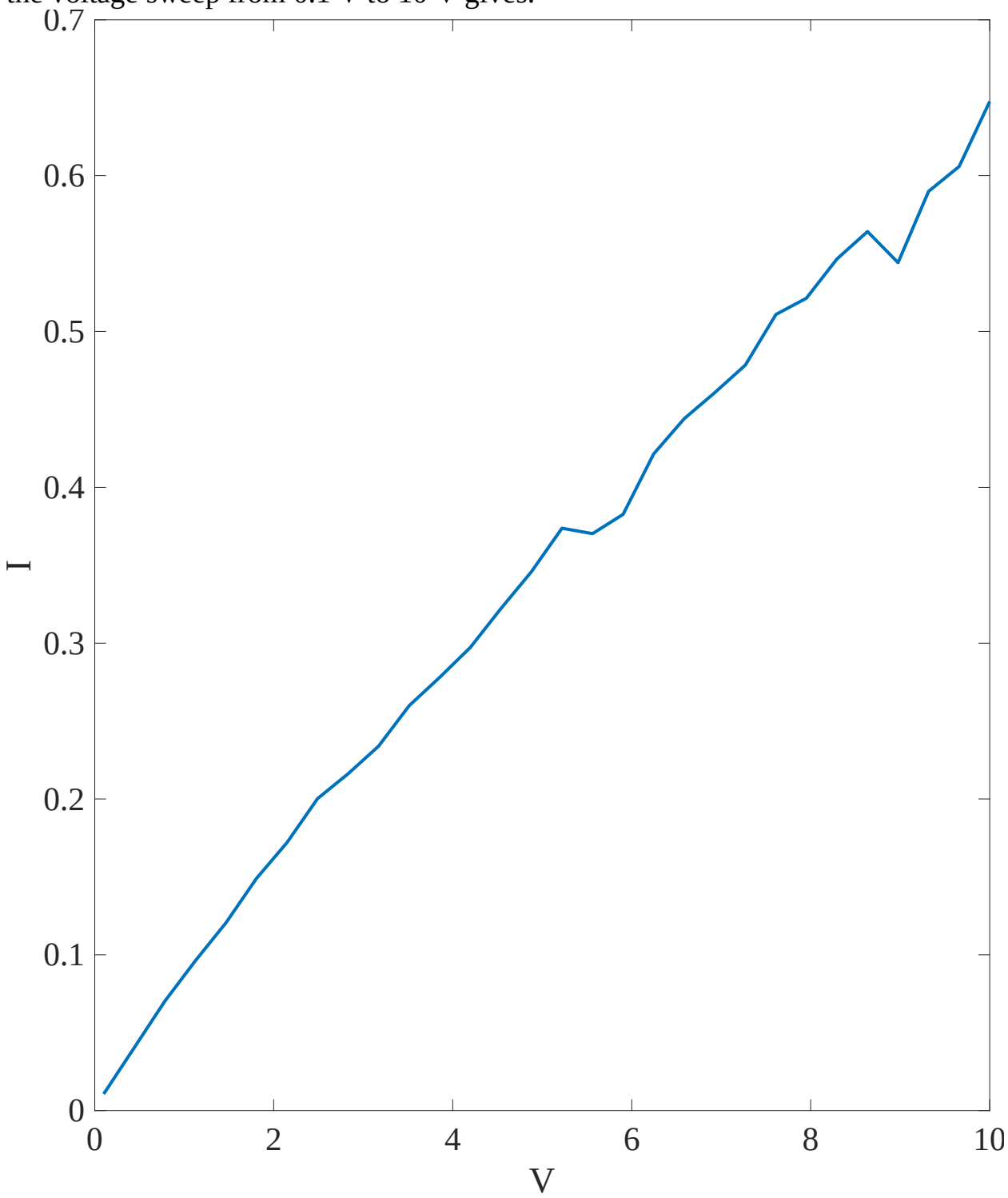

Figure 1. The current-voltage characteristics plot

2. Using linear fit to extract the resistance R_3 from the slope of figure 1:

$$y = ax = 15x$$

So, the value is **15 Ω**

3. Transient circuit simulation

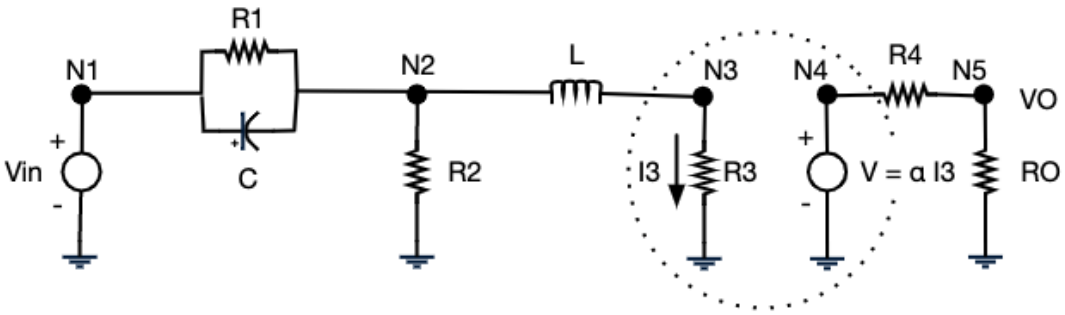

Figure 2. The circuit with R_1=1, Capacitance=0.25, R_2=2, L=0.2, α=100, R_4=0.1, and R_0=1000

Based on these parameters, $G_1 = \frac{1}{R_1} = \frac{1}{1} = 1\ \Omega^{-1}, G_2 = \frac{1}{R_2} = \frac{1}{2}\Omega^{-1}, G_4 = \frac{1}{R_4} = \frac{1}{0.1} = 10\Omega^{-1}, G_0 = \frac{1}{R_0} = \frac{1}{1000} = 10^{-3}\Omega^{-1}$

The value of R_3 is obtained from the previous part which is 15 Ω, so $G_3 = \frac{1}{15} = 0.067\ \Omega^{-1}$

a. C and G matrices

$$C\frac{dV}{dt} + GV = F$$

Using KCL on the circuit in the figure 1, we have:

$$\frac{d(V_1 - V_2)}{dt}C + (V_1 - V_2)G_1 + I_{in} = 0 \quad (1)$$

$$V_1 = V_{in} \quad (2)$$

$$\frac{d(V_2 - V_1)}{dt}C + (V_2 - V_1)G_1 + V_2G_2 + I_L = 0$$

$$V_3G_3 - I_L = 0 \quad (4)$$

$$(V_5 - V_4)G_4 + V_5 G_0 = 0$$
$$\rightarrow\ V_4 \times (-G_4)\ + V_5(G_4 + G_0) = 0 \tag{5}$$

$$\alpha V_3 G_3 - V_4 = 0 \tag{6}$$

$$V_2 - V_3 = L\frac{dI_L}{dt} \tag{7}$$

$$X = [V_1 \quad V_2 \quad V_3 \quad V_4 \quad V_5 \quad I_{in} \quad I_L]$$

$$G = \begin{bmatrix} G_1 & -G_1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -G_1 & G_1 + G_2 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & G_3 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & -G_4 & G_4 + G_0 & 0 & 0 \\ 0 & 0 & \alpha G_3 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$= \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 + 0.5 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & -0.067 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -10 & -10 + 0.001 & 0 & 0 \\ 0 & 0 & 100 * 0.067 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$= \begin{bmatrix} \mathbf{1} & \mathbf{-1} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{1} & \mathbf{0} \\ \mathbf{1} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{-1} & \mathbf{1.5} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{1} \\ \mathbf{0} & \mathbf{0} & \mathbf{-0.067} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{1} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{-10} & \mathbf{-10.001} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{6.67} & \mathbf{-1} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{1} & \mathbf{-1} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix}$$

$$C = \begin{bmatrix} C & -C & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -C & C & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -L \end{bmatrix}$$

$$\boldsymbol{C} = \begin{bmatrix} \mathbf{0.25} & \mathbf{-0.25} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{-0.25} & \mathbf{0.25} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0.2} \end{bmatrix}$$

$$\boldsymbol{F} = \begin{bmatrix} \mathbf{0} \\ \boldsymbol{V_{in}} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix}$$

The type of circuit is linear RCL circuit works as a frequency filter and amplifier.

b. DC sweep

There are both inductor and capacitor in the circuit, so when the frequency is high, the capacitor shorts circuit and inductor will cause open circuit. Meanwhile, if the frequency is low, the capacitance will result in open circuit and oppositely, the inductor leads to short circuit. Therefore, there is a certain range of frequency that can pass in this circuit. In another word, this behaves like band-pass filter.

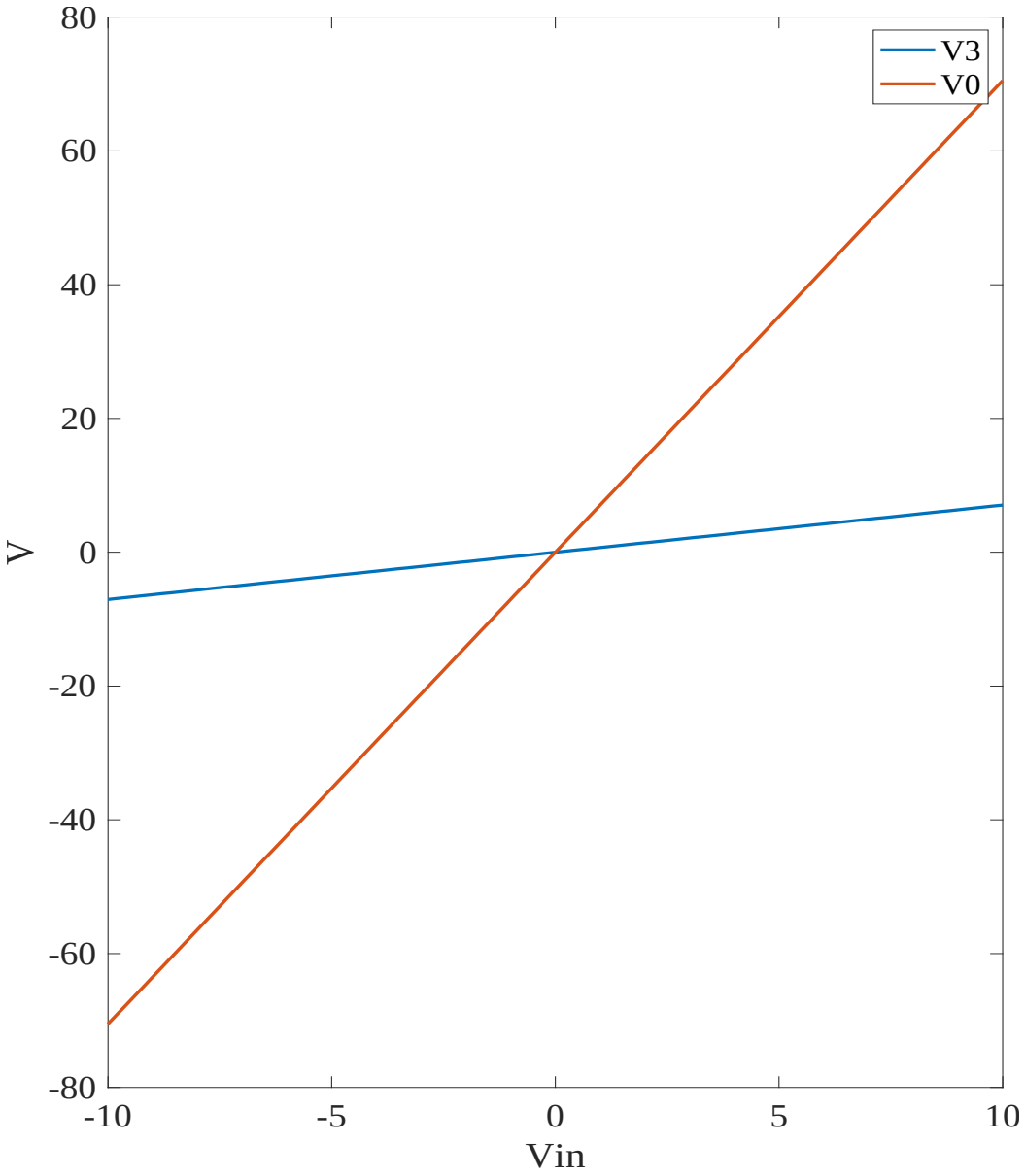

Figure 3. The plot of DC sweep from -10V to 10V.

It is observed that the output voltage keeps increasing as input voltage increases with DC sweep. Both capacitor and inductor work but they don't show any effect because the frequency is set to be 0.

c. AC gain of V_{out}/V_{in}

The formula using finite difference for the numerical solution of the time domain equation is:

$$C\frac{dV}{dt} + GV = F$$

Replace $\frac{dV}{dt} with \frac{V_i - V_{i-1}}{dt}$, we have:

$$C\frac{V_i - V_{i-1}}{dt} + GV_i = F$$

$$V_i\left(\frac{C}{dt} + G\right) - \frac{CV_{i-1}}{dt} = F$$

Calling H=$\frac{C}{dt} + G$, that results in:

$$V_i H - \frac{CV_{i-1}}{dt} = F$$

Thus, V_i is:

$$V_i = \frac{F + \frac{CV_{i-1}}{dt}}{H}$$

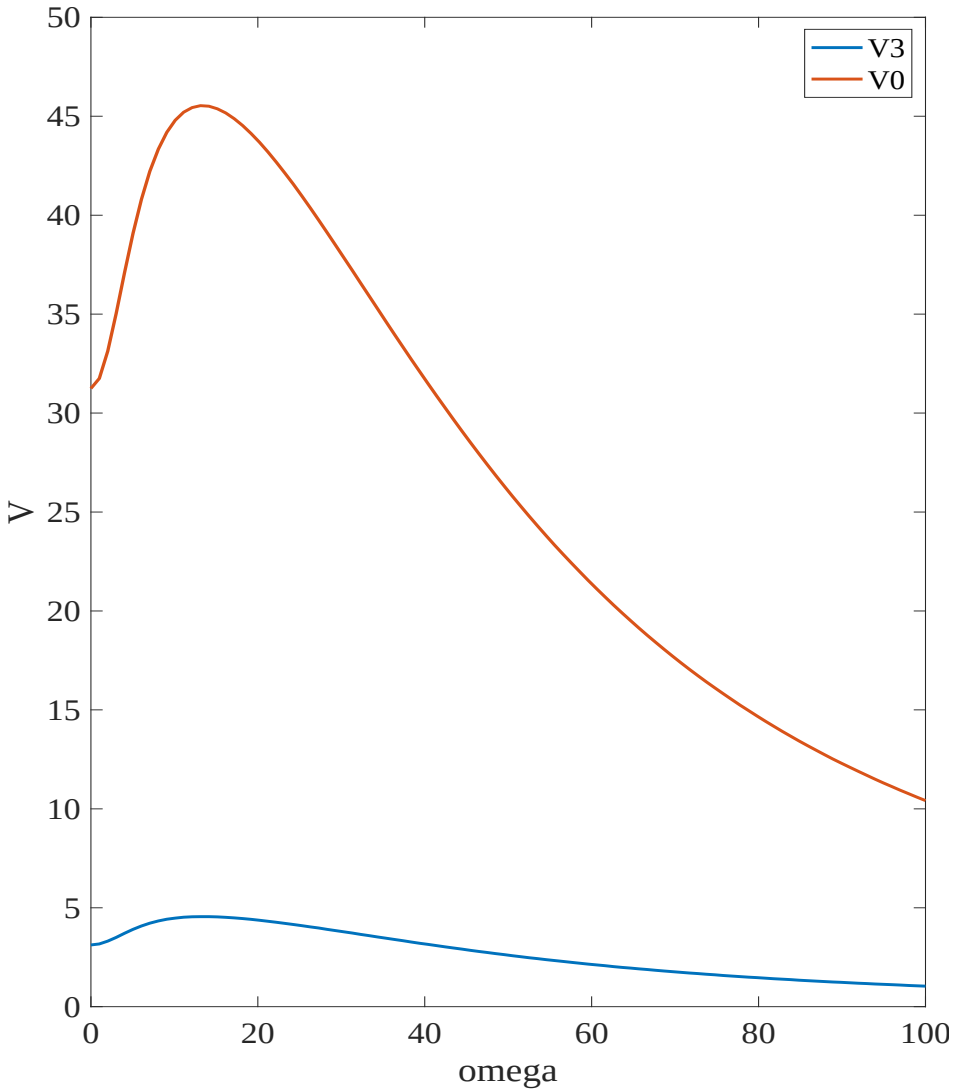

Figure 4. The plot of gain V_{out}/V_{in} in AC case.

The output voltage tends to decrease as omega increases simply because when the frequency ω is too high, it will likely cause inductor L to open circuit. Based on the circuit in figure 2, that will reduce the voltage V_3, so the output voltage depends on V_3 will decrease as well.

d. V_{in} and V_{out} from numerical solution in time domain

   A. Step voltage: The voltage is set to 0 V from 0 to 0.03 second and 1V from 0.03 second to 1 second.

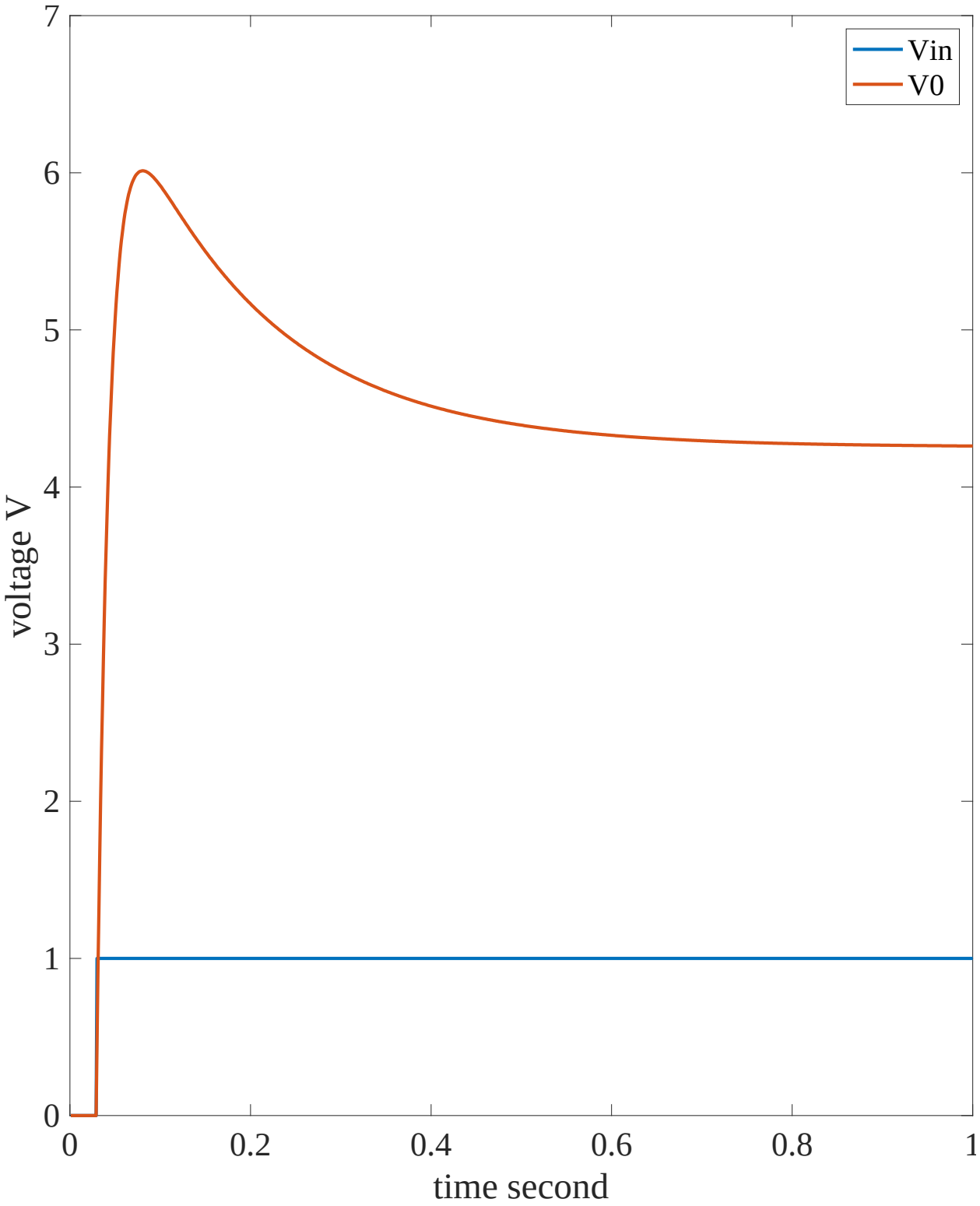

Figure 5. Plot of V_{in} and V_{out} from step voltage input.

The output voltage shows a gain along with the step input voltage and get stabilized at the end.

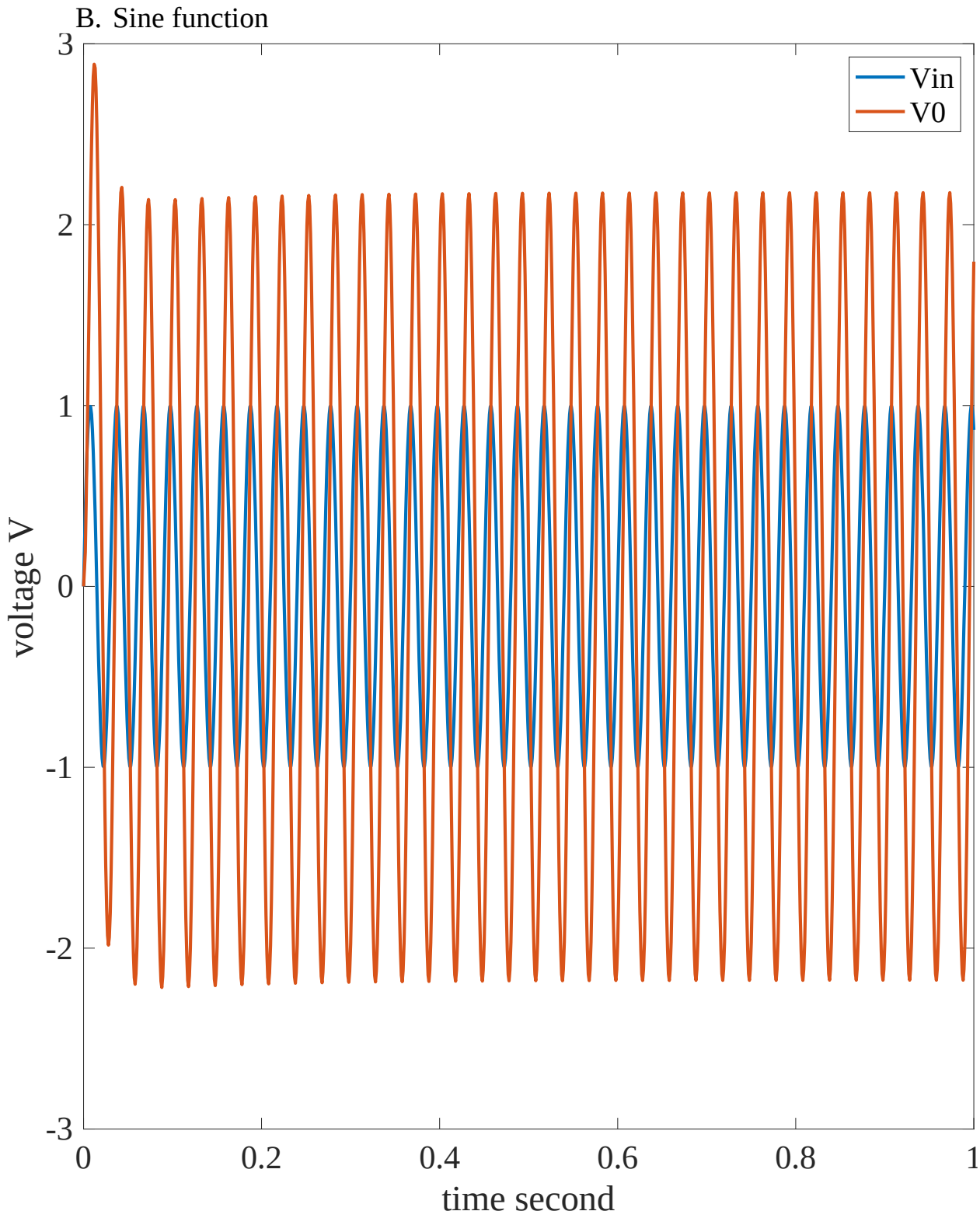

Figure 6. The plot of V_{in} and V_{out} from sin input signal and frequency is 33.33 Hz.

The output signal at the beginning is slightly higher than the rest because the circuit is not stabilized yet at first due to oscillations. The problem of oscillation is

caused by phase margin between input and output at the beginning because of feedback. But after the first two cycles, the circuit seems to be more stabilized, and the output peaks stay the same eventually.
The difference between the peak of the output and the input is because of phase shift caused by capacitor and inductor.

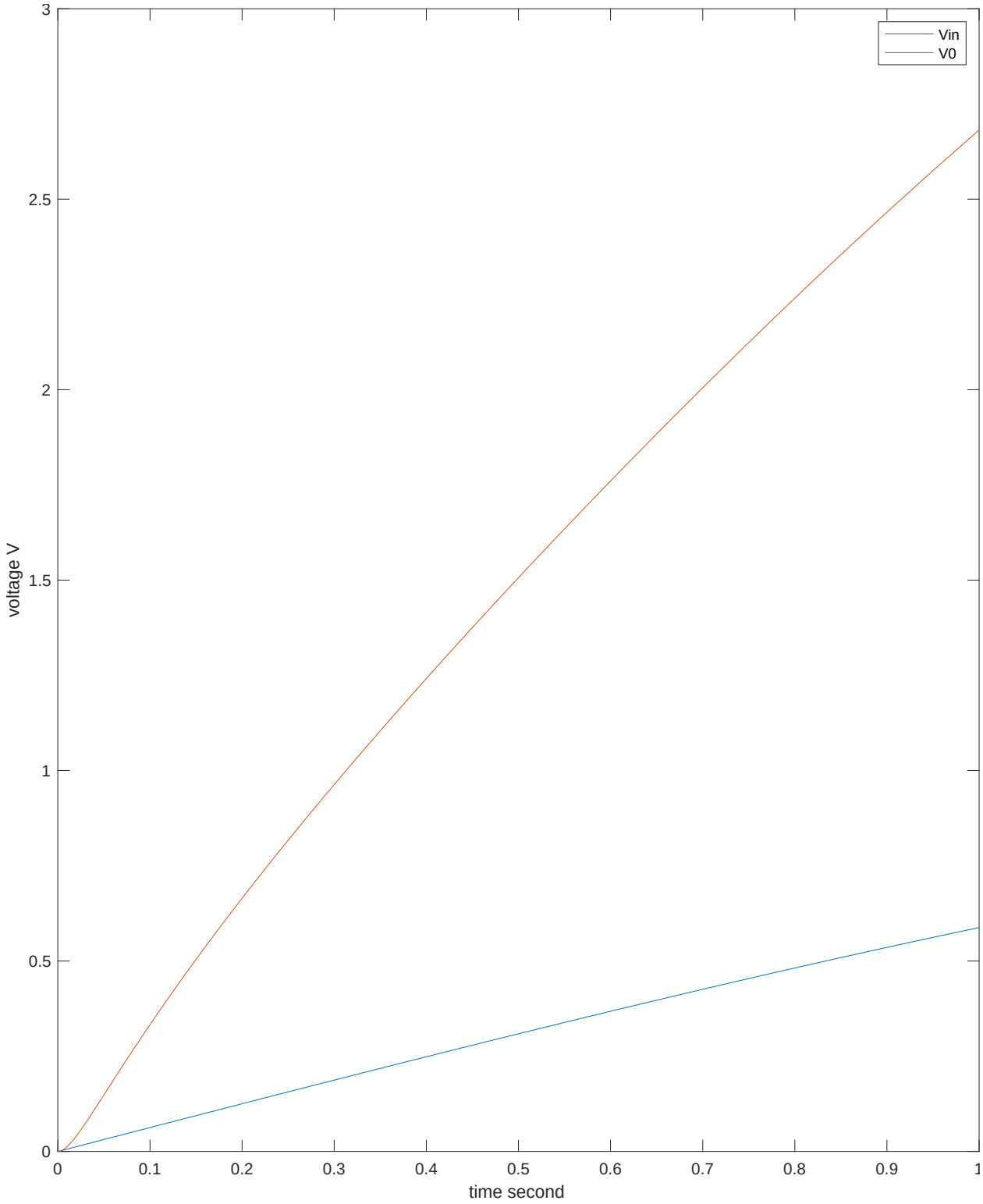

Figure 7. The plot of Vin and Vout from sin input signal and frequency is 0.1 Hz

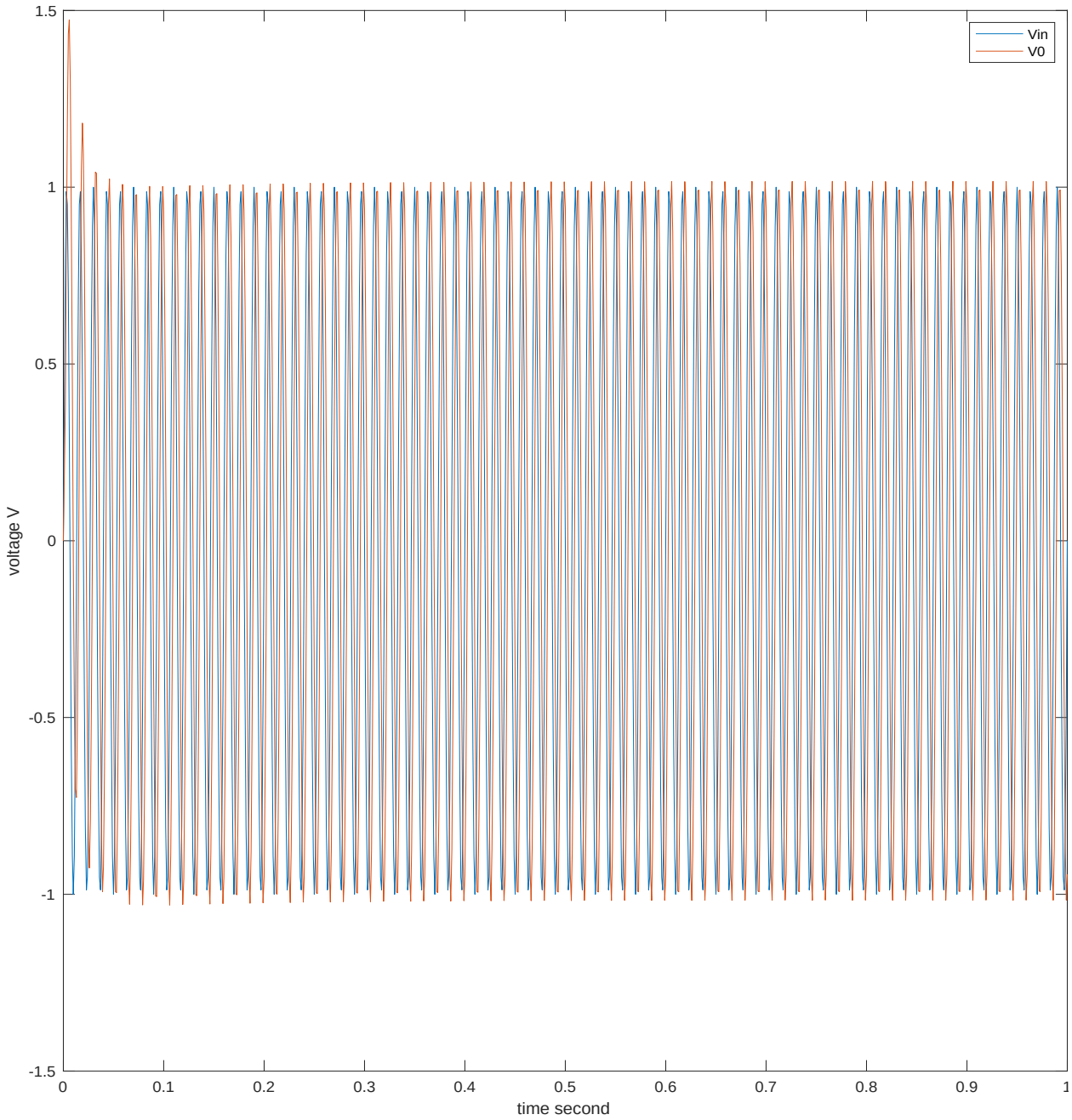

Figure 8. The plot of Vin and Vout from sin input signal and frequency is 75 Hz

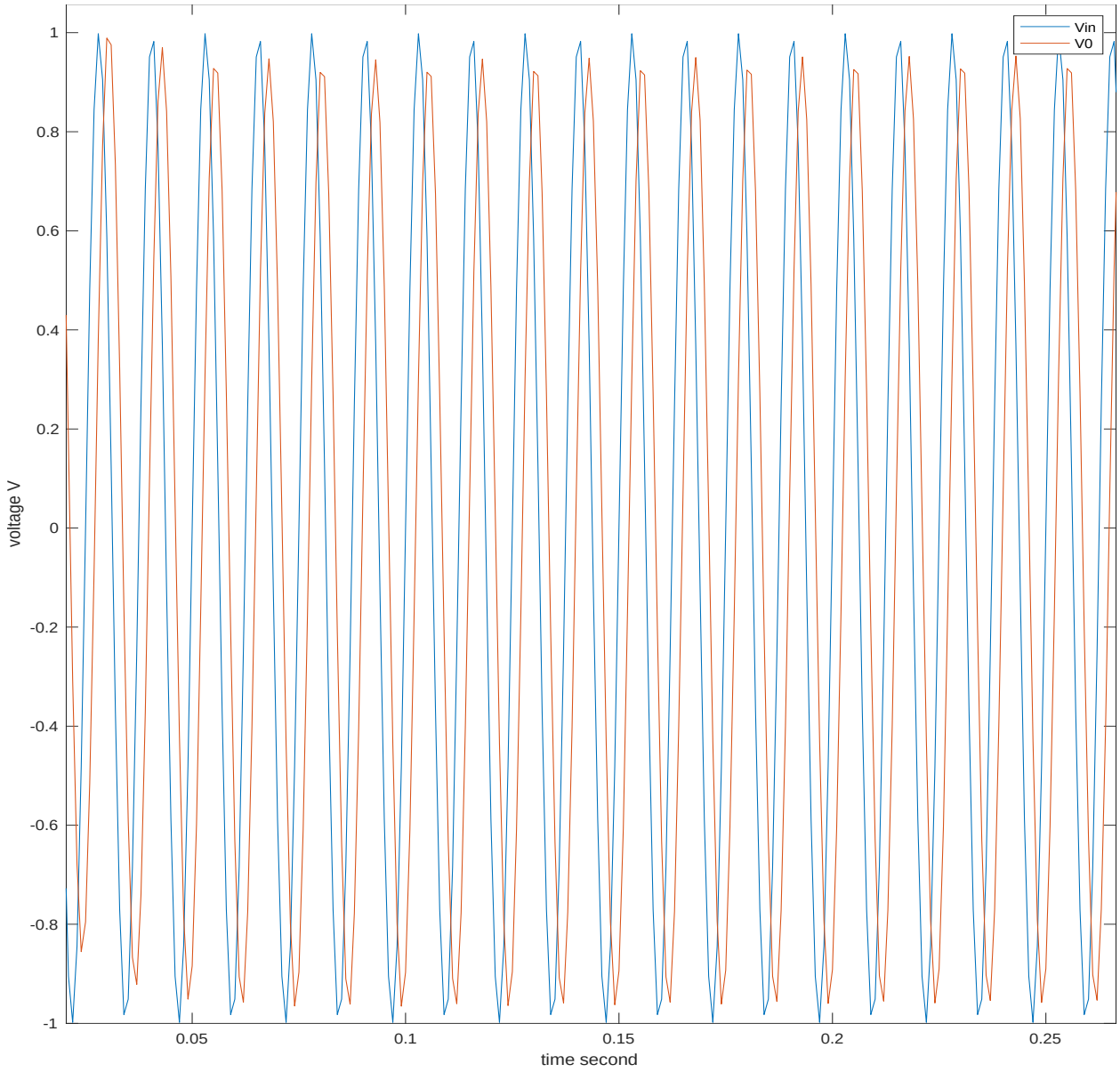

Figure 9. The plot of Vin and Vout from sin input signal and frequency is 80 Hz

At small frequency 0.1 Hz, the capacitor causes open circuit while the inductor causes short circuit. The signal can pass through probably, so it breaks the shape of sin wave (figure 7).

At higher frequency, the gain gets smaller (figure 8). The gain of output voltage is smaller than input voltage when the frequency reaches 80 Hz, because at this frequency, the inductor causes open circuit and capacitor cause short circuit. Voltage V_3 decreases sustainably and reduces the gain. Therefore, the behaviour of circuit with alternating frequency confirms the expectation that the circuit works properly at a certain range of frequency. In another word, it is a band-pass filter.

C. Gaussian pulse

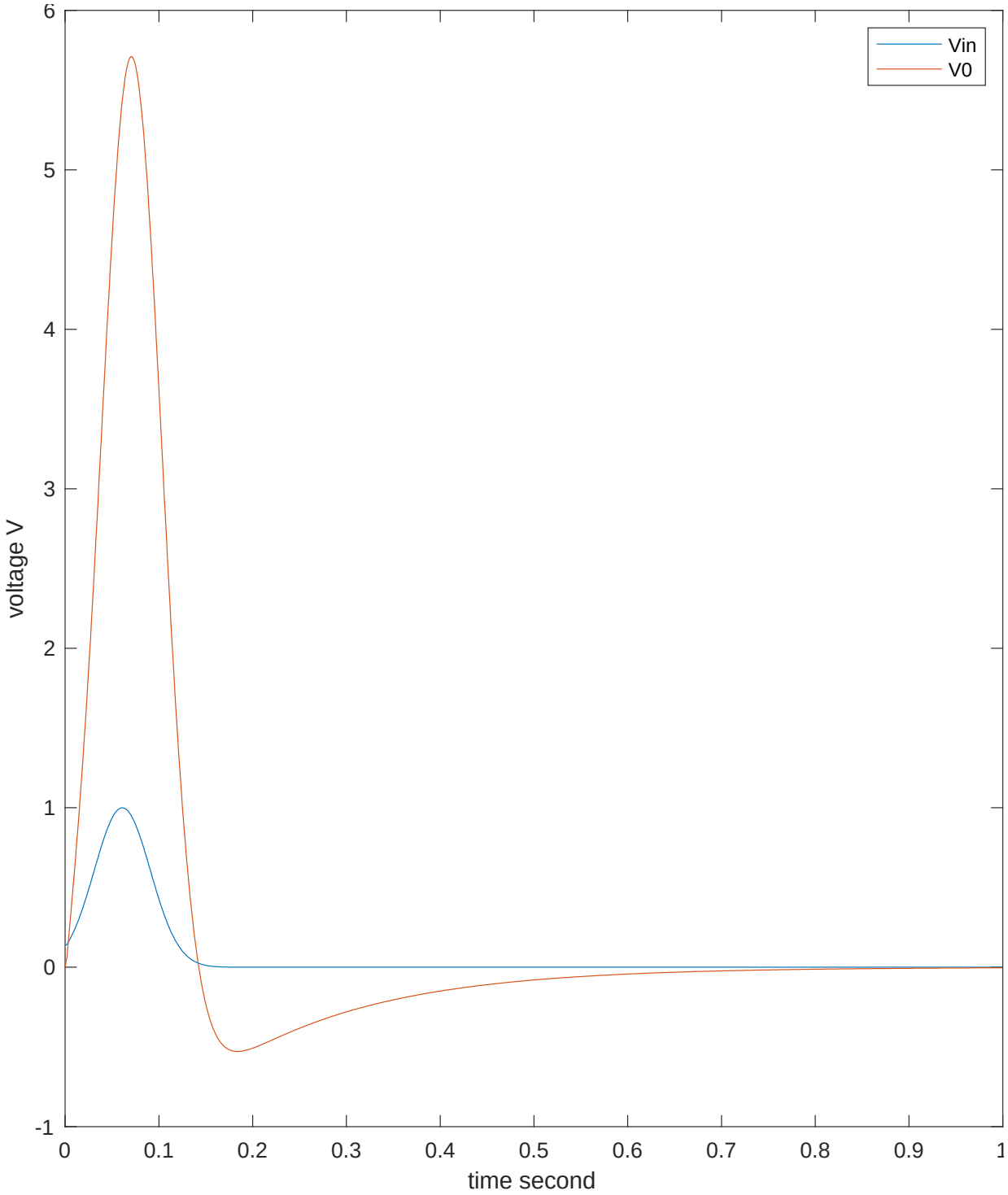

Figure 10.The plot of Vin and Vout from gaussian pulse input signal with magnitude of 1, standard deviation of 0.03s and delay of 0.06s.

The drop of output to negative could be due to the discharging behaviour of capacitor. As the time goes on, the charge stored in capacitor has been used up, so the output voltage is back to zero.

e. Fourier Transform plots of Frequency response
   As mentioned above, the circuit behaves as frequency filter, so converting voltage from time domain to frequency domain (Fourier Transform) allows us to determine voltage as the function of frequency.
   - Step voltage

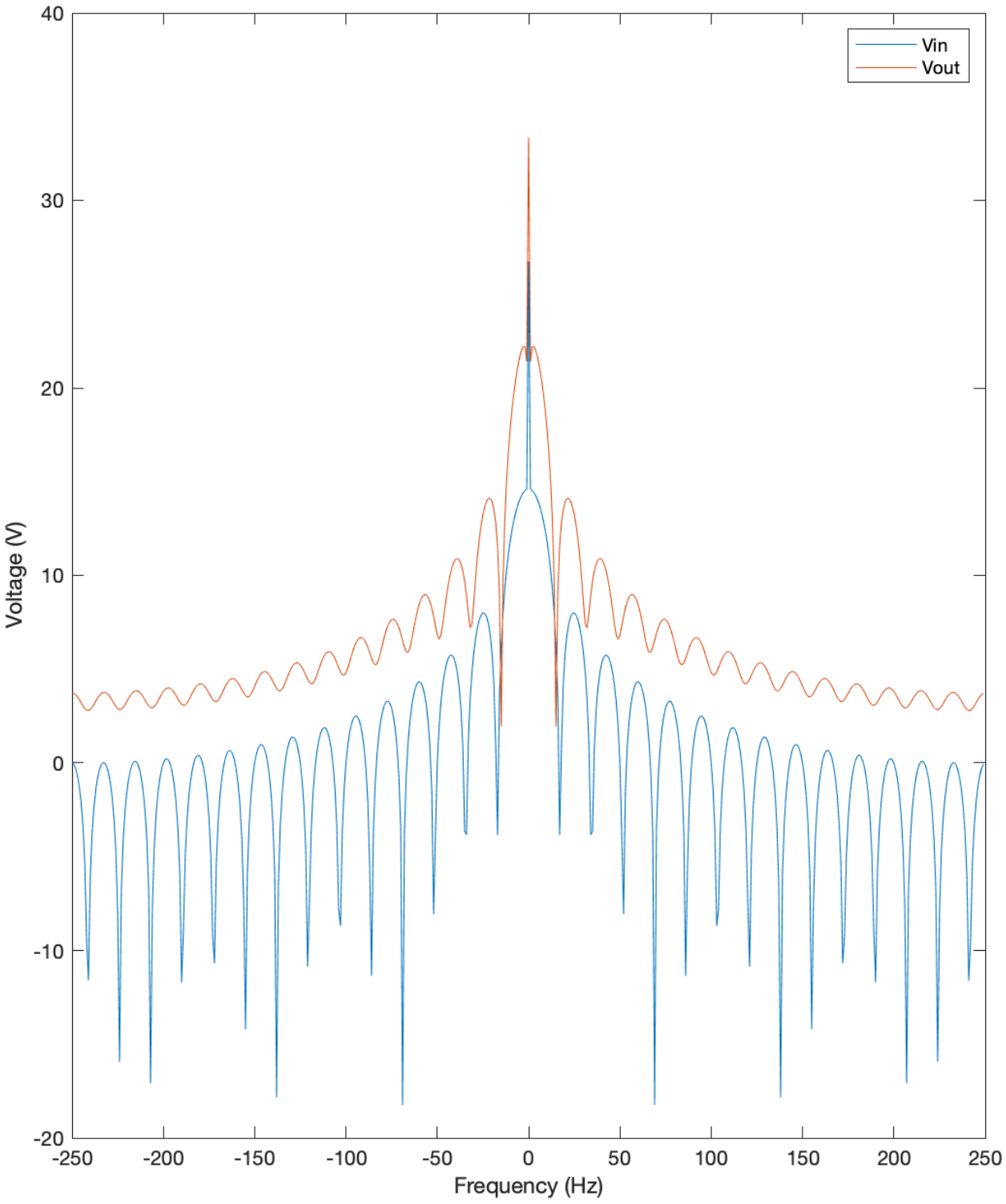

Figure 11. The Fourier Transform plot form the step input voltage.

-Sine voltage

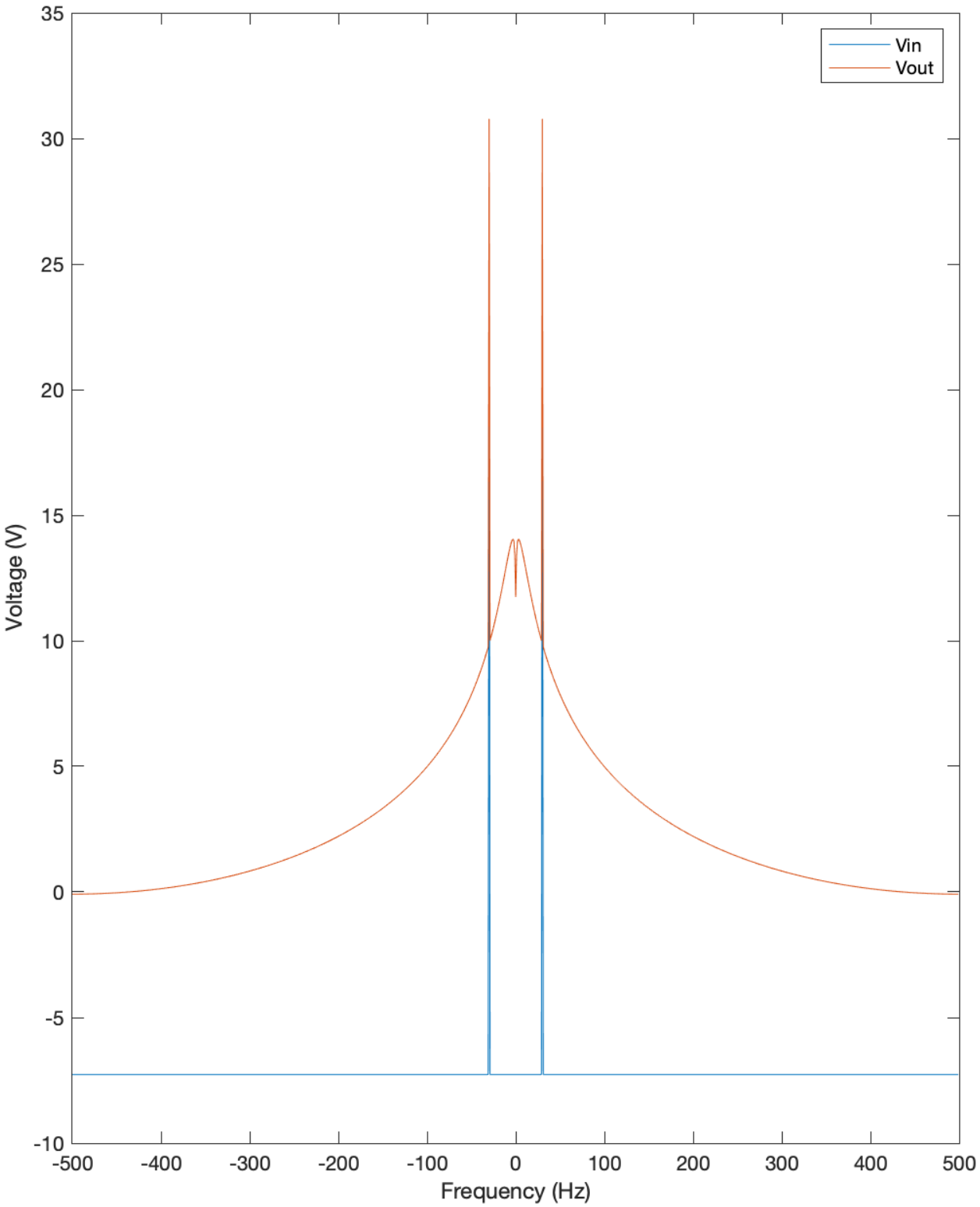

Figure 12.The Fourier Transform plot form the sine input voltage.

-Gaussian pulse

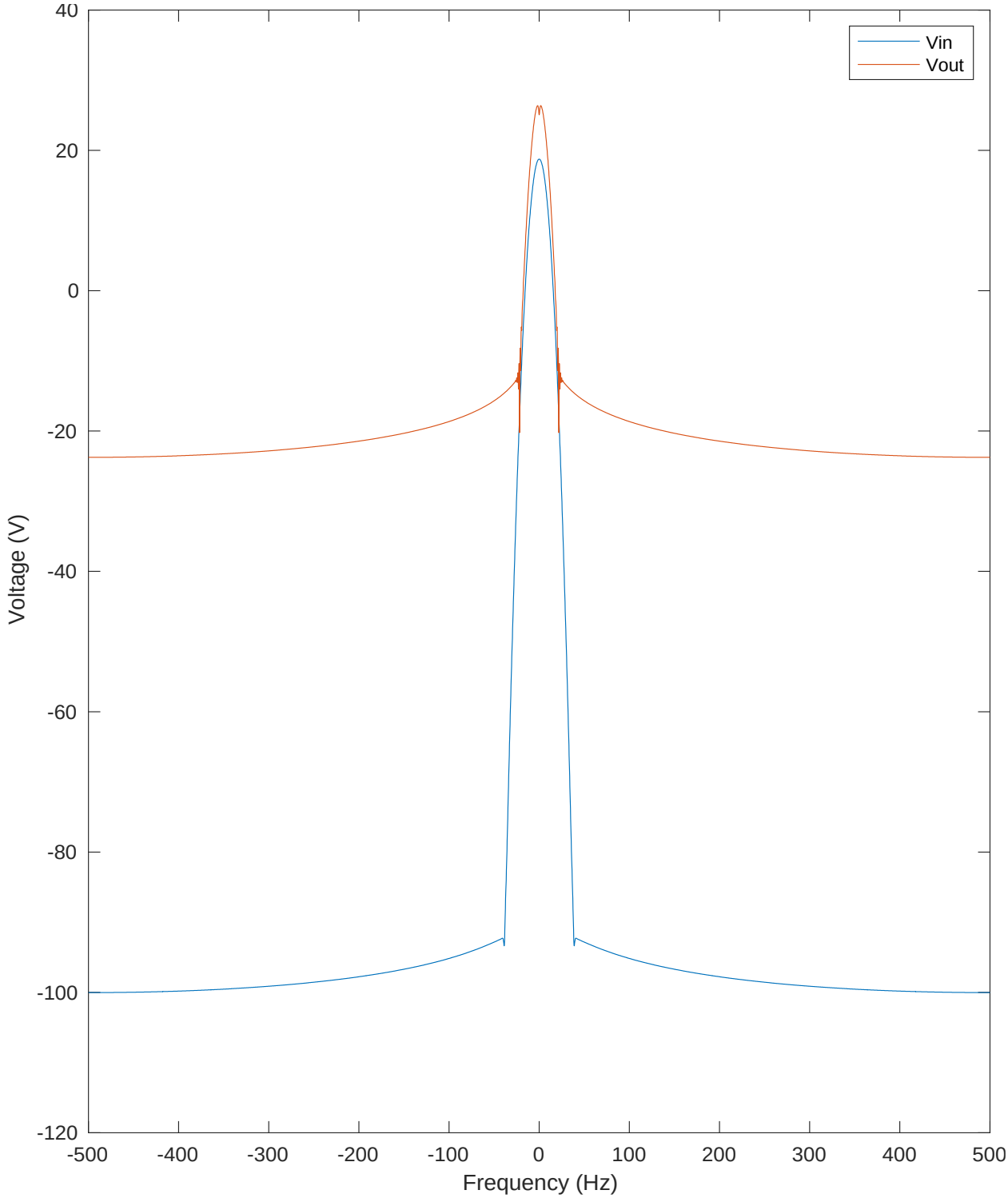

Figure 13.The Fourier Transform plot form the gaussian pulse input voltage.

4. Circuit with noise source

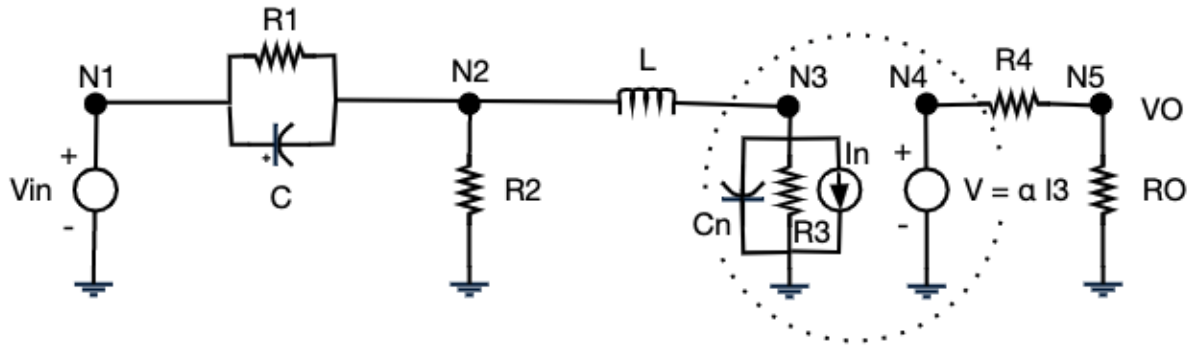

Figure 14. The circuit with added noise source.

a. New matrix CN with Cn=0.00001

$$\frac{d(V_1 - V_2)}{dt} C + (V_1 - V_2)G_1 + I_{in} = 0$$

$$V_1 = V_{in} \quad (2)$$

$$\frac{d(V_2 - V_1)}{dt} C + (V_2 - V_1)G_1 + V_2 G_2 + I_L = 0$$

$$\frac{d(V_3)}{dt} C_n - I_L + V_3 G_3 = I_n \quad (4)$$

$$(V_5 - V_4)G_4 + V_5 G_0 = 0 \quad (5)$$
$$V_4 \times (-G_4) + V_5(G_4 + G_0) = 0$$

$$\alpha V_3 G_3 - V_4 = 0 \quad (6)$$

$$V_2 - V_3 = L\frac{dI_L}{dt} \quad (7)$$

$$X = [V_1 \quad V_2 \quad V_3 \quad V_4 \quad V_5 \quad I_{in} \quad I_L]$$

$$G = \begin{bmatrix} G_1 & -G_1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -G_1 & G_1 + G_2 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & G_3 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & -G_4 & G_4 + G_0 & 0 & 0 \\ 0 & 0 & \alpha G_3 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$CN = \begin{bmatrix} C & -C & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -C & C & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & Cn & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -L \end{bmatrix}$$

$$\boldsymbol{F} = \begin{bmatrix} \mathbf{0} \\ \boldsymbol{V_{in}} \\ \mathbf{0} \\ \boldsymbol{I_n} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix}$$

b. The plot of V_{out} with noise source
   - Step voltage:

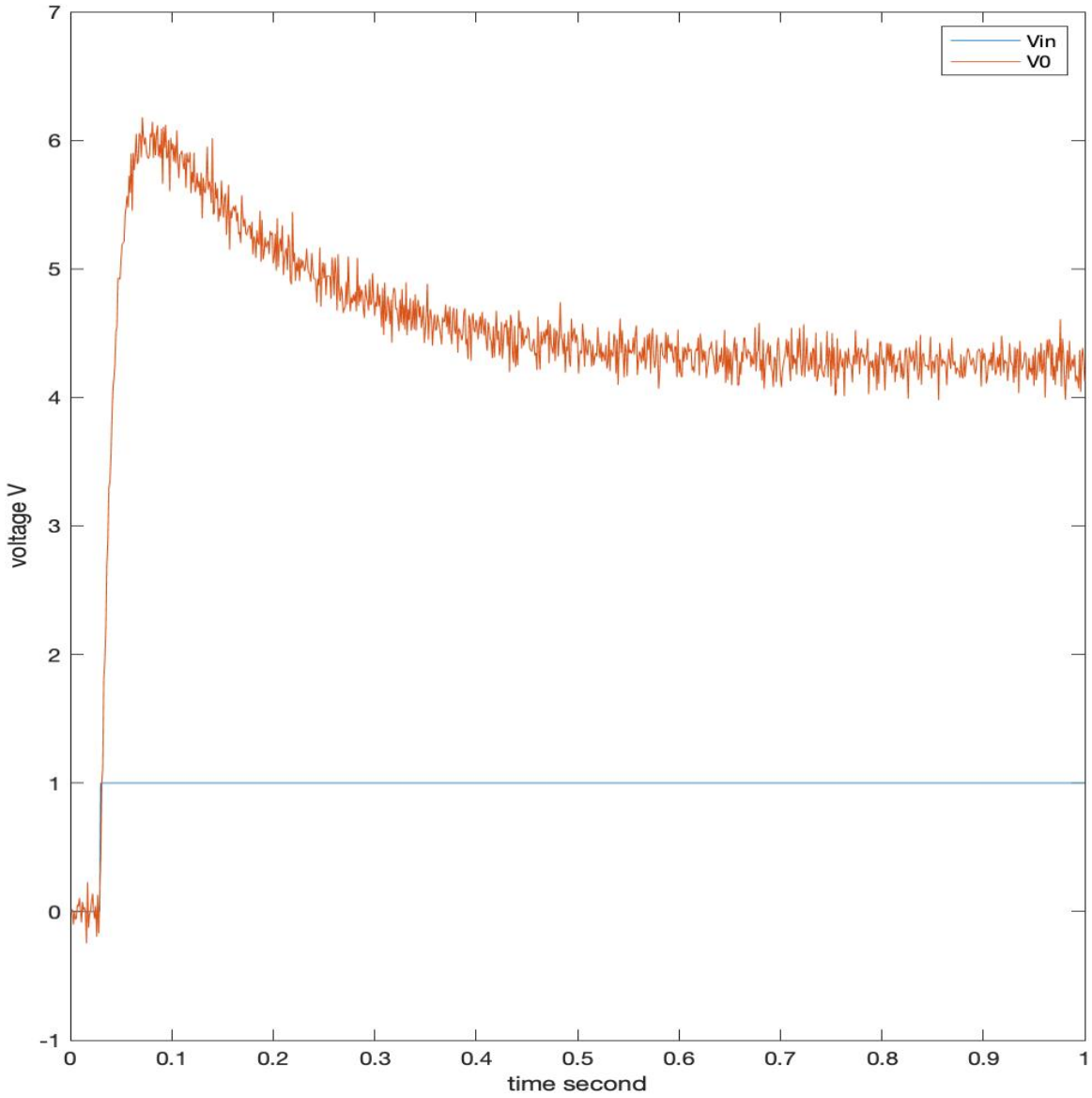

Figure 15. The plot of Vout and Vin with noise source of step input voltage.

- Sine voltage:

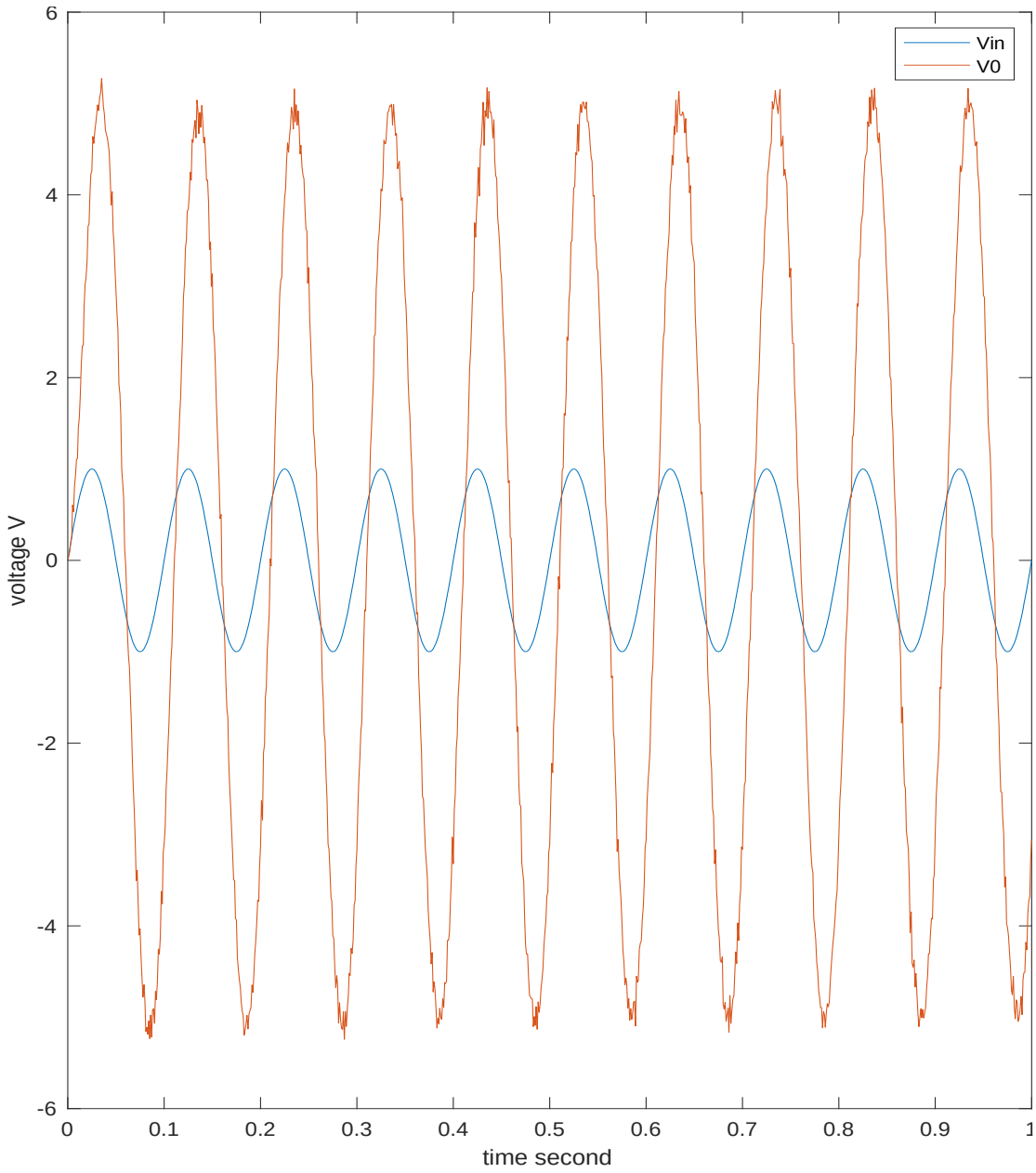

Figure 16.The plot of V_{out} and V_{in} with noise source of Sine input voltage.

- Gaussian pulse:

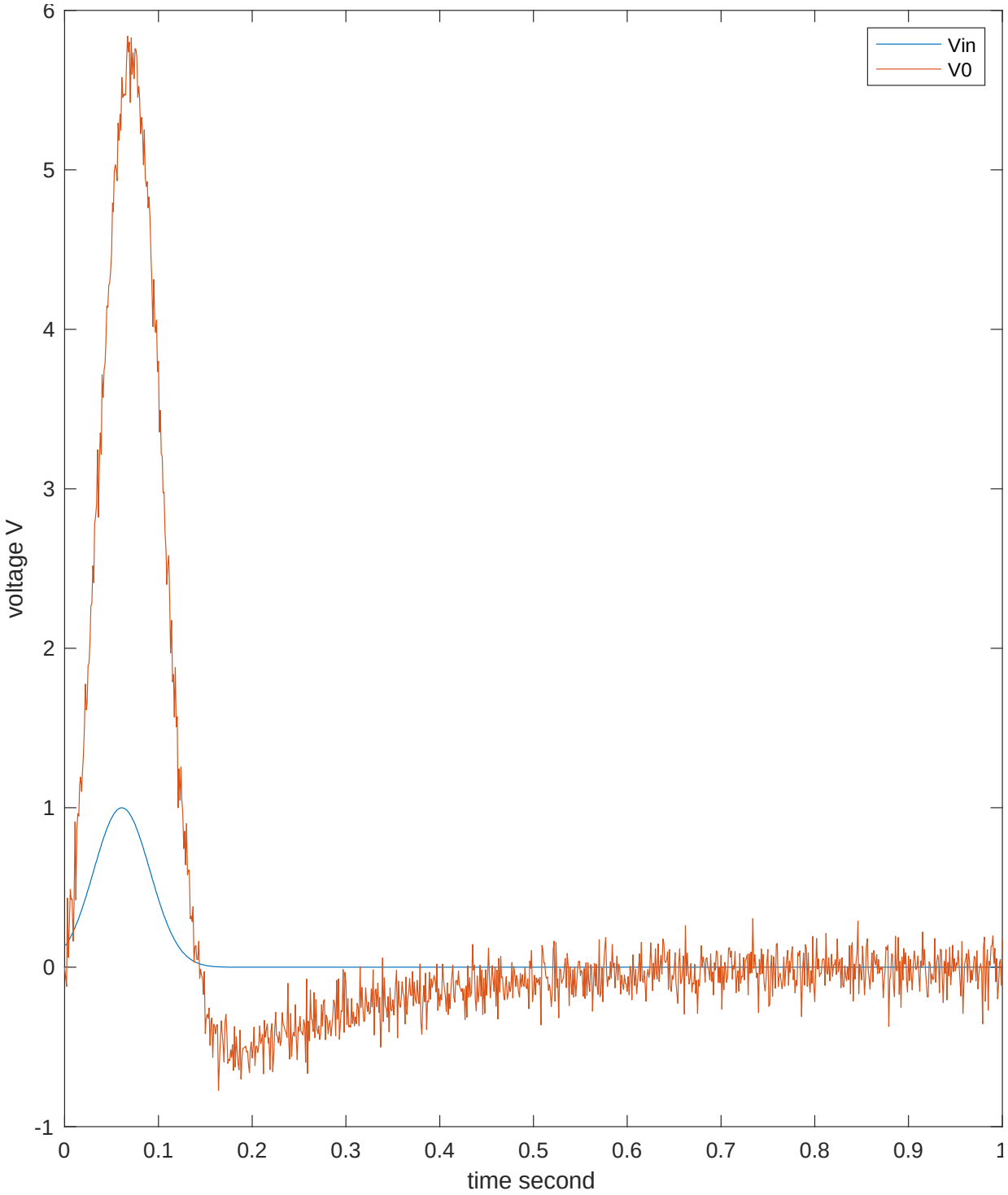

Figure 17.The plot of V_{out} and V_{in} with noise source of gaussian pulse input voltage with magnitude of 1, standard deviation is 0.03s and delay is 0.06 s.

c. Fourier Transform plot

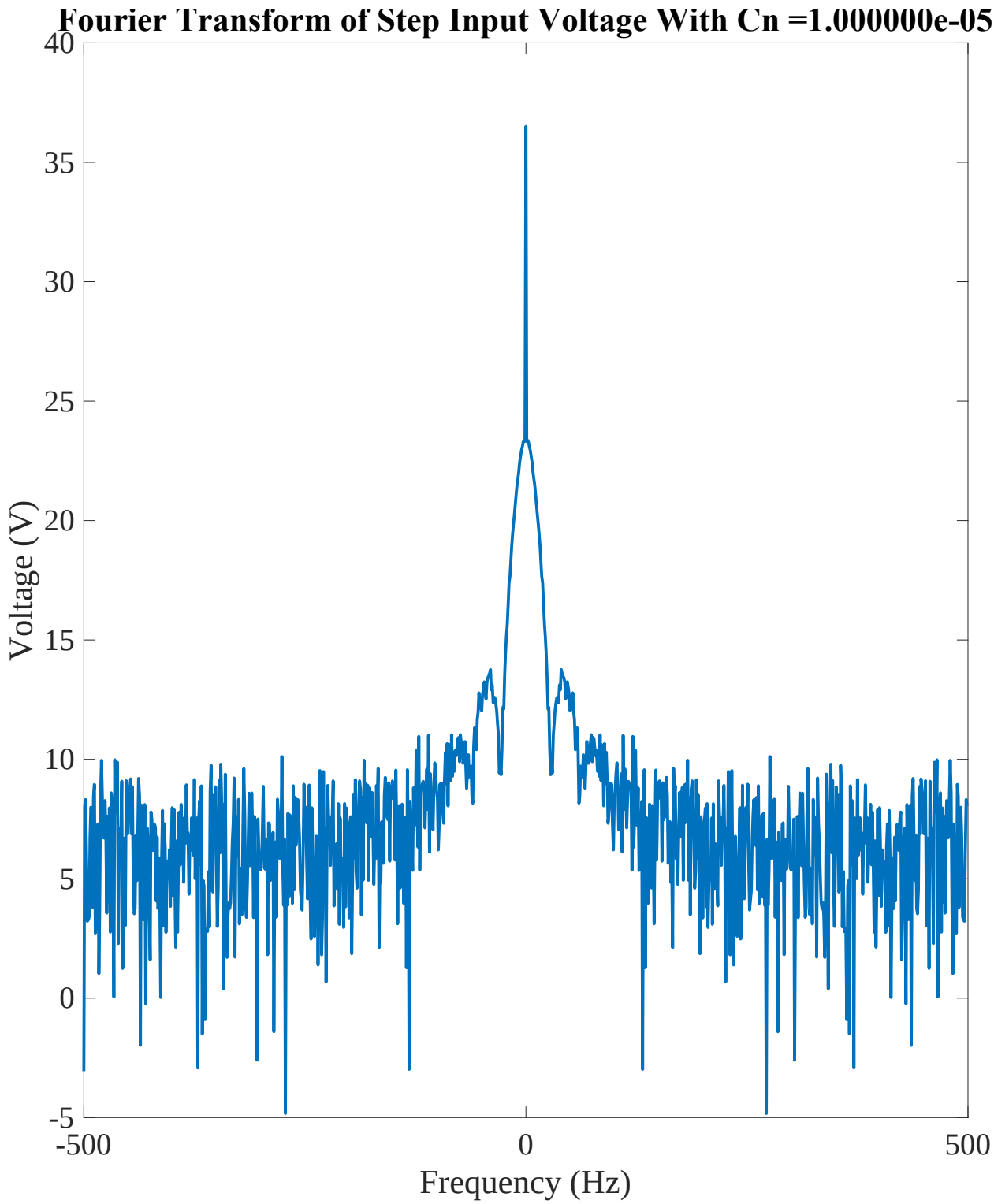

Figure 18. Fourier Transform plot of step input voltage.

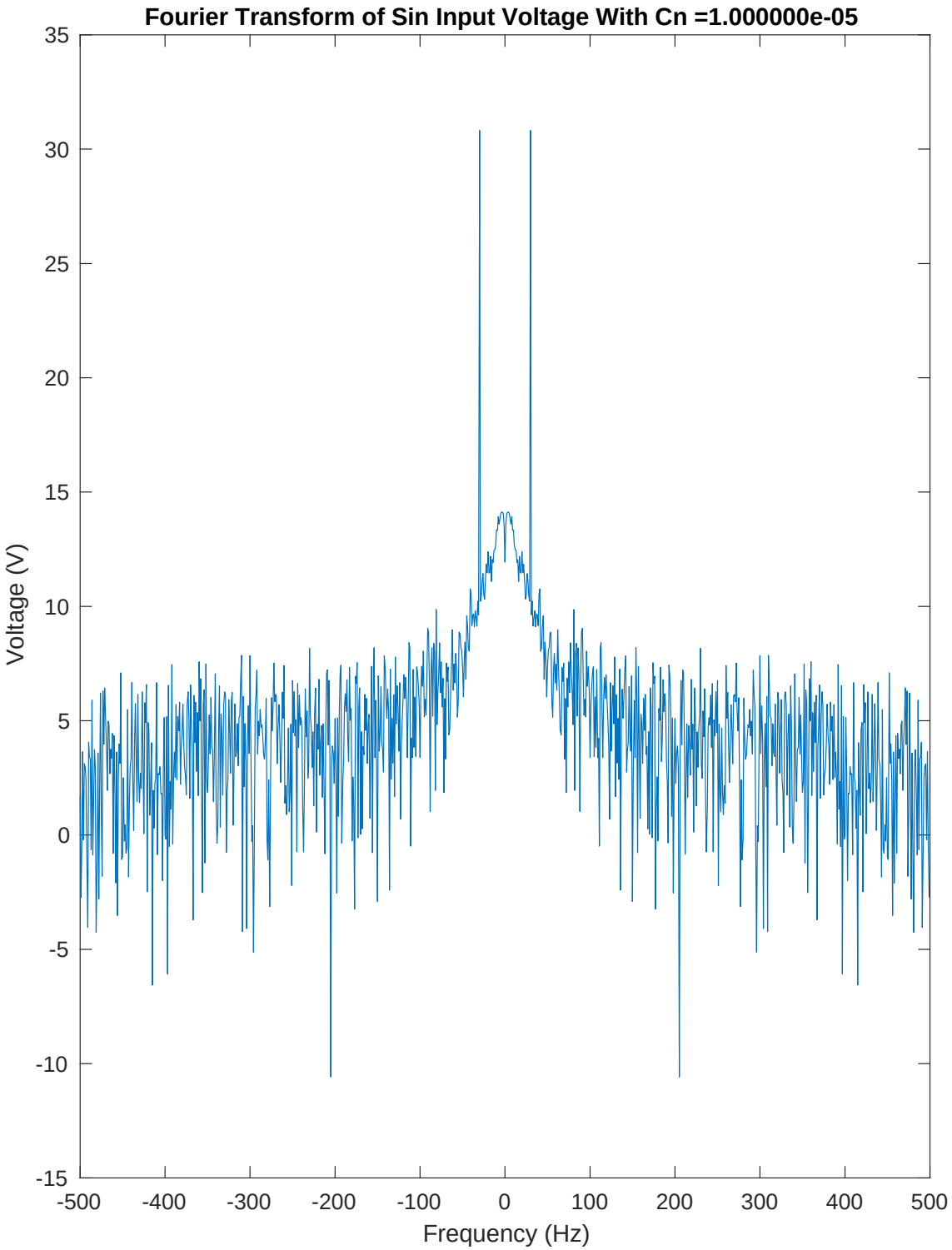

Figure 19. Fourier Transform plot of sin input voltage.

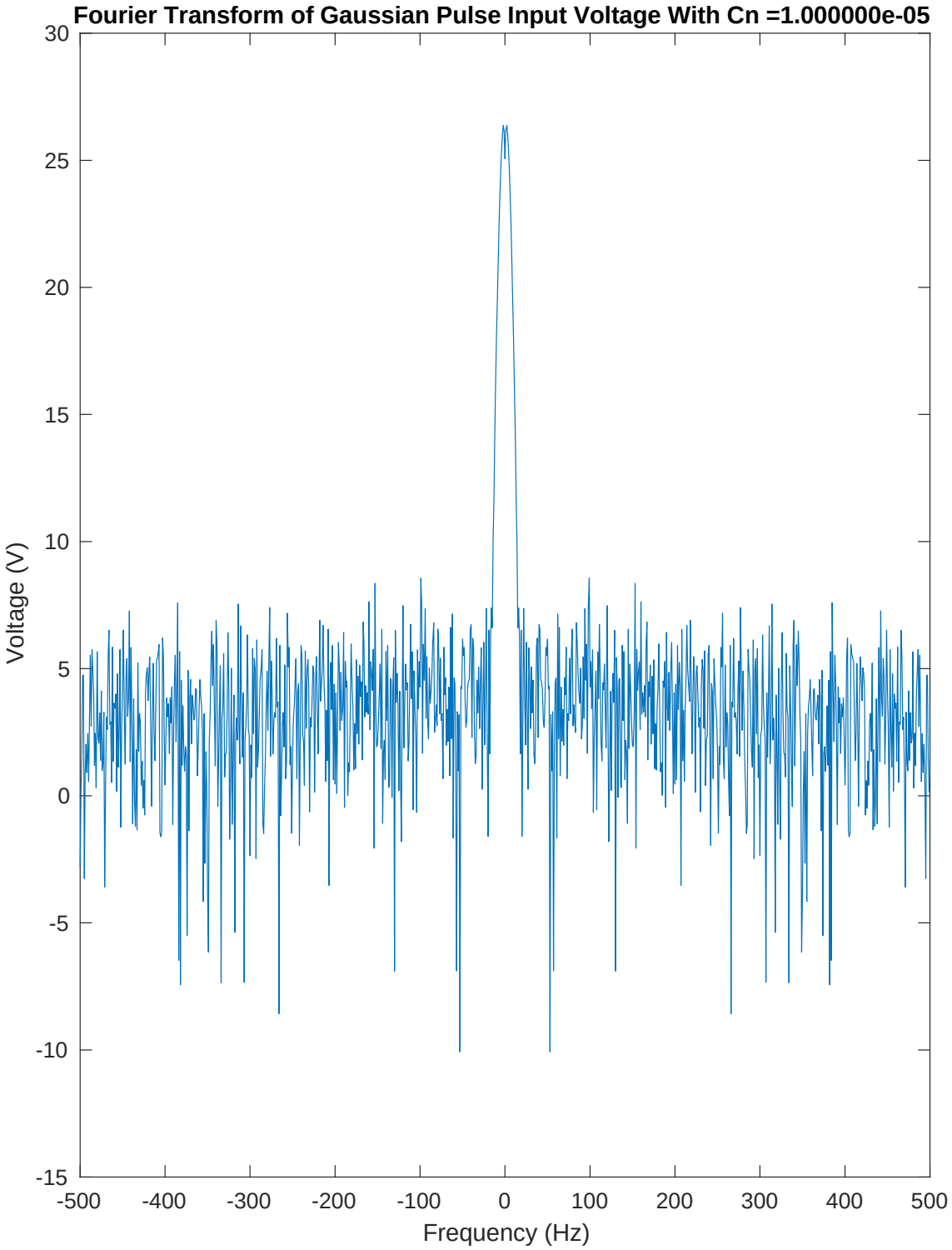

Figure 20. Fourier Transform plot of Gaussian pulse input voltage.

d. Plots of V_{out} with different values of C_n

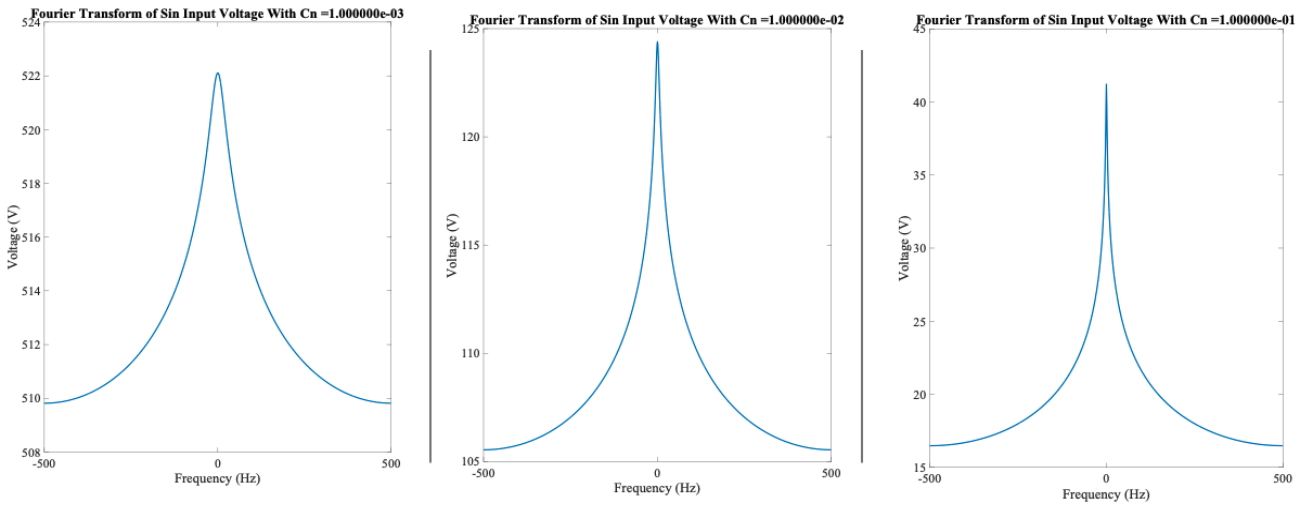

Figure 21. The Fourier transform plot of V_{out} from the sin input voltage with Cn values are 0.001, 0.01, 0.1 from left to right.

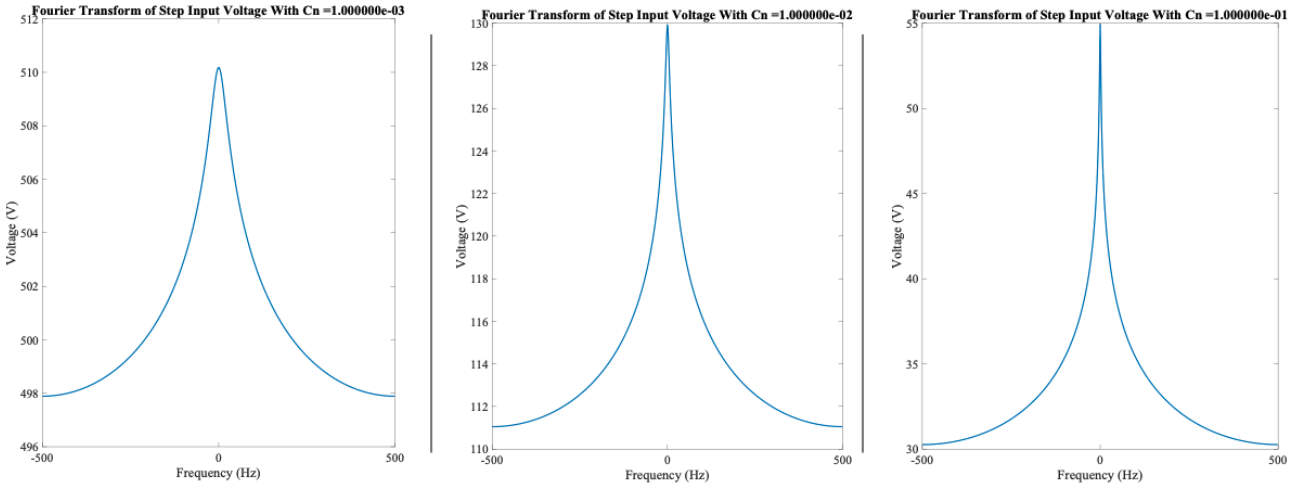

Figure 22. The Fourier transform plot of V_{out} from the step input voltage with Cn values are 0.001, 0.01, 0.1 from left to right.

When increase magnitude of C_n, the bandwidth is narrower. This behaviour is remained despite of the types on input voltage. Indeed, the trend occurs at both sin input voltage and step input voltage. The reason this happened because of the capacity of the capacitor, when its capacitance rises, the ability of capacitors of absorbing noise increases. Eventually, less noise voltage passthrough results in less output voltage.

e. Plot the V_{out} with different time steps

Varying the time step and how the simulation changes

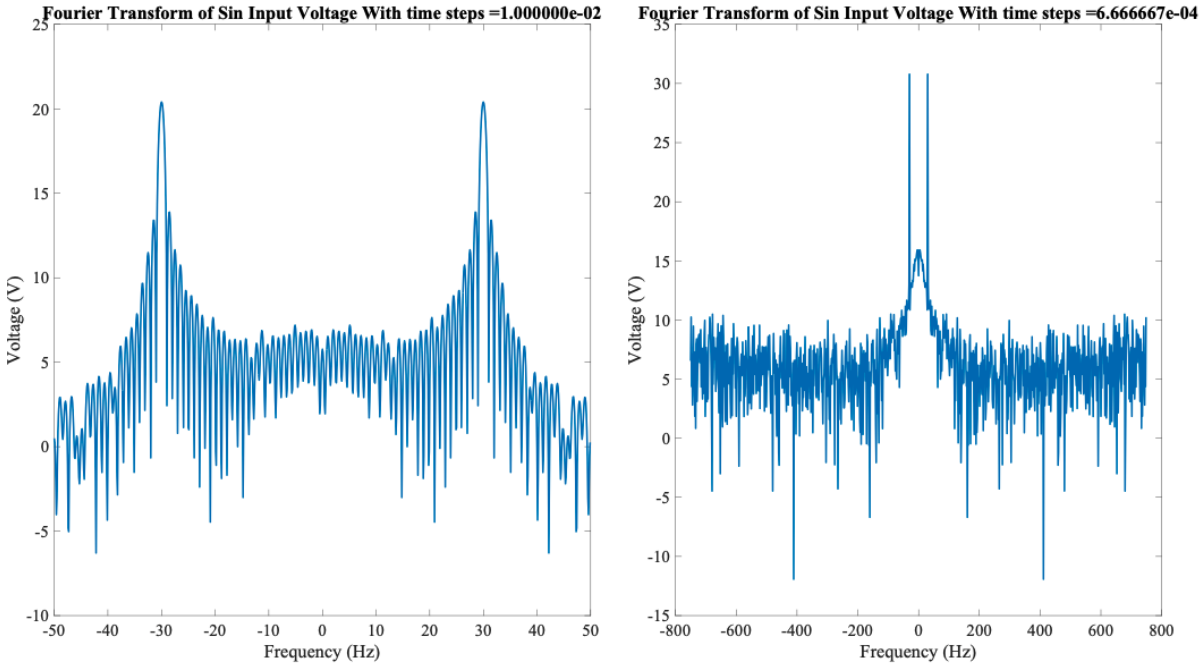

Figure 23. The Fourier transform plot of Vout from the sin input voltage with different time steps.

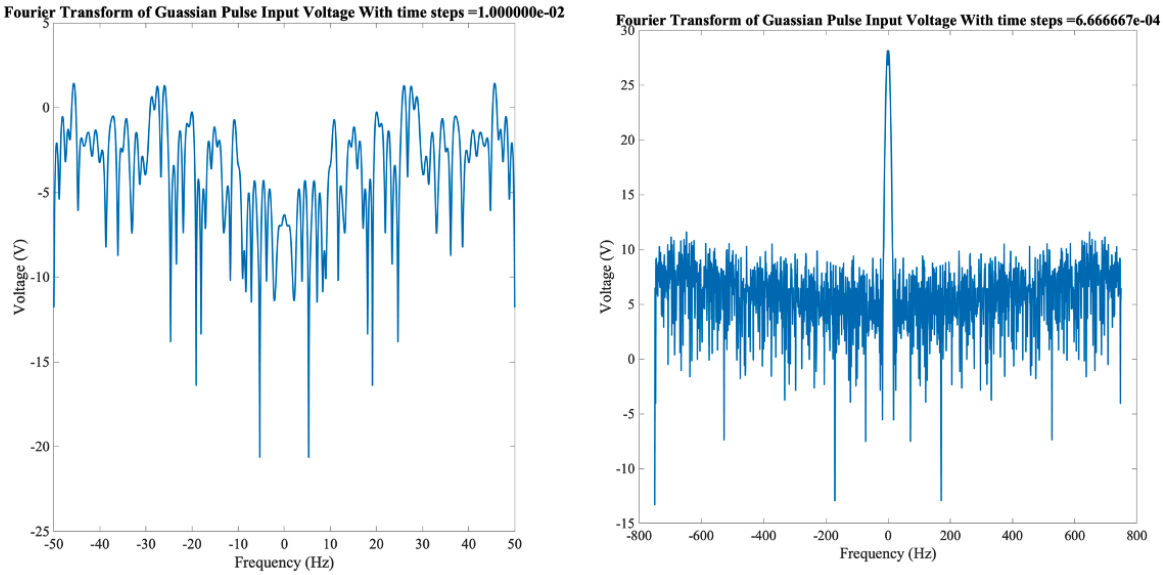

Figure 24.The Fourier transform plot of Vout from the Gaussian pulse input voltage with different time steps.

If the time step is too small, the resistance of capacitor is very big. That means the amount of voltage passthrough (output voltage) is more likely going to the capacitor than the circuit. Therefore, the time steps are very important because it decides whether the circuit would function properly.

5. **Non-linearity**
   a. If the voltage source on the output state is no longer linear and as the function of $V = \alpha I_3 + \beta I_3^2 + \gamma I_3^3$, the new vector presenting non-linear part of V is added to demonstrate the non-linear part, called B.
   b.
   - Thus, the new equation becomes:

$$\boldsymbol{C}\frac{d\boldsymbol{V}}{dt} + \boldsymbol{GV} + \boldsymbol{BV} = \boldsymbol{F}$$

   Where B is the new vector represents for non-linearity of the V matrix.
   - The implementation should be like the linear part, just add another matrix in, isolate V and solve for it with matrix B.
   - Using finite difference method results in:

$$\boldsymbol{C}\frac{\boldsymbol{V_i} - \boldsymbol{V_{i-1}}}{dt} + \boldsymbol{GV_i} + \boldsymbol{BV_i} = \boldsymbol{F}$$

$$V_i\left(\frac{C}{dt} + G + B\right) - C\frac{V_{i-1}}{dt} = F$$

   - Replace $\frac{C}{dt} + G + B$ with H, gives:

$$V_i H - C\frac{V_{i-1}}{dt} = F$$

   - Therefore, V_i is:

$$V_i = \frac{F + C\frac{V_{i-1}}{dt}}{H}$$