Instruction Set

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1 Micro-instructions

- `0x0000` - do nothing
- `0x0001` - begin instruction (and increment `pk`)
- `0xNK02` - output `srN` to data bus for K clock cycles
- `0xNK03` - output `srN` to addr bus for K clock cycles
- `0xNK04` - output *`srN` to data bus for K clock cycles
- `0xNK05` - output *(`srN`+`offs`) to data bus for K clock cycles
- `0xN006` - write to `srN` from data bus
- `0xN_1M` - Special register N special function M
- `0x0010` - increment `pk`
- `0x0K11` - output *`srK` to data bus for K cycles and increment `pk`
- `0x0012` - write to `pk` from `tmpA`
- `0x0013` - write to `pk` from `tmpB`
- `0x0014` - write to `pk` from `tmpA` if data bus is zero; increment otherwise
- `0x0015` - write to `pk` from `tmpA` if data bus is nonzero; increment otherwise
- `0x0016` - write to `pk` from `tmpA` if data bus is negative; increment otherwise
- `0x0017` - write to `pk` from `tmpA` if data bus is non-negative; increment otherwise
- `0x0018` - write to `pk` from `tmpA` if data bus is positive; increment otherwise
- `0x0019` - write to `pk` from `tmpA` if data bus is non-positive; increment otherwise
- `0x1010` - increment `sp`
- `0x1011` - decrement `sp`
- `0x2K10` - output `tmpA` to `pk` via secret line for K clock cycles
- `0x2K10` - output `tmpB` to `pk` via secret line for K clock cycles
- `0xNK20` - output `rN` to data bus for K clock cycles
- `0xNK21` - output `rN` to addr bus for K clock cycles
- `0xNK22` - output *`rN` to data bus for K clock cycles
- `0xNK23` - output *(`rN`+`offs`) to data bus for K clock cycles
- `0xN024` - write to `rN` from data bus
- `0x0025` - write data bus to *(addr bus)
- `0x0026` - write data bus to *(addr bus+`offs`)

- `0x0K27` - output *(addr bus) RAM to data bus for K clock cycles
- `0x0K28` - output *(addr bus+`offs`) RAM to data bus for K clock cycles
- `0xNM4A` - output ALU operation A on (`rN`, `rM`) to data bus for K clock cycles
- `0xN030` - set I/O pin `N` to input mode
- `0xN031` - set I/O pin `N` to output mode
- `0xN032` - set I/O pin `N` to low
- `0xN033` - set I/O pin `N` to high
- `0xNK34` - output I/O pin `N` to data bus for K clock cycles
- `0xN035` - write data bus to I/O pin `N`
- `0x0K50` - prevent data bus from updating for K clock cycles
- `0x0K51` - prevent addr bus from updating for K clock cycles
- `0xfffe` - end instruction
- `0xffff` - reset everything