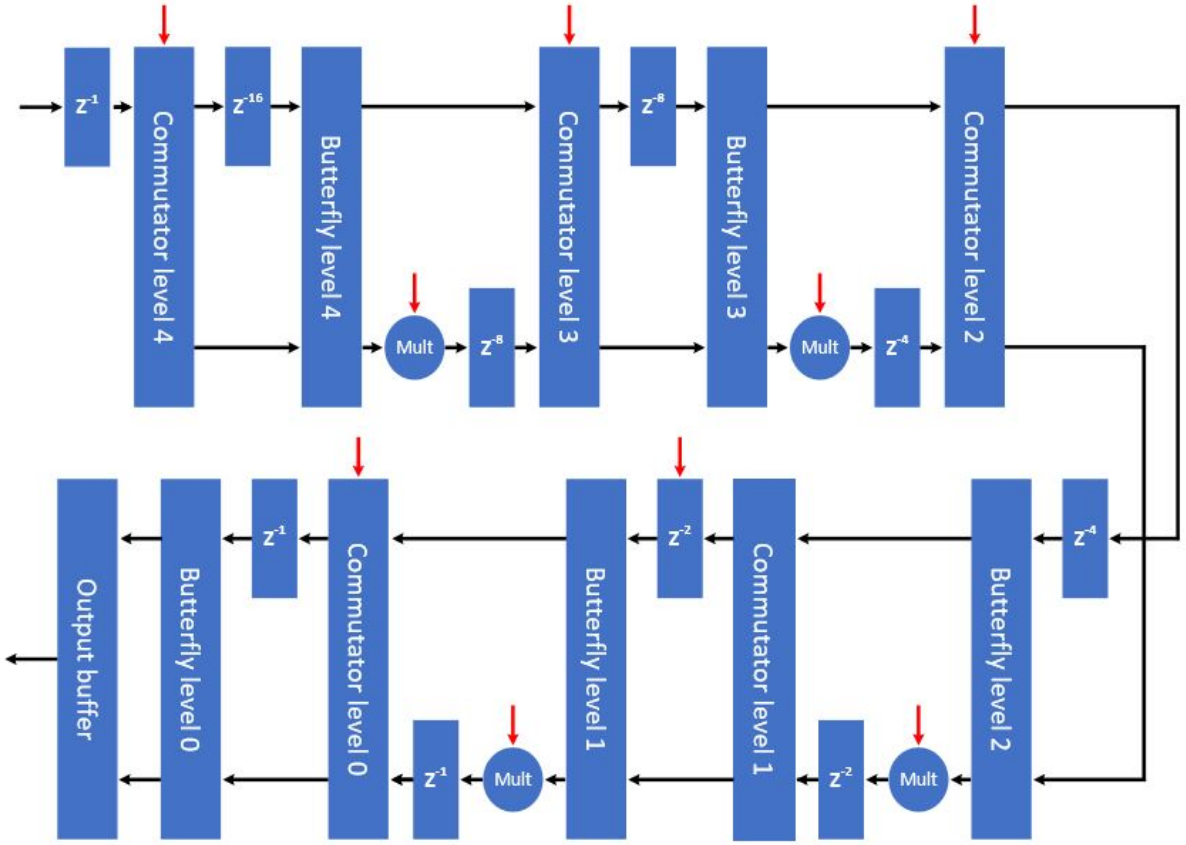
CommIC HW2 report

Block diagrams



- All butterfly are radix-2
- Red lines are control signals

Design strategy

- We apply the shift and add scheme for maximum 8 bits for all multipliers. For instance, rotating -11.25 degrees, be multiply the approximate rotating matrix below by shifting one by 1, 2, 3, 4, 5 and the other 2, 3, then adding it all up.
  \begin{bmatrix} 0.11111 & 0.011 \\ -0.011 & 0.11111 \end{bmatrix}
- Also, we apply CSDC representation to simplify the hardware resources. For instance, the constant multiply \(0.11111\) can be replaced by \(1.0000\bar{1}\).
- We apply the retiming techniques provide by DC compiler to reduce critical path, thus reducing dynamic power (about 8%).

Performance

- Simulation SNR: 40.52, 41.01, 41.27, 41.15, 41.25 dB for 5 testcases
- Latency: 10 (ns/cycle) * 40 (cycles, the time for the first output data)
- Total power: 6.384e-03
- Total Cell area: 149274.448003