MSOC

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Insights and Improvements of Lab1 & Lab2

Presenter: Ting-Yung Chen, Yu-Cheng Lin, I-Hsuan Liu

Team#: 1

Outline

- C synthesis
  - Synthesis Report
  - Pipeline

- Optimization in Vivado
  - Place_design and Route_design
  - Optimization

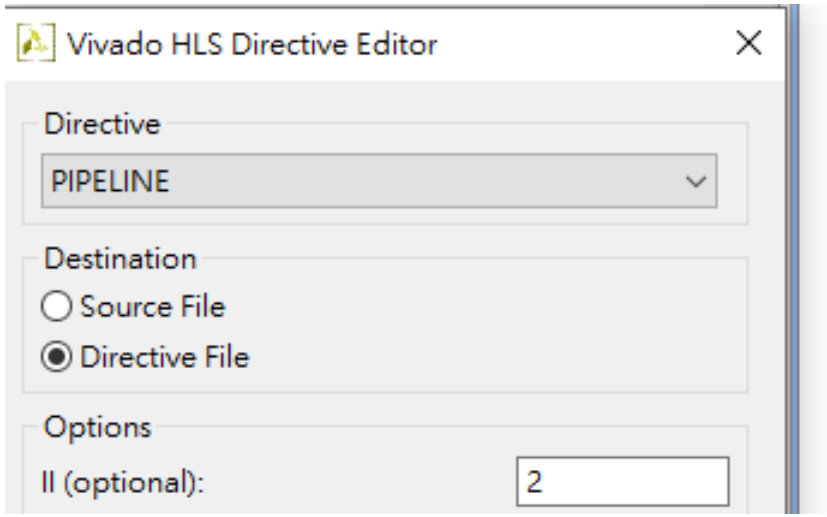
Synthesis Report

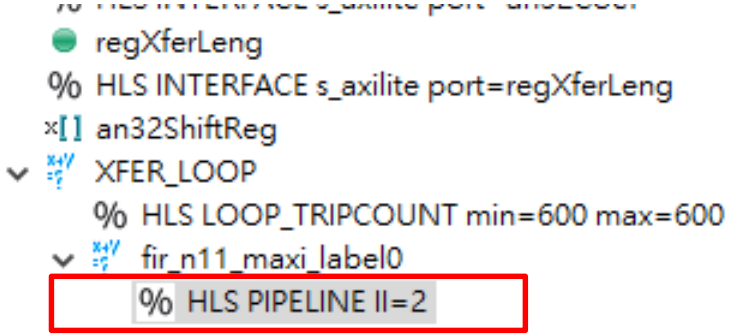
- C synthesis of fir_n11_maxi module
  - Long latency in the inner loop

Loop

	Latency (cycles)			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- XFER_LOOP	?	?	101 ~ 112	-	-	?	no
+ SHIFT_ACC_LOOP	99	110	9 ~ 10	-	-	11	no

- Pipeline can be added to the current design

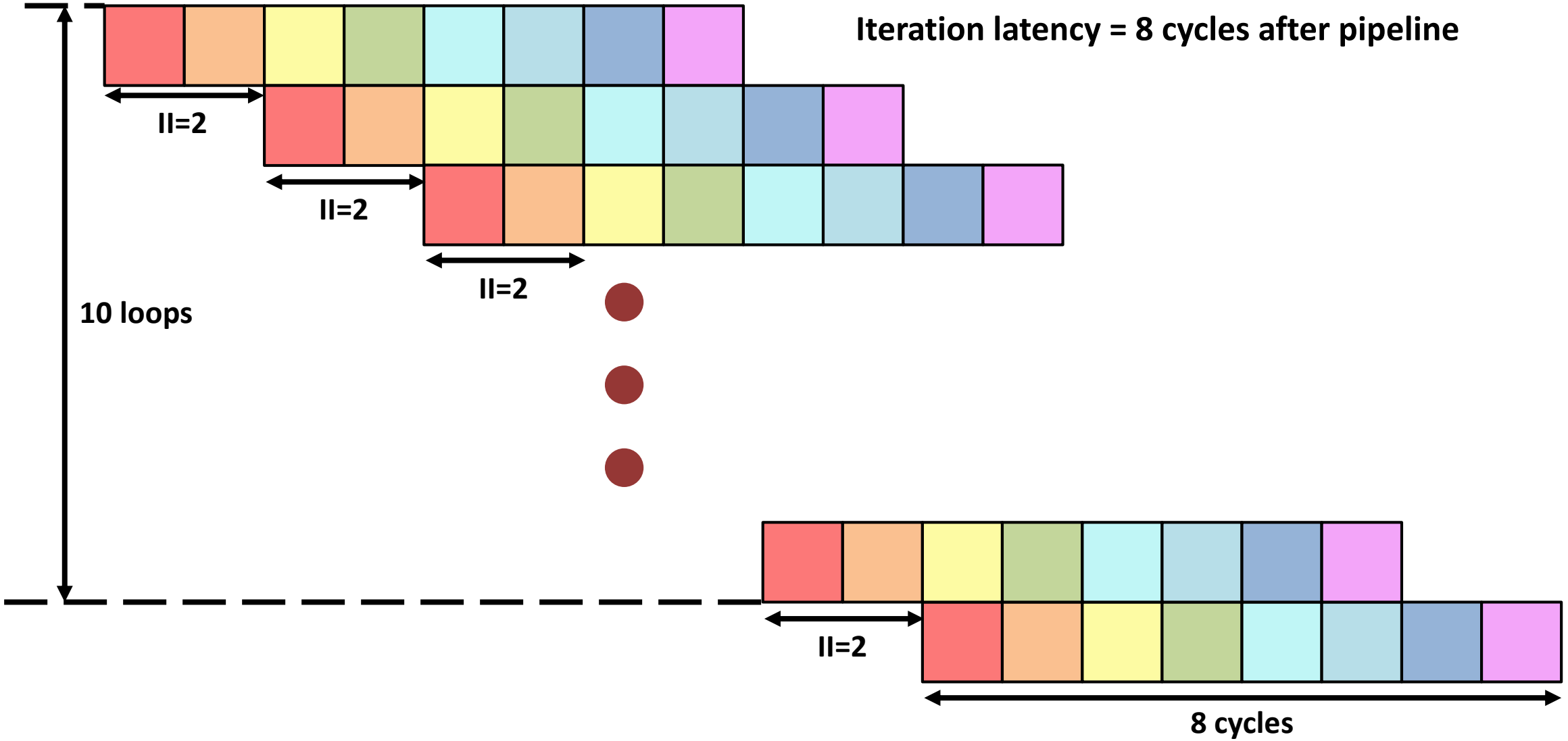




Initiation interval (II) = 2

Pipeline Details

- SHIFT_ACC_LOOP Pipelining



Pipeline Details

- Latency (cycles) formula = II*(N-1) + Iteration Latency - 1

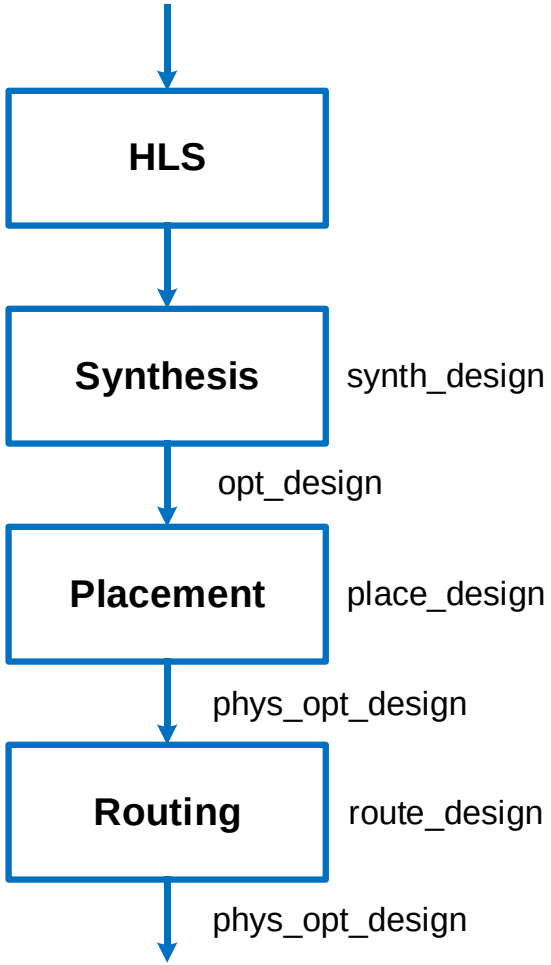
- Reason: The latency is one cycle less than the initiation interval (the next input is read when the final output is written).

- A shorter latency can be obtained

Loop

	Latency (cycles)			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- XFER_LOOP	?	?	30	-	-	?	no
+ SHIFT_ACC_LOOP	27	27	8	2	2	11	yes

Optimization commands in Vivado



- Syth_design: perform synthesize
- Opt_design: perform logic & memory optimization
- Place_design: perform placing
- Route_design: perform routing
- Phys_opt_design: physical design optimization (post placed or post route)

Place_design command

```
place_design [-directive <arg>] [-no_timing_driven] [-timing_summary]
 [-unplace] [-post_place_opt] [-no_fanout_opt] [-no_bufg_opt] [-quiet] [-verbose]
```

- Directive: Apply different algorithms to optimize placement
  - Explore
  - EarlyBlockPlacement
- Unplace: Set all cell unlocked except TRUE IS_LOC_FIXED
- Post_place_opt: Improve critical path timing after initial placement (will resulted in unroute connections, need re-route design)

Route_design command

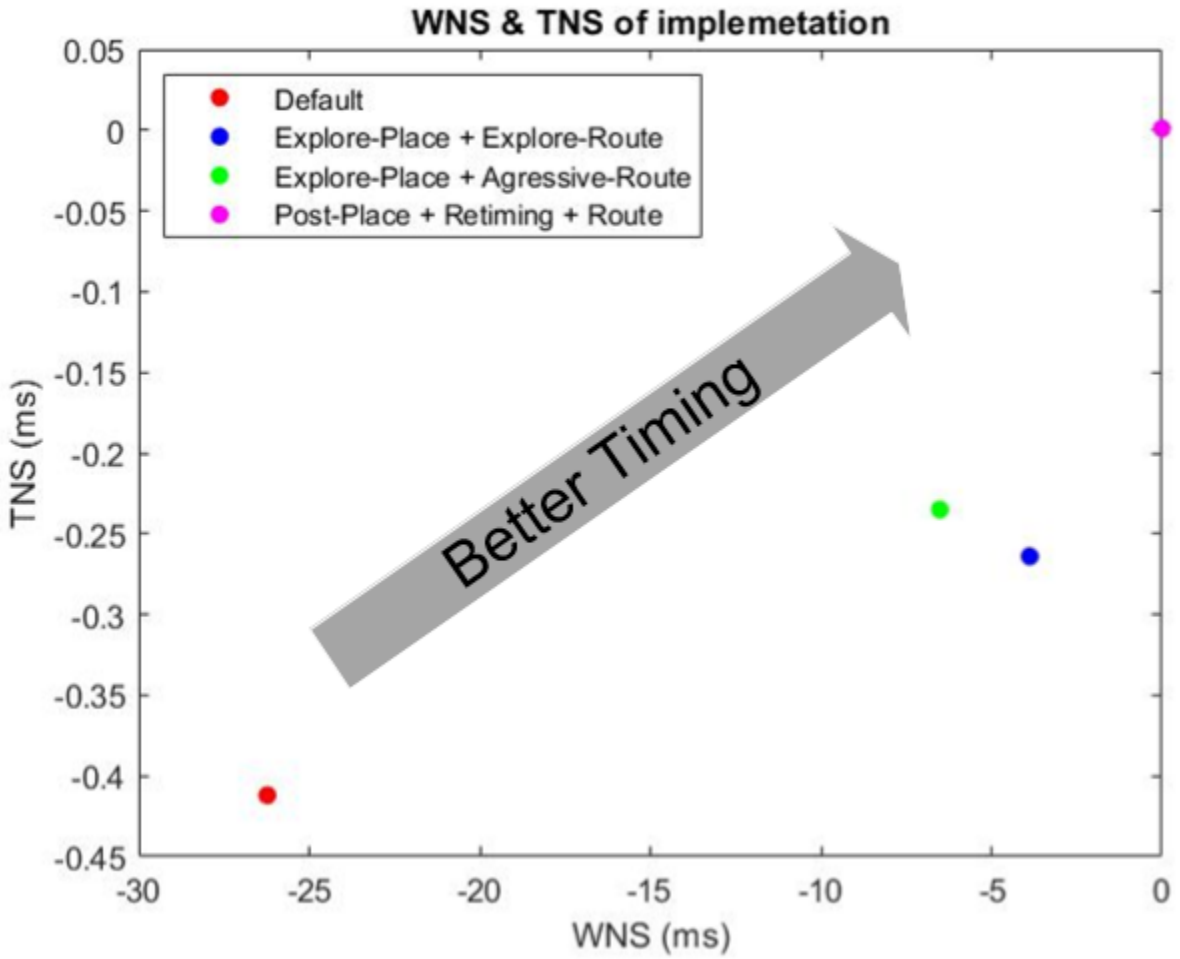
route_design [-unroute] [-release_memory] [-nets <args>] [-physical_nets]
[-pins <arg>] [-directive <arg>] [-tns_cleanup] [-no_timing_driven] [-preserve]
[-delay] [-auto_delay] -max_delay <arg> -min_delay <arg> [-timing_summary]
[-finalize] [-ultrathreads] [-quiet] [-verbose]

- Unroute: unroute all nets or specific nets
- Directive: Apply different algorithms to optimize routing
  - Explore
  - AggresiveExplore
  - RuntimeOptimized
- Nets/Pins: specify specific net or pins
- An example:

```
route_design -delay -nets $criticalNets
set_property IS_ROUTE_FIXED 1 $criticalNets
route_design -directive RuntimeOptimized
```

Optimization

- Set clock frequency to 200M gets negative worst negative slack (WNS) & total negative slack (TNS) under default optimization in Lab2-1
- Timing violation can be fixed by applying optimization command
- The optimized design can function correctly for python code simulation



Results

Messages for running retiming command

```
INFO: [Physopt 32-952] Improved path group WNS = -0.075. Path group: clk_fpga_0. Processed net: design_1_i/fir_n11_maxi_0/inst/fir_n11_maxi_gmem_m_axi_U/bus_write/could_multi_bursts.sect_handling_reg_n_0.
INFO: [Physopt 32-703] Processed net design_1_i/axi_mem_intercon/s00_couplers/auto_pc/inst/gen_axi4_axi3.axi3_conv_inst/USE_WRITE.write_data_inst/first_mi_word. Clock skew was adjusted for instance design_1_i/axi_mem_
INFO: [Physopt 32-952] Improved path group WNS = -0.060. Path group: clk_fpga_0. Processed net: design_1_i/axi_mem_intercon/s00_couplers/auto_pc/inst/gen_axi4_axi3.axi3_conv_inst/USE_WRITE.write_data_inst/first_mi_wo
INFO: [Physopt 32-953] Path group WNS did not improve. Path group: clk_fpga_0. Processed net: design_1_i/axi_mem_intercon/s00_couplers/auto_pc/inst/gen_axi4_axi3.axi3_conv_inst/USE_READ.USE_SPLIT_R.read_addr_inst/USE_
INFO: [Physopt 32-703] Processed net design_1_i/axi_mem_intercon/s00_couplers/auto_us/inst/gen_upsizer.gen_full_upsizer.axi_upsizer_inst/USE_READ.gen_non_fifo_r_upsizer.read_data_inst/first_word. Clock skew was adjust
INFO: [Physopt 32-952] Improved path group WNS = -0.029. Path group: clk_fpga_0. Processed net: design_1_i/axi_mem_intercon/s00_couplers/auto_us/inst/gen_upsizer.gen_full_upsizer.axi_upsizer_inst/USE_READ.gen_non_fif
INFO: [Physopt 32-953] Path group WNS did not improve. Path group: clk_fpga_0. Processed net: design_1_i/ps7_0_axi_periph/s00_couplers/auto_pc/inst/gen_axilite.gen_b2s_conv.axilite_b2s/WR.aw_channel_0/cmd_translator_0
INFO: [Physopt 32-703] Processed net design_1_i/ps7_0_axi_periph/s00_couplers/auto_pc/inst/gen_axilite.gen_b2s_conv.axilite_b2s/SI_REG/aw.aw_pipe/m_payload_i_reg[61]_0[38]. Clock skew was adjusted for instance design_
INFO: [Physopt 32-952] Improved path group WNS = -0.016. Path group: clk_fpga_0. Processed net: design_1_i/ps7_0_axi_periph/s00_couplers/auto_pc/inst/gen_axilite.gen_b2s_conv.axilite_b2s/SI_REG/aw.aw_pipe/m_payload_i_
INFO: [Physopt 32-663] Processed net design_1_i/fir_n11_maxi_0/inst/fir_n11_maxi_gmem_m_axi_U/wreq_throttl/Q[1]. Re-placed instance design_1_i/fir_n11_maxi_0/inst/fir_n11_maxi_gmem_m_axi_U/wreq_throttl/throttl_cnt_re
INFO: [Physopt 32-952] Improved path group WNS = -0.011. Path group: clk_fpga_0. Processed net: design_1_i/fir_n11_maxi_0/inst/fir_n11_maxi_gmem_m_axi_U/wreq_throttl/Q[1].
INFO: [Physopt 32-953] Path group WNS did not improve. Path group: clk_fpga_0. Processed net: design_1_i/fir_n11_maxi_0/inst/fir_n11_maxi_gmem_m_axi_U/bus_write/fifo_wreq/q_reg[60]_0[54].
INFO: [Physopt 32-953] Path group WNS did not improve. Path group: clk_fpga_0. Processed net: design_1_i/fir_n11_maxi_0/inst/fir_n11_maxi_gmem_m_axi_U/bus_write/fifo_wreq/E[0]_repN_1.
INFO: [Physopt 32-953] Path group WNS did not improve. Path group: clk_fpga_0. Processed net: design_1_i/fir_n11_maxi_0/inst/fir_n11_maxi_gmem_m_axi_U/bus_write/fifo_wreq/align_len[31]_i_4_n_0.
INFO: [Physopt 32-710] Processed net design_1_i/fir_n11_maxi_0/inst/fir_n11_maxi_gmem_m_axi_U/bus_write/fifo_wreq/align_len[31]_i_4_n_0. Critical path length was reduced through logic transformation on cell design_1_
INFO: [Physopt 32-735] Processed net design_1_i/fir_n11_maxi_0/inst/fir_n11_maxi_gmem_m_axi_U/bus_write/fifo_wreq/align_len[31]_i_8_n_0. Optimization improves timing on the net.
```

Timing report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.012 ns	Worst Hold Slack (WHS):	0.018 ns	Worst Pulse Width Slack (WPWS):	1.116 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8388	Total Number of Endpoints:	8388	Total Number of Endpoints:	3269

All user specified timing constraints are met.