Course Information	
Course title	Computer-aided Vlsi System Design
Semester	108-1
Designated for	COLLEGE OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE GRADUATE INSTITUTE OF ELECTRONICS ENGINEERING
Instructor	CHIA-HSIANG YANG
Curriculum Number	EEE5022
Curriculum Identity Number	943 U0240
Credits	3.0

Course Syllabus	
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Course Description	Computer-Aided VLSI System Design
Course Objective	Verilog, Synthesis, DFT/ATPG, Static Timing Analysis, Placement and Routing, DRC/LVS/LPE, Verification
Course Requirement	9 Labs, 7 Homework Assignments, 1 Midterm, 1 Group Final Project

Progress

Week	Date	Topic
第 1 週	2019/09/12	Introduction
第 2 週	2019/09/19	Verilog - I
第 3 週	2019/09/26	Verilog - II
第 4 週	2019/10/03	Verilog - III
第 5 週	2019/10/10	國慶日放假
第 6 週	2019/10/17	Verilog - IV
第 7 週	2019/10/24	Synthesis - I
第 8 週	2019/10/31	Synthesis - II
第 9 週	2019/11/07	期中考放假

第 10 週	2019/11/14	Static Timing Analysis
第 11 週	2019/11/21	Midterm
第 12 週	2019/11/28	Verification [Final Project] team up
第 13 週	2019/12/05	Cadence Formal Verification (JasperGold) [Final Project] announce
第 14 週	2019/12/12	Placement
第 15 週	2019/12/19	Routing
第 16 週	2019/12/26	DRC/LVS
第 17 週	2020/01/02	Testing
第 18 週	2020/01/09	Cadence Formal High Level Synthesis
第 19 週	2020/01/16	Project Presentation