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| |  | | --- | | **Course Information** |  |  |  | | --- | --- | | Course title | Computer-aided Vlsi System Design | | Semester | 108-1 | | Designated for | COLLEGE OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE  GRADUATE INSTITUTE OF ELECTRONICS ENGINEERING | | Instructor | [CHIA-HSIANG YANG](https://nol2.aca.ntu.edu.tw/nol/coursesearch/teacher.php?op=s2&td=901126) | | Curriculum Number | EEE5022 | | Curriculum Identity Number | 943 U0240 | | Credits | 3.0 | | **Course Syllabus** | | | **Please respect the intellectual property rights of others and do not copy any of the course information without permission** | | | Course Description | Computer-Aided VLSI System Design | | Course Objective | Verilog, Synthesis, DFT/ATPG, Static Timing Analysis, Placement and Routing, DRC/LVS/LPE, Verification | | Course Requirement | 9 Labs, 7 Homework Assignments, 1 Midterm, 1 Group Final Project |  |  | | --- | | **Progress** |  |  |  |  | | --- | --- | --- | | Week | Date | Topic | | 第1週 | 2019/09/12 | Introduction | | 第2週 | 2019/09/19 | Verilog - I | | 第3週 | 2019/09/26 | Verilog - II | | 第4週 | 2019/10/03 | Verilog - III | | 第5週 | 2019/10/10 | 國慶日放假 | | 第6週 | 2019/10/17 | Verilog - IV | | 第7週 | 2019/10/24 | Synthesis - I | | 第8週 | 2019/10/31 | Synthesis - II | | 第9週 | 2019/11/07 | 期中考放假 | | 第10週 | 2019/11/14 | Static Timing Analysis | | 第11週 | 2019/11/21 | Midterm | | 第12週 | 2019/11/28 | Verification [Final Project] team up | | 第13週 | 2019/12/05 | Cadence Formal Verification (JasperGold) [Final Project] announce | | 第14週 | 2019/12/12 | Placement | | 第15週 | 2019/12/19 | Routing | | 第16週 | 2019/12/26 | DRC/LVS | | 第17週 | 2020/01/02 | Testing | | 第18週 | 2020/01/09 | Cadence Formal High Level Synthesis | | 第19週 | 2020/01/16 | Project Presentation | |

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