

UBC Department of Electrical and Computer Engineering

CPEN 211: Introduction to Microcomputers (2025W)

Course Syllabus

Calendar Description: Boolean algebra; combinational and sequential circuits; organization and operation of microcomputers, memory addressing modes, representation of information, instruction sets, machine and assembly language programming, systems programs, I/O structures, I/O interfacing and I/O programming, introduction to digital system design using microcomputers. Credit will be granted for only one of CPEN 211, CPEN 312, EECE 256, EECE 259 or EECE 355. Prerequisites: APSC 160.

Contact Information

Prof. Guy Lemieux lemieux+cpen211@ece.ubc.ca

TAs: see Canvas

Course Structure

Lectures:	2 hours	every Tues., Thur. 1530-1730 (in person ESB 1013), beginning Sept 2
Tutorial:	2 hours	alternate weeks, Fri. 1600-1800 (in person ESB 1013), beginning Sept 5
Labs:	2 hours	one of Wed 1300, 1500, Thu 1100, Thu 1300, Fri 1400, beginning Sept 3
Lab Tests	3 hours	Fri 1600-1900 (in person ESB 1013), Oct 17 and Nov 28
Midterm Exam	2 hours	Fri 1600-1800 (in person ESB 1013), Nov 14
Office hours:	TBD	see Canvas.

Required Materials (see Canvas for details)

Terasic DE10-Lite FPGA Development Kit: <http://ubc-de10-lite.terasic.com/>

Second Year Tools and Parts Kit: <https://www.rpelectronics.com/en/product/589743/cpen-elec-2025-ece-ubc-second-year-tools-and/>

Textbook: *Digital Design and Computer Architecture: RISC-V Edition*, Sarah L. Harris and David Harris, Elsevier/Morgan Kaufmann, 2022. <https://pages.hmc.edu/harris/ddca/ddcarv.html>

Learning Objectives: By the end of CPEN 211 you will be able explain how a computer works from the bottom up; from the operation of individual transistors up to the C programming language. You will be able to explain how software is represented in 1's and 0's at the machine level and to write programs in ARM assembly corresponding to C programs. You will be able to design and optimize digital logic circuits both manually using the principles of Boolean algebra and automatically with the assistance of modern computer aided design (CAD) tools using the Verilog Hardware Description Language (HDL). You will be able to describe rules for using Verilog to ensure it can be synthesized into hardware that behaves correctly. You will be able to construct larger circuits by combining smaller circuits. You will be able to identify design errors in Verilog using testbenches and simulation. You will be able to describe the von Neumann computing model and design a simple computer implementing this model in Verilog.

Assessment: Your mark is based upon multiple components. The weight of each component is:

Problem Sets:	0% (not collected / not marked)
Labs (TA Marked):	20% (12 labs, marked by demonstrating to a TA)
Lab Proficiency Tests:	10% (5% + 5%, laptop and DE10-Lite required; must-pass to pass the course)
Midterm Exam:	20% (laptop and DE10-Lite may be required)
Final Exam:	50% (laptop and DE10-Lite may be required; must-pass to pass the course)

Webpages: CPEN 211 makes use of Canvas, Piazza, and GitHub Classroom.

Slides/Notes: The lectures slides posted on Canvas are not a complete record of the course. You should take notes while attending lectures. Updates to slides may be posted after lectures.

Problem Sets: Problem sets are mostly taken from the textbook which has solutions to all ODD-numbered problems. Although these are not marked, there will be related questions on the midterm, LPTs and final exam.

Lab Assignments: Expect to spend 6+ hours per week on labs. CPEN 211 emphasizes practical engineering skills through weekly labs. Labs will be marked in-person by a TA, but you will submit your solutions on Canvas and/or GitHub Classroom. Many labs will be done with a partner, forming a group. To give you a chance to LEARN from OTHER STUDENTS, each student/group will evaluate 3-5 other students/groups as part of a Peer Review process – please be kind and leave some encouraging comments and tips for each other!

The first lab is the week of September 2. You will need an ECE account:

https://help.ece.ubc.ca/How_To_Get_An_Account.

You will also need to install and setup VPN access to UBC:

<https://it.ubc.ca/services/email-voice-internet/myvpn/setup-documents>

https://ubc.service-now.com/selfservice?id=kb_article&sysparm_article=KB0016157

Course Policies

Lab Grades: Due to limited number of TA hours you are permitted to attend **ONLY** the lab marking session to which you are assigned. Your lab grades will be entered directly into Canvas by your TA as you are marked. Please confirm the grade is recorded correctly before leaving the lab, as there will be no chance to change it after.

Requests for Academic Concessions (In-term): Due to the size of the class, a late lab gets a grade of 0, **no exceptions!** To request concession for a **missed** lab, LPT or midterm, e.g. due to illness, submit a request using:

<https://academicservices.engineering.ubc.ca/exams-grades/academic-concession/>

In almost all cases, a missing grade will be ESTIMATED based on your standing in the Final Exam.

Lab illnesses will be considered as pre-approved. You may ask a TA to pre-approve a **Planned** delayed lab grading to attend an important event where you have no control over the schedule (e.g., funeral, presenting a research paper at a conference, or competing at an official sports event). In this case, you (together with your partner) must complete the lab at the earliest opportunity (including a different lab section). Note that most **Unplanned** reasons for a delayed lab grading **will not be approved**, including: late bus, sick family member sick, personal employment schedule, computer troubles, other homework/workload, partner did not the work, etc.

Academic Integrity: Use of code written by anyone but your lab partner (as indicated in Canvas) is forbidden. Code from **textbooks** can be used if the source is cited. Code from **all other sources**, including the web, **AI-generated or compiler-generated code** (except where asked), and any previous CPEN211 instances (including your own code!) is strictly forbidden.

Lab Partners: Some labs require a partner which you must indicate in Canvas. Once you pick your partner, you cannot change partners! You are expected to use a “paired programming” approach. Your partner must be registered in the same lab section as you. Pair programming means both partners meet and work on the lab together and both partners are active participants in the development process of the entire lab solution. Specifically, each partner must contribute at least one third to every lab. It may be considered “unauthorized collaboration” if you write less than one third of the code submitted for any lab and do not acknowledge this fact. Select a lab partner that wishes to invest the same amount of time per week for labs in CPEN 211 as you do and who has a schedule that enables you to meet to work together of scheduled lab sessions.

In case of any concerns around academic integrity with your partner, document as much as you can and present it to the instructor.

Midterm and Final Exam: Both midterm and exam are expected to take place in person. You must pass the final exam to pass the course.

Regrade requests:

- **Regrade requests** for the midterm must be submitted on Piazza within 7 days after midterms are returned.
- **Final Exam viewing requests** must follow the UBC process and deadlines:

<https://vancouver.calendar.ubc.ca/campus-wide-policies-and-regulations/academic-assessment/viewing-marked-work>

Note that viewing requests are “purely pedagogic **and distinct from the Review of Assigned Standing.**”

- **Review of Assigned Standing requests** (if you think your grade is incorrect) must also follow UBC policy:

<https://vancouver.calendar.ubc.ca/campus-wide-policies-and-regulations/review-assigned-standing>