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1 Basic Test Results

```
1 ***** TESTING FOLDER STRUCTURE START *****
2 Checking your submission for presence of invalid (non-ASCII) characters...
3 No invalid characters found.
4 Submission logins are: linorcohen
5 Is this OK?
6 ***** TESTING FOLDER STRUCTURE END *****
7
8 ***** PROJECT TEST START *****
9 Testing.
10 Add16 passed test.
11 FullAdder passed test.
12 HalfAdder passed test.
13 Inc16 passed test.
14 ***** PROJECT TEST END *****
15
16 Note: the tests you see above are all the presubmission tests
17 for this project. The tests might not check all the different
18 parts of the project or all corner cases, so write your own
19 tests and use them!
```

2 ALU.hdl

```
1 // This file is part of nand2tetris, as taught in The Hebrew University, and
2 // was written by Aviv Yaish. It is an extension to the specifications given
3 // [here](https://www.nand2tetris.org) (Shimon Schocken and Noam Nisan, 2017),
4 // as allowed by the Creative Common Attribution-NonCommercial-ShareAlike 3.0
5 // Unported [License](https://creativecommons.org/licenses/by-nc-sa/3.0/).
6 // File name: projects/02/ALU.hdl
7
8 /**
9  * The ALU (Arithmetic Logic Unit).
10  * Computes one of the following functions:
11  * x+y, x-y, y-x, 0, 1, -1, x, y, -x, -y, !x, !y,
12  * x+1, y+1, x-1, y-1, x&y, x|y on two 16-bit inputs,
13  * according to 6 input bits denoted zx,nx,zy,ny,f,no.
14  * In addition, the ALU computes two 1-bit outputs:
15  * if the ALU output == 0, zr is set to 1; otherwise zr is set to 0;
16  * if the ALU output < 0, ng is set to 1; otherwise ng is set to 0.
17  */
18
19 // Implementation: the ALU logic manipulates the x and y inputs
20 // and operates on the resulting values, as follows:
21 // if (zx == 1) set x = 0 // 16-bit constant
22 // if (nx == 1) set x = !x // bitwise not
23 // if (zy == 1) set y = 0 // 16-bit constant
24 // if (ny == 1) set y = !y // bitwise not
25 // if (f == 1) set out = x + y // integer 2's complement addition
26 // if (f == 0) set out = x & y // bitwise and
27 // if (no == 1) set out = !out // bitwise not
28 // if (out == 0) set zr = 1
29 // if (out < 0) set ng = 1
30
31 CHIP ALU {
32     IN
33     x[16], y[16], // 16-bit inputs
34     zx, // zero the x input?
35     nx, // negate the x input?
36     zy, // zero the y input?
37     ny, // negate the y input?
38     f, // compute out = x + y (if 1) or x & y (if 0)
39     no; // negate the out output?
40
41     OUT
42     out[16], // 16-bit output
43     zr, // 1 if (out == 0), 0 otherwise
44     ng; // 1 if (out < 0), 0 otherwise
45
46     PARTS:
47     // You're advised to work on the ALU chip in two steps:
48     // - First, without handling status outputs (ALU-nostat)
49     // - Then, adding the missing functionality for the "full" chip (ALU).
50     // You only need to submit the "full" ALU, no need to submit the partial
51     // implementation (ALU-nostat).
52     // Put your code here:
53
54     Mux16(a=y, b=false, sel=zy, out=zyres);
55     Not16(in=zyres, out=yNot);
56     Mux16(a=zyres, b=yNot, sel=ny, out=nyres);
57     And16(a=nyres, b=nxres, out=nyresAndnxres);
58
59     Mux16(a=x, b=false, sel=zx, out=zxres);
```

```

60     Not16(in=zxres, out=xNot);
61     Mux16(a=zxres, b=xNot, sel=nx, out=nxres);
62     Add16(a=nyres, b=nxres, out=nyresAddnxres);
63
64     Mux16(a=nyresAndnxres, b=nyresAddnxres, sel=f, out=fres);
65     Not16(in=fres, out=fresNot);
66     Mux16(a=fres, b=fresNot, sel=no, out[0..7]=subout1, out[8..15]=subout2, out=out);
67
68     Or8Way(in=subout1, out=subout10r);
69     Or8Way(in=subout2, out=subout20r);
70     Or(a=subout10r, b=subout20r, out=sub10rsub2);
71     Not(in=sub10rsub2, out=zr);
72
73     And16(a[0..7]=subout1, a[8..15]=subout2, b=true, out[15]=ng);
74 }

```

3 AUTHORS

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3 Remarks:

4 Add16.hdl

```
1  // This file is part of www.nand2tetris.org
2  // and the book "The Elements of Computing Systems"
3  // by Nisan and Schocken, MIT Press.
4  // File name: projects/02/Adder16.hdl
5
6  /**
7   * Adds two 16-bit values.
8   * The most significant carry bit is ignored.
9   */
10
11 CHIP Add16 {
12     IN a[16], b[16];
13     OUT out[16];
14
15     PARTS:
16         HalfAdder(a=a[0], b=b[0], sum=out[0], carry=carry1);
17         FullAdder(a=a[1], b=b[1], c=carry1, sum=out[1], carry=carry2);
18         FullAdder(a=a[2], b=b[2], c=carry2, sum=out[2], carry=carry3);
19         FullAdder(a=a[3], b=b[3], c=carry3, sum=out[3], carry=carry4);
20         FullAdder(a=a[4], b=b[4], c=carry4, sum=out[4], carry=carry5);
21         FullAdder(a=a[5], b=b[5], c=carry5, sum=out[5], carry=carry6);
22         FullAdder(a=a[6], b=b[6], c=carry6, sum=out[6], carry=carry7);
23         FullAdder(a=a[7], b=b[7], c=carry7, sum=out[7], carry=carry8);
24         FullAdder(a=a[8], b=b[8], c=carry8, sum=out[8], carry=carry9);
25         FullAdder(a=a[9], b=b[9], c=carry9, sum=out[9], carry=carry10);
26         FullAdder(a=a[10], b=b[10], c=carry10, sum=out[10], carry=carry11);
27         FullAdder(a=a[11], b=b[11], c=carry11, sum=out[11], carry=carry12);
28         FullAdder(a=a[12], b=b[12], c=carry12, sum=out[12], carry=carry13);
29         FullAdder(a=a[13], b=b[13], c=carry13, sum=out[13], carry=carry14);
30         FullAdder(a=a[14], b=b[14], c=carry14, sum=out[14], carry=carry15);
31         FullAdder(a=a[15], b=b[15], c=carry15, sum=out[15], carry=carry);
32 }
```

5 FullAdder.hdl

```
1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/02/FullAdder.hdl
5
6 /**
7  * Computes the sum of three bits.
8  */
9
10 CHIP FullAdder {
11     IN a, b, c; // 1-bit inputs
12     OUT sum,    // Right bit of a + b + c
13         carry; // Left bit of a + b + c
14
15     PARTS:
16     HalfAdder(a=a, b=b, sum=sum1, carry=carry1);
17     HalfAdder(a=sum1, b=c, sum=sum, carry=carry2);
18     Or(a=carry1, b=carry2, out=carry);
19 }
```

6 HalfAdder.hdl

```
1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/02/HalfAdder.hdl
5
6 /**
7  * Computes the sum of two bits.
8  */
9
10 CHIP HalfAdder {
11     IN a, b;      // 1-bit inputs
12     OUT sum,      // Right bit of a + b
13         carry;    // Left bit of a + b
14
15     PARTS:
16         Xor(a=a, b=b, out=sum);
17         And(a=a, b=b, out=carry);
18 }
```


7 Inc16.hdl

```
1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/02/Inc16.hdl
5
6 /**
7  * 16-bit incrementer:
8  * out = in + 1 (arithmetic addition)
9  */
10
11 CHIP Inc16 {
12     IN in[16];
13     OUT out[16];
14
15     PARTS:
16         Add16(a=in, b[1..15]=false, b[0]=true, out=out);
17 }
```

8 ShiftLeft.hdl

```
1 // This file is part of nand2tetris, as taught in The Hebrew University, and
2 // was written by Aviv Yaish. It is an extension to the specifications given
3 // [here](https://www.nand2tetris.org) (Shimon Schocken and Noam Nisan, 2017),
4 // as allowed by the Creative Common Attribution-NonCommercial-ShareAlike 3.0
5 // Unported [License](https://creativecommons.org/licenses/by-nc-sa/3.0/).
6
7 /**
8  * 16-bit left shifter.
9  *
10 * The chip's output is a "left-shift" of the input:
11 * - Every input bit is moved one position to the left
12 * - A new "0" bit is inserted as the new right-most bit
13 *
14 * For example:
15 * ShiftLeft(0000000000000001)=0000000000000010 // ShiftLeft(1)=2
16 * ShiftLeft(0100000000000000)=1000000000000000
17 * ShiftLeft(1000000000000000)=0000000000000000
18 *
19 * This operation is (usually) equivalent to multiplying the input by 2.
20 * This definition is also called an arithmetic left-shift, and is useful for
21 * the efficient implementation of various operations which we will see later on
22 * in the course.
23 */
24
25 CHIP ShiftLeft {
26     IN in[16];
27     OUT out[16];
28
29     PARTS:
30         Add16(a=in, b=in, out=out);
31 }
```

9 ShiftRight.hdl

```
1 // This file is part of nand2tetris, as taught in The Hebrew University, and
2 // was written by Aviv Yaish. It is an extension to the specifications given
3 // [here](https://www.nand2tetris.org) (Shimon Schocken and Noam Nisan, 2017),
4 // as allowed by the Creative Common Attribution-NonCommercial-ShareAlike 3.0
5 // Unported [License](https://creativecommons.org/licenses/by-nc-sa/3.0/).
6
7 /**
8  * 16-bit right-shifter.
9  *
10 * The chip's output is a "right-shift" of the input:
11 * - Every input bit is moved one position to the right
12 * - A new bit which is equal to the sign bit is inserted as the left-most bit
13 *
14 * For example:
15 * ShiftRight(0000000000000001)=0000000000000000 // ShiftRight(1)=0
16 * ShiftRight(0100000000000000)=0010000000000000
17 * ShiftRight(1100000000000000)=1110000000000000
18 *
19 * Note that this operation is (usually) equivalent to dividing the input by 2.
20 * This definition is also called an arithmetic right-shift, and is useful for
21 * the efficient implementation of various operations which we will see later on
22 * in the course.
23 * Another variant is the logical right-shift, which always inserts a new '0'
24 * bit.
25 */
26
27 CHIP ShiftRight {
28     IN in[16];
29     OUT out[16];
30
31     PARTS:
32     Or16(a[0..14]=in[1..15], a[15]=in[15], b=false, out=out);
33 }
```