Department of Electronic and Telecommunication Engineering

University of Moratuwa

EN2031 - Fundamentals of Computer Organization and Design

ISA and Microarchitecture Design Stage 1

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Required Instructions

1. Arithmetic and Logic Instructions (ADD, SUB, AND, OR)

2. Stack Operations (PUSH, POP)

    PUSH: push contents in a register to the stack
    POP: pop contents in a register to the stack

3. Memory Operations (LOAD, LOADM, STORE)

    LOAD: Load data from memory.
    LOADM: Load data from memory and post-increment the address.
    STORE: Store register values to the memory.

4. Data Transfer (MOV):

    MOV: Move data from one register to another.

5. Branch Instructions (BRANCH, BEQ, BLE, BGE)

    BRANCH: Unconditionally add immediate value in the instruction to PC.
    BEQ: Branch if the two registers are equal (Using SREG).
    BLE: Branch if less than or equal (Using SREG).
    BGE: Branch if greater than or equal (Using SREG).

    [SREG: Register which stores status of the last operation.]

6. Load operations (LOADL, LOADU)

    LOADL: Load the first 8-bits of the immediate into a register.
    LOADU: Load the last 8-bits of the immediate into a register.

(4-bit opcode is sufficient)

Instruction Formats

1. ALU Instruction Format:

Opcode (4 bits) | Rd (3 bits) | Ra (3 bits) | Rb (3 bits)
[This format allows for ALU instructions to specify three registers: Ra and Rb as source operands, and Rd as the destination register. The 4-bit opcode identifies the operation type.]

2. Control Flow Instruction Format:

Opcode (4 bits) | Ra (3 bits) | Rb (3 bits) | IMM8 (4 bits)
[Control flow instructions primarily involve immediate values for branch offsets. Using an 8-bit immediate value provides sufficient range for branching within the program. The 4-bit opcode specifies the type of branch operation.]

3. Load and Store Instruction Format:

Opcode (4 bits) | Rd (3 bits) | Ra (3 bits)
[This format is used for both loading and storing data. The opcode indicates the operation type. Rd represents the destination or source register, and Ra represents the base address register. Since the processor can handle 16-bit words, no additional bits are needed for offset.]

4. Register Move Instruction Format:

Opcode (4 bits) | Rd (3 bits) | Ra (3 bits)
[Register moves instructions involve transferring data between registers. The same format as Load and Store instructions is used here, simplifying the overall design. The opcode specifies the operation type, and Rd and Ra represent the destination and source registers, respectively.]