Arm® Mali-IV009 Register Map

Version R0P0-00REL0 / Revision r0p0

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Confidential Proprietary Notice

This document is CONFIDENTIAL and any use by you is subject to the terms of the agreement between you and Arm or the terms of the agreement between you and the party authorised by Arm to disclose this document to you.

This document is protected by copyright and other related rights and the practice or implementation of the information contained in this document may be protected by one or more patents or pending patent applications. No part of this document may be reproduced in any form by any means without the express prior written permission of Arm. No license, express or implied, by estoppel or otherwise to any intellectual property rights is granted by this document unless specifically stated.

Your access to the information in this document is conditional upon your acceptance that you will not use or permit others to use the information: (i) for the purposes of determining whether implementations infringe any third party patents; (ii) for developing technology or products which avoid any of Arm's intellectual property; or (iii) as a reference for modifying existing patents or patent applications or creating any continuation, continuation in part, or extension of existing patents or patent applications; or (iv) for generating data for publication or disclosure to third parties, which compares the performance or functionality of the Arm technology described in this document with any other products created by you or a third party, without obtaining Arm's prior written consent.

THIS DOCUMENT IS PROVIDED "AS IS". ARM PROVIDES NO REPRESENTATIONS AND NO WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, SATISFACTORY QUALITY, NON-INFRINGEMENT OR FITNESS FOR A PARTICULAR PURPOSE WITH RESPECT TO THE DOCUMENT. For the avoidance of doubt, Arm makes no representation with respect to, and has undertaken no analysis to identify or understand the scope and content of, third party patents, copyrights, trade secrets, or other rights.

This document may include technical inaccuracies or typographical errors.

TO THE EXTENT NOT PROHIBITED BY LAW, IN NO EVENT WILL ARM BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT, EVEN IF ARM HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

This document consists solely of commercial items. You shall be responsible for ensuring that any use, duplication or disclosure of this document complies fully with any relevant export laws and regulations to assure that this document or any portion thereof is not exported, directly or indirectly, in violation of such export laws. Use of the word "partner" in reference to Arm's customers is not intended to create or refer to any partnership relationship with any other company. Arm may make changes to this document at any time and without notice.

If any of the provisions contained in these terms conflict with any of the provisions of any signed written agreement covering this document with Arm, then the signed written agreement prevails over and supersedes the conflicting provisions of these terms. This document may be translated into other languages for convenience, and you agree that if there is any conflict between the

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

English version of this document and any translation, the terms of the English version of the Agreement shall prevail.

Words and logos marked with ® or ™ are registered trademarks or trademarks of Arm Limited or its affiliates in the EU and/or elsewhere. All rights reserved. Other brands and names mentioned in this document may be the trademarks of their respective owners. Please follow Arm's trademark usage guidelines at http://www.arm.com/about/trademarks/guidelines/index.php.

Copyright © 2018, Arm Limited or its affiliates. All rights reserved.

Arm Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

LES-PRE-20348

Confidentiality Status

This document is Confidential. This document may only be used and distributed in accordance with the terms of the agreement entered into by Arm and the party that Arm delivered this document to.

Product Status

The information in this document is final, that is for a developed product.

Contents

1. ISP_COMMON (COMMON_CONFIG) 12
1.1. id 12
1.2. isp global 13
1.3. isp global interrupt 16
1.4. isp global lp 19
1.5. isp global monitor 21
1.6. isp global chicken bit 24
1.7. isp global parameter status 25
1.8. input port 26
1.9. input port frame stats 28
2. CMD_QUEUES (CMD_QUEUES) 31
2.1. Array 31
3. LUT3D_MEM (LUT3D_MEM) 32
3.1. Array 32
4. DS_SCALER_HFILT_COEFMEM (DS_SCALER_HFILT_COEFMEM) 33
4.1. Array 33
5. DS_SCALER_VFILT_COEFMEM (DS_SCALER_VFILT_COEFMEM) 34
5.1. Array 34
6. AEXP_HIST_STATS_MEM (AEXP_HIST_STATS_MEM) 35
6.1. Array 35
7. IHIST_STATS_MEM (IHIST_STATS_MEM) 36
7.1. Array 36
8. METERING_STATS_PING_MEM (METERING_STATS_PING_MEM) 37
8.1. Array 37
9. DECOMPANDER0_PING_MEM (DECOMPANDER0_PING_MEM) 38
9.1. Array 38
10. DECOMPANDER1_PING_MEM (DECOMPANDER1_PING_MEM) 39
10.1. Array 39
11. DPC_PING_MEM (DPC_PING_MEM) 40
11.1. Array 40
12. CA_CORRECTION_FILTER_PING_MEM (CA_CORRECTION_FILTER_PING_MEM) 41
12.1. Array 41
13. CA_CORRECTION_MESH_PING_MEM (CA_CORRECTION_MESH_PING_MEM) 42

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

13.1. Array 42
14. MESH_SHADING_PING_MEM (MESH_SHADING_PING_MEM) 43
14.1. Array 43
15. RADIAL_SHADING_PING_MEM (RADIAL_SHADING_PING_MEM) 44
15.1. Array 44
16. IRIDIX_RP_PING_MEM (IRIDIX_RP_PING_MEM) 45
16.1. Array 45
17. IRIDIX_FP1_PING_MEM (IRIDIX_FP1_PING_MEM) 46
17.1. Array 46
18. FR_GAMMA_RGB_PING_MEM (FR_GAMMA_RGB_PING_MEM) 47
18.1. Array 47
19. DS_GAMMA_RGB_PING_MEM (DS_GAMMA_RGB_PING_MEM) 48
19.1. Array 48
20. LUMVAR_STATS_PING_MEM (LUMVAR_STATS_PING_MEM) 49
20.1. Array 49
21. ISP_CONFIG_PING (SINGLE_CONTEXT_CONFIG) 49
21.1. top 49
21.2. crossbar 55
21.3. video test gen ch0 55
21.4. video test gen ch1 57
21.5. video test gen ch2 59
21.6. video test gen ch3 61
21.7. input formatter 63
21.8. sensor offset wdr l 65
21.9. sensor offset wdr m 65
21.10. sensor offset wdr s 66
21.11. sensor offset wdr vs 66
21.12. gain wdr 67
21.13. frame stitch 68
21.14. frame stitch NP LUT VS 73
21.15. frame stitch NP LUT S 73
21.16. frame stitch NP LUT M 74
21.17. frame stitch NP LUT L 74
21.18. decompander0 75
21.19. decompander1 75

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

21.20. digital gain 75
21.21. sensor offset fe 76
21.22. sqrt 76
21.23. raw frontend 77
21.24. raw frontend np 78
21.25. raw frontend np lut 79
21.26. defect pixel 79
21.27. sinter 80
21.28. sinter Noise Profile 82
21.29. sinter Noise Profile LUT 83
21.30. sinter shading 84
21.31. temper 84
21.32. temper Noise Profile 85
21.33. temper Noise Profile LUT 86
21.34. temper dma 87
21.35. ca correction 91
21.36. square be 91
21.37. sensor offset pre shading 92
21.38. radial shading 92
21.39. mesh shading 94
21.40. white balance 95
21.41. white balance aexp 96
21.42. iridix gain 96
21.43. iridix 97
21.44. iridix LUT 100
21.45. demosaic rgb 101
21.46. demosaic rgb Noise Profile 106
21.47. demosaic rgbir 107
21.48. pf correction 110
21.49. pf correction Shading 114
21.50. ccm 114
21.51. cnr 118
21.52. nonequ gamma 123
21.53. lumvar 124
21.54. metering aexp 125

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

21.55. metering awb 126
21.56. metering af 129
21.57. metering hist aexp 129
21.58. metering ihist 132
21.59. fr crop 135
21.60. fr gamma rgb 136
21.61. fr sharpen 137
21.62. fr cs conv 138
21.63. fr cs conv dither 141
21.64. fr dma writer 142
21.65. fr uv dma writer 146
21.66. ds crop 150
21.67. ds scaler 151
21.68. ds gamma rgb 153
21.69. ds sharpen 154
21.70. ds cs conv 155
21.71. ds cs conv dither 158
21.72. ds dma writer 159
21.73. ds uv dma writer 163
21.74. multi ctx 167
22. METERING_STATS_PONG_MEM (METERING_STATS_PONG_MEM) 167
22.1. Array 167
23. DECOMPANDER0_PONG_MEM (DECOMPANDER0_PONG_MEM) 168
23.1. Array 168
24. DECOMPANDER1_PONG_MEM (DECOMPANDER1_PONG_MEM) 169
24.1. Array 169
25. DPC_PONG_MEM (DPC_PONG_MEM) 170
25.1. Array 170
26. CA_CORRECTION_FILTER_PONG_MEM (CA_CORRECTION_FILTER_PONG_MEM) 171
26.1. Array 171
27. CA_CORRECTION_MESH_PONG_MEM (CA_CORRECTION_MESH_PONG_MEM) 172
27.1. Array 172
28. MESH_SHADING_PONG_MEM (MESH_SHADING_PONG_MEM) 173
28.1. Array 173
29. RADIAL_SHADING_PONG_MEM (RADIAL_SHADING_PONG_MEM) 174

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

29.1. Array 174
30. IRIDIX_RP_PONG_MEM (IRIDIX_RP_PONG_MEM) 175
30.1. Array 175
31. IRIDIX_FP1_PONG_MEM (IRIDIX_FP1_PONG_MEM) 176
31.1. Array 176
32. FR_GAMMA_RGB_PONG_MEM (FR_GAMMA_RGB_PONG_MEM) 177
32.1. Array 177
33. DS_GAMMA_RGB_PONG_MEM (DS_GAMMA_RGB_PONG_MEM) 178
33.1. Array 178
34. LUMVAR_STATS_PONG_MEM (LUMVAR_STATS_PONG_MEM) 179
34.1. Array 179
35. ISP_CONFIG_PONG (SINGLE_CONTEXT_CONFIG) 179
35.1. top 179
35.2. crossbar 185
35.3. video test gen ch0 185
35.4. video test gen ch1 187
35.5. video test gen ch2 189
35.6. video test gen ch3 191
35.7. input formatter 193
35.8. sensor offset wdr l 195
35.9. sensor offset wdr m 195
35.10. sensor offset wdr s 196
35.11. sensor offset wdr vs 196
35.12. gain wdr 197
35.13. frame stitch 198
35.14. frame stitch NP LUT VS 203
35.15. frame stitch NP LUT S 203
35.16. frame stitch NP LUT M 204
35.17. frame stitch NP LUT L 204
35.18. decompander0 205
35.19. decompander1 205
35.20. digital gain 205
35.21. sensor offset fe 206
35.22. sqrt 206
35.23. raw frontend 207

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

35.24. raw frontend np 208
35.25. raw frontend np lut 209
35.26. defect pixel 209
35.27. sinter 210
35.28. sinter Noise Profile 212
35.29. sinter Noise Profile LUT 213
35.30. sinter shading 214
35.31. temper 214
35.32. temper Noise Profile 215
35.33. temper Noise Profile LUT 216
35.34. temper dma 217
35.35. ca correction 221
35.36. square be 221
35.37. sensor offset pre shading 222
35.38. radial shading 222
35.39. mesh shading 224
35.40. white balance 225
35.41. white balance aexp 226
35.42. iridix gain 226
35.43. iridix 227
35.44. iridix LUT 230
35.45. demosaic rgb 231
35.46. demosaic rgb Noise Profile 236
35.47. demosaic rgbir 237
35.48. pf correction 240
35.49. pf correction Shading 244
35.50. ccm 244
35.51. cnr 248
35.52. nonequ gamma 253
35.53. lumvar 254
35.54. metering aexp 255
35.55. metering awb 256
35.56. metering af 259
35.57. metering hist aexp 259
35.58. metering ihist 262

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.59. fr crop 265
35.60. fr gamma rgb 266
35.61. fr sharpen 267
35.62. fr cs conv 268
35.63. fr cs conv dither 271
35.64. fr dma writer 272
35.65. fr uv dma writer 276
35.66. ds crop 280
35.67. ds scaler 281
35.68. ds gamma rgb 283
35.69. ds sharpen 284
35.70. ds cs conv 285
35.71. ds cs conv dither 288
35.72. ds dma writer 289
35.73. ds uv dma writer 293
35.74. multi ctx 297

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:

- The title.
- The number ARM-EPM-136050.
- The page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Note

ARM tests the PDF only in Adobe Acrobat and Acrobat Reader, and cannot guarantee the quality of the represented document when used with any other PDF reader.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

1. ISP_COMMON (COMMON_CONFIG)

1.1. id

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00000	**R/O**	**API**																																--

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

1.2. isp global

Miscellaneous top-level ISP controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x00010	R/W		dma global config [26:12]															0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		dma global config [11:0]														scaler fsm reset	Global FSM reset	

Global FSM reset 1 = synchronous reset of FSMs in design (faster recovery after broken frame)
when the MCU detects a broken frame or any other abnormal condition, the global_fsm_rest is
expected to be used.
MCU needs to follow a certain sequence for the same
1. Read the status register to know the exact source of the error interrupt.
2. Read the details of the error status register.
3. Mask all the interrupts.
4. Configure the input port register ISP_COMMON:input port: mode request to safe_stop mode.
5. Read back the ISP_COMMON:input port: mode status register to see the status of mode request.
And wait until it shows the correct status.
6. Wait for the ISP_COMMON:isp global monitor: fr pipeline busy signal to become low.
7. Assert the global fsm reset.
8. Clear the global fsm reset.
9. Reconfigure the ISP configuration space.
10. Unmask the necessary interrupt sources.
11. Configure the input port in safe_start mode.

scaler fsm reset 1 = synchronous reset of FSMs in scaler design

dma global config [26:0] [0] : check bid
[1] : check rid

The following signals are diagnostic signals which helps identifying some of the AXI interface
error cases. This must be used only as debug signals. You should follow these sequence
- Mask the dma error interrupt
- clear DMA interrupt if there is an active interrupt
- Write appropriate values to these registers
- Clear DMA alarms to clear the existing alarm
- unmask the DMA error interrpt

[2] : frame_write_cancel/frame_read_cancel
[10:3] : awmaxwait_limit/armaxwait_limit
[18:11]: wmaxwait_limit
[26:19]: waxct_ostand_limit/rxnfr_ostand_limit

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x00014	R/W														ISP monitor select			0x00040020
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		Flush hblank																

Flush hblank [15:0] Horizontal blanking interval during regeneration (0=measured input interval)

ISP monitor select [2:0]
0 = linearised data after linearised cluster, MSB aligned. {data[19:0], 16'd0}
1 = static DPC output, MSB aligned. {data[15:0], 20'd0}
2 = Output of CA correction, MSB aligned. {data[15:0], 20'd0}
3 = CNR output, {B[11:0], G[11:0], R[11:0]}
4 = output forces to 0
5 = Reserved
6 = Reserved
7 = Reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00018	R/W	interframe blanks min																interline blanks min																0x00280020

interline_blanks_min [15:0] Minimun H-blank. The frame monitor will checke the frame geometry against this value

interframe_blanks_min [15:0] Minimun V-blank. The frame monitor will checke the frame geometry against this value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x0001C	R/W	watchdog timer max count																																0xFFFFFFFF

watchdog timer max count [31:0] Max count after which watchdog timer should give an interrupt. this count is between frame start and frame end

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x00020	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
									multi context mode							**Mcu ping pong config select**	**Mcu override config select**	

Mcu override config select mcu override config select. When this bit is set, MCU takes control of the ISP ping-pong config swap.
when is signal is set to 1, ISP core works in slave mode and selects configuration space based on MCU instruction.

Mcu ping pong config select This signal is valid when Mcu_override_config_select is set to 1.
when mcu takes control of the config select, this signal indicated whether to use ping and pong config space
If this signal is changed during active active frame, the hardware makes sure that the config space is changed
in the next vertical blanking
0 = Use pong address space
1 = Use Ping address space

multi context mode Multi-context control mode
0 = default mode, this is for single context
1 = multi-context mode

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x00024	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
															ping pong config select	pong locked	ping locked	

ping locked context swap status. when a address space is locked, all write to that address space will be rejected internally
This signal is set when the 1st pixel comes out of input port and gets cleared when the last pixel comes out of ISp in streaming channels
1: ping locked
0: ping free

pong locked context swap status. when a address space is locked, all write to that address space will be rejected internally.
This signal is set when the 1st pixel comes out of input port and gets cleared when the last pixel comes out of ISp in streaming channels
1: pong locked
0: pong free

ping pong config select this signal indicates which of the PING/PONG config is being used by ISP. when MCU takes control of the config management through
Mcu_override_config_select signal, then this signal is just a reflection of what MCU has instructed through Mcu_ping_pong_config_select
signal.

This signal is a good point to synchronize with hardware. MCU should read this signal in a regular interval to synchronize with its
internal state.

This signal is changed when the 1st pixel comes in. So this signal must be sampled at the frame_start interrupt.

0: pong in use by ISP
1: ping in use by ISP

1.3. isp global interrupt

interrupt controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00030	R/W	mask vector																																0x00000000

mask_vector [31:0] Interrupt mask vector
0: Interrupt is enabled
1: interrupt is masked

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00034	R/W	clear vector																																0x00000000

clear_vector [31:0] Interrupt clear vector. its bitwise cleared. When a bit is set to 1. that interrupt bit in the status register is cleared

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00038	R/W	shadow disable vector																																0x00000000

shadow_disable_vector [31:0] Interrupt shadow disable vector.
To disable shadow feature for the specific interrupt event by setting the related bit to 1.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x0003C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	pulse mode	

pulse_mode When set to 1, the output interrupt will be a pulse. Otherwise it should be level.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x00040	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	clear	

clear Interrupt clear vector register qualifier. First the vector must be written. Then this bit must be set to 1 and then cleared

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00044	R/O	status vector																																--

status_vector [31:0]

bit[0] : Isp_start
bit[1] : Isp_done
bit[2] : Context management error
bit[3] : Broken frame error
bit[4] : Metering AF done
bit[5] : Metering aexp done
bit[6] : Metering awb done
bit[7] : Metering aexp 1024 bin hist done
bit[8] : Metering antifog hist done
bit[9] : Lut init done
bit[10] : FR y-dma write done
bit[11] : FR uv-dma write done
bit[12] : DS y-dma write done
bit[13] : DS uv-dma write done
bit[14] : Linearization done
bit[15] : Static dpc done
bit[16] : Ca correction done
bit[17] : Iridix done
bit[18] : 3d LIUT done
bit[19] : Watchdog timer timed out
bit[20] : Frame collision error
bit[21] : luma variance done
bit[22] : DMA error interrupt
bit[23] : Input port safely stopped

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

1.4. isp global lp

CLK DIS register:
This register shitches off clock of certain blocks.

CLK DIS register:
This register controls the clock gate cell which gates clock during V-blank. When this is set to 1, the v-blank clock
gating will be disabled. This register doesnt control the static clock gating which is controlled through CLK DIS register

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x00048	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													CLK Dis temper dma	CLK Dis DS UV dma writer	CLK Dis DS Y dma writer	CLK Dis FR UV dma writer	CLK Dis FR Y dma writer	

CLK Dis FR Y dma writer When set, the output Y/RGB/YUV DMA writer in FR channel will be clock gated. This is applicable
to Y channel of the semi-planner mode and all other non-planner modes. This must be used only when the DMA writer is not used and SOC
environment uses the streaming outputs from ISP

CLK Dis FR UV dma writer When set, the output UV DMA writer in FR channel will be clock gated. This is applicable to UV channel of the semi-planner mode . This must be used only when the DMA writer is not used and SOC
environment uses the streaming outputs from ISP, or format is NOT semi-planner

CLK Dis DS Y dma writer When set, the output Y/RGB/YUV DMA writer in DS channel will be clock gated. This is applicable
to Y channel of the semi-planner mode and all other non-planner modes. This must be used only when the DMA writer is not used and SOC
environment uses the streaming outputs from ISP

CLK Dis DS UV dma writer When set, the output UV DMA writer in DS channel will be clock gated. This is applicable to UV channel of the semi-planner mode . This must be used only when the DMA writer is not used and SOC
environment uses the streaming outputs from ISP, or format is NOT semi-planner

CLK Dis temper dma This signal gates the clock for all temper write and read dma. This should be used only when Temper is not used.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x0004C	R/W	23	22	21	20	19	18	17	16	0x00000000
							CG Dis Sharpen DS	CG Dis Sharpen FR	CG Dis RGB Gamma DS	
		15	14	13	12	11	10	9	8	
		CG Dis RGB Gamma FR	CG Dis RGB Scaler	CG Dis 3D LUT	CG Dis CNR	CG Dis PF correction	CG Dis demosaic RGBIr	CG Dis demosaic RGGB	CG Dis Iridix	
		7	6	5	4	3	2	1	0	
		CG Dis mesh shading	CG Dis radial shading	CG Dis CA Correction	CG Dis Temper	CG Dis Sinter	CG Dis defect pixel	CG Dis raw frontend	CG Dis frame stitch	

CG Dis frame_stitch when set, this will disable V-blank Clock gating for WDR path channels.
CG Dis raw frontend when set, this will disable V-blank Clock gating for raw frontend.
CG Dis defect pixel when set, this will disable V-blank Clock gating for defect pixel.
CG Dis Sinter when set, this will disable V-blank Clock gating for Sinter.
CG Dis Temper when set, this will disable V-blank Clock gating for Temper.
CG Dis CA Correction when set, this will disable V-blank Clock gating for CA correction.
CG Dis radial shading when set, this will disable V-blank Clock gating for radial shading.
CG Dis mesh shading when set, this will disable V-blank Clock gating for mesh shading.
CG Dis Iridix when set, this will disable V-blank Clock gating for Iridix.
CG Dis demosaic RGGB when set, this will disable V-blank Clock gating for Demosaic RGGB.
CG Dis demosaic RGBIr when set, this will disable V-blank Clock gating for Demosaic RGBIr.
CG Dis PF correction when set, this will disable V-blank Clock gating for PF correction.
CG Dis CNR when set, this will disable V-blank Clock gating for CNR and pre-square root and post-square.
CG Dis 3D LUT when set, this will disable V-blank Clock gating for 3D LUT.
CG Dis RGB Scaler when set, this will disable V-blank Clock gating for RGB scaler.
CG Dis RGB Gamma FR when set, this will disable V-blank Clock gating for RGB gamma in FR pipeline.
CG Dis RGB Gamma DS when set, this will disable V-blank Clock gating for RGB gamma in DS pipeline.
CG Dis Sharpen FR when set, this will disable V-blank Clock gating for sharpen in FR pipeline.
CG Dis Sharpen DS when set, this will disable V-blank Clock gating for sharpen in DS pipeline.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

1.5. isp global monitor

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x00050	R/O																fr pipeline busy	--
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
														broken frame status				

broken_frame status [3:0]
bit[0] : active width mismatch
bit[1] : active_height mismatch
bit[2] : minimum v-blank violated
bit[3] : minimum h-blank violated

fr_pipeline_busy
This signal indicates if ISP pipeline is busy or Not, This signal doesnt include the metereing modules.
This information is expected to be used when a broken frame is detected and global_fsm_reset needs to be asserted
global_fsm_reset must be set when this busy signal is low.
0: ISP main pipeline (excluding metering) is free
1: ISP main pipeline (excluding metering) is busy

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x00054	R/O			DMA alarms [13:8]						--
		23	22	21	20	19	18	17	16	
		DMA alarms [7:0]								
		15	14	13	12	11	10	9	8	
						Temper DMA RFIFO fail full	Temper DMA RFIFO fail empty	Temper DMA WFIFO fail full	Temper DMA WFIFO fail empty	
		7	6	5	4	3	2	1	0	
		DS UV DMA WFIFO fail empty	DS UV DMA WFIFO fail full	DS Y DMA WFIFO fail empty	DS Y DMA WFIFO fail full	FR UV DMA WFIFO fail empty	FR UV DMA WFIFO fail full	FR Y DMA WFIFO fail empty	FR Y DMA WFIFO fail full	

DMA alarms [13:0]

[0] : temper_dma_lsb_wtr_axi_alarm
[1] : temper_dma_lsb_rdr_axi_alarm
[2] : temper_dma_msb_wtr_axi_alarm
[3] : temper_dma_msb_rdr_axi_alarm
[4] : FR UV dma axi alarm
[5] : FR dma axi alarm
[6] : DS UV dma axi alarm
[7] : DS dma axi alarm
[8] : Temper LSB dma frame dropped
[9] : Temper MSB dma frame dropped
[10]: FR UV-DMA frame dropped
[11]: FR Y-DMA frame dropped
[12]: DS UV-DMA frame dropped
[13]: DS Y-DMA frame dropped

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x00058	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														temper dma clr alarm	output dma clr alarm	context error clr	broken frame error clear	

broken_frame error clear This signal must be asserted when the MCu gets broken frame interrupt.
this signal must be 0->1->0 pulse. The duration of the pulse is not relevant. This rising edge will clear the
broken frame error status signal

context error clr This signal must be asserted when the MCU gets the context error interrupt.
this signal must be 0->1->0 pulse. The duration of the pulse is not relevant. This rising edge will clear the
context error status signal

output dma clr alarm This signal must be asserted when the MCU gets the DMA error interrupt.
This signal will clear all DMA error status signals for all the output DMA writers (Y/UV DMAs in both of the output channels)
MCU must follow the following sequance to clear the alarms
step-1: set this bit to 1
step-2: Read back the alarm signals
step-3: If the alarms are cleared, then clear the clr_alarm signal back to 0.

temper dma clr alarm This signal must be asserted when the MCU gets the DMA error interrupt.
This signal will clear all DMA error status signals for all the Temper DMA writers/readers
MCU must follow the following sequance to clear the alarms
step-1: set this bit to 1
step-2: Read back the alarm signals

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00060	R/O	MAX address delay line ds																MAX address delay line fr																--

MAX address delay line fr [15:0] Delay line max address value for the full resolution ISP set outside ISP

MAX address delay line ds [15:0] Delay line max address value for the DS pipeline set outside ISP

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

1.6. isp global chicken bit

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x00064	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000004
												dma writer timeout disable	**soft rst apply immediately**	Rsvd	Rsvd	Rsvd	Rsvd	

soft_rst_apply_immediately 0 = When this chicken bit is et to 0, the soft reset (SW or HW generated) will be stretched by 1024 cycles
so that it is asserted till the the pipeline delay of internal acl signals.
1 = When thiss set to 1, the soft reset will not be stretched internally. The SW must make sure its
kept high enough.

dma_writer_timeout_disable 0=timeout enabled. At the end of the frame, if the last data is not drained out from DMA writer within 4000
AXI clock, cycle, DMA will flush the FIFO and ignore the remainign data.

1=timeout is disabled. If the last data is not drained out and the next frame starts coming in, DMA will drop the next frame and
give an interrupt.
If the timeout is disabled, its S/W responsibility to cancel the frame in all dma engines if frame drop interrupt comes.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

1.7. isp global parameter status

ISP provides few CHICKEN_OUT parameters through which certain modules can be removed from ISP. This reggister indicates the status of that CHICKEN BIT

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x00068	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
													sinter version	LUT 3d	ds pipe	cac	dmsc rgbir	

dmsc_rgbir
0: Demosaic RGBIr is present in the design
1: Demodaic RGBIr is statically removed from the ISP.
S/W must not access the ISP_CONFIG_PING:demosaic rgbir and the ISP_CONFIG_PONG:demosaic rgbir registers

cac
0: CA Correction is present in the design
1: CA Correction is statically removed from the ISP.
S/W must not access the ISP_CONFIG_PING:ca correction and the ISP_CONFIG_PONG:ca correction registers

Also SW must not access the following memories
- CA_CORRECTION_FILTER_PING_MEM
- CA_CORRECTION_FILTER_PONG_MEM
- CA_CORRECTION_MESH_PING_MEM
- CA_CORRECTION_MESH_PONG_MEM

ds_pipe
0: DS pipeline is present in the design
1: DS pipeline is statically removed from ISP.
S/W must not access the following register spaces
- ISP_CONFIG_PING:ds crop and ISP_CONFIG_PONG:ds crop
- ISP_CONFIG_PING:ds scaler and ISP_CONFIG_PONG:ds scaler
- ISP_CONFIG_PING:ds gamma rgb and ISP_CONFIG_PONG:ds gamma rgb
- ISP_CONFIG_PING:ds sharpen and ISP_CONFIG_PONG:ds sharpen
- ISP_CONFIG_PING:ds cs conv and ISP_CONFIG_PONG:ds cs conv
- ISP_CONFIG_PING:ds dma writer and ISP_CONFIG_PONG:ds dma writer
- ISP_CONFIG_PING:ds uv dma writer and ISP_CONFIG_PONG:ds uv dma writer

Also the S/W must not access the following memories
- DS_SCALER_HFILT_COEFMEM
- DS_SCALER_VFILT_COEFMEM
- DS_GAMMA_RGB_PING_MEM
- DS_GAMMA_RGB_PONG_MEM

LUT 3d
0: sRGB gamma and 3D LUT is present in the design
1: sRGB gamma and 3D LUT is statically removed from ISP.
The S/W must not accees the following register spaces
- ISP_CONFIG_PING:nonequ gamma and ISP_CONFIG_PING: nonequ gamma and

Also, the S/W must not access the following memories
- LUT3D_MEM

sinter_version
0: SINTER2.5 used
1: SINTER3 used

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

1.8. input port

Controls video input port.

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x00080	R/W								Reserved	0x00100002
		23	22	21	20	19	18	17	16	
		hc r select			**hs polarity vc**	Reserved	Reserved	Reserved	Reserved	
		15	14	13	12	11	10	9	8	
		vc r select	**vc c select**		Reserved	Reserved	Reserved	Reserved	Reserved	
		7	6	5	4	3	2	1	0	
						preset				

preset [3:0] Allows selection of various input port presets for standard sensor inputs. See ISP Guide for details of available presets.
2: preset mode 2, check ISP guide for details
6: preset mode 6, check ISP guide for details
others: reserved

vc_c select
0 = vertical counter counts on hs
1 = vertical counter counts on horizontal counter overflow or reset

vc_r select
0 = vertical counter is reset on edge of vs
1 = vertical counter is reset after timeout on hs

hs_polarity vc
0 = vertical counter increments on rising edge of HS
1 = vertical counter increments on falling edge of HS

hc_r select
0 = vertical counter is reset on rising edge of hs
1 = vertical counter is reset on rising edge of vs

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00088	R/W	**hc start0**																**hc limit**																0x0000FFFF

hc limit [15:0] horizontal counter limit value (counts: 0,1,...hc_limit-1,hc_limit,0,1,...)
hc start0 [15:0] window0 start for ACL gate. See ISP guide for further details.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x0008C	R/W	**hc start1**																**hc size0**																0x00000000

hc size0 [15:0] window0 size for ACL gate. See ISP guide for further details.
hc start1 [15:0] window1 start for HS gate. See ISP guide for further details.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00090	R/W	vc limit																hc size1																0xFFFF0000

hc size1 [15:0] window1 size for HS gate. See ISP guide for further details.
vc limit [15:0] vertical counter limit value (counts: 0,1,...vc_limit-1,vc_limit,0,1,...)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00094	R/W	vc size																vc start																0x00000000

vc start [15:0] window2 start for ACL gate. See ISP guide for further details.
vc size [15:0] window2 size for ACL gate. See ISP guide for further details.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00098	R/O	frame height																frame width																--

frame width [15:0] detected frame width. Read only value.
frame height [15:0] detected frame height. Read only value.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x0009C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										freeze config					mode request			

mode request [2:0] Used to stop and start input port. See ISP guide for further details.
Only modes-0 and 1 are used. all other values are reserved
- 0 = safe stop
- 1 = safe start
- 2 = Reserved
- 3 = Reserved
- 4 = Reserved
- 5 = Reserved
- 6 = Reserved
- 7 = Reserved

freeze config Used to freeze input port configuration. Used when multiple register writes are required to change input port configuration.
- 0 = normal operation
- 1 = hold previous input port config state

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x000A0	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
															mode status			

mode status [2:0] Used to monitor input port status:
bit 0: 1=running, 0=stopped, bits 1,2-reserved

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

1.9. input port frame stats

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x000A4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	stats reset	

stats reset Resets the frame statistics registers and starts the sampling period. Note all the frame statistics saturate at 2^31

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x000A8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	stats hold	

stats hold Synchronously disables the update of the statistics registers. This should be used prior to reading out the register values so as to ensure consistent values

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000B4	R/O	active width min																																--

active width min [31:0] The minimum number of active pixels observed in a line within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000B8	R/O	active width max																																--

active width max [31:0] The maximum number of active pixels observed in a line within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000BC	R/O	active width sum																																--

active width sum [31:0] The total number of the active pixels values observed in a line within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000C0	R/O	active width num																																--

active width num [31:0] The number of lines observed within the sampling period

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000C4	R/O	active height min																																--

active height min [31:0] The minimum number of active lines in the frames observed within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000C8	R/O	active height max																																--

active height max [31:0] The maximum number of active lines in the frames observed within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000CC	R/O	active height sum																																--

active height sum [31:0] The total number of active lines in the frames observed within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000D0	R/O	active height num																																--

active height num [31:0] The total number of frames observed within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000D4	R/O	hblank min																																--

hblank min [31:0] The minimum number of horizontal blanking samples observed within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000D8	R/O	hblank max																																--

hblank max [31:0] The maximum number of horizontal blanking samples observed within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000DC	R/O	hblank sum																																--

hblank sum [31:0] The total number of the horizontal blanking samples observed within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000E0	R/O	hblank num																																--

hblank num [31:0] The total number of the lines observed within the sampling period

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000E4	R/O	vblank min																																--

vblank min [31:0] The minimum number of vertical blanking samples observed within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000E8	R/O	vblank max																																--

vblank max [31:0] The maximum number of vertical blanking samples observed within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000EC	R/O	vblank sum																																--

vblank sum [31:0] The total number of the vertical blanking samples observed within the sampling period

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x000F0	R/O	vblank num																																--

vblank num [31:0] The total number of frames observed within the sampling period

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

2. CMD_QUEUES (CMD_QUEUES)

Scratchpad area for communicating with ISP firmware. Please refer to ISP firmware guide for layout of this block.

2.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00108	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x0010C	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x00504	R/W	Data(255)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 256 32-bit registers. The address for element (i) is: 0x00108 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

3. LUT3D_MEM (LUT3D_MEM)

3.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x00508	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x0050C	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x014A4	R/W	Data(999)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 1000 32-bit registers. The address for element (i) is: 0x00508 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

4. DS_SCALER_HFILT_COEFMEM (DS_SCALER_HFILT_COEFMEM)

4.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x014A8	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x014AC	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x01CA4	R/W	Data(511)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 512 32-bit registers. The address for element (i) is: 0x014A8 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

5. DS_SCALER_VFILT_COEFMEM (DS_SCALER_VFILT_COEFMEM)

5.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x01CA8	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x01CAC	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x024A4	R/W	Data(511)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 512 32-bit registers. The address for element (i) is: 0x01CA8 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

6. AEXP_HIST_STATS_MEM (AEXP_HIST_STATS_MEM)

6.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x024A8	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x024AC	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x034A4	R/W	Data(1023)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 1024 32-bit registers. The address for element (i) is: 0x024A8 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

7. IHIST_STATS_MEM (IHIST_STATS_MEM)

7.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x034A8	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x034AC	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x044A4	R/W	Data(1023)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 1024 32-bit registers. The address for element (i) is: 0x034A8 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

8. METERING_STATS_PING_MEM (METERING_STATS_PING_MEM)

8.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x044B0	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x044B4	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x0AB68	R/W	Data(6574)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 6575 32-bit registers. The address for element (i) is: 0x044B0 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

9. DECOMPANDER0_PING_MEM (DECOMPANDER0_PING_MEM)

9.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x0AB6C	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x0AB70	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x0ABEC	R/W	Data(32)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 33 32-bit registers. The address for element (i) is: 0x0AB6C + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

10. DECOMPANDER1_PING_MEM (DECOMPANDER1_PING_MEM)

10.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
`0x0ABF0`	**R/W**	**Data(0)**																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x0ABF4`	**R/W**	**Data(1)**																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x0AFF0`	**R/W**	**Data(256)**																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 257 32-bit registers. The address for element (i) is: 0x0ABF0 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

11. DPC_PING_MEM (DPC_PING_MEM)

the content of the memory is {y-coord[11:0], x-coord[12:0]}. Phisical memory width is 25bits.
the top-left corner of the frame is indicated by {1,1}

11.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
`0x0AFF4`	**R/W**	**Data(0)**																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x0AFF8`	**R/W**	**Data(1)**																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x0EFF0`	**R/W**	**Data(4095)**																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 4096 32-bit registers. The address for element (i) is: 0x0AFF4 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

12. CA_CORRECTION_FILTER_PING_MEM (CA_CORRECTION_FILTER_PING_MEM)

Cromatic aberration correction polyphase filter lookup table, 32 entries of 32 bits each.
Each entry address corresponds to fractional part of the pixel displacement.
Each entry is four 8-bit filter coefficients in fix point format.
- Codes 0...128 correspond to values 0.0 ... 1.0 (with resolution 1/128)
- Codes 129...191 correspond to values 129/128 ... 191/128
- Codes 192...255 correspond to values -64/128 ... -1/128

12.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
`0x0EFF4`	**R/W**	**Data(0)**																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x0EFF8`	**R/W**	**Data(1)**																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x0F070`	**R/W**	**Data(31)**																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 32 32-bit registers. The address for element (i) is: 0x0EFF4 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

13. CA_CORRECTION_MESH_PING_MEM (CA_CORRECTION_MESH_PING_MEM)

Chromatic aberration correction coordinate lookup table, 8192 entries for tile displacement of 16 bits each. Each entry is 16 bits, 8 LSBs is X displacement of the tile and 8 MSBs is Y displacement. The coordiantes are coded as two's complement, 3.5 fixed point.

13.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
`0x0F074`	**R/W**	**Data(0)**																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x0F078`	**R/W**	**Data(1)**																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x13070`	**R/W**	**Data(4095)**																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 4096 32-bit registers. The address for element (i) is: 0x0F074 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

14. MESH_SHADING_PING_MEM (MESH_SHADING_PING_MEM)

14.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x13074	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x13078	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x17070	R/W	Data(4095)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 4096 32-bit registers. The address for element (i) is: 0x13074 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

15. RADIAL_SHADING_PING_MEM (RADIAL_SHADING_PING_MEM)

4 banks of radial shading lookup tables - for R,G,B,Ir channels.
The banks start at the addresses 0, 256, 512, 768.
Each bank has 129 entries for piecewise linear table, each entry occupies 32 bits, of which 16 least significant bits are encoding shading correction factor in 4.12 fix point format.

15.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
`0x17074`	**R/W**	**Data(0)**																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x17078`	**R/W**	**Data(1)**																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x17E74`	**R/W**	**Data(896)**																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 897 32-bit registers. The address for element (i) is: 0x17074 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

16. IRIDIX_RP_PING_MEM (IRIDIX_RP_PING_MEM)

16.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
`0x17E78`	**R/W**	**Data(0)**																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x17E7C`	**R/W**	**Data(1)**																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x18078`	**R/W**	**Data(128)**																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 129 32-bit registers. The address for element (i) is: 0x17E78 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

17. IRIDIX_FP1_PING_MEM (IRIDIX_FP1_PING_MEM)

17.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1807C	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x18080	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1827C	R/W	Data(128)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 129 32-bit registers. The address for element (i) is: 0x1807C + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

18. FR_GAMMA_RGB_PING_MEM (FR_GAMMA_RGB_PING_MEM)

18.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18280	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x18284	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x18480	R/W	Data(128)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 129 32-bit registers. The address for element (i) is: 0x18280 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

19. DS_GAMMA_RGB_PING_MEM (DS_GAMMA_RGB_PING_MEM)

19.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
`0x18484`	**R/W**	**Data(0)**																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x18488`	**R/W**	**Data(1)**																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x18684`	**R/W**	**Data(128)**																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 129 32-bit registers. The address for element (i) is: 0x18484 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

20. LUMVAR_STATS_PING_MEM (LUMVAR_STATS_PING_MEM)

20.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18688	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1868C	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x18E84	R/W	Data(511)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 512 32-bit registers. The address for element (i) is: 0x18688 + 4i.

21. ISP_CONFIG_PING (SINGLE_CONTEXT_CONFIG)

21.1. top

Miscellaneous top-level ISP controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18E88	R/W	Active Height																Active Width																0x04380780

Active Width [15:0] Active video width in pixels

Active Height [15:0] Active video height in lines

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18E8C	R/W							Linear data src								Cfa pattern		0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
								RGGB start post mirror								RGGB start pre mirror		

RGGB start pre mirror [1:0] Starting color of the rggb pattern for all the modules before mirror
0 = R Gr
Gb B
1 = Gr R
B Gb
2 = Gb B
R Gr
3 = B Gb
Gr R

RGGB start post mirror [1:0] Starting color of the rggb pattern for all the modules after mirror
this must be same as RGGB start pre mirror if mirror is bypassed

Cfa pattern [1:0] The pixel arrangement of the CFA array on the sensor. Set in the Top register group and used by several blocks in the pipeline:
0 = RGGB
1 = reserved
2 = RIrGB
3 = RGIrB

Linear data src [1:0] Linear data src
0 = Sensor stitched and linear data directly coming from sensor
1 = linear data from frame stitch
2 = Sensor companded data linearised through decompander
3 = reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18EAC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
												Bypass frame stitch	Bypass gain wdr	Bypass sensor offset wdr	Bypass decompander	Bypass input formatter	Bypass video test gen	

Bypass video test gen Bypass video test generator
Bypass input formatter Bypass input formatter module.
Bypass decompander Bypass front end decompander
Bypass sensor offset wdr Bypass sensor offset wdr
Bypass gain wdr Bypass gain wdr
Bypass frame stitch Bypass frame stitching logic

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18EB0	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000004
													Bypass defect pixel	Bypass RAW frontend	Bypass fe sqrt	Bypass frontend sensor offset	Bypass digital gain	

Bypass digital gain Bypass digital gain module
Bypass frontend sensor offset Bypass digital gain module
Bypass fe sqrt Bypass square root function before raw frontend
Bypass RAW frontend Bypass RAW frontend (green equalization and dynamic defect pixel)
Bypass defect pixel Bypass static defect pixel

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18EB8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000002
															Bypass ca correction	Bypass temper	Bypass sinter	

Bypass sinter Bypass sinter
Bypass temper Bypass temper
Bypass ca correction Bypass chromatic abberation correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18EBC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
											Bypass iridix	Bypass iridix gain	Bypass white balance	Bypass mesh shading	Bypass radial shading	Bypass sensor offset pre shading	Bypass square be	

Bypass square_be Bypass backend square
Bypass sensor_offset_pre_shading Bypass sensor offset pre shading
Bypass radial shading Bypass radial shading
Bypass mesh shading Bypass mesh ashading
Bypass white balance Bypass white balance
Bypass iridix gain Bypass
Bypass iridix Bypass

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18EC0	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										Bypass nonequ gamma	**Bypass 3D lut**	**Bypass CNR**	**Bypass CCM**	**Bypass pf correction**	**Bypass demosaic rgbir**	**Bypass demosaic rgb**	**Bypass mirror**	

Bypass mirror Bypass EW mirror
Bypass demosaic rgb Bypass demosaic rgb
Bypass demosaic rgbir Bypass demosaic rgbir
Bypass pf correction Bypass pf correction
Bypass CCM Bypass CCM
Bypass CNR Bypass CNR
Bypass 3D lut Bypass 3d lut
Bypass nonequ gamma Bypass nonequ gamma

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18EC4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Bypass fr cs conv	**Bypass fr sharpen**	**Bypass fr gamma rgb**	**Bypass fr crop**	

Bypass fr crop Bypass fr crop
Bypass fr gamma rgb Bypass fr gamma rgb
Bypass fr sharpen Bypass fr sharpen
Bypass fr cs conv Bypass fr cs conv

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18EC8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Bypass ds cs conv	**Bypass ds sharpen**	**Bypass ds gamma rgb**	**Bypass ds scaler**	**Bypass ds crop**	

Bypass ds crop Bypass ds crop
Bypass ds scaler Bypass ds scaler
Bypass ds gamma rgb Bypass ds gamma rgb
Bypass ds sharpen Bypass ds sharpen
Bypass ds cs conv Bypass ds cs conv

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18ECC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
								ISP processing fr bypass mode								ISP downscale pipe disable	ISP RAW bypass	

ISP RAW bypass
Used to select between normal ISP processing with image sensor data and up to 12 bit RGB input.
In the latler case data is reinserted into pipeline after purple fringing correction block.
0 = Select processed.
1 = Bypass ISP RAW processing.

ISP downscale pipe disable
0: Downscale pipeline is enabled
1: Downscale pipeline is disabled. No data is sent out in DMA and streaming channel
0 = Select processed.
1 = Bypass ISP RAW processing.

ISP processing fr bypass mode [1:0]
ISP FR bypass modes. For debug purposes only. Should be set to 0 during normal operation.
Used to bypass entire ISP after input port or to pass the stitched image directly to the output.
0 = Full processing
1 = Bypass entire ISP processing and output [19:4] of raw sensor data After video test gen
2 = Bypass entire ISP processing and output LSB 10-bits bits of raw sensor data After video test gen. Data must be MSB aligned
3 = Reserved

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18ED0	R/W								aexp src					Lumavar switch	Lumavar Disable		iHist disable	0x00010000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
			AEXP Histogram switch		AEXP hist disable			AWB switch	AWB disable			AF switch	AF disable		AE switch		AE 5bin hist disable	

AE 5bin hist disable
0: AEXP 5-bin histogram enabled
1: AEXP 5-bin histogram disabled

AE switch [1:0]
AE 5bin histogram tap in the pipeline. Location of AE statistic collection.
- 0 = After static white balance whose position is selected by aexp_src signal
- 1 = After WDR Frame Stitch. if its sensor companded data, then use decompanded output. If its sensor linearised data, then use it directly
- 2 = After VTPG
- 3 = reserved

AF disable
0: AF enabled
1: AF disabled

AF switch
AF tap in the pipeline. .
- 0 = After Sinter
- 1 = before Sinter

AWB disable
0: AWB enabled
1: AWB disabled

AWB switch
AWB tap in the pipeline. Location of AWB statistics collection.
- 0 = Immediately after demosaic
- 1 = Immediately after CNR

AEXP hist disable
0: AEXP 1024-bin histogram enabled
1: AEXP 1024-bin histogram disabled

AEXP Histogram switch [1:0]
AE global histogram tap in the pipeline. Location of statistics gathering for 1024 bin global histogram
- 0 = After static white balance whose position is selected by aexp_src signal
- 1 = After WDR Frame Stitch. if its sensor companded data, then use decompanded output. If its sensor linearised data, then use it directly
- 2 = After VTPG
- 3 = reserved

iHist disable
Post iridix histogram enable. Enables statistics gathering for global histogram
- 0 = Enabled
- 1 = Disabled

Lumavar Disable
- 0 = Enabled
- 1 = Disabled

Lumavar switch
Luma variance tap in the pipeline.
- 0 = Full resolution pipeline
- 1 = Downscaled pipeline

aexp_src
- 0 = After static white balance when applied before shading
- 1 = After static white balance when applied after shading

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

21.2. crossbar

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18ED4	R/W							channel4 select								channel3 select		0x03020100
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
								channel2 select								channel1 select		

channel1_select [1:0] channel0 selection from the input 4 channels
channel2_select [1:0] channel1 selection from the input 4 channels
channel3_select [1:0] channel2 selection from the input 4 channels
channel4_select [1:0] channel4 selection from the input 4 channels

21.3. video test gen ch0

Video test generator controls. See ISP Guide for further details

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18ED8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Rsvd	Generate mode	bayer rgb o sel	bayer rgb i sel	test pattern off on	

test_pattern_off on Test pattern off-on: 0=off, 1=on
bayer_rgb_i sel Bayer or rgb select for input video: 0=bayer, 1=rgb
bayer_rgb_o sel Bayer or rgb select for output video: 0=bayer, 1=rgb
Generate mode 0 = One Shot (on request) generation. 1 = free run (continuous) generation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18EDC	R/W																									pattern type								0x00000003

pattern type [7:0] Pattern type select: 0=Flat field,1=Horizontal gradient,2=Vertical Gradient,3=Vertical Bars,4=Rectangle,5-255=Default white frame on black

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18EE0	R/W													r backgnd																				0x0000FFFF

r backgnd [19:0] Red background value 16bit, MSB aligned to used width

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18EE4	R/W													g backgnd																				0x0000FFFF

g backgnd [19:0] Green background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18EE8	R/W													b backgnd																				0x0000FFFF

b backgnd [19:0] Blue background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18EEC	R/W													r foregnd																				0x00008FFF

r foregnd [19:0] Red foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18EF0	R/W													g foregnd																				0x00008FFF

g foregnd [19:0] Green foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18EF4	R/W													b foregnd																				0x00008FFF

b foregnd [19:0] Blue foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18EF8	R/W																	rgb gradient																0x00003CAA

rgb gradient [15:0] RGB gradient increment per pixel (0-15) for first channel
Format: unsigned 4.12-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18EFC	R/W													rgb gradient start																				0x00000000

rgb_gradient start [19:0] RGB gradient start value for first channel 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F00	R/W			rect bot																rect top														0x01000001

rect top [13:0] Rectangle top line number 1-n
rect bot [13:0] Rectangle bottom line number 1-n

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F04	R/W			rect right																rect left														0x01000001

rect left [13:0] Rectangle left pixel number 1-n
rect right [13:0] Rectangle right pixel number 1-n

21.4. video test gen ch1

Video test generator controls. See ISP Guide for further details

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18F08	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Rsvd	Generate mode	bayer rgb o sel	bayer rgb i sel	test pattern off on	

test_pattern_off on Test pattern off-on: 0=off, 1=on
bayer_rgb_i sel Bayer or rgb select for input video: 0=bayer, 1=rgb
bayer_rgb_o sel Bayer or rgb select for output video: 0=bayer, 1=rgb
Generate mode 0 = One Shot (on request) generation. 1 = free run (continuous) generation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F0C	R/W																									pattern type								0x00000003

pattern type [7:0] Pattern type select: 0=Flat field,1=Horizontal gradient,2=Vertical Gradient,3=Vertical Bars,4=Rectangle,5-255=Default white frame on black

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F10	R/W													r backgnd																				0x0000FFFF

r backgnd [19:0] Red background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F14	R/W													g backgnd																				0x0000FFFF

g backgnd [19:0] Green background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F18	R/W													b backgnd																				0x0000FFFF

b backgnd [19:0] Blue background value 16bit, MSB aligned to used width

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F1C	R/W													r foregnd																				0x00008FFF

r foregnd [19:0] Red foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F20	R/W													g foregnd																				0x00008FFF

g foregnd [19:0] Green foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F24	R/W													b foregnd																				0x00008FFF

b foregnd [19:0] Blue foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F28	R/W																	rgb gradient																0x00003CAA

rgb gradient [15:0] RGB gradient increment per pixel (0-15) for first channel
Format: unsigned 4.12-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F2C	R/W													rgb gradient start																				0x00000000

rgb_gradient start [19:0] RGB gradient start value for first channel 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F30	R/W			rect bot																rect top														0x01000001

rect top [13:0] Rectangle top line number 1-n
rect bot [13:0] Rectangle bottom line number 1-n

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F34	R/W			rect right																rect left														0x01000001

rect left [13:0] Rectangle left pixel number 1-n
rect right [13:0] Rectangle right pixel number 1-n

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.5. video test gen ch2

Video test generator controls. See ISP Guide for further details

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18F38	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Rsvd	Generate mode	bayer rgb o sel	bayer rgb i sel	test pattern off on	

test_pattern_off on Test pattern off-on: 0=off, 1=on
bayer_rgb_i sel Bayer or rgb select for input video: 0=bayer, 1=rgb
bayer_rgb_o sel Bayer or rgb select for output video: 0=bayer, 1=rgb
Generate mode 0 = One Shot (on request) generation. 1 = free run (continuous) generation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F3C	R/W																									pattern type								0x00000003

pattern type [7:0] Pattern type select: 0=Flat field,1=Horizontal gradient,2=Vertical Gradient,3=Vertical Bars,4=Rectangle,5-255=Default white frame on black

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F40	R/W													r backgnd																				0x0000FFFF

r backgnd [19:0] Red background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F44	R/W													g backgnd																				0x0000FFFF

g backgnd [19:0] Green background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F48	R/W													b backgnd																				0x0000FFFF

b backgnd [19:0] Blue background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F4C	R/W													r foregnd																				0x00008FFF

r foregnd [19:0] Red foreground value 16bit, MSB aligned to used width

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F50	R/W													g foregnd																				0x00008FFF

g foregnd [19:0] Green foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F54	R/W													b foregnd																				0x00008FFF

b foregnd [19:0] Blue foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F58	R/W																	rgb gradient																0x00003CAA

rgb gradient [15:0] RGB gradient increment per pixel (0-15) for first channel
Format: unsigned 4.12-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F5C	R/W													rgb gradient start																				0x00000000

rgb_gradient start [19:0] RGB gradient start value for first channel 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F60	R/W			rect bot																rect top														0x01000001

rect top [13:0] Rectangle top line number 1-n
rect bot [13:0] Rectangle bottom line number 1-n

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F64	R/W			rect right																rect left														0x01000001

rect left [13:0] Rectangle left pixel number 1-n
rect right [13:0] Rectangle right pixel number 1-n

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.6. video test gen ch3

Video test generator controls. See ISP Guide for further details

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18F68	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Rsvd	**Generate mode**	**bayer rgb o sel**	**bayer rgb i sel**	**test pattern off on**	

test_pattern_off on Test pattern off-on: 0=off, 1=on
bayer_rgb_i sel Bayer or rgb select for input video: 0=bayer, 1=rgb
bayer_rgb_o sel Bayer or rgb select for output video: 0=bayer, 1=rgb
Generate mode 0 = One Shot (on request) generation. 1 = free run (continuous) generation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F6C	R/W																									**pattern type**								0x00000003

pattern type [7:0] Pattern type select: 0=Flat field,1=Horizontal gradient,2=Vertical Gradient,3=Vertical Bars,4=Rectangle,5-255=Default white frame on black

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F70	R/W													**r backgnd**																				0x0000FFFF

r backgnd [19:0] Red background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F74	R/W													**g backgnd**																				0x0000FFFF

g backgnd [19:0] Green background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F78	R/W													**b backgnd**																				0x0000FFFF

b backgnd [19:0] Blue background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F7C	R/W													**r foregnd**																				0x00008FFF

r foregnd [19:0] Red foreground value 16bit, MSB aligned to used width

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F80	R/W													g foregnd																				0x00008FFF

g foregnd [19:0] Green foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F84	R/W													b foregnd																				0x00008FFF

b foregnd [19:0] Blue foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F88	R/W																	rgb gradient																0x00003CAA

rgb gradient [15:0] RGB gradient increment per pixel (0-15) for first channel
Format: unsigned 4.12-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F8C	R/W													rgb gradient start																				0x00000000

rgb_gradient start [19:0] RGB gradient start value for first channel 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F90	R/W			rect bot																rect top														0x01000001

rect top [13:0] Rectangle top line number 1-n
rect bot [13:0] Rectangle bottom line number 1-n

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F94	R/W			rect right																rect left														0x01000001

rect left [13:0] Rectangle left pixel number 1-n
rect right [13:0] Rectangle right pixel number 1-n

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.7. input formatter

Adapts received data format to ISP format see ISP guide for a table of setting to be used for various sensors/modes.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18F98	R/W														input bitwidth select			0x00020000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
															mode in			

mode in [2:0] Input mode
- 0 = Linear data
- 1 = 2:3 multiple exposure multiplexing
- 2 = Logarithmic encoding
- 3 = Companding curve with knee points
- 4 = 16bit linear+ 12bit VS
- 5 = 12bit companded + 12bit VS
- 6 = Reserved
- 7 = pass through mode

input bitwidth select [2:0] Input bitwidth select
- 0 = 8 bits
- 1 = 10 bits
- 2 = 12 bits
- 3 = 14 bits
- 4 = 16 bits
- 5 = 20 bits (no 18 bits)
- 6 = Reserved
- 7 = Reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18F9C	R/W															factor ML																		0x00001000

factor ML [17:0] 18 bit, 6.12 fix point - ratio between long and medium exposure for 2:3 multiplexed mode

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FA0	R/W																				factor MS													0x00001000

factor MS [12:0] 13 bit, 1.12 fix point - ratio between short and medium exposure for 2:3 multiplexed mode

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FA4	R/W																					black level												0x00000000

black level [11:0] Black level of sensor data for 2:3 multiplexed mode

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FA8	R/W	knee point1																knee point0																0x05800200

knee point0 [15:0] First knee point
knee point1 [15:0] Second knee point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FAC	R/W																	knee point2																0x00000881

knee point2 [15:0] Third knee point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18FB0	R/W					slope3 select								slope2 select				0x09060402
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						slope1 select								slope0 select				

slope0 select [3:0] First slope for companding table segments
0 = 1x
1 = 2x
2 = 4x
3 = 8x
4 = 16x
5 = 32x
6 = 64x
7 = 128x
8 = 256x
9 = 512x
10 = 1024x
11 = 2048x
12 = 4096x
13 = 8192x
14 = 16384x
15 = 32768x

slope1 select [3:0] Second slope for companding table segments (encoding is the same as slope0 select)
slope2 select [3:0] Third slope for companding table segments (encoding is the same as slope0 select)
slope3 select [3:0] Last slope for companding table segments (encoding is the same as slope0 select)

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.8. sensor offset wdr l

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FB4	R/W					offset 01																offset 00												0x00000000

offset 00 [11:0] offset offset for color channel 00 (R)
offset 01 [11:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FB8	R/W					offset 11																offset 10												0x00000000

offset 10 [11:0] offset offset for color channel 10 (Gb)
offset 11 [11:0] offset offset for color channel 11 (B)

21.9. sensor offset wdr m

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FBC	R/W					offset 01																offset 00												0x00000000

offset 00 [11:0] offset offset for color channel 00 (R)
offset 01 [11:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FC0	R/W					offset 11																offset 10												0x00000000

offset 10 [11:0] offset offset for color channel 10 (Gb)
offset 11 [11:0] offset offset for color channel 11 (B)

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.10. sensor offset wdr s

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FC4	R/W					offset 01																offset 00												0x00000000

offset 00 [11:0] offset offset for color channel 00 (R)
offset 01 [11:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FC8	R/W					offset 11																offset 10												0x00000000

offset 10 [11:0] offset offset for color channel 10 (Gb)
offset 11 [11:0] offset offset for color channel 11 (B)

21.11. sensor offset wdr vs

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FCC	R/W					offset 01																offset 00												0x00000000

offset 00 [11:0] offset offset for color channel 00 (R)
offset 01 [11:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FD0	R/W					offset 11																offset 10												0x00000000

offset 10 [11:0] offset offset for color channel 10 (Gb)
offset 11 [11:0] offset offset for color channel 11 (B)

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.12. gain wdr

Gain adjustment for the WDR stitching

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FD4	R/W				Gain m																Gain l													0x01000100

Gain_l [12:0] Gain applied to ch-long data in 5.8 format
Gain_m [12:0] Gain applied to ch-medium data in 5.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FD8	R/W				Gain vs																Gain s													0x01000100

Gain_s [12:0] Gain applied to ch-short data in 5.8 format
Gain_vs [12:0] Gain applied to ch-vs data in 5.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FDC	R/W					black level m																black level l												0x00000000

black_level_l [11:0] Sensor offset applied to ch-long data
black_level_m [11:0] Sensor offset applied to ch-medium data

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FE0	R/W					black level vs																black level s												0x00000000

black_level_s [11:0] Sensor offset applied to ch-short data
black_level_vs [11:0] Sensor offset applied to ch-veryshort data

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.13. frame stitch

4-exposure wide-dynamic-range blending

NOTE:
If the WDR is configured to stitch 2 exposures, then the configuration must be done through the LM_ pair the short exposures black level must be programmed through the med_black_level register so that the LM pair
can be used.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x18FE4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
		output select														mode in		

mode_in [1:0]
0 : 4-exposure
1 : 2-exposure
2 : 3-exposure
3 : 4-exposure

output_select [7:0]
This register is only for debug purpose. for normal operation it must be kept in its default value (0)
0 : normal stitched output
1 : long data routed out
2 : medium data routed out
4 : short data routed out
8 : very short data routed out
16: LM stitched output taken out
32: MS stitched output taken out
64: SVS stitched output taken out
others: reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FE8	R/W					MS Exposure Ratio																LM Exposure Ratio												0x01000100

LM_Exposure_Ratio [11:0]
Sets ratio between long and medium exposures - this must match the actual exposure ratio on the sensor
Format: unsigned 6.6-bit fixed-point

MS_Exposure_Ratio [11:0]
Sets ratio between medium and short exposures - this must match the actual exposure ratio on the sensor
Format: unsigned 6.6-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FEC	R/W																					SVS Exposure Ratio												0x00000100

SVS_Exposure_Ratio [11:0]
Sets ratio between short and very short exposures - this must match the actual exposure ratio on the sensor
Format: unsigned 6.6-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FF0	R/W					LM Thresh low																LM Thresh high												0x0C000F00

LM_Thresh_high [11:0] These two thresholds are for LM pairs. Both are with respect to the longer stitches. Data above this threshold will be taken from short exposure only

LM_Thresh_low [11:0] Data below this threshold will be taken from long exposure only

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FF4	R/W					MS Thresh low																MS Thresh high												0x0C000F00

MS_Thresh_high [11:0] These two thresholds are for MS pairs. Both are with respect to the longer stitches. Data above this threshold will be taken from short exposure only

MS_Thresh_low [11:0] Data below this threshold will be taken from long exposure only

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FF8	R/W					SVS Thresh low																SVS Thresh high												0x0C000F00

SVS_Thresh_high [11:0] These two thresholds are for SVS pairs. Both are with respect to the longer stitches. Data above this threshold will be taken from short exposure only

SVS_Thresh_low [11:0] Data below this threshold will be taken from long exposure only

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x18FFC	R/W					Black level Medium																Black level long												0x00000000

Black_level_long [11:0] Black level for long exposure input

Black_level_Medium [11:0] Black level for medium exposure input
*** NOTE ***:
If the wdr unit is configured to use as 2-exposure, THIS REGISTER POSITION must contain the black level of
short exposure as the LM pair is used for all other configurations

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19000	R/W					Black level very Short																Black level Short												0x00000000

Black_level_Short [11:0] Black level for short exposure input

Black_level_very_Short [11:0] Black level for very short exposure input

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19004	R/W													Black level Out																				0x00000000

Black_level_Out [19:0] Black level for module output

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19008	R/W					MS NP mult																LM NP mult												0x06000180

LM_NP_mult [11:0] The noise profile weights are multiplied by this value to give expected noise amplitude.

MS_NP_mult [11:0] The noise profile weights are multiplied by this value to give expected noise amplitude.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1900C	R/W					LM Alpha MOV slope																SVS NP mult												0x0C000600

SVS_NP_mult [11:0] The noise profile weights are multiplied by this value to give expected noise amplitude.

LM_Alpha_MOV_slope [11:0] This defines the gradient of the motion alpha ramp. Higher values mean a steeper ramp and so a more rapid transition between
non-motion-corrected and motion-corrected regions.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19010	R/W					SVS Alpha MOV slope																MS Alpha MOV slope												0x01800180

MS_Alpha_MOV_slope [11:0] his defines the gradient of the motion alpha ramp. Higher values mean a steeper ramp and so a more rapid transition between
non-motion-corrected and motion-corrected regions.

SVS_Alpha_MOV_slope [11:0] his defines the gradient of the motion alpha ramp. Higher values mean a steeper ramp and so a more rapid transition between
non-motion-corrected and motion-corrected regions.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19014	R/W					Gain B																Gain R												0x01000100

Gain_R [11:0] Multiplier for color channel R
Format: unsigned 4.8-bit fixed-point

Gain_B [11:0] Multiplier for color channel B
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19018	R/W																					Consistency thresh mov												0x00000100

Consistency_thresh_mov [11:0] Pixel consistency reporting - motion threshold
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1901C	R/W													Consistency thresh lvl																				0x00080000

Consistency_thresh_lvl [19:0] Pixel consistency reporting - flicker threshold
Format: unsigned 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x19020	R/W											lm neg weight						0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
				lm pos weight								lm noise thresh						

lm_noise_thresh [5:0] Higher values make it more likely to interpret differences between the long and medium exposures as noise (and thus do no motion correction).

lm_pos_weight [5:0] Lower values make it more likely to interpret differences between the long and medium exposures as noise (and thus do no motion correction).

lm_neg_weight [5:0] Higher values make it more likely to interpret differences between the long and medium exposures as noise (and thus do no motion correction).

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19024	R/W					lm med noise intensity thresh																lm med noise alpha thresh												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19028	R/W											lm mc blend slope																						0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1902C	R/W					lm mc blend offset																				lm mc blend thresh								0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19030	R/W											lm mc thresh slope																						0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19034	R/W													lm mc thresh thresh																				0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19038	R/W																					lm mc thresh offset												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1903C	R/W											lm mc mag thresh slope																						0x00000000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19040	R/W													lm mc mag thresh thresh																				0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19044	R/W					lm mc mag lblend thresh																lm mc mag thresh offset												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19048	R/W									Exposure mask thresh												MCoff WB offset												0x00200000

Exposure_mask_thresh [7:0] Threshold for selection of exposure mask in blending regions.
Where the alpha value is above this value the shorter exposure will be indicated.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1904C	R/W																lm alg select	0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
									mcoff mode enable						MCoff NC Enable	use 3x3 max	bwb select	

lm_alg_select Select which L/M stitching algorithm to use.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19050	R/W					MCoff M max																MCoff L max												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19054	R/W					MCoff vs max																MCoff S max												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19058	R/W					MCoff LM scaler																MCoff L scaler												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1905C	R/W					MCoff NC thresh low																MCoff LMS scaler												0x00000000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19060	R/W					MCoff NC scale																MCoff NC thresh high												0x00000000

21.14. frame stitch NP LUT VS

Noise profile for short exposure data at frame stitch

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19064	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x19068	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x190E0	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x19064 + 4 * int(i / 4).

21.15. frame stitch NP LUT S

Noise profile for med2 exposure data at frame stitch

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x190E4	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x190E8	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x19160	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x190E4 + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

21.16. frame stitch NP LUT M

Noise profile for med1 exposure data at frame stitch

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19164	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x19168	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x191E0	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x19164 + 4 * int(i / 4).

21.17. frame stitch NP LUT L

Noise profile for long exposure data at frame stitch

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x191E4	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x191E8	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x19260	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x191E4 + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.18. decompander0

Frontend lookup (for companded WDR sensor inputs)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x19264	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Offset Mode				Enable	

Enable Frontend lookup0 enable: 0=off 1=on

Offset Mode Lookup0 reflection mode for black offset region
0 = Manual curve reflection
1 = Automatic curve reflection

21.19. decompander1

Frontend lookup (for companded WDR sensor inputs)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x19268	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Offset Mode				Enable	

Enable Frontend lookup0 enable: 0=off 1=on

Offset Mode Lookup0 reflection mode for black offset region
0 = Manual curve reflection
1 = Automatic curve reflection

21.20. digital gain

Digital gain for RAW sensor data

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1926C	R/W																				Gain													0x00000100

Gain [12:0] Gain applied to data in 5.8 format

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19270	R/W													Offset																				0x00000000

Offset [19:0] Data black level

21.21. sensor offset fe

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19274	R/W													offset 00																				0x00000000

offset 00 [19:0] offset offset for color channel 00 (R)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19278	R/W													offset 01																				0x00000000

offset 01 [19:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1927C	R/W													offset 10																				0x00000000

offset 10 [19:0] offset offset for color channel 10 (Gb)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19280	R/W													offset 11																				0x00000000

offset 11 [19:0] offset offset for color channel 11 (B)

21.22. sqrt

sensor offset for the sqrt module

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19284	R/W													black level in																				0x00000000

black_level_in [19:0] input Data black level

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19288	R/W																	black level out																0x00000000

black_level_out [15:0] output Data black level

21.23. raw frontend

RAW frontend processing

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1928C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000005
										bright disable	dark disable			show dynamic defect pixel	dp enable		ge enable	

ge enable Green equalization enable: 0=off, 1=on
dp enable Dynamic Defect Pixel enable: 0=off, 1=on
show dynamic defect pixel Show Defect Pixel: 0=off, 1=on
dark disable Disable detection of dark pixels
bright disable Disable detection of bright pixels

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19290	R/W																	debug sel																0x00000000

debug sel [15:0] Debug selection port

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19294	R/W					dp threshold																dp slope												0x00400200

dp slope [11:0] Slope for HP Mask function
dp threshold [11:0] Defect pixel threshold.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19298	R/W									dp blend								dpdev threshold																0x00000266

dpdev threshold [15:0] Controls the aggressiveness of the dynamic defect pixel correction near edges.
dp blend [7:0] Controls blending between non-directional and directional replacement values in dynamic defect pixel correction.
0x00 Replace detected defects with non-directional replacement value
0xFF Replace detected defects with directional replacement value

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1929C	R/W	ge threshold																								ge strength								0x04000000

ge strength [7:0] Controls strength of Green equalization. Set during calibration.
ge threshold [15:0] green equalization threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x192A0	R/W									ge sens												ge slope												0x008000AA

ge slope [11:0] Slope for GE Mask function
ge sens [7:0] Controls the sensitivity of green equalization to edges.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x192A4	R/W	Sigma In																line thresh																0x00000150

line thresh [15:0] Controls the directional nature of the dynamic defect pixel correction near edges..
Sigma In [15:0] Manual override of noise estimation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x192A8	R/W																	Thresh Long								Thresh Short								0x00003000

Thresh Short [7:0] Noise threshold for short exposure data
Format: unsigned 4.4-bit floating-point

Thresh Long [7:0] Noise threshold for long exposure data
Format: unsigned 4.4-bit floating-point

21.24. raw frontend np

Noise profile controls for RAW frontend

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x192AC	R/W																	Exp Thresh																0x0000FFFF

Exp Thresh [15:0] Threshold for determining long/short exposure data

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x192B0	R/W																	Long Ratio								Short Ratio								0x00000420

Short Ratio [7:0] Multiplier applied to short exposure data for noise profile calculation
Format: unsigned 6.2-bit fixed-point

Long Ratio [7:0] Multiplier applied to long exposure data for noise profile calculation
Format: unsigned 6.2-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x192B4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
									NP off reflect		NP off							

NP off [6:0] Noise profile black level offset

NP off reflect Defines how values below black level are obtained.
0: Repeat the first table entry.
1: Reflect the noise profile curve below black level.

21.25. raw frontend np lut

Noise profile controls for RAW frontend

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x192B8	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x192BC	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x19334	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x192B8 + 4 * int(i / 4).

21.26. defect pixel

Detection and processing of static defect-pixels

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1933C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Detection enable	Show Static Defect Pixels	Correction Enable	Show Reference	

Show Reference For debug purposes. Show reference values which are compared with actual values to detect bad pixels
Correction Enable Correction enable: 0=off 1=on
Show Static Defect Pixels Show which pixels have been detected as bad
Detection enable Starts detection

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x19340	R/O					Table Start												--
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
					Defect Pixel Count												Overflow	

Overflow Table overflow flag
Defect Pixel Count [11:0] Number of defect-pixels detected
Table Start [11:0] Address of first defect-pixel in defect-pixel store

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19344	R/W																					Defect Pixel Count In												0x00000000

Defect Pixel Count In [11:0] Number of defect-pixels in the written table

21.27. sinter

Spatial noise reduction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x19348	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x0000001C
										rm enable	Int select	Filter select	Enable	Rsvd	Rsvd	Rsvd	Rsvd	

Enable Sinter enable: 0=off 1=on
Filter select Sinter filter fine tuning. Should not be modified from suggested values.
Int select Select intensity filter. Should not be modified from suggested values.
rm_enable Adjusts sinter strength radially from center to compensate for Lens shading correction. enable: 0=off, 1=on

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1934C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000034
										Rsvd	Rsvd	nonlinear wkgen	nlm en	int config				

int_config [3:0] Intensity blending with mosaic raw
nlm_en This config is only valid fr sinter3
Enables (1) or disables (0) the NLM filter
nonlinear_wkgen This config is only valid fr sinter3
Enables (1) or disables (0) nonlinear weight generation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19350	R/W																									sad filt thresh								0x00000009

sad_filt_thresh [7:0] Block match difference filtering threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19354	R/W	rm center y																rm center x																0x01680280

rm_center_x [15:0] Center x coordinate of shading map
rm_center_y [15:0] Center y coordinate of shading map

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19358	R/W																	rm off center mult																0x00000100

rm_off_center_mult [15:0] Normalizing factor which scales the radial table to the edge of the image.
Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1935C	R/W	Thresh 4h								Thresh 2h								Thresh 1h								Thresh 0h								0x00000000

Thresh 0h [7:0] Noise threshold for high horizontal spatial frequencies
Thresh 1h [7:0] Noise threshold for high horizontal spatial frequencies
Thresh 2h [7:0] Noise threshold for low horizontal spatial frequencies
Thresh 4h [7:0] Noise threshold for low horizontal spatial frequencies

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19360	R/W	Thresh 4v								Thresh 2v								Thresh 1v								Thresh 0v								0x00000000

Thresh 0v [7:0] Noise threshold for high vertical spatial frequencies
Thresh 1v [7:0] Noise threshold for high vertical spatial frequencies
Thresh 2v [7:0] Noise threshold for low vertical spatial frequencies
Thresh 4v [7:0] Noise threshold for low vertical spatial frequencies

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19364	R/W	Strength 4								Strength 2								Strength 1								Strength 0								0xFFFFFFFF

Strength 0 [7:0] Unused - no effect
Strength 1 [7:0] Noise reduction effect for high spatial frequencies
Strength 2 [7:0] Unused - no effect
Strength 4 [7:0] Noise reduction effect for low spatial frequencies

21.28. sinter Noise Profile

Noise profile controls for Sinter

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x19368	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000803
		global offset													Black Reflect	use exp mask	use LUT	

use LUT 1 = use LUT data
0 = use exposure mask provided by Frame stitching or threshold
use_exp_mask 1 = use exposure mask provided by Frame stitching or threshold
Black Reflect Specifies how to deal with data below black level. 0: Clip to zero, 1: Reflect.
global offset [7:0] A global offset that will be added to each of the hlog... values above..

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1936C	R/W																	Black Level																0x00000000

Black Level [15:0] Black level offset for Mode 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19370	R/W																	Thresh1																0x00004000

Thresh1 [15:0] Exposure thresholds. Used to determine which exposure generated the current pixel. Pixels with a value greater than or equal to a given threshold will be deemed to have been generated by the shorter exposure.
Pixels with a value less than a given threshold will be deemed to have been generated by the longer exposure.

E.G. Where 4 exposures are used:
VS >= Thresh 3 > S >= Thresh 2 > M >= Thresh 1 > L

For 3 exposures set Thresh 1 to 0
For 2 exposures set Thresh 1 and Thresh 2 to 0
For 1 exposures set all exposure thresholds to 0

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19374	R/W																	Thresh2																0x00008000

Thresh2 [15:0] See above.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19378	R/W																	Thresh3																0x0000C000

Thresh3 [15:0] See above.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1937C	R/W	noise level 3								noise level 2								noise level 1								noise level 0								0x00000000

noise_level_0 [7:0] Noise level of VS exposure
noise_level_1 [7:0] Noise level of S exposure
noise_level_2 [7:0] Noise level of M exposure
noise_level_3 [7:0] Noise level of L exposure

21.29. sinter Noise Profile LUT

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x19438	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1943C	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x194B4	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x19438 + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.30. sinter shading

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1A9F8	R/W	rm shading lut(3)								rm shading lut(2)								rm shading lut(1)								rm shading lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1A9FC	R/W	rm shading lut(7)								rm shading lut(6)								rm shading lut(5)								rm shading lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1AA14	R/W	rm shading lut(31)								rm shading lut(30)								rm shading lut(29)								rm shading lut(28)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1AA18	R/W																									rm shading lut(32)								--

rm_shading_lut [7:0] Radial Sinter LUT. See ISP guide for more details

This is an array of 33 8-bit registers. The address for element (i) is: 0x1A9F8 + 4 * int(i / 4).

21.31. temper

Temporal noise reduction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AA1C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																Temper2 Mode	Enable	

Enable Temper enable: 0=off 1=on

Temper2 Mode 0: 0=Temper3 mode 1=Temper2 mode

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AA24	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000202
		Delta												Recursion Limit				

Recursion Limit [3:0] Controls length of filter history. Low values result in longer history and stronger temporal filtering.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.32. temper Noise Profile

Noise profile controls for Temper

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AA28	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000803
		global offset													Black Reflect	use exp mask	use LUT	

use LUT 1 = use LUT data
0 = use exposure mask provided by Frame stitching or threshold

use_exp_mask 1 = use exposure mask provided by Frame stitching or threshold

Black Reflect Specifies how to deal with data below black level. 0: Clip to zero, 1: Reflect.

global offset [7:0] A global offset that will be added to each of the hlog... values above..

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AA2C	R/W																	Black Level																0x00000000

Black Level [15:0] Black level offset for Mode 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AA30	R/W																	Thresh1																0x00004000

Thresh1 [15:0] Exposure thresholds. Used to determine which exposure generated the current pixel. Pixels with a value greater than or equal to a given threshold will be deemed to have been generated by the shorter exposure.
Pixels with a value less than a given threshold will be deemed to have been generated by the longer exposure.

E.G. Where 4 exposures are used:
VS >= Thresh 3 > S >= Thresh 2 > M >= Thresh 1 > L

For 3 exposures set Thresh 1 to 0
For 2 exposures set Thresh 1 and Thresh 2 to 0
For 1 exposures set all exposure thresholds to 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AA34	R/W																	Thresh2																0x00008000

Thresh2 [15:0] See above.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AA38	R/W																	Thresh3																0x0000C000

Thresh3 [15:0] See above.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AA3C	R/W	noise level 3								noise level 2								noise level 1								noise level 0								0x00000000

noise_level_0 [7:0] Noise level of VS exposure
noise_level_1 [7:0] Noise level of S exposure
noise_level_2 [7:0] Noise level of M exposure
noise_level_3 [7:0] Noise level of L exposure

21.33. temper Noise Profile LUT

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AAF8	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1AAFC	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1AB74	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x1AAF8 + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.34. temper dma

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AB78	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x0000000F
							temper dw							Frame read on LSB dma	Frame read on MSB dma	Frame write on LSB dma	Frame write on MSB dma	

Frame write on MSB dma This must be set to 1 only in Temper-3 mode
Frame write on LSB dma This must be set to 1 whenever Temper (either T2 or T3 mode) is enabled
Frame read on MSB dma This must be set to 1 only in Temper-3 mode
Frame read on LSB dma This must be set to 1 whenever Temper (either T2 or T3 mode) is enabled
temper_dw 0: 16bit valid data
1: upto 12 bit valid data, MSB aligened to 16 bit

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AB7C	R/W																									format								0x00000014

format [7:0] 20: for 16bit data both in T3 and T2 modes
6 : for 12bit data both in T3 and T2 modes

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AB80	R/O	blk status																																--

blk_status [31:0]

The bits are defined as follows:
0 Write FIFO Fail (Full)
1 Write FIFO Fail (Empty)
2 Read FIFO Fail (Full)
3 Read FIFO Fail (Empty)
4 Pack Fail (Overflow)
5 Unpack Fail (Overflow)
6 Writer fail (Active Width)
7 Writer fail (Active Height)
8 Writer fail (Interline blanking)
9 Writer fail (Interframe blanking)
10 Reader fail (Active Width)
11 Reader fail (Active Height)
12 Reader fail (Interline blanking)
13 Reader fail (Interframe blanking)
14 0
15 0
16 Writer fail (A resp)
17 Writer fail (AW wait)
18 Writer fail (W wait)
19 Writer fail (Outstanding Transactions)
20 Reader fail (AR wait)
21 Reader fail (R resp)
22 Reader fail (Oustanding Transfers)
23 0
24 intw_fail_user_intfc_sig
25 intr_fail_user_intfc_sig
26 0
27 0
28 0
29 0
30 0
31 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AB84	R/W	msb bank base writer																																0x00000000

msb_bank_base_writer [31:0]

base address for frame buffer, should be word-aligned. This is used only in 16bit temper3 mode.
In 16bit temper3 mode, each 40 bit temper data (32bit data+8bit meta data) is split into 2 chunks and each
is stored in one of the buffers. The MSB part is stored into this buffer

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AB88	R/W	lsb bank base writer																																0x00000000

lsb_bank_base_writer [31:0] base address for frame buffer, should be word-aligned. This is used all the times temper is used..
In 16bit temper3 mode, each 40 bit temper data (32bit data+8bit meta data) is split into 2 chunks and each
is stored in one of the buffers. The LSB part is stored into this buffer.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AB8C	R/W	msb bank base reader																																0x00000000

msb_bank_base_reader [31:0] base address for frame buffer, should be word-aligned. This is used only in 16bit temper3 mode.
In 16bit temper3 mode, each 40 bit temper data (32bit data+8bit meta data) is split into 2 chunks and each
is stored in one of the buffers. The MSB part is stored into this buffer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AB90	R/W	lsb bank base reader																																0x00000000

lsb_bank_base_reader [31:0] base address for frame buffer, should be word-aligned. This is used all the times temper is used..
In 16bit temper3 mode, each 40 bit temper data (32bit data+8bit meta data) is split into 2 chunks and each
is stored in one of the buffers. The LSB part is stored into this buffer.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AB94	R/W	Line offset																																0x00001000

Line_offset [31:0] Indicates the offset in bytes from the start of one line to the next line.
This value should be equal to or larger than one line of image data and should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AB98	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000002
																linetick eol		

linetick_eol linetick start/end of line control. 0 = use start of line, 1 = use end of line

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABA0	R/W	linetick repeat																linetick first																0x00000040

linetick_first [15:0] line number of first linetick. 0 = no linetick

linetick_repeat [15:0] line number of first linetick. 0 = no repeat

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1ABA8	R/W				Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F007E00
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
			Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	**writer axi id multi**	**lsb writer axi id value**				**msb writer axi id value**				

msb_writer_axi_id_value [3:0] value to send for awid, wid and expected on bid.

lsb_writer_axi_id_value [3:0] value to send for awid, wid and expected on bid.

writer_axi_id_multi 0= static value (axi_id_value) for awid/wid, 1 = incrementing value per transaction for awid/wid wrapping to 0 after axi_id_value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1ABAC	R/W				Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F007E00
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
			Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd		**lsb reader axi id value**				**msb reader axi id value**				

msb_reader_axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = "0000"

lsb_reader_axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = "0000"

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.35. ca correction

Ca Correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1ABB0	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
												Mesh Scale					Enable	

Enable module enable, if 0 the data_i(dw*(kh-1)/2+dw-1 downto dw*(kh-1)/2) is presented at data_o after pipeline length

Mesh Scale [1:0] extra shift of mesh data: 00- no shift, 01- shift left by 1, ..., 11- shift left by 3, used to increase the range at cost of accuracy

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1ABB4	R/W										Mesh Height							0x00400040
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
											Mesh Width							

Mesh Width [6:0] number of tiles across. Maximum supported mesh width is 64.

Mesh Height [6:0] number of tiles vertically. Maximum supported mesh height is 64 for RGGB sensor and 42 for RGBIr sensors.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABB8	R/W				Plane Offset																Line Offset													0x00400040

Line Offset [12:0] offset between lines of tiles, can differ from mesh_width, but its safe to keep same as mesh width

Plane Offset [12:0] offset between colour planes, can differ from line_offset*mesh_height

21.36. square be

sensor offset for the square module

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABC0	R/W																	black level in																0x00000000

black_level_in [15:0] input Data black level

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABC4	R/W													black level out																				0x00000000

black_level_out [19:0] output Data black level

21.37. sensor offset pre shading

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABC8	R/W													offset 00																				0x00000000

offset 00 [19:0] offset offset for color channel 00 (R)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABCC	R/W													offset 01																				0x00000000

offset 01 [19:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABD0	R/W													offset 10																				0x00000000

offset 10 [19:0] offset offset for color channel 10 (Gb)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABD4	R/W													offset 11																				0x00000000

offset 11 [19:0] offset offset for color channel 11 (B)

21.38. radial shading

Radial Lens shading correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1ABD8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Enable	

Enable Lens shading correction enable: 0=off, 1=on

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABDC	R/W	centerR y																centerR x																0x021C03C0

centerR x [15:0] Center x coordinate of the red shading map
centerR y [15:0] Center y coordinate of the red shading map

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABE0	R/W	centerG y																centerG x																0x021C03C0

centerG x [15:0] Center x coordinate of the green shading map
centerG y [15:0] Center y coordinate of the green shading map

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABE4	R/W	centerB y																centerB x																0x021C03C0

centerB x [15:0] Center x coordinate of the blue shading map
centerB y [15:0] Center y coordinate of the blue shading map

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABE8	R/W	centerIr y																centerIr x																0x021C03C0

centerIr x [15:0] Center x coordinate of the IR shading map
centerIr y [15:0] Center y coordinate of the IR shading map

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABEC	R/W	off center multRy																off center multRx																0x06EA06EA

off center multRx [15:0] Normalizing X factor which scales the Red radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.
off center multRy [15:0] Normalizing Y factor which scales the Red radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABF0	R/W	off center multGy																off center multGx																0x06EA06EA

off center multGx [15:0] Normalizing X factor which scales the green radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.
off center multGy [15:0] Normalizing Y factor which scales the green radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABF4	R/W	off center multBy																off center multBx																0x06EA06EA

off center multBx [15:0] Normalizing X factor which scales the blue radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

off center multBy [15:0] Normalizing Y factor which scales the blue radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ABF8	R/W	off center multIRy																off center multIRx																0x06EA06EA

off center multIRx [15:0] Normalizing X factor which scales the Ir radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

off center multIRy [15:0] Normalizing Y factor which scales the Ir radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

21.39. mesh shading

Mesh Lens shading correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1ABFC	R/W			Mesh height								Mesh width						0x3F3FE406
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		Mesh page Ir		Mesh page B		Mesh page G		Mesh page R			Mesh alpha mode		Mesh scale			Mesh show	Enable	

Enable Lens shading correction enable: 0=off, 1=on

Mesh show Lens shading correction debug: 0=off, 1=on (show mesh data)

Mesh scale [2:0] Selects the precision and maximal gain range of mesh shading correction
Gain range: 00- 0..2; 01- 0..4; 02- 0..8; 03- 0..16; 04- 1..2; 05- 1..3; 06- 1..5; 07- 1..9(float)

Mesh alpha mode [1:0] Sets alpha blending between mesh shading tables.
0 = no alpha blending;
1=2 banks (odd/even bytes)
2=4 banks (one per 8 bit lane in each dword)

Mesh page R [1:0] Selects memory page for red pixels correction. See ISP guide for further details

Mesh page G [1:0] Selects memory page for green pixels correction. See ISP guide for further details

Mesh page B [1:0] Selects memory page for blue pixels correction. See ISP guide for further details

Mesh page Ir [1:0] Selects memory page for IR pixels correction. See ISP guide for further details

Mesh width [5:0] Number of horizontal nodes minus 1

Mesh height [5:0] Number of vertical nodes minus 1

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AC04	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
						Mesh alpha bank Ir			Mesh alpha bank B			Mesh alpha bank G			Mesh alpha bank R			

Mesh alpha bank R [2:0] Bank selection for R blend: 0: 0+1; 1: 1+2; 2: 2:3; 3: 3+0; 4:0+2; 5: 1+3; 6,7: reserved
Mesh alpha bank G [2:0] Bank selection for G blend: 0: 0+1; 1: 1+2; 2: 2:3; 3: 3+0; 4:0+2; 5: 1+3; 6,7: reserved:
Mesh alpha bank B [2:0] Bank selection for B blend: 0: 0+1; 1: 1+2; 2: 2:3; 3: 3+0; 4:0+2; 5: 1+3; 6,7: reserved
Mesh alpha bank Ir [2:0] Bank selection for Ir blend: 0: 0+1; 1: 1+2; 2: 2:3; 3: 3+0; 4:0+2; 5: 1+3; 6,7: reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC08	R/W	Mesh alpha Ir								Mesh alpha B								Mesh alpha G								Mesh alpha R								0x00000000

Mesh alpha R [7:0] Alpha blend coeff for R
Mesh alpha G [7:0] Alpha blend coeff for G
Mesh alpha B [7:0] Alpha blend coeff for B
Mesh alpha Ir [7:0] Alpha blend coeff for IR

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC0C	R/W																	Mesh strength																0x00001000

Mesh strength [15:0] Mesh strength in 4.12 format, e.g. 0 - no correction, 4096 - correction to match mesh data. Can be used to reduce shading correction based on AE.

21.40. white balance

Static white balance - independent gain for each color channel

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC10	R/W					Gain 01																Gain 00												0x01000100

Gain 00 [11:0] Multiplier for color channel 00 (R)
Format: unsigned 4.8-bit fixed-point
Gain 01 [11:0] Multiplier for color channel 01 (Gr)
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC14	R/W					Gain 11																Gain 10												0x01000100

Gain 10 [11:0] Multiplier for color channel 10 (Gb)
Format: unsigned 4.8-bit fixed-point
Gain 11 [11:0] Multiplier for color channel 11 (B)
Format: unsigned 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.41. white balance aexp

Static white balance - independent gain for each color channel

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC18	R/W					Gain 01																Gain 00												0x01000100

Gain 00 [11:0] Multiplier for color channel 00 (R)
Format: unsigned 4.8-bit fixed-point

Gain 01 [11:0] Multiplier for color channel 01 (Gr)
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC1C	R/W					Gain 11																Gain 10												0x01000100

Gain 10 [11:0] Multiplier for color channel 10 (Gb)
Format: unsigned 4.8-bit fixed-point

Gain 11 [11:0] Multiplier for color channel 11 (B)
Format: unsigned 4.8-bit fixed-point

21.42. iridix gain

Digital gain for RAW sensor data

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC20	R/W																					Gain												0x00000100

Gain [11:0] Gain applied to data in 4.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC24	R/W													Offset																				0x00000000

Offset [19:0] Data black level

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.43. iridix

Iridix is an adaptive, space-variant tone mapping engine.
It is used to maintain or enhance shadow detail while preserving highlights.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AC28	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00004629
		stat mult					Rsvd	Rsvd	Rsvd		postgamma pos	black level amp0		max alg type			iridix on	

iridix_on Iridix enable: 0=off 1=on
max_alg_type Max Bayer Algorithm Type.
black_level_amp0 1=Ignore Black level (set to zero) in amplificator. 0=Use Black level value.
postgamma_pos PosGamma application 0=gain 1=data

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AC2C	R/W									slope min								0x00408012
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		slope max								variance intensity				variance space				

variance_space [3:0] Sets the degree of spatial sensitivity of the algorithm(Irdx7F)
variance_intensity [3:0] Sets the degree of luminance sensitivity of the algorithm(Irdx7F)
slope_max [7:0] Restricts the maximum slope (gain) which can be generated by the adaptive algorithm
slope_min [7:0] Restricts the minimum slope (gain) which can be generated by the adaptive algorithm

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC30	R/W													black level																				0x00000000

black_level [19:0] Iridix black level. Values below this will not be affected by Iridix.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC34	R/W													white level																				0x0000FFFF

white_level [19:0] Iridix white level. Values above this will not be affected by Iridix.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC38	R/W																					collection correction												0x00000100

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AC3C	R/W							strength inroi										0x02000101
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
								rev percept control								fwd percept control		

fwd_percept_control [1:0] Iridix gamma processing select: 0=pass through 1=gamma_dl 2=sqrt 3=gamma_lut.
rev_percept_control [1:0] Iridix gamma processing select: 0=pass through 1=gamma_dl 2=sqrt 3=gamma_lut.
strength_inroi [9:0] Manual Strength value for inside of ROI

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC40	R/W																							strength outroi										0x00000200

strength_outroi [9:0] Manual Strength value for outside of ROI

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC44	R/W	roi hor end																roi hor start																0xFFFF0000

roi_hor_start [15:0] Horizontal starting point of ROI
roi_hor_end [15:0] Horizontal ending point of ROI

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC48	R/W	roi ver end																roi ver start																0xFFFF0000

roi_ver_start [15:0] Vertical starting point of ROI
roi_ver_end [15:0] Vertical ending point of ROI

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AC4C	R/W	contrast								bright pr								0xB0A00001
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						svariance											filter mux	

filter_mux Selects between Iridix8 and Iridix7, 1=Iridix8 and 0=Iridix7
svariance [3:0] Iridix8 transform sensitivity to different areas of image
bright_pr [7:0] Manual Bright_Preserve value to control Iridix core
contrast [7:0] Iridix8 contrast control parameter

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC50	R/W																	dark enh																0x00001000

dark_enh [15:0] Manual Dark_Enhance value to control Iridix core

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC54	R/W															fwd alpha																		0x00000100

fwd_alpha [17:0] alpha for gamma_dl

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC58	R/W															rev alpha																		0x00001000

rev_alpha [17:0] alpha for gamma_dl

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AC5C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																context no		

context_no [1:0] Context id of a input Frame

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC60	R/W													wb offset																				0x00000000

wb_offset [19:0] White balance offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC64	R/W					gain gr																gain r												0x01000100

gain_r [11:0] White balance gain for R
Format: unsigned 4.8-bit fixed-point

gain_gr [11:0] White balance gain for GR
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC68	R/W					gain b																gain gb												0x01000100

gain_gb [11:0] White balance gain for GB
Format: unsigned 4.8-bit fixed-point

gain_b [11:0] White balance gain for B
Format: unsigned 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AC6C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	GTm select	

GTm_select Global Tone map select : 0 : Local TM 1: Full Global TM

21.44. iridix LUT

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AC70	R/W													Asymmetry LUT(0)																				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1AC74	R/W													Asymmetry LUT(1)																				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1AD70	R/W													Asymmetry LUT(64)																				--

Asymmetry LUT [19:0] Iridix target curve.

This is an array of 65 20-bit registers. The address for element (i) is: 0x1AC70 + 4i.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AD74	R/W													GlobalTM X LUT(0)																				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1AD78	R/W													GlobalTM X LUT(1)																				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1ADF4	R/W													GlobalTM X LUT(32)																				--

This is an array of 33 20-bit registers. The address for element (i) is: 0x1AD74 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1ADF8	R/W													GlobalTM Y LUT(0)																				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1ADFC	R/W													GlobalTM Y LUT(1)																				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1AE78	R/W													GlobalTM Y LUT(32)																				--

This is an array of 33 20-bit registers. The address for element (i) is: 0x1ADF8 + 4i.

21.45. demosaic rgb

Bayer Demosaic

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AE7C	R/W	UU Slope								VA Slope								AA Slope								VH Slope								0xADAAC0C0

VH Slope [7:0] Slope of vertical/horizontal blending threshold in 4.4 logarithmic format.
High values will tend to favor one direction over the other (depending on VH Thresh) while lower values will give smoother blending.

AA Slope [7:0] Slope of angular (45/135) blending threshold in 4.4 format.
High values will tend to favor one direction over the other (depending on AA Thresh) while lower values will give smoother blending.

VA Slope [7:0] Slope of VH-AA blending threshold in 4.4 log format.
High values will tend to favor one direction over the other (depending on VA Thresh) while lower values will give smoother blending.

UU Slope [7:0] Slope of undefined blending threshold in 4.4 logarithmic format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AE80	R/W																									Sat Slope								0x0000005D

Sat Slope [7:0] Slope of saturation blending threshold in linear format 2.6

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AE84	R/W					AA Thresh																VH Thresh												0x00A00131

VH Thresh [11:0] Threshold for the range of vertical/horizontal blending
The threshold defines the difference of vertical and horizontal gradients at which the vertical gradient will
start to be taken into account in the blending (if VH Offset is set to 0).
Setting the offset not null (or the slope low) will include proportion of the vertical gradient in the blending before even the gradient difference reaches the threshold (see VH Offset for more details).

AA Thresh [11:0] Threshold for the range of angular (45/135) blending.
The threshold defines the difference of 45 and 135 gradients at which the 45 gradient will start to be taken into account in the
blending (if AA Offset is set to 0).
Setting the offset not null (or the slope low) will include proportion of the 45 gradient in the blending before
even the gradient difierence reaches the threshold (see AA Offset for more details).

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AE88	R/W					UU Thresh																VA Thresh												0x01710070

VA Thresh [11:0] Threshold for the range of VH-AA blending.
The threshold defines the difference of VH and AA gradients at which the VH gradient will start to be taken into account in the blending
(if VA Offset is set to 0). Setting the offset not null (or the slope low) will include proportion of the VH gradient
in the blending before even the gradient difference reaches the threshold (see VA Offiset for more details).

UU Thresh [11:0] Threshold for the range of undefined blending

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AE8C	R/W					lum thresh																Sat Thresh												0x00600171

Sat Thresh [11:0] Threshold for the range of saturation blending in signed 2.9 format
lum_thresh [11:0] Luminance threshold for directional sharpening

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AE90	R/W					AA Offset																VH Offset												0x08000800

VH Offset [11:0] Offset for vertical/horizontal blending threshold
AA Offset [11:0] Offset for angular (A45/A135) blending threshold.
This register has great impact on how AA Thresh is used.
Setting this register to a value offset tells the blending process to weight the 45 and 135 gradients,
at the threshold, with respectively offset/16 and 255 - (offset/16).
If AA Thresh not equals to 0, these same blending weights apply from -AA Thresh to +AA Thresh.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AE94	R/W					UU Offset																VA Offset												0x00000800

VA Offset [11:0] Offset for VH-AA blending threshold. This register has great impact on how VA Thresh is used.
Setting this register to a value offset tells the blending process to weight the VH and AA gradients,
at the threshold, with respectively offset/16 and 255 - (offset/16).
If VA Thresh not equals to 0, these same blending weights apply from -VA Thresh to +VA Thresh.

UU Offset [11:0] Offset for undefined blending threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AE9C	R/W									np offset								sharp alt ud								sharp alt d								0x00002030

sharp_alt_d [7:0] Directional sharp mask strength in signed 4.4 format
sharp_alt_ud [7:0] Non-directional sharp mask strength in signed 4.4 format
np_offset [7:0] Noise profile offset in logarithmic 4.4 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEA0	R/W																									Dmsc config								0x00000000

Dmsc config [7:0] Debug output select. Set to 0x00 for normal operation.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEA4	R/W									AC Slope												AC Thresh												0x00CF01B3

AC Thresh [11:0] Threshold for the range of AC blending in signed 2.9 format
AC Slope [7:0] Slope of AC blending threshold in linear format 2.6

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEA8	R/W									FC Alias Thresh								FC Alias Slope								FC Slope								0x00005580

FC Slope [7:0] Slope (strength) of false color correction
FC Alias Slope [7:0] Slope (strength) of false colour correction after blending with saturation value in 2.6 unsigned format
FC Alias Thresh [7:0] Threshold of false colour correction after blending with saturation valuet in in 0.8 unsigned format

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AEAC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										NP off reflect	NP off							

NP off [6:0] Noise profile black level offset

NP off reflect Defines how values below black level are obtained.
0: Repeat the first table entry.
1: Reflect the noise profile curve below black level.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEB0	R/W	sad amp								sharp alt lu								sharp alt ldu								sharp alt ld								0x10101010

sharp_alt_ld [7:0] Sharpen strength for L_Ld in unsigned 4.4 format
sharp_alt_ldu [7:0] Sharpen strength for L_Ldu in unsigned 4.4 format
sharp_alt_lu [7:0] Sharpen strength for L_Lu in unsigned 4.4 format
sad_amp [7:0] Sad amplifier in unsigned 4.4 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEB4	R/W																				min d strength													0x00001F33

min_d_strength [12:0] Min threshold for the directional L_L in signed 2's complement s.12 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEB8	R/W																				min ud strength													0x00001F48

min_ud_strength [12:0] Min threshold for the un-directional L_Lu in signed 2's complement s.12 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AEBC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	sharpen alg select	

sharpen_alg_select To select new sharp algorithm or not

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEC0	R/W									grey det thresh								lg det thresh								UU SH Slope								0x00080880

UU SH Slope [7:0] Slope of undefined blending threshold in 4.4 logarithmic format
lg_det_thresh [7:0] Level to which the green channel is considered low in which case the gradient is calculated using only the blue and red channels
grey_det_thresh [7:0] Threshold applied to the inter-channel difference for detecting grey region

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEC4	R/W					UU SH Offset																UU SH Thresh												0x00000008

UU SH Thresh [11:0] Threshold for the range of undefined blending
UU SH Offset [11:0] Offset for undefined blending threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEC8	R/W	grey det slope																lg det slope																0x10688000

lg_det_slope [15:0] Control the ramp of the linear thresholding for the low green detector
grey_det_slope [15:0] Control the ramp of the linear thresholding for the grey detector

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AECC	R/W				max ud strength																max d strength													0x03330333

max_d_strength [12:0] Max threshold for the directional L_L in signed 2's complement s1+0.12 format
max_ud_strength [12:0] Max threshold for the undirectional L_Lu in signed 2's complement s1+0.12 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AED0	R/W									luma offset low d												luma thresh low d												0x00000008

luma_thresh_low_d [11:0] Intensity values above this value will be sharpen
luma_offset_low_d [7:0] Linear threshold offset corresponding to luma_thresh_low_d

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AED4	R/W													luma slope low d																				0x00004000

luma_slope_low_d [19:0] Linear threshold slope corresponding to luma_thresh_low_d

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AED8	R/W					luma thresh high d																												0x0FA00000

luma_thresh_high_d [11:0] Intensity values below this value will be sharpen

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEDC	R/W													luma slope high d																				0x00004000

luma_slope_high_d [19:0] Linear threshold slope corresponding to luma_thresh_high_d

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEE0	R/W									luma offset low ud												luma thresh low ud												0x00000008

luma_thresh_low_ud [11:0] Intensity values above this value will be sharpen
luma_offset_low_ud [7:0] Linear threshold offset corresponding to luma_thresh_low_ud

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEE4	R/W													luma slope low ud																				0x00004000

luma_slope_low_ud [19:0] Linear threshold slope corresponding to luma_thresh_low_ud

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEE8	R/W																					luma thresh high ud												0x00000FA0

luma_thresh_high_ud [11:0] Intensity values below this value will be sharpen

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEEC	R/W													luma slope high ud																				0x00004000

luma_slope_high_ud [19:0] Linear threshold slope corresponding to luma_thresh_high_ud

21.46. demosaic rgb Noise Profile

Bayer Demosaic lookup

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AEF0	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1AEF4	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1AF6C	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT

This is an array of 128 8-bit registers. The address for element (i) is: 0x1AEF0 + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.47. demosaic rgbir

Demosaic rgbir Config

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AF70	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
															rgbir config			

rgbir_config [2:0] Debug related configurations to select out different internal signals, and normal RGBIR will be outputted by default

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AF74	R/W																					clip level												0x00000E66

clip_level [11:0] clip level

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AF78	R/W																					clip debloom												0x00000CCD

clip_debloom [11:0] clip level for debloom

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AF7C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	ir on blue row	

ir_on_blue_row to indicate that the IR is on the same line of Blue

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AF80	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	declip mode	

declip_mode Declip mode

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AF84	R/W					gain b																gain r												0x01000100

gain_r [11:0] gain for red
gain_b [11:0] gain for blue

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AF88	R/W					static gain b																static gain r												0x01000100

static_gain_r [11:0] static gain for red
static_gain_b [11:0] static gain for red

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AF8C	R/W																					static gain i												0x00000100

static_gain_i [11:0] static gain for ir

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AF90	R/W																					interpolation directionality												0x00000400

interpolation_directionality [11:0] Interpolation Directionality

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AF94	R/W																					sharp limit												0x000005C8

sharp_limit [11:0] sharp limit

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AF98	R/W																					sharp high												0x00000666

sharp_high [11:0] sharp high

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AF9C	R/W																					sharp low												0x00000032

sharp_low [11:0] sharp low

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFA0	R/W																					fc low												0x000008F2

fc_low [11:0] fc low

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFA4	R/W																					fc grad												0x000000E6

fc_grad [11:0] fc grad

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFA8	R/W					ir correct mat01																ir correct mat00												0x00000400

ir_correct_mat00 [11:0] ir correct mat 00
ir_correct_mat01 [11:0] ir correct mat 01

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFAC	R/W					ir correct mat03																ir correct mat02												0x00000000

ir_correct_mat02 [11:0] ir correct mat 02
ir_correct_mat03 [11:0] ir correct mat 03

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFB0	R/W					ir correct mat11																ir correct mat10												0x04000000

ir_correct_mat10 [11:0] ir correct mat 10
ir_correct_mat11 [11:0] ir correct mat 11

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFB4	R/W					ir correct mat13																ir correct mat12												0x00000000

ir_correct_mat12 [11:0] ir correct mat 12
ir_correct_mat13 [11:0] ir correct mat 13

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFB8	R/W					ir correct mat21																ir correct mat20												0x00000000

ir_correct_mat20 [11:0] ir correct mat 20
ir_correct_mat21 [11:0] ir correct mat 21

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFBC	R/W					ir correct mat23																ir correct mat22												0x00000400

ir_correct_mat22 [11:0] ir correct mat 22
ir_correct_mat23 [11:0] ir correct mat 23

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFC0	R/W					ir correct mat31																ir correct mat30												0x00000000

ir_correct_mat30 [11:0] ir correct mat 30
ir_correct_mat31 [11:0] ir correct mat 31

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFC4	R/W					ir correct mat33																ir correct mat32												0x04000000

ir_correct_mat32 [11:0] ir correct mat 32
ir_correct_mat33 [11:0] ir correct mat 33

21.48. pf correction

purple fringing correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1AFC8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	use color corrected rgb	

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFCC	R/W																					hue strength												0x00000200

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFD0	R/W					luma strength																sat strength												0x04000200

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFD4	R/W									saturation strength												purple strength												0x00260400

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFD8	R/W																	off center mult																0x00000F8F

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFDC	R/W	center y																center x																0x02800168

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFE0	R/W																				ccm coeff rr													0x000001CB

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFE4	R/W																				ccm coeff rg													0x000010C1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFE8	R/W																				ccm coeff rb													0x0000100A

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFEC	R/W																				ccm coeff gr													0x00001028

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFF0	R/W																				ccm coeff gg													0x0000016D

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFF4	R/W																				ccm coeff gb													0x00001045

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFF8	R/W																				ccm coeff br													0x00000012

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1AFFC	R/W																				ccm coeff bg													0x000010AC

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B000	R/W																				ccm coeff bb													0x0000019A

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B004	R/W					sad offset																sad slope												0x00000001

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B008	R/W																					sad thresh												0x00000148

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B00C	R/W					hue low offset																hue low slope												0x00000131

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B010	R/W																					hue low thresh												0x00000733

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B014	R/W					hue high offset																hue high slope												0x00000855

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B018	R/W																					hue high thresh												0x000008E1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B01C	R/W					sat low offset																sat low slope												0x00000021

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B020	R/W																					sat low thresh												0x000000A4

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B024	R/W					sat high offset																sat high slope												0x0FFF0000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B028	R/W																					sat high thresh												0x00000000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B02C	R/W					luma1 low offset																luma1 low slope												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B030	R/W																					luma1 low thresh												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B034	R/W					luma1 high offset																luma1 high slope												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B038	R/W																					luma1 high thresh												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B03C	R/W					luma2 low offset																luma2 low slope												0x00000140

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B040	R/W																					luma2 low thresh												0x000000CD

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B044	R/W					luma2 high offset																luma2 high slope												0x00000026

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B048	R/W																					luma2 high thresh												0x000001A0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B04C	R/W					hsl offset																hsl slope												0x00000024

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B050	R/W																					hsl thresh												0x00000000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B054	R/W																									debug sel								0x00000000

debug_sel [7:0]
0: normal operation
1: radial weight in 0.8 format
2: sad_mask in 0.12 format
3: hue mask in 0.12 format
4: saturation mask in 0.12 format
5: luma mask in 12.0 format
6: pf mask in 12.0 format

21.49. pf correction Shading

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B058	R/W	shading lut(3)								shading lut(2)								shading lut(1)								shading lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B05C	R/W	shading lut(7)								shading lut(6)								shading lut(5)								shading lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B074	R/W	shading lut(31)								shading lut(30)								shading lut(29)								shading lut(28)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B078	R/W																									shading lut(32)								--

shading_lut [7:0] Radial Purple Fringe Correction LUT.

This is an array of 33 8-bit registers. The address for element (i) is: 0x1B058 + 4 * int(i / 4).

21.50. ccm

Color correction on RGB data using a 3x3 color matrix

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B07C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	Enable	

Enable Color matrix enable: 0=off 1=on

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B080	R/W																				Coefft R-R													0x00000100

Coefft R-R [12:0] Matrix coefficient for red-red multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B084	R/W																				Coefft R-G													0x00000000

Coefft R-G [12:0] Matrix coefficient for red-green multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B088	R/W																				Coefft R-B													0x00000000

Coefft R-B [12:0] Matrix coefficient for red-blue multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B08C	R/W																				Coefft R-IR													0x00000000

Coefft R-IR [12:0] Matrix coefficient for red-ir multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B090	R/W																				Coefft G-R													0x00000000

Coefft G-R [12:0] Matrix coefficient for green-red multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B094	R/W																				Coefft G-G													0x00000100

Coefft G-G [12:0] Matrix coefficient for green-green multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B098	R/W																				Coefft G-B													0x00000000

Coefft G-B [12:0] Matrix coefficient for green-blue multiplier
Format: sign/magnitude 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B09C	R/W																				Coefft G-IR													0x00000000

Coefft G-IR [12:0] Matrix coefficient for green-ir multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0A0	R/W																				Coefft B-R													0x00000000

Coefft B-R [12:0] Matrix coefficient for blue-red multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0A4	R/W																				Coefft B-G													0x00000000

Coefft B-G [12:0] Matrix coefficient for blue-green multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0A8	R/W																				Coefft B-B													0x00000100

Coefft B-B [12:0] Matrix coefficient for blue-blue multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0AC	R/W																				Coefft B-IR													0x00000100

Coefft B-IR [12:0] Matrix coefficient for blue-ir multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0B0	R/W																					Coefft WB R												0x00000100

Coefft WB R [11:0] gain for Red channel for antifog function
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0B4	R/W																					Coefft WB G												0x00000100

Coefft WB G [11:0] gain for Green channel for antifog function
Format: sign/magnitude 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0B8	R/W																					Coefft WB B												0x00000100

Coefft WB B [11:0] gain for Blue channel for antifog function
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0BC	R/W																					Coefft WB IR												0x00000100

Coefft WB IR [11:0] gain for IR channel for antifog function
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0C0	R/W																					Coefft fog offset R												0x00000000

Coefft fog offset R [11:0] Offset R for antifog function
Format: unsigned 12-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0C4	R/W																					Coefft fog offset G												0x00000000

Coefft fog offset G [11:0] Offset G for antifog function
Format: unsigned 12-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0C8	R/W																					Coefft fog offset B												0x00000000

Coefft fog offset B [11:0] Offset B for antifog function
Format: unsigned 12-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0CC	R/W																					Coefft fog offset IR												0x00000000

Coefft fog offset IR [11:0] Offset Ir for antifog function
Format: unsigned 12-bit integer

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.51. cnr

Colour Noise Reduction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B0D0	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	square root enable	

square_root_enable pre-CNR square root and the post-CNR square modules enable condition enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B0D4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	enable	

enable CNR enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0D8	R/W																	debug reg																0x00000000

debug_reg [15:0] CNR Debug: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0DC	R/W																									mode								0x00000000

mode [7:0] CNR enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0E0	R/W																					delta factor												0x00000277

delta_factor [11:0] CNR enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B0E4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x0000003F
											effective kernel							

effective_kernel [6:0] Effective kernel

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0E8	R/W																					u center												0x00000200

u_center [11:0] Coordinates of u center

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0EC	R/W																					v center												0x00000200

v_center [11:0] Coordinates of v center

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0F0	R/W																					global offset												0x00000332

global_offset [11:0] umean1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0F4	R/W																	global slope																0x000000CD

global_slope [15:0] umean1 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0F8	R/W																					uv seg1 threshold												0x00000000

uv_seg1_threshold [11:0] uv_seg1 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B0FC	R/W																					uv seg1 offset												0x000000AE

uv_seg1_offset [11:0] uv_seg1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B100	R/W																	uv seg1 slope																0x0000FBD8

uv_seg1_slope [15:0] uv_seg1 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B104	R/W																					umean1 threshold												0x00000000

umean1_threshold [11:0] umean1 threshold

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B108	R/W																					umean1 offset												0x0000003E

umean1_offset [11:0] umean1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B10C	R/W																	umean1 slope																0x0000E7B4

umean1_slope [15:0] umean1 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B110	R/W																					umean2 threshold												0x00000000

umean2_threshold [11:0] umean2 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B114	R/W																					umean2 offset												0x0000003E

umean2_offset [11:0] umean2 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B118	R/W																	umean2 slope																0x0000E7B4

umean2_slope [15:0] umean2 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B11C	R/W																					vmean1 threshold												0x00000000

vmean1_threshold [11:0] vmean1 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B120	R/W																					vmean1 offset												0x0000003E

vmean1_offset [11:0] vmean1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B124	R/W																	vmean1 slope																0x0000E7B4

vmean1_slope [15:0] vmean1 slope

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B128	R/W																					vmean2 threshold												0x00000000

vmean2_threshold [11:0] vmean2 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B12C	R/W																					vmean2 offset												0x0000003E

vmean2_offset [11:0] vmean2 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B130	R/W																	vmean2 slope																0x0000E7B4

vmean2_slope [15:0] vmean2 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B134	R/W																					uv var1 threshold												0x00000000

uv_var1_threshold [11:0] uv_var1 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B138	R/W																					uv var1 offset												0x000003FF

uv_var1_offset [11:0] uv_var1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B13C	R/W																	uv var1 slope																0x0000FFFF

uv_var1_slope [15:0] uv_var2 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B140	R/W																					uv var2 threshold												0x00000000

uv_var2_threshold [11:0] uv_var2 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B144	R/W																					uv var2 offset												0x000003FF

uv_var2_offset [11:0] uv_var2 offset

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B148	R/W																	uv var2 slope																0x0000FFFF

uv_var2_slope [15:0] uv_var2 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B14C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00001010
				uv var2 scale								uv var1 scale						

uv_var1_scale [5:0] uv_var1 scale
uv_var2_scale [5:0] uv_var2 scale

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B150	R/W																					uv delta1 threshold												0x00000000

uv_delta1_threshold [11:0] uv_delta1 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B154	R/W																					uv delta1 offset												0x000000B9

uv_delta1_offset [11:0] uv_delta1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B158	R/W																	uv delta1 slope																0x00000600

uv_delta1_slope [15:0] uv_delta1 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B15C	R/W																					uv delta2 threshold												0x00000000

uv_delta2_threshold [11:0] uv_delta2 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B160	R/W																					uv delta2 offset												0x000000B9

uv_delta2_offset [11:0] uv_delta2 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B164	R/W																	uv delta2 slope																0x00000600

uv_delta2_slope [15:0] uv_delta2 slope

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B168	R/O	Statusb																Statusa																--

Statusa [15:0] CNR Debug Port
Statusb [15:0] CNR Debug Port

21.52. nonequ gamma

nonequ_gamma module

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B16C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	srgb lut enable	

srgb_lut_enable enables gamma sRGB

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B170	R/W																			srgb lut coeff LUT(0)														--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B174	R/W																			srgb lut coeff LUT(1)														--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B178	R/W																			srgb lut coeff LUT(2)														--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B17C	R/W																			srgb lut coeff LUT(3)														--
... repeated until ...																																		
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B268	R/W																			srgb lut coeff LUT(62)														--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B26C	R/W																			srgb lut coeff LUT(63)														--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B270	R/W																			srgb lut coeff LUT(64)														--

srgb_lut_coeff LUT [13:0] Color space (HDR Linear to sRGB) LUT

This is an array of 65 14-bit registers. The address for element (i) is: 0x1B170 + 4i.

21.53. lumvar

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B274	R/W	active height																active width																0x04380780

active_width [15:0] Active width. This depends on the position of the luma variance module. if this module is connected to the
full resolution pipeline, then the active_width should be the full resolution frame width.
if its in the downscaled pipeline, then the active_width should be the post-scaler width

active_height [15:0] Active height. This depends on the position of the luma variance module. if this module is connected to the
full resolution pipeline, then the active_height should be the full resolution frame height.
if its in the downscaled pipeline, then the active_height should be the post-scaler height

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.54. metering aexp

Derives information for use by the AE and AWB modules

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B278	R/W																					Hist Thresh 0 1												0x00000010

Hist Thresh 0 1 [11:0] Histogram threshold for bin 0/1 boundary

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B27C	R/W																					Hist Thresh 1 2												0x00000020

Hist Thresh 1 2 [11:0] Histogram threshold for bin 1/2 boundary

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B280	R/W																					Hist Thresh 3 4												0x000000D0

Hist Thresh 3 4 [11:0] Histogram threshold for bin 2/3 boundary

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B284	R/W																					Hist Thresh 4 5												0x000000E0

Hist Thresh 4 5 [11:0] Histogram threshold for bin 3/4 boundary

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B288	R/O																	Hist 0																--

Hist 0 [15:0] Normalized histogram results for bin 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B28C	R/O																	Hist 1																--

Hist 1 [15:0] Normalized histogram results for bin 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B290	R/O																	Hist 3																--

Hist 3 [15:0] Normalized histogram results for bin 3

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B294	R/O																	Hist 4																--

Hist 4 [15:0] Normalized histogram results for bin 4

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B298	R/W																	Nodes Used Vert								Nodes Used Horiz								0x00001517

Nodes Used Horiz [7:0] Number of active zones horizontally for AE stats collection
Nodes Used Vert [7:0] Number of active zones vertically for AE stats collection

21.55. metering awb

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B29C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	stats mode	

stats mode Statistics mode: 0 - legacy(G/R,B/R), 1 - current (R/G, B/G)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2A0	R/W																							White Level AWB										0x000003FF

White Level AWB [9:0] Upper limit of valid data for AWB

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2A4	R/W																							Black Level AWB										0x00000000

Black Level AWB [9:0] Lower limit of valid data for AWB

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2A8	R/W																					Cr Ref Max AWB												0x000001FF

Cr Ref Max AWB [11:0] Maximum value of R/G for white region
Format: unsigned 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2AC	R/W																					Cr Ref Min AWB												0x00000040

Cr Ref Min AWB [11:0] Minimum value of R/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2B0	R/W																					Cb Ref Max AWB												0x000001FF

Cb Ref Max AWB [11:0] Maximum value of B/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2B4	R/W																					Cb Ref Min AWB												0x00000040

Cb Ref Min AWB [11:0] Minimum value of B/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2B8	R/O																					RG												--

RG [11:0] AWB statistics R/G color ratio output
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2BC	R/O																					BG												--

BG [11:0] AWB statistics B/G color ratio output
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2C0	R/O	SUM																																--

SUM [31:0] AWB output population. Number of pixels used for AWB statistics
Format: unsigned 32-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2C4	R/W																	Nodes Used Vert								Nodes Used Horiz								0x00000F0F

Nodes Used Horiz [7:0] Number of active zones horizontally for AWB stats
Nodes Used Vert [7:0] Number of active zones vertically for AWB stats

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2C8	R/W																					Cr Ref High AWB												0x00000FFF

Cr Ref High AWB [11:0] Maximum value of R/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2CC	R/W																					Cr Ref Low AWB												0x00000000

Cr Ref Low AWB [11:0] Minimum value of R/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2D0	R/W																					Cb Ref High AWB												0x00000FFF

Cb Ref High AWB [11:0] Maximum value of B/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2D4	R/W																					Cb Ref Low AWB												0x00000000

Cb Ref Low AWB [11:0] Minimum value of B/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B2DC	R/W					Zones Weight(3)								Zones Weight(2)								Zones Weight(1)								Zones Weight(0)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B2E0	R/W					Zones Weight(7)								Zones Weight(6)								Zones Weight(5)								Zones Weight(4)				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B718	R/W					Zones Weight(1087)								Zones Weight(1086)								Zones Weight(1085)								Zones Weight(1084)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B71C	R/W																													Zones Weight(1088)				--

Zones Weight [3:0] Sets zone weighting for auto white balance. Index is (row,col) where (0,0) is top-left zone
This is an array of 1089 4-bit registers. The address for element (i) is: 0x1B2DC + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

21.56. metering af

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B720	R/W																	Nodes Used Vert								Nodes Used Horiz								0x00000F0F

Nodes Used Horiz [7:0] Number of active zones horizontally for AF stats
Nodes Used Vert [7:0] Number of active zones vertically for AF stats

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B728	R/W	Active Height																Active Width																0x04380780

Active Width [15:0] Active video width for AF module
Active Height [15:0] Active video height for AF module

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B72C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																kernel select		

kernel select [1:0] Size of Narrow AF Kernel
0 = 3x3
1 = 7x3
2 = 11x3
3 = 15x3

21.57. metering hist aexp

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B730	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										offset y	skip y			offset x	skip x			

skip x [2:0] Histogram decimation in horizontal direction: 0=every 2nd pixel; 1=every 3rd pixel; 2=every 4th pixel; 3=every 5th pixel; 4=every 8th pixel ; 5+=every 9th pixel
offset x 0= start from the first column; 1=start from second column
skip y [2:0] Histogram decimation in vertical direction: 0=every pixel; 1=every 2nd pixel; 2=every 3rd pixel; 3=every 4th pixel; 4=every 5th pixel; 5=every 8th pixel ; 6+=every 9th pixel
offset y 0= start from the first row; 1= start from second row

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B734	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										scale top				scale bottom				

scale bottom [3:0] scale of bottom half of the range: 0=1x ,1=2x, 2=4x, 4=8x, 4=16x
scale top [3:0] scale of top half of the range: 0=1x ,1=2x, 2=4x, 4=8x, 4=16x

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B738	R/O	Total Pixels																																--

Total Pixels [31:0] Total number of pixels processed (skip x and skip y are taken into account)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B73C	R/O	Counted Pixels																																--

Counted Pixels [31:0] Number of pixels accumulated (with nonzero weight)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1B740	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
															Plane mode			

Plane mode [2:0] Plane separation mode
0 = Collect all the planes in one histogram
1 = Collect 4 Bayer planes into 4 separate banks
2 = Reserved
3 = Reserved
4 = Collect odd x odd y plane to bank 0, rest to bank 1
5 = Collect even x odd y plane to bank 0, rest to bank 1
6 = Collect odd x even y plane to bank 0, rest to bank 1
7 = Collect even x even y plane to bank 0, rest to bank 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B744	R/O	Plane Total 0																																--

Plane Total 0 [31:0] Total pixels processed for plane 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B748	R/O	Plane Total 1																																--

Plane Total 1 [31:0] Total pixels processed for plane 1

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B74C	R/O	Plane Total 2																																--

Plane Total 2 [31:0] Total pixels processed for plane 2

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B750	R/O	Plane Total 3																																--

Plane Total 3 [31:0] Total pixels processed for plane 3

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B754	R/O	Plane Counted 0																																--

Plane Counted 0 [31:0] Total pixels accumulated for plane 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B758	R/O	Plane Counted 1																																--

Plane Counted 1 [31:0] Total pixels accumulated for plane 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B75C	R/O	Plane Counted 2																																--

Plane Counted 2 [31:0] Total pixels accumulated for plane 2

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B760	R/O	Plane Counted 3																																--

Plane Counted 3 [31:0] Total pixels accumulated for plane 3

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B764	R/W																	Nodes Used Vert								Nodes Used Horiz								0x00000F0F

Nodes Used Horiz [7:0] Number of active zones horizontally for Histogram
Nodes Used Vert [7:0] Number of active zones vertically for Histogram

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1B768	R/W					Zones Weight(3)								Zones Weight(2)								Zones Weight(1)								Zones Weight(0)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1B76C	R/W					Zones Weight(7)								Zones Weight(6)								Zones Weight(5)								Zones Weight(4)				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1BBA4	R/W					Zones Weight(1087)								Zones Weight(1086)								Zones Weight(1085)								Zones Weight(1084)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1BBA8	R/W																													Zones Weight(1088)				--

Zones Weight [3:0] Sets zone weighting for Histogram. Index is (row,col) where (0,0) is top-left zone

This is an array of 1089 4-bit registers. The address for element (i) is: 0x1B768 + 4 * int(i / 4).

21.58. metering ihist

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1BBAC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										offset y	skip y			offset x	skip x			

skip x [2:0] Histogram decimation in horizontal direction: 0=every 2nd pixel; 1=every 3rd pixel; 2=every 4th pixel; 3=every 5th pixel; 4=every 8th pixel ; 5+=every 9th pixel

offset x 0= start from the first column; 1=start from second column

skip y [2:0] Histogram decimation in vertical direction: 0=every pixel; 1=every 2nd pixel; 2=every 3rd pixel; 3=every 4th pixel; 4=every 5th pixel; 5=every 8th pixel ; 6+=every 9th pixel

offset y 0= start from the first row; 1= start from second row

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1BBB0	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										scale top				scale bottom				

scale bottom [3:0] scale of bottom half of the range: 0=1x ,1=2x, 2=4x, 4=8x, 4=16x

scale top [3:0] scale of top half of the range: 0=1x ,1=2x, 2=4x, 4=8x, 4=16x

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBB4	R/O	Total Pixels																																--

Total Pixels [31:0] Total number of pixels processed (skip x and skip y are taken into account)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBB8	R/O	Counted Pixels																																--

Counted Pixels [31:0] Number of pixels accumulated (with nonzero weight)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1BBBC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
															Plane mode			

Plane mode [2:0] Plane separation mode

0 = Collect all the planes in one histogram
1 = Collect 4 Bayer planes into 4 separate banks
2 = Reserved
3 = Reserved
4 = Collect odd x odd y plane to bank 0, rest to bank 1
5 = Collect even x odd y plane to bank 0, rest to bank 1
6 = Collect odd x even y plane to bank 0, rest to bank 1
7 = Collect even x even y plane to bank 0, rest to bank 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBC0	R/O	Plane Total 0																																--

Plane Total 0 [31:0] Total pixels processed for plane 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBC4	R/O	Plane Total 1																																--

Plane Total 1 [31:0] Total pixels processed for plane 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBC8	R/O	Plane Total 2																																--

Plane Total 2 [31:0] Total pixels processed for plane 2

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBCC	R/O	Plane Total 3																																--

Plane Total 3 [31:0] Total pixels processed for plane 3

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBD0	R/O	Plane Counted 0																																--

Plane Counted 0 [31:0] Total pixels accumulated for plane 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBD4	R/O	Plane Counted 1																																--

Plane Counted 1 [31:0] Total pixels accumulated for plane 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBD8	R/O	Plane Counted 2																																--

Plane Counted 2 [31:0] Total pixels accumulated for plane 2

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBDC	R/O	Plane Counted 3																																--

Plane Counted 3 [31:0] Total pixels accumulated for plane 3

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBE0	R/W																	Nodes Used Vert								Nodes Used Horiz								0x00000F0F

Nodes Used Horiz [7:0] Number of active zones horizontally for Histogram
Nodes Used Vert [7:0] Number of active zones vertically for Histogram

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1BBE4	R/W					Zones Weight(3)								Zones Weight(2)								Zones Weight(1)								Zones Weight(0)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1BBE8	R/W					Zones Weight(7)								Zones Weight(6)								Zones Weight(5)								Zones Weight(4)				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1C020	R/W					Zones Weight(1087)								Zones Weight(1086)								Zones Weight(1085)								Zones Weight(1084)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1C024	R/W																													Zones Weight(1088)				--

Zones Weight [3:0] Sets zone weighting for Histogram. Index is (row,col) where (0,0) is top-left zone

This is an array of 1089 4-bit registers. The address for element (i) is: 0x1BBE4 + 4 * int(i / 4).

21.59. fr crop

Crop for full resolution output

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C028	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Enable crop	

Enable crop Crop enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C02C	R/W																	start x																0x00000000

start x [15:0] Horizontal offset from left side of image in pixels for output crop window

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C030	R/W																	start y																0x00000000

start y [15:0] Vertical offset from top of image in lines for output crop window

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C034	R/W																	size x																0x0000FFFF

size x [15:0] width of output crop window

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C038	R/W																	size y																0x0000FFFF

size y [15:0] height of output crop window

21.60. fr gamma rgb

Gamma correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C064	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	Enable	

Enable Gamma enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C068	R/W					gain g																gain r												0x01000100

gain_r [11:0] gain applied to the R chanel in 4.8 format
gain_g [11:0] gain applied to the G chanel in 4.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C06C	R/W																					gain b												0x00000100

gain_b [11:0] gain applied to the B chanel in 4.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C070	R/W					offset g																offset r												0x00000000

offset_r [11:0] Offset subtracted from the R chanel
offset_g [11:0] Offset subtracted from the G chanel

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C074	R/W																					offset b												0x00000000

offset_b [11:0] Offset subtracted from the B chanel

21.61. fr sharpen

Sharpen
Luma transform red coefficient. u0.8
Luma transform blue coefficient. u0.8

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C078	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Enable	

Enable Sharpening enable: 0=off, 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C07C	R/W																									Strength								0x00000010

Strength [8:0] Controls strength of sharpening effect. u5.4

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C080	R/W									Alpha Undershoot								Control B								Control R								0x00131E4C

Alpha Undershoot [7:0] Alpha blending of undershoot and overshoot u0.7, 0 = only unsershoot, 255 = only overshoot

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C084	R/W									Luma Offset Low														Luma Thresh Low										0x00000000

Luma Thresh Low [9:0] Luma threshold below this value, no sharpening will be applied.
Luma Offset Low [7:0] Luma offset (min value) of thre region of less than Luma Thresh Low.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C088	R/W							Luma Thresh High										Luma Slope Low																0x033203FC

Luma Slope Low [15:0] Luma linear threshold slope at dark luminance region
Luma Thresh High [9:0] Luma threshold above this value, sharpening level will be dicreased.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C08C	R/W	Luma Slope High																								Luma Offset High								0x06A40000

Luma Offset High [7:0] Luma offset (min value) of thre region of more than Luma Thresh High.
Luma Slope High [15:0] Luma linear threshold slope at bright luminance region

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C090	R/W			Clip Str Min																Clip Str Max														0x00CD3FFF

Clip Str Max [13:0] clips sharpening mask of max value. This will control overshoot. U0.14. (0 ~ 16383)
Clip Str Min [13:0] clips sharpening mask of min value. This will control undershoot. U0.14. It is used as negative value. (0 ~ -16383)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C094	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Debug				

Debug [3:0] To support different debug output. 0 = normal operation, 1 = luma, 2 = sharpening mask

21.62. fr cs conv

Conversion of RGB to YUV data using a 3x3 color matrix plus offsets

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C098	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Enable vertical downsample	Enable horizontal downsample	Enable filter	Enable matrix	

Enable matrix Color matrix enable: 0=off 1=on
Enable filter Filter enable: 0=off 1=on
Enable horizontal downsample Horizontal Downsampling Enable: 0=off 1=on
Enable vertical downsample Vertical Downsampling Enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C09C	R/W																	Coefft 11																0x0000002F

Coefft 11 [15:0] Matrix coefficient for R-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0A0	R/W																	Coefft 12																0x0000009D

Coefft 12 [15:0] Matrix coefficient for G-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0A4	R/W																	Coefft 13																0x00000010

Coefft 13 [15:0] Matrix coefficient for B-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0A8	R/W																	Coefft 21																0x0000801A

Coefft 21 [15:0] Matrix coefficient for R-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0AC	R/W																	Coefft 22																0x00008057

Coefft 22 [15:0] Matrix coefficient for G-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0B0	R/W																	Coefft 23																0x00000070

Coefft 23 [15:0] Matrix coefficient for B-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0B4	R/W																	Coefft 31																0x00000070

Coefft 31 [15:0] Matrix coefficient for R-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0B8	R/W																	Coefft 32																0x00008066

Coefft 32 [15:0] Matrix coefficient for G-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0BC	R/W																	Coefft 33																0x0000800A

Coefft 33 [15:0] Matrix coefficient for B-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0C0	R/W																						Coefft o1											0x00000000

Coefft o1 [10:0] Offset for Y
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0C4	R/W																						Coefft o2											0x00000200

Coefft o2 [10:0] Offset for Cb
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0C8	R/W																						Coefft o3											0x00000200

Coefft o3 [10:0] Offset for Cr
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0CC	R/W																							Clip min Y										0x00000000

Clip min Y [9:0] Minimal value for Y. Values below this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0D0	R/W																							Clip max Y										0x000003FF

Clip max Y [9:0] Maximal value for Y. Values above this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0D4	R/W																							Clip min UV										0x00000000

Clip min UV [9:0] Minimal value for Cb, Cr. Values below this are clipped.
Format: signed (2's complement) 10-bit integer

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0D8	R/W																							Clip max UV										0x000003FF

Clip max UV [9:0] Maximal value for Cb, Cr. Values above this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0DC	R/W																							Data mask RY										0x000003FF

Data mask RY [9:0] Data mask for channel 1 (R or Y). Bit-wise and of this value and video data.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0E0	R/W																							Data mask GU										0x000003FF

Data mask GU [9:0] Data mask for channel 2 (G or U). Bit-wise and of this value and video data.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0E4	R/W																							Data mask BV										0x000003FF

Data mask BV [9:0] Data mask for channel 3 (B or V). Bit-wise and of this value and video data.

21.63. fr cs conv dither

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C0E8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Shift mode		Dither amount		Enable dither	

Enable dither Enables dithering module
Dither amount [1:0] 0= dither to 9 bits; 1=dither to 8 bits; 2=dither to 7 bits; 3=dither to 6 bits
Shift mode 0= output is LSB aligned; 1=output is MSB aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.64. fr dma writer

DMA writer controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C0EC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
						axi xact comp		frame write on	Rsvd	Plane select		Rsvd	Base mode					

Base mode [4:0] Base DMA packing mode for RGB/RAW/YUV etc (see ISP guide)

Plane select [1:0] Plane select for planar base modes. Only used if planar outputs required. Not used. Should be set to 0

frame write on 0 = no frames written(when switched from 1, current frame completes writing before stopping),
1= write frame(s) (write single or continous frame(s))

axi xact comp 0 = dont wait for axi transaction completion at end of frame(just all transfers accepted). 1 = wait for all transactions completed

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0F0	R/W	active height																active width																0x04380780

active width [15:0] Active video width in pixels 128-8000

active height [15:0] Active video height in lines 128-8000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0F4	R/W	bank0 base																																0x00000000

bank0_base [31:0] bank 0 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0F8	R/W	bank1 base																																0x00000000

bank1_base [31:0] bank 1 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C0FC	R/W	bank2 base																																0x00000000

bank2_base [31:0] bank 2 base address for frame buffer, should be word-aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C100	R/W	bank3 base																																0x00000000

bank3_base [31:0] bank 3 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C104	R/W	bank4 base																																0x00000000

bank4_base [31:0] bank 4 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C108	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Rsvd	max bank			

max bank [2:0] highest bank*_base to use for frame writes before recycling to bank0_base, only 0 to 4 are valid

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C10C	R/W	Line offset																																0x00001000

Line_offset [31:0] Indicates the offset in bytes from the start of one line to the next line.
This value should be equal to or larger than one line of image data and should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C110	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
														wbank curr			wbank active	

wbank active 1 = wbank_curr is being written to. Goes high at start of writes, low at last write transfer/completion on axi.

wbank curr [2:0] write bank currently active. valid values =0-4. updated at start of frame write

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C11C	R/O	frame wcount																frame icount																--

frame icount [15:0] count of incomming frames (starts) to vdma_writer on video input, non resetable, rolls over, updates at pixel 1 of new frame on video in

frame wcount [15:0] count of outgoing frame writes (starts) from vdma_writer sent to AXI output, non resetable, rolls over, updates at pixel 1 of new frame on video in

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x1C124	R/O	23	22	21	20	19	18	17	16	--
		15	14	13	12	11	10	9	8	
									video alarm	
		7	6	5	4	3	2	1	0	
		vi fail interframe blanks	**vi fail interline blanks**	**vi fail active height**	**vi fail active width**	**axi fail wxact ostand**	**axi fail wmaxwait**	**axi fail awmaxwait**	**axi fail bresp**	

axi_fail_bresp	clearable alarm, high to indicate bad bresp captured
axi_fail_awmaxwait	clearable alarm, high when awmaxwait_limit reached
axi_fail_wmaxwait	clearable alarm, high when wmaxwait_limit reached
axi_fail_wxact_ostand	clearable alarm, high when wxact_ostand_limit reached
vi_fail_active_width	clearable alarm, high to indicate mismatched active_width detected
vi_fail_active_height	clearable alarm, high to indicate mismatched active_height detected (also raised on missing field!)
vi_fail_interline_blanks	clearable alarm, high to indicate interline blanking below min
vi_fail_interframe_blanks	clearable alarm, high to indicate interframe blanking below min
video_alarm	active high, problem found on video port(s) (active width/height or interline/frame blanks failure)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C128	R/O	**blk status**																																--

blk_status [31:0] block status output (reserved)
-- blk_status(0) = wfifo_fail_full
-- blk_status(1) = wfifo_fail_empty
-- blk_status(4) = pack_fail_overflow
-- blk_status(24) = intw_fail_user_intfc_sig
-- blk_status(others) = zero

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C12C	R/W																	**lines wrapped**																0x00000000

lines_wrapped [15:0] Number of lines to write from base address before wrapping back to base address. 0 = no wrapping, >0 = last line written before wrapping

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C130	R/W																	**linetick first**																0x00000000

linetick_first [15:0] Line number of first linetick. 0 = no linetick, >0 = line number to generate linetick

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C134	R/W																	linetick repeat																0x00000000

linetick_repeat [15:0] Line repeat interval of linetick. 0 = no repeat, >0 = repeat interval in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C138	R/W	linetick delay																0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																	linetick eol	

linetick_eol Linetick start/end of line control. 0 = use start of line, 1 = use end of line to generate linetick

linetick_delay [15:0] Linetick delay in vcke cycles to add to min 3 cycle latency from acl_vi. 0-65535.
Must be less than next linetick generation time or count will not mature and no linetick is not produced.
--NOTE: linetick delay can run past end of frame/field and also into next frame!
-- Take care maturity time is less than next configured linetick generation postion!
-- Take care when changing config between frame too!

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C13C	R/W					Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F000F0C
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						Rsvd	Rsvd	Rsvd	Rsvd					Rsvd	Rsvd	axi id multi	Rsvd	

axi_id_multi 0= static value (axi_id_value) for awid/wid, 1 = incrementing value per transaction for awid/wid wrapping to 0 after axi_id_value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C140	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														axi id value				

axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = 0000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.65. fr uv dma writer

DMA writer controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C144	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
						axi xact comp		frame write on	Rsvd	Plane select		Rsvd	Base mode					

Base mode [4:0] Base DMA packing mode for RGB/RAW/YUV etc (see ISP guide)

Plane select [1:0] Plane select for planar base modes. Only used if planar outputs required. Not used. Should be set to 0

frame write on 0 = no frames written(when switched from 1, current frame completes writing before stopping),
1= write frame(s) (write single or continous frame(s))

axi xact comp 0 = dont wait for axi transaction completion at end of frame(just all transfers accepted). 1 = wait for all transactions completed

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C148	R/W	active height																active width																0x04380780

active width [15:0] Active video width in pixels 128-8000

active height [15:0] Active video height in lines 128-8000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C14C	R/W	bank0 base																																0x00000000

bank0_base [31:0] bank 0 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C150	R/W	bank1 base																																0x00000000

bank1_base [31:0] bank 1 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C154	R/W	bank2 base																																0x00000000

bank2_base [31:0] bank 2 base address for frame buffer, should be word-aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C158	R/W	bank3 base																																0x00000000

bank3_base [31:0] bank 3 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C15C	R/W	bank4 base																																0x00000000

bank4_base [31:0] bank 4 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C160	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Rsvd	max bank			

max bank [2:0] highest bank*_base to use for frame writes before recycling to bank0_base, only 0 to 4 are valid

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C164	R/W	Line offset																																0x00001000

Line_offset [31:0] Indicates the offset in bytes from the start of one line to the next line.
This value should be equal to or larger than one line of image data and should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C168	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
														wbank curr			wbank active	

wbank active 1 = wbank_curr is being written to. Goes high at start of writes, low at last write transfer/completion on axi.

wbank curr [2:0] write bank currently active. valid values =0-4. updated at start of frame write

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C174	R/O	frame wcount																frame icount																--

frame icount [15:0] count of incomming frames (starts) to vdma_writer on video input, non resetable, rolls over, updates at pixel 1 of new frame on video in

frame wcount [15:0] count of outgoing frame writes (starts) from vdma_writer sent to AXI output, non resetable, rolls over, updates at pixel 1 of new frame on video in

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x1C17C	R/O	23	22	21	20	19	18	17	16	--
		15	14	13	12	11	10	9	8	
									video alarm	
		7	6	5	4	3	2	1	0	
		vi fail interframe blanks	**vi fail interline blanks**	**vi fail active height**	**vi fail active width**	**axi fail wxact ostand**	**axi fail wmaxwait**	**axi fail awmaxwait**	**axi fail bresp**	

axi_fail_bresp	clearable alarm, high to indicate bad bresp captured
axi_fail_awmaxwait	clearable alarm, high when awmaxwait_limit reached
axi_fail_wmaxwait	clearable alarm, high when wmaxwait_limit reached
axi_fail_wxact_ostand	clearable alarm, high when wxact_ostand_limit reached
vi_fail_active_width	clearable alarm, high to indicate mismatched active_width detected
vi_fail_active_height	clearable alarm, high to indicate mismatched active_height detected (also raised on missing field!)
vi_fail_interline_blanks	clearable alarm, high to indicate interline blanking below min
vi_fail_interframe_blanks	clearable alarm, high to indicate interframe blanking below min
video_alarm	active high, problem found on video port(s) (active width/height or interline/frame blanks failure)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C180	R/O	**blk status**																																--

blk_status [31:0] block status output (reserved)
-- blk_status(0) = wfifo_fail_full
-- blk_status(1) = wfifo_fail_empty
-- blk_status(4) = pack_fail_overflow
-- blk_status(24) = intw_fail_user_intfc_sig
-- blk_status(others) = zero

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C184	R/W																	**lines wrapped**																0x00000000

lines_wrapped [15:0] Number of lines to write from base address before wrapping back to base address. 0 = no wrapping, >0 = last line written before wrapping

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C188	R/W																	**linetick first**																0x00000000

linetick_first [15:0] Line number of first linetick. 0 = no linetick, >0 = line number to generate linetick

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C18C	R/W																	linetick repeat																0x00000000

linetick_repeat [15:0] Line repeat interval of linetick. 0 = no repeat, >0 = repeat interval in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C190	R/W	linetick delay																0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																	linetick eol	

linetick_eol Linetick start/end of line control. 0 = use start of line, 1 = use end of line to generate linetick

linetick_delay [15:0] Linetick delay in vcke cycles to add to min 3 cycle latency from acl_vi. 0-65535.
Must be less than next linetick generation time or count will not mature and no linetick is not produced.
--NOTE: linetick delay can run past end of frame/field and also into next frame!
-- Take care maturity time is less than next configured linetick generation postion!
-- Take care when changing config between frame too!

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C194	R/W					Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F000F0C
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						Rsvd	Rsvd	Rsvd	Rsvd					Rsvd	Rsvd	axi id multi	Rsvd	

axi_id_multi 0= static value (axi_id_value) for awid/wid, 1 = incrementing value per transaction for awid/wid wrapping to 0 after axi_id_value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C198	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														axi id value				

axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = 0000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.66. ds crop

Crop for full resolution output

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C19C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Enable crop	

Enable crop Crop enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1A0	R/W																	start x																0x00000000

start x [15:0] Horizontal offset from left side of image in pixels for output crop window

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1A4	R/W																	start y																0x00000000

start y [15:0] Vertical offset from top of image in lines for output crop window

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1A8	R/W																	size x																0x0000FFFF

size x [15:0] width of output crop window

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1AC	R/W																	size y																0x0000FFFF

size y [15:0] height of output crop window

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.67. ds scaler

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C1B0	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
										Rsvd	Rsvd	Rsvd	Rsvd	**Timeout IRQ**	**Underflow IRQ**	Rsvd	**Overflow IRQ**	

Overflow IRQ 0 : No overflow
1 : FIFO overflow has occurred

Underflow IRQ 0 : No underflow
1 : FIFO underflow has occurred

Timeout IRQ 0 : No timeout
1 : Timeout on frame done

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C1B4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000010
												Rsvd	**Timeout Enable**	**Clear Alarms**				

Clear Alarms Scaler control
IRQ CLR bit
0 : In-active
1 : Clear-off IRQ status to 0

Timeout Enable 0 : Timeout disabled.
1 : Timeout enabled. Automatic frame reset if frame has not completed after anticipated time.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1B8	R/W																	**WIDTH**																0x00000780

WIDTH [15:0] Input frame width in pixels

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1BC	R/W																	**HEIGHT**																0x00000438

HEIGHT [15:0] Input frame height in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1C0	R/W																				**OWIDTH**													0x00000500

OWIDTH [12:0] Output frame width in pixels

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1C4	R/W																	OHEIGHT																0x000002D0

OHEIGHT [15:0] Output frame height in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1C8	R/W									HFILT TINC																								0x00180000

HFILT_TINC [23:0] Horizontal scaling factor equal to the

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C1CC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														HFILT COEFSET				

HFILT_COEFSET [3:0] HFILT Coeff. control.
HFILT_COEFSET[3:0] - Selects horizontal Coef set for scaler.
0000 : use set 0
0001 : use set 1
.....
1111 : use set 15

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1D0	R/W									VFILT TINC																								0x00180000

VFILT_TINC [23:0] VFILT TINC

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C1D4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														VFILT COEFSET				

VFILT_COEFSET [3:0] VFILT Coeff. control
FILT_COEFSET[3:0] - Selects vertical Coef set for scaler
0000 : use set 0
0001 : use set 1
.....
1111 : use set 15

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.68. ds gamma rgb

Gamma correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C1D8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	Enable	

Enable Gamma enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1DC	R/W					gain g																gain r												0x01000100

gain_r [11:0] gain applied to the R chanel in 4.8 format
gain_g [11:0] gain applied to the G chanel in 4.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1E0	R/W																					gain b												0x00000100

gain_b [11:0] gain applied to the B chanel in 4.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1E4	R/W					offset g																offset r												0x00000000

offset_r [11:0] Offset subtracted from the R chanel
offset_g [11:0] Offset subtracted from the G chanel

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1E8	R/W																					offset b												0x00000000

offset_b [11:0] Offset subtracted from the B chanel

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.69. ds sharpen

Sharpen
Luma transform red coefficient. u0.8
Luma transform blue coefficient. u0.8

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C1EC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Enable	

Enable Sharpening enable: 0=off, 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1F0	R/W																									Strength								0x00000010

Strength [8:0] Controls strength of sharpening effect. u5.4

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1F4	R/W									Alpha Undershoot								Control B								Control R								0x00131E4C

Alpha Undershoot [7:0] Alpha blending of undershoot and overshoot u0.7, 0 = only unsershoot, 255 = only overshoot

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1F8	R/W									Luma Offset Low														Luma Thresh Low										0x00000000

Luma Thresh Low [9:0] Luma threshold below this value, no sharpening will be applied.
Luma Offset Low [7:0] Luma offset (min value) of thre region of less than Luma Thresh Low.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C1FC	R/W							Luma Thresh High										Luma Slope Low																0x033203FC

Luma Slope Low [15:0] Luma linear threshold slope at dark luminance region
Luma Thresh High [9:0] Luma threshold above this value, sharpening level will be dicreased.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C200	R/W									Luma Slope High																Luma Offset High								0x06A40000

Luma Offset High [7:0] Luma offset (min value) of thre region of more than Luma Thresh High.
Luma Slope High [15:0] Luma linear threshold slope at bright luminance region

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C204	R/W			Clip Str Min																Clip Str Max														0x00CD3FFF

Clip Str Max [13:0] clips sharpening mask of max value. This will control overshoot. U0.14. (0 ~ 16383)

Clip Str Min [13:0] clips sharpening mask of min value. This will control undershoot. U0.14. It is used as negative value. (0 ~ -16383)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C208	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Debug				

Debug [3:0] To support different debug output. 0 = normal operation, 1 = luma, 2 = sharpening mask

21.70. ds cs conv

Conversion of RGB to YUV data using a 3x3 color matrix plus offsets

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C20C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Enable vertical downsample	Enable horizontal downsample	Enable filter	Enable matrix	

Enable matrix Color matrix enable: 0=off 1=on

Enable filter Filter enable: 0=off 1=on

Enable horizontal downsample Horizontal Downsampling Enable: 0=off 1=on

Enable vertical downsample Vertical Downsampling Enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C210	R/W																	Coefft 11																0x0000002F

Coefft 11 [15:0] Matrix coefficient for R-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C214	R/W																	Coefft 12																0x0000009D

Coefft 12 [15:0] Matrix coefficient for G-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C218	R/W																	Coefft 13																0x00000010

Coefft 13 [15:0] Matrix coefficient for B-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C21C	R/W																	Coefft 21																0x0000801A

Coefft 21 [15:0] Matrix coefficient for R-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C220	R/W																	Coefft 22																0x00008057

Coefft 22 [15:0] Matrix coefficient for G-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C224	R/W																	Coefft 23																0x00000070

Coefft 23 [15:0] Matrix coefficient for B-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C228	R/W																	Coefft 31																0x00000070

Coefft 31 [15:0] Matrix coefficient for R-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C22C	R/W																	Coefft 32																0x00008066

Coefft 32 [15:0] Matrix coefficient for G-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C230	R/W																	Coefft 33																0x0000800A

Coefft 33 [15:0] Matrix coefficient for B-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C234	R/W																						Coefft o1											0x00000000

Coefft o1 [10:0] Offset for Y
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C238	R/W																						Coefft o2											0x00000200

Coefft o2 [10:0] Offset for Cb
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C23C	R/W																						Coefft o3											0x00000200

Coefft o3 [10:0] Offset for Cr
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C240	R/W																							Clip min Y										0x00000000

Clip min Y [9:0] Minimal value for Y. Values below this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C244	R/W																							Clip max Y										0x000003FF

Clip max Y [9:0] Maximal value for Y. Values above this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C248	R/W																							Clip min UV										0x00000000

Clip min UV [9:0] Minimal value for Cb, Cr. Values below this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C24C	R/W																							Clip max UV										0x000003FF

Clip max UV [9:0] Maximal value for Cb, Cr. Values above this are clipped.
Format: signed (2's complement) 10-bit integer

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C250	R/W																							Data mask RY										0x000003FF

Data mask RY [9:0] Data mask for channel 1 (R or Y). Bit-wise and of this value and video data.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C254	R/W																							Data mask GU										0x000003FF

Data mask GU [9:0] Data mask for channel 2 (G or U). Bit-wise and of this value and video data.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C258	R/W																							Data mask BV										0x000003FF

Data mask BV [9:0] Data mask for channel 3 (B or V). Bit-wise and of this value and video data.

21.71. ds cs conv dither

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C25C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Shift mode		Dither amount		Enable dither	

Enable dither Enables dithering module

Dither amount [1:0] 0= dither to 9 bits; 1=dither to 8 bits; 2=dither to 7 bits; 3=dither to 6 bits

Shift mode 0= output is LSB aligned; 1=output is MSB aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.72. ds dma writer

DMA writer controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C260	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
						axi xact comp		frame write on	Rsvd	Plane select		Rsvd	Base mode					

Base mode [4:0] Base DMA packing mode for RGB/RAW/YUV etc (see ISP guide)

Plane select [1:0] Plane select for planar base modes. Only used if planar outputs required. Not used. Should be set to 0

frame write on 0 = no frames written(when switched from 1, current frame completes writing before stopping),
1= write frame(s) (write single or continous frame(s))

axi xact comp 0 = dont wait for axi transaction completion at end of frame(just all transfers accepted). 1 = wait for all transactions completed

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C264	R/W	active height																active width																0x04380780

active width [15:0] Active video width in pixels 128-8000

active height [15:0] Active video height in lines 128-8000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C268	R/W	bank0 base																																0x00000000

bank0_base [31:0] bank 0 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C26C	R/W	bank1 base																																0x00000000

bank1_base [31:0] bank 1 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C270	R/W	bank2 base																																0x00000000

bank2_base [31:0] bank 2 base address for frame buffer, should be word-aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C274	R/W	bank3 base																																0x00000000

bank3_base [31:0] bank 3 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C278	R/W	bank4 base																																0x00000000

bank4_base [31:0] bank 4 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C27C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Rsvd	max bank			

max bank [2:0] highest bank*_base to use for frame writes before recycling to bank0_base, only 0 to 4 are valid

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C280	R/W	Line offset																																0x00001000

Line_offset [31:0] Indicates the offset in bytes from the start of one line to the next line.
This value should be equal to or larger than one line of image data and should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C284	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
														wbank curr			wbank active	

wbank active 1 = wbank_curr is being written to. Goes high at start of writes, low at last write transfer/completion on axi.

wbank curr [2:0] write bank currently active. valid values =0-4. updated at start of frame write

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C290	R/O	frame wcount																frame icount																--

frame icount [15:0] count of incomming frames (starts) to vdma_writer on video input, non resetable, rolls over, updates at pixel 1 of new frame on video in

frame wcount [15:0] count of outgoing frame writes (starts) from vdma_writer sent to AXI output, non resetable, rolls over, updates at pixel 1 of new frame on video in

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x1C298	R/O	23	22	21	20	19	18	17	16	--
		15	14	13	12	11	10	9	8	
									video alarm	
		7	6	5	4	3	2	1	0	
		vi fail interframe blanks	**vi fail interline blanks**	**vi fail active height**	**vi fail active width**	**axi fail wxact ostand**	**axi fail wmaxwait**	**axi fail awmaxwait**	**axi fail bresp**	

axi_fail_bresp clearable alarm, high to indicate bad bresp captured
axi_fail_awmaxwait clearable alarm, high when awmaxwait_limit reached
axi_fail_wmaxwait clearable alarm, high when wmaxwait_limit reached
axi_fail_wxact_ostand clearable alarm, high when wxact_ostand_limit reached
vi_fail_active_width clearable alarm, high to indicate mismatched active_width detected
vi_fail_active_height clearable alarm, high to indicate mismatched active_height detected (also raised on missing field!)
vi_fail_interline_blanks clearable alarm, high to indicate interline blanking below min
vi_fail_interframe_blanks clearable alarm, high to indicate interframe blanking below min
video_alarm active high, problem found on video port(s) (active width/height or interline/frame blanks failure)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C29C	R/O	**blk status**																																--

blk_status [31:0] block status output (reserved)
-- blk_status(0) = wfifo_fail_full
-- blk_status(1) = wfifo_fail_empty
-- blk_status(4) = pack_fail_overflow
-- blk_status(24) = intw_fail_user_intfc_sig
-- blk_status(others) = zero

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2A0	R/W																	**lines wrapped**																0x00000000

lines_wrapped [15:0] Number of lines to write from base address before wrapping back to base address. 0 = no wrapping, >0 = last line written before wrapping

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2A4	R/W																	**linetick first**																0x00000000

linetick_first [15:0] Line number of first linetick. 0 = no linetick, >0 = line number to generate linetick

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2A8	R/W																	linetick repeat																0x00000000

linetick_repeat [15:0] Line repeat interval of linetick. 0 = no repeat, >0 = repeat interval in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C2AC	R/W	linetick delay																0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																	linetick eol	

linetick_eol Linetick start/end of line control. 0 = use start of line, 1 = use end of line to generate linetick

linetick_delay [15:0] Linetick delay in vcke cycles to add to min 3 cycle latency from acl_vi. 0-65535.
Must be less than next linetick generation time or count will not mature and no linetick is not produced.
--NOTE: linetick delay can run past end of frame/field and also into next frame!
-- Take care maturity time is less than next configured linetick generation postion!
-- Take care when changing config between frame too!

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C2B0	R/W					Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F000F0C
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						Rsvd	Rsvd	Rsvd	Rsvd					Rsvd	Rsvd	axi id multi	Rsvd	

axi_id_multi 0= static value (axi_id_value) for awid/wid, 1 = incrementing value per transaction for awid/wid wrapping to 0 after axi_id_value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C2B4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														axi id value				

axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = 0000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.73. ds uv dma writer

DMA writer controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C2B8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
						axi xact comp		frame write on	Rsvd	Plane select		Rsvd	Base mode					

Base mode [4:0] Base DMA packing mode for RGB/RAW/YUV etc (see ISP guide)

Plane select [1:0] Plane select for planar base modes. Only used if planar outputs required. Not used. Should be set to 0

frame write on 0 = no frames written(when switched from 1, current frame completes writing before stopping),
1= write frame(s) (write single or continous frame(s))

axi xact comp 0 = dont wait for axi transaction completion at end of frame(just all transfers accepted). 1 = wait for all transactions completed

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2BC	R/W	active height																active width																0x04380780

active width [15:0] Active video width in pixels 128-8000

active height [15:0] Active video height in lines 128-8000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2C0	R/W	bank0 base																																0x00000000

bank0_base [31:0] bank 0 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2C4	R/W	bank1 base																																0x00000000

bank1_base [31:0] bank 1 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2C8	R/W	bank2 base																																0x00000000

bank2_base [31:0] bank 2 base address for frame buffer, should be word-aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2CC	R/W	bank3 base																																0x00000000

bank3_base [31:0] bank 3 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2D0	R/W	bank4 base																																0x00000000

bank4_base [31:0] bank 4 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C2D4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Rsvd	max bank			

max bank [2:0] highest bank*_base to use for frame writes before recycling to bank0_base, only 0 to 4 are valid

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2D8	R/W	Line offset																																0x00001000

Line_offset [31:0] Indicates the offset in bytes from the start of one line to the next line.
This value should be equal to or larger than one line of image data and should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C2DC	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
														wbank curr			wbank active	

wbank active 1 = wbank_curr is being written to. Goes high at start of writes, low at last write transfer/completion on axi.

wbank curr [2:0] write bank currently active. valid values =0-4. updated at start of frame write

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2E8	R/O	frame wcount																frame icount																--

frame icount [15:0] count of incomming frames (starts) to vdma_writer on video input, non resetable, rolls over, updates at pixel 1 of new frame on video in

frame wcount [15:0] count of outgoing frame writes (starts) from vdma_writer sent to AXI output, non resetable, rolls over, updates at pixel 1 of new frame on video in

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x1C2F0	R/O	23	22	21	20	19	18	17	16	--
		15	14	13	12	11	10	9	8	
									video alarm	
		7	6	5	4	3	2	1	0	
		vi fail interframe blanks	**vi fail interline blanks**	**vi fail active height**	**vi fail active width**	**axi fail wxact ostand**	**axi fail wmaxwait**	**axi fail awmaxwait**	**axi fail bresp**	

axi_fail_bresp clearable alarm, high to indicate bad bresp captured
axi_fail_awmaxwait clearable alarm, high when awmaxwait_limit reached
axi_fail_wmaxwait clearable alarm, high when wmaxwait_limit reached
axi_fail_wxact_ostand clearable alarm, high when wxact_ostand_limit reached
vi_fail_active_width clearable alarm, high to indicate mismatched active_width detected
vi_fail_active_height clearable alarm, high to indicate mismatched active_height detected (also raised on missing field!)
vi_fail_interline_blanks clearable alarm, high to indicate interline blanking below min
vi_fail_interframe_blanks clearable alarm, high to indicate interframe blanking below min
video_alarm active high, problem found on video port(s) (active width/height or interline/frame blanks failure)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2F4	R/O	**blk status**																																--

blk_status [31:0] block status output (reserved)
-- blk_status(0) = wfifo_fail_full
-- blk_status(1) = wfifo_fail_empty
-- blk_status(4) = pack_fail_overflow
-- blk_status(24) = intw_fail_user_intfc_sig
-- blk_status(others) = zero

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2F8	R/W																	**lines wrapped**																0x00000000

lines_wrapped [15:0] Number of lines to write from base address before wrapping back to base address. 0 = no wrapping, >0 = last line written before wrapping

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C2FC	R/W																	**linetick first**																0x00000000

linetick_first [15:0] Line number of first linetick. 0 = no linetick, >0 = line number to generate linetick

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C300	R/W																	linetick repeat																0x00000000

linetick_repeat [15:0] Line repeat interval of linetick. 0 = no repeat, >0 = repeat interval in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C304	R/W	linetick delay																0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																	linetick eol	

linetick_eol Linetick start/end of line control. 0 = use start of line, 1 = use end of line to generate linetick

linetick_delay [15:0] Linetick delay in vcke cycles to add to min 3 cycle latency from acl_vi. 0-65535.
Must be less than next linetick generation time or count will not mature and no linetick is not produced.
--NOTE: linetick delay can run past end of frame/field and also into next frame!
-- Take care maturity time is less than next configured linetick generation postion!
-- Take care when changing config between frame too!

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C308	R/W					Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F000F0C
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						Rsvd	Rsvd	Rsvd	Rsvd					Rsvd	Rsvd	axi id multi	Rsvd	

axi_id_multi 0= static value (axi_id_value) for awid/wid, 1 = incrementing value per transaction for awid/wid wrapping to 0 after axi_id_value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C30C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														axi id value				

axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = 0000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

21.74. multi ctx

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x1C310	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Config done	

Config done This signal is only required in multi-context mode
Once configuration for ping/pong address space is done, MCU must write 1 into this address
This register is self-clearing. So the read-back will be 0

22. METERING_STATS_PONG_MEM (METERING_STATS_PONG_MEM)

22.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x1C470	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x1C474	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x22B28	R/W	Data(6574)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 6575 32-bit registers. The address for element (i) is: 0x1C470 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

23. DECOMPANDER0_PONG_MEM (DECOMPANDER0_PONG_MEM)

23.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x22B2C	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x22B30	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x22BAC	R/W	Data(32)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 33 32-bit registers. The address for element (i) is: 0x22B2C + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

24. DECOMPANDER1_PONG_MEM (DECOMPANDER1_PONG_MEM)

24.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x22BB0	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x22BB4	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x22FB0	R/W	Data(256)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 257 32-bit registers. The address for element (i) is: 0x22BB0 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

25. DPC_PONG_MEM (DPC_PONG_MEM)

the content of the memory is {y-coord[11:0], x-coord[12:0]}. Phisical memory width is 25bits.
the top-left corner of the frame is indicated by {1,1}

25.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x22FB4	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x22FB8	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x26FB0	R/W	Data(4095)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 4096 32-bit registers. The address for element (i) is: 0x22FB4 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

26. CA_CORRECTION_FILTER_PONG_MEM (CA_CORRECTION_FILTER_PONG_MEM)

Cromatic aberration correction polyphase filter lookup table, 32 entries of 32 bits each.
Each entry address corresponds to fractional part of the pixel displacement.
Each entry is four 8-bit filter coefficients in fix point format.
- Codes 0...128 correspond to values 0.0 ... 1.0 (with resolution 1/128)
- Codes 129...191 correspond to values 129/128 ... 191/128
- Codes 192...255 correspond to values -64/128 ... -1/128

26.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x26FB4	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x26FB8	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x27030	R/W	Data(31)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 32 32-bit registers. The address for element (i) is: 0x26FB4 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

27. CA_CORRECTION_MESH_PONG_MEM (CA_CORRECTION_MESH_PONG_MEM)

Chromatic aberration correction coordinate lookup table, 8192 entries for tile displacement of 16 bits each. Each entry is 16 bits, 8 LSBs is X displacement of the tile and 8 MSBs is Y displacement. The coordiantes are coded as two's complement, 3.5 fixed point.

27.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x27034	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x27038	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x2B030	R/W	Data(4095)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 4096 32-bit registers. The address for element (i) is: 0x27034 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

28. MESH_SHADING_PONG_MEM (MESH_SHADING_PONG_MEM)

28.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x2B034	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x2B038	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x2F030	R/W	Data(4095)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 4096 32-bit registers. The address for element (i) is: 0x2B034 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

29. RADIAL_SHADING_PONG_MEM (RADIAL_SHADING_PONG_MEM)

4 banks of radial shading lookup tables - for R,G,B,Ir channels.
The banks start at the addresses 0, 256, 512, 768.
Each bank has 129 entries for piecewise linear table, each entry occupies 32 bits, of which 16 least significant bits are encoding shading correction factor in 4.12 fix point format.

29.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
`0x2F034`	**R/W**	**Data(0)**																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x2F038`	**R/W**	**Data(1)**																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
`0x2FE34`	**R/W**	**Data(896)**																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 897 32-bit registers. The address for element (i) is: 0x2F034 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

30. IRIDIX_RP_PONG_MEM (IRIDIX_RP_PONG_MEM)

30.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x2FE38	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x2FE3C	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x30038	R/W	Data(128)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 129 32-bit registers. The address for element (i) is: 0x2FE38 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

31. IRIDIX_FP1_PONG_MEM (IRIDIX_FP1_PONG_MEM)

31.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3003C	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x30040	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x3023C	R/W	Data(128)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 129 32-bit registers. The address for element (i) is: 0x3003C + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

32. FR_GAMMA_RGB_PONG_MEM (FR_GAMMA_RGB_PONG_MEM)

32.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30240	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x30244	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x30440	R/W	Data(128)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 129 32-bit registers. The address for element (i) is: 0x30240 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

33. DS_GAMMA_RGB_PONG_MEM (DS_GAMMA_RGB_PONG_MEM)

33.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30444	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x30448	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x30644	R/W	Data(128)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 129 32-bit registers. The address for element (i) is: 0x30444 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

34. LUMVAR_STATS_PONG_MEM (LUMVAR_STATS_PONG_MEM)

34.1. Array

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30648	R/W	Data(0)																																--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x3064C	R/W	Data(1)																																--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x30E44	R/W	Data(511)																																--

Data [31:0] Please see other documentation for a description of the contents of this array.

This is an array of 512 32-bit registers. The address for element (i) is: 0x30648 + 4i.

35. ISP_CONFIG_PONG (SINGLE_CONTEXT_CONFIG)

35.1. top

Miscellaneous top-level ISP controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30E48	R/W	Active Height																Active Width																0x04380780

Active Width [15:0] Active video width in pixels

Active Height [15:0] Active video height in lines

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E4C	R/W							Linear data src								Cfa pattern		0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
								RGGB start post mirror								RGGB start pre mirror		

RGGB start pre mirror [1:0] Starting color of the rggb pattern for all the modules before mirror
0 = R Gr
Gb B
1 = Gr R
B Gb
2 = Gb B
R Gr
3 = B Gb
Gr R

RGGB start post mirror [1:0] Starting color of the rggb pattern for all the modules after mirror
this must be same as RGGB start pre mirror if mirror is bypassed

Cfa pattern [1:0] The pixel arrangement of the CFA array on the sensor. Set in the Top register group and used by several blocks in the pipeline:
0 = RGGB
1 = reserved
2 = RIrGB
3 = RGIrB

Linear data src [1:0] Linear data src
0 = Sensor stitched and linear data directly coming from sensor
1 = linear data from frame stitch
2 = Sensor companded data linearised through decompander
3 = reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E6C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
												Bypass frame stitch	Bypass gain wdr	Bypass sensor offset wdr	Bypass decompander	Bypass input formatter	Bypass video test gen	

Bypass video test gen Bypass video test generator
Bypass input formatter Bypass input formatter module.
Bypass decompander Bypass front end decompander
Bypass sensor offset wdr Bypass sensor offset wdr
Bypass gain wdr Bypass gain wdr
Bypass frame stitch Bypass frame stitching logic

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E70	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000004
													Bypass defect pixel	**Bypass RAW frontend**	**Bypass fe sqrt**	**Bypass frontend sensor offset**	**Bypass digital gain**	

Bypass digital gain Bypass digital gain module
Bypass frontend sensor offset Bypass digital gain module
Bypass fe sqrt Bypass square root function before raw frontend
Bypass RAW frontend Bypass RAW frontend (green equalization and dynamic defect pixel)
Bypass defect pixel Bypass static defect pixel

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E78	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000002
															Bypass ca correction	**Bypass temper**	**Bypass sinter**	

Bypass sinter Bypass sinter
Bypass temper Bypass temper
Bypass ca correction Bypass chromatic abberation correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E7C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
											Bypass iridix	**Bypass iridix gain**	**Bypass white balance**	**Bypass mesh shading**	**Bypass radial shading**	**Bypass sensor offset pre shading**	**Bypass square be**	

Bypass square_be Bypass backend square
Bypass sensor_offset_pre_shading Bypass sensor offset pre shading
Bypass radial shading Bypass radial shading
Bypass mesh shading Bypass mesh ashading
Bypass white balance Bypass white balance
Bypass iridix gain Bypass
Bypass iridix Bypass

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E80	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										Bypass nonequ gamma	**Bypass 3D lut**	**Bypass CNR**	**Bypass CCM**	**Bypass pf correction**	**Bypass demosaic rgbir**	**Bypass demosaic rgb**	**Bypass mirror**	

Bypass mirror Bypass EW mirror
Bypass demosaic rgb Bypass demosaic rgb
Bypass demosaic rgbir Bypass demosaic rgbir
Bypass pf correction Bypass pf correction
Bypass CCM Bypass CCM
Bypass CNR Bypass CNR
Bypass 3D lut Bypass 3d lut
Bypass nonequ gamma Bypass nonequ gamma

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E84	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Bypass fr cs conv	**Bypass fr sharpen**	**Bypass fr gamma rgb**	**Bypass fr crop**	

Bypass fr crop Bypass fr crop
Bypass fr gamma rgb Bypass fr gamma rgb
Bypass fr sharpen Bypass fr sharpen
Bypass fr cs conv Bypass fr cs conv

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E88	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Bypass ds cs conv	**Bypass ds sharpen**	**Bypass ds gamma rgb**	**Bypass ds scaler**	**Bypass ds crop**	

Bypass ds crop Bypass ds crop
Bypass ds scaler Bypass ds scaler
Bypass ds gamma rgb Bypass ds gamma rgb
Bypass ds sharpen Bypass ds sharpen
Bypass ds cs conv Bypass ds cs conv

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E8C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
								ISP processing fr bypass mode								ISP downscale pipe disable	ISP RAW bypass	

ISP RAW bypass
Used to select between normal ISP processing with image sensor data and up to 12 bit RGB input.
In the latler case data is reinserted into pipeline after purple fringing correction block.
0 = Select processed.
1 = Bypass ISP RAW processing.

ISP downscale pipe disable
0: Downscale pipeline is enabled
1: Downscale pipeline is disabled. No data is sent out in DMA and streaming channel
0 = Select processed.
1 = Bypass ISP RAW processing.

ISP processing fr bypass mode [1:0]
ISP FR bypass modes. For debug purposes only. Should be set to 0 during normal operation.
Used to bypass entire ISP after input port or to pass the stitched image directly to the output.
0 = Full processing
1 = Bypass entire ISP processing and output [19:4] of raw sensor data After video test gen
2 = Bypass entire ISP processing and output LSB 10-bits bits of raw sensor data After video test gen. Data must be MSB aligned
3 = Reserved

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E90	R/W								aexp src					Lumavar switch	Lumavar Disable		iHist disable	0x00010000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
			AEXP Histogram switch		AEXP hist disable			AWB switch	AWB disable			AF switch	AF disable		AE switch		AE 5bin hist disable	

AE 5bin hist disable
0: AEXP 5-bin histogram enabled
1: AEXP 5-bin histogram disabled

AE switch [1:0]
AE 5bin histogram tap in the pipeline. Location of AE statistic collection.
0 = After static white balance whose position is selected by aexp_src signal
1 = After WDR Frame Stitch. if its sensor companded data, then use decompanded output. If its sensor linearised data, then use it directly
2 = After VTPG
3 = reserved

AF disable
0: AF enabled
1: AF disabled

AF switch
AF tap in the pipeline. .
0 = After Sinter
1 = before Sinter

AWB disable
0: AWB enabled
1: AWB disabled

AWB switch
AWB tap in the pipeline. Location of AWB statistics collection.
0 = Immediately after demosaic
1 = Immediately after CNR

AEXP hist disable
0: AEXP 1024-bin histogram enabled
1: AEXP 1024-bin histogram disabled

AEXP Histogram switch [1:0]
AE global histogram tap in the pipeline. Location of statistics gathering for 1024 bin global histogram
0 = After static white balance whose position is selected by aexp_src signal
1 = After WDR Frame Stitch. if its sensor companded data, then use decompanded output. If its sensor linearised data, then use it directly
2 = After VTPG
3 = reserved

iHist disable
Post iridix histogram enable. Enables statistics gathering for global histogram
0 = Enabled
1 = Disabled

Lumavar Disable
0 = Enabled
1 = Disabled

Lumavar switch
Luma variance tap in the pipeline.
0 = Full resolution pipeline
1 = Downscaled pipeline

aexp_src
0 = After static white balance when applied before shading
1 = After static white balance when applied after shading

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.2. crossbar

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E94	R/W							channel4 select								channel3 select		0x03020100
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
								channel2 select								channel1 select		

channel1_select [1:0] channel0 selection from the input 4 channels
channel2_select [1:0] channel1 selection from the input 4 channels
channel3_select [1:0] channel2 selection from the input 4 channels
channel4_select [1:0] channel4 selection from the input 4 channels

35.3. video test gen ch0

Video test generator controls. See ISP Guide for further details

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30E98	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Rsvd	Generate mode	bayer rgb o sel	bayer rgb i sel	test pattern off on	

test_pattern_off on Test pattern off-on: 0=off, 1=on
bayer_rgb_i sel Bayer or rgb select for input video: 0=bayer, 1=rgb
bayer_rgb_o sel Bayer or rgb select for output video: 0=bayer, 1=rgb
Generate mode 0 = One Shot (on request) generation. 1 = free run (continuous) generation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30E9C	R/W																									pattern type								0x00000003

pattern type [7:0] Pattern type select: 0=Flat field,1=Horizontal gradient,2=Vertical Gradient,3=Vertical Bars,4=Rectangle,5-255=Default white frame on black

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EA0	R/W													r backgnd																				0x0000FFFF

r backgnd [19:0] Red background value 16bit, MSB aligned to used width

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EA4	R/W													g backgnd																				0x0000FFFF

g backgnd [19:0] Green background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EA8	R/W													b backgnd																				0x0000FFFF

b backgnd [19:0] Blue background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EAC	R/W													r foregnd																				0x00008FFF

r foregnd [19:0] Red foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EB0	R/W													g foregnd																				0x00008FFF

g foregnd [19:0] Green foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EB4	R/W													b foregnd																				0x00008FFF

b foregnd [19:0] Blue foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EB8	R/W																	rgb gradient																0x00003CAA

rgb gradient [15:0] RGB gradient increment per pixel (0-15) for first channel
Format: unsigned 4.12-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EBC	R/W													rgb gradient start																				0x00000000

rgb_gradient start [19:0] RGB gradient start value for first channel 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EC0	R/W			rect bot																rect top														0x01000001

rect top [13:0] Rectangle top line number 1-n
rect bot [13:0] Rectangle bottom line number 1-n

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EC4	R/W			rect right																rect left														0x01000001

rect left [13:0] Rectangle left pixel number 1-n
rect right [13:0] Rectangle right pixel number 1-n

35.4. video test gen ch1

Video test generator controls. See ISP Guide for further details

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30EC8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Rsvd	Generate mode	bayer rgb o sel	bayer rgb i sel	test pattern off on	

test_pattern_off on Test pattern off-on: 0=off, 1=on
bayer_rgb_i sel Bayer or rgb select for input video: 0=bayer, 1=rgb
bayer_rgb_o sel Bayer or rgb select for output video: 0=bayer, 1=rgb
Generate mode 0 = One Shot (on request) generation. 1 = free run (continuous) generation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30ECC	R/W																									pattern type								0x00000003

pattern type [7:0] Pattern type select: 0=Flat field,1=Horizontal gradient,2=Vertical Gradient,3=Vertical Bars,4=Rectangle,5-255=Default white frame on black

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30ED0	R/W													r backgnd																				0x0000FFFF

r backgnd [19:0] Red background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30ED4	R/W													g backgnd																				0x0000FFFF

g backgnd [19:0] Green background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30ED8	R/W													b backgnd																				0x0000FFFF

b backgnd [19:0] Blue background value 16bit, MSB aligned to used width

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EDC	R/W													r foregnd																				0x00008FFF

r foregnd [19:0] Red foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EE0	R/W													g foregnd																				0x00008FFF

g foregnd [19:0] Green foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EE4	R/W													b foregnd																				0x00008FFF

b foregnd [19:0] Blue foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EE8	R/W																	rgb gradient																0x00003CAA

rgb gradient [15:0] RGB gradient increment per pixel (0-15) for first channel
Format: unsigned 4.12-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EEC	R/W													rgb gradient start																				0x00000000

rgb_gradient start [19:0] RGB gradient start value for first channel 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EF0	R/W			rect bot																rect top														0x01000001

rect top [13:0] Rectangle top line number 1-n
rect bot [13:0] Rectangle bottom line number 1-n

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EF4	R/W			rect right																rect left														0x01000001

rect left [13:0] Rectangle left pixel number 1-n
rect right [13:0] Rectangle right pixel number 1-n

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

35.5. video test gen ch2

Video test generator controls. See ISP Guide for further details

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30EF8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Rsvd	**Generate mode**	**bayer rgb o sel**	**bayer rgb i sel**	**test pattern off on**	

test_pattern_off on Test pattern off-on: 0=off, 1=on
bayer_rgb_i sel Bayer or rgb select for input video: 0=bayer, 1=rgb
bayer_rgb_o sel Bayer or rgb select for output video: 0=bayer, 1=rgb
Generate mode 0 = One Shot (on request) generation. 1 = free run (continuous) generation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30EFC	R/W																									**pattern type**								0x00000003

pattern type [7:0] Pattern type select: 0=Flat field,1=Horizontal gradient,2=Vertical Gradient,3=Vertical Bars,4=Rectangle,5-255=Default white frame on black

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F00	R/W													**r backgnd**																				0x0000FFFF

r backgnd [19:0] Red background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F04	R/W													**g backgnd**																				0x0000FFFF

g backgnd [19:0] Green background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F08	R/W													**b backgnd**																				0x0000FFFF

b backgnd [19:0] Blue background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F0C	R/W													**r foregnd**																				0x00008FFF

r foregnd [19:0] Red foreground value 16bit, MSB aligned to used width

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F10	R/W													g foregnd																				0x00008FFF

g foregnd [19:0] Green foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F14	R/W													b foregnd																				0x00008FFF

b foregnd [19:0] Blue foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F18	R/W																	rgb gradient																0x00003CAA

rgb gradient [15:0] RGB gradient increment per pixel (0-15) for first channel
Format: unsigned 4.12-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F1C	R/W													rgb gradient start																				0x00000000

rgb_gradient start [19:0] RGB gradient start value for first channel 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F20	R/W			rect bot																rect top														0x01000001

rect top [13:0] Rectangle top line number 1-n
rect bot [13:0] Rectangle bottom line number 1-n

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F24	R/W			rect right																rect left														0x01000001

rect left [13:0] Rectangle left pixel number 1-n
rect right [13:0] Rectangle right pixel number 1-n

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.6. video test gen ch3

Video test generator controls. See ISP Guide for further details

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30F28	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Rsvd	**Generate mode**	**bayer rgb o sel**	**bayer rgb i sel**	**test pattern off on**	

test_pattern_off on Test pattern off-on: 0=off, 1=on
bayer_rgb_i sel Bayer or rgb select for input video: 0=bayer, 1=rgb
bayer_rgb_o sel Bayer or rgb select for output video: 0=bayer, 1=rgb
Generate mode 0 = One Shot (on request) generation. 1 = free run (continuous) generation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F2C	R/W																									**pattern type**								0x00000003

pattern type [7:0] Pattern type select: 0=Flat field,1=Horizontal gradient,2=Vertical Gradient,3=Vertical Bars,4=Rectangle,5-255=Default white frame on black

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F30	R/W													**r backgnd**																				0x0000FFFF

r backgnd [19:0] Red background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F34	R/W													**g backgnd**																				0x0000FFFF

g backgnd [19:0] Green background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F38	R/W													**b backgnd**																				0x0000FFFF

b backgnd [19:0] Blue background value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F3C	R/W													**r foregnd**																				0x00008FFF

r foregnd [19:0] Red foreground value 16bit, MSB aligned to used width

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F40	R/W													g foregnd																				0x00008FFF

g foregnd [19:0] Green foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F44	R/W													b foregnd																				0x00008FFF

b foregnd [19:0] Blue foreground value 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F48	R/W																	rgb gradient																0x00003CAA

rgb gradient [15:0] RGB gradient increment per pixel (0-15) for first channel
Format: unsigned 4.12-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F4C	R/W													rgb gradient start																				0x00000000

rgb_gradient start [19:0] RGB gradient start value for first channel 16bit, MSB aligned to used width

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F50	R/W			rect bot																rect top														0x01000001

rect top [13:0] Rectangle top line number 1-n
rect bot [13:0] Rectangle bottom line number 1-n

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F54	R/W			rect right																rect left														0x01000001

rect left [13:0] Rectangle left pixel number 1-n
rect right [13:0] Rectangle right pixel number 1-n

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.7. input formatter

Adapts received data format to ISP format see ISP guide for a table of setting to be used for various sensors/modes.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30F58	R/W														input bitwidth select			0x00020000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
															mode in			

mode in [2:0] Input mode
- 0 = Linear data
- 1 = 2:3 multiple exposure multiplexing
- 2 = Logarithmic encoding
- 3 = Companding curve with knee points
- 4 = 16bit linear+ 12bit VS
- 5 = 12bit companded + 12bit VS
- 6 = Reserved
- 7 = pass through mode

input bitwidth select [2:0] Input bitwidth select
- 0 = 8 bits
- 1 = 10 bits
- 2 = 12 bits
- 3 = 14 bits
- 4 = 16 bits
- 5 = 20 bits (no 18 bits)
- 6 = Reserved
- 7 = Reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F5C	R/W															factor ML																		0x00001000

factor ML [17:0] 18 bit, 6.12 fix point - ratio between long and medium exposure for 2:3 multiplexed mode

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F60	R/W																				factor MS													0x00001000

factor MS [12:0] 13 bit, 1.12 fix point - ratio between short and medium exposure for 2:3 multiplexed mode

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F64	R/W																					black level												0x00000000

black level [11:0] Black level of sensor data for 2:3 multiplexed mode

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F68	R/W	knee point1																knee point0																0x05800200

knee point0 [15:0] First knee point
knee point1 [15:0] Second knee point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F6C	R/W																	knee point2																0x00000881

knee point2 [15:0] Third knee point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30F70	R/W					slope3 select								slope2 select				0x09060402
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						slope1 select								slope0 select				

slope0 select [3:0] First slope for companding table segments
0 = 1x
1 = 2x
2 = 4x
3 = 8x
4 = 16x
5 = 32x
6 = 64x
7 = 128x
8 = 256x
9 = 512x
10 = 1024x
11 = 2048x
12 = 4096x
13 = 8192x
14 = 16384x
15 = 32768x

slope1 select [3:0] Second slope for companding table segments (encoding is the same as slope0 select)
slope2 select [3:0] Third slope for companding table segments (encoding is the same as slope0 select)
slope3 select [3:0] Last slope for companding table segments (encoding is the same as slope0 select)

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.8. sensor offset wdr l

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F74	R/W					offset 01																offset 00												0x00000000

offset 00 [11:0] offset offset for color channel 00 (R)
offset 01 [11:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F78	R/W					offset 11																offset 10												0x00000000

offset 10 [11:0] offset offset for color channel 10 (Gb)
offset 11 [11:0] offset offset for color channel 11 (B)

35.9. sensor offset wdr m

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F7C	R/W					offset 01																offset 00												0x00000000

offset 00 [11:0] offset offset for color channel 00 (R)
offset 01 [11:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F80	R/W					offset 11																offset 10												0x00000000

offset 10 [11:0] offset offset for color channel 10 (Gb)
offset 11 [11:0] offset offset for color channel 11 (B)

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.10. sensor offset wdr s

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F84	R/W					offset 01																offset 00												0x00000000

offset 00 [11:0] offset offset for color channel 00 (R)
offset 01 [11:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F88	R/W					offset 11																offset 10												0x00000000

offset 10 [11:0] offset offset for color channel 10 (Gb)
offset 11 [11:0] offset offset for color channel 11 (B)

35.11. sensor offset wdr vs

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F8C	R/W					offset 01																offset 00												0x00000000

offset 00 [11:0] offset offset for color channel 00 (R)
offset 01 [11:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F90	R/W					offset 11																offset 10												0x00000000

offset 10 [11:0] offset offset for color channel 10 (Gb)
offset 11 [11:0] offset offset for color channel 11 (B)

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.12. gain wdr

Gain adjustment for the WDR stitching

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F94	R/W				Gain m																Gain l													0x01000100

Gain_l [12:0] Gain applied to ch-long data in 5.8 format
Gain_m [12:0] Gain applied to ch-medium data in 5.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F98	R/W				Gain vs																Gain s													0x01000100

Gain_s [12:0] Gain applied to ch-short data in 5.8 format
Gain_vs [12:0] Gain applied to ch-vs data in 5.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30F9C	R/W					black level m																black level l												0x00000000

black_level_l [11:0] Sensor offset applied to ch-long data
black_level_m [11:0] Sensor offset applied to ch-medium data

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FA0	R/W					black level vs																black level s												0x00000000

black_level_s [11:0] Sensor offset applied to ch-short data
black_level_vs [11:0] Sensor offset applied to ch-veryshort data

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.13. frame stitch

4-exposure wide-dynamic-range blending

NOTE:
If the WDR is configured to stitch 2 exposures, then the configuration must be done through the LM_ pair the short exposures black level must be programmed through the med_black_level register so that the LM pair
can be used.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30FA4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
		output select														mode in		

mode_in [1:0]
0 : 4-exposure
1 : 2-exposure
2 : 3-exposure
3 : 4-exposure

output_select [7:0]
This register is only for debug purpose. for normal operation it must be kept in its default value (0)
0 : normal stitched output
1 : long data routed out
2 : medium data routed out
4 : short data routed out
8 : very short data routed out
16: LM stitched output taken out
32: MS stitched output taken out
64: SVS stitched output taken out
others: reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FA8	R/W					MS Exposure Ratio																LM Exposure Ratio												0x01000100

LM_Exposure_Ratio [11:0]
Sets ratio between long and medium exposures - this must match the actual exposure ratio on the sensor
Format: unsigned 6.6-bit fixed-point

MS_Exposure_Ratio [11:0]
Sets ratio between medium and short exposures - this must match the actual exposure ratio on the sensor
Format: unsigned 6.6-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FAC	R/W																					SVS Exposure Ratio												0x00000100

SVS_Exposure_Ratio [11:0]
Sets ratio between short and very short exposures - this must match the actual exposure ratio on the sensor
Format: unsigned 6.6-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FB0	R/W					LM Thresh low																LM Thresh high												0x0C000F00

LM_Thresh_high [11:0] These two thresholds are for LM pairs. Both are with respect to the longer stitches. Data above this threshold will be taken from short exposure only

LM_Thresh_low [11:0] Data below this threshold will be taken from long exposure only

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FB4	R/W					MS Thresh low																MS Thresh high												0x0C000F00

MS_Thresh_high [11:0] These two thresholds are for MS pairs. Both are with respect to the longer stitches. Data above this threshold will be taken from short exposure only

MS_Thresh_low [11:0] Data below this threshold will be taken from long exposure only

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FB8	R/W					SVS Thresh low																SVS Thresh high												0x0C000F00

SVS_Thresh_high [11:0] These two thresholds are for SVS pairs. Both are with respect to the longer stitches. Data above this threshold will be taken from short exposure only

SVS_Thresh_low [11:0] Data below this threshold will be taken from long exposure only

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FBC	R/W					Black level Medium																Black level long												0x00000000

Black_level_long [11:0] Black level for long exposure input

Black_level_Medium [11:0] Black level for medium exposure input
*** NOTE ***:
If the wdr unit is configured to use as 2-exposure, THIS REGISTER POSITION must contain the black level of
short exposure as the LM pair is used for all other configurations

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FC0	R/W					Black level very Short																Black level Short												0x00000000

Black_level_Short [11:0] Black level for short exposure input

Black_level_very_Short [11:0] Black level for very short exposure input

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FC4	R/W													Black level Out																				0x00000000

Black_level_Out [19:0] Black level for module output

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FC8	R/W					MS NP mult																LM NP mult												0x06000180

LM_NP_mult [11:0] The noise profile weights are multiplied by this value to give expected noise amplitude.

MS_NP_mult [11:0] The noise profile weights are multiplied by this value to give expected noise amplitude.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FCC	R/W					LM Alpha MOV slope																SVS NP mult												0x0C000600

SVS_NP_mult [11:0] The noise profile weights are multiplied by this value to give expected noise amplitude.

LM_Alpha_MOV_slope [11:0] This defines the gradient of the motion alpha ramp. Higher values mean a steeper ramp and so a more rapid transition between
non-motion-corrected and motion-corrected regions.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FD0	R/W					SVS Alpha MOV slope																MS Alpha MOV slope												0x01800180

MS_Alpha_MOV_slope [11:0] his defines the gradient of the motion alpha ramp. Higher values mean a steeper ramp and so a more rapid transition between
non-motion-corrected and motion-corrected regions.

SVS_Alpha_MOV_slope [11:0] his defines the gradient of the motion alpha ramp. Higher values mean a steeper ramp and so a more rapid transition between
non-motion-corrected and motion-corrected regions.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FD4	R/W					Gain B																Gain R												0x01000100

Gain_R [11:0] Multiplier for color channel R
Format: unsigned 4.8-bit fixed-point

Gain_B [11:0] Multiplier for color channel B
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FD8	R/W																					Consistency thresh mov												0x00000100

Consistency_thresh_mov [11:0] Pixel consistency reporting - motion threshold
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FDC	R/W													Consistency thresh lvl																				0x00080000

Consistency_thresh_lvl [19:0] Pixel consistency reporting - flicker threshold
Format: unsigned 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x30FE0	R/W											lm neg weight						0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
				lm pos weight								lm noise thresh						

lm_noise_thresh [5:0] Higher values make it more likely to interpret differences between the long and medium exposures as noise (and thus do no motion correction).

lm_pos_weight [5:0] Lower values make it more likely to interpret differences between the long and medium exposures as noise (and thus do no motion correction).

lm_neg_weight [5:0] Higher values make it more likely to interpret differences between the long and medium exposures as noise (and thus do no motion correction).

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FE4	R/W					lm med noise intensity thresh																lm med noise alpha thresh												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FE8	R/W											lm mc blend slope																						0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FEC	R/W					lm mc blend offset																				lm mc blend thresh								0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FF0	R/W											lm mc thresh slope																						0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FF4	R/W													lm mc thresh thresh																				0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FF8	R/W																					lm mc thresh offset												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x30FFC	R/W											lm mc mag thresh slope																						0x00000000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31000	R/W													lm mc mag thresh thresh																				0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31004	R/W					lm mc mag lblend thresh																lm mc mag thresh offset												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31008	R/W									Exposure mask thresh												MCoff WB offset												0x00200000

Exposure_mask_thresh [7:0] Threshold for selection of exposure mask in blending regions. Where the alpha value is above this value the shorter exposure will be indicated.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3100C	R/W																lm alg select	0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
									mcoff mode enable						MCoff NC Enable	use 3x3 max	bwb select	

lm_alg_select Select which L/M stitching algorithm to use.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31010	R/W					MCoff M max																MCoff L max												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31014	R/W					MCoff vs max																MCoff S max												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31018	R/W					MCoff LM scaler																MCoff L scaler												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3101C	R/W					MCoff NC thresh low																MCoff LMS scaler												0x00000000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31020	R/W					MCoff NC scale																MCoff NC thresh high												0x00000000

35.14. frame stitch NP LUT VS

Noise profile for short exposure data at frame stitch

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31024	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x31028	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x310A0	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x31024 + 4 * int(i / 4).

35.15. frame stitch NP LUT S

Noise profile for med2 exposure data at frame stitch

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x310A4	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x310A8	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x31120	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x310A4 + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

35.16. frame stitch NP LUT M

Noise profile for med1 exposure data at frame stitch

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31124	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x31128	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x311A0	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x31124 + 4 * int(i / 4).

35.17. frame stitch NP LUT L

Noise profile for long exposure data at frame stitch

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x311A4	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x311A8	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x31220	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x311A4 + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

35.18. decompander0

Frontend lookup (for companded WDR sensor inputs)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x31224	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Offset Mode				Enable	

Enable Frontend lookup0 enable: 0=off 1=on

Offset Mode Lookup0 reflection mode for black offset region
0 = Manual curve reflection
1 = Automatic curve reflection

35.19. decompander1

Frontend lookup (for companded WDR sensor inputs)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x31228	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Offset Mode				Enable	

Enable Frontend lookup0 enable: 0=off 1=on

Offset Mode Lookup0 reflection mode for black offset region
0 = Manual curve reflection
1 = Automatic curve reflection

35.20. digital gain

Digital gain for RAW sensor data

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3122C	R/W																				Gain													0x00000100

Gain [12:0] Gain applied to data in 5.8 format

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31230	R/W													Offset																				0x00000000

Offset [19:0] Data black level

35.21. sensor offset fe

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31234	R/W													offset 00																				0x00000000

offset 00 [19:0] offset offset for color channel 00 (R)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31238	R/W													offset 01																				0x00000000

offset 01 [19:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3123C	R/W													offset 10																				0x00000000

offset 10 [19:0] offset offset for color channel 10 (Gb)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31240	R/W													offset 11																				0x00000000

offset 11 [19:0] offset offset for color channel 11 (B)

35.22. sqrt

sensor offset for the sqrt module

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31244	R/W													black level in																				0x00000000

black_level_in [19:0] input Data black level

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31248	R/W																	black level out																0x00000000

black_level_out [15:0] output Data black level

35.23. raw frontend

RAW frontend processing

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3124C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000005
										bright disable	dark disable			show dynamic defect pixel	dp enable		ge enable	

ge enable Green equalization enable: 0=off, 1=on
dp enable Dynamic Defect Pixel enable: 0=off, 1=on
show dynamic defect pixel Show Defect Pixel: 0=off, 1=on
dark disable Disable detection of dark pixels
bright disable Disable detection of bright pixels

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31250	R/W																	debug sel																0x00000000

debug sel [15:0] Debug selection port

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31254	R/W					dp threshold																dp slope												0x00400200

dp slope [11:0] Slope for HP Mask function
dp threshold [11:0] Defect pixel threshold.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31258	R/W									dp blend								dpdev threshold																0x00000266

dpdev threshold [15:0] Controls the aggressiveness of the dynamic defect pixel correction near edges.
dp blend [7:0] Controls blending between non-directional and directional replacement values in dynamic defect pixel correction.
0x00 Replace detected defects with non-directional replacement value
0xFF Replace detected defects with directional replacement value

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3125C	R/W	ge threshold																								ge strength								0x04000000

ge strength [7:0] Controls strength of Green equalization. Set during calibration.
ge threshold [15:0] green equalization threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31260	R/W									ge sens												ge slope												0x008000AA

ge slope [11:0] Slope for GE Mask function
ge sens [7:0] Controls the sensitivity of green equalization to edges.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31264	R/W	Sigma In																line thresh																0x00000150

line thresh [15:0] Controls the directional nature of the dynamic defect pixel correction near edges..
Sigma In [15:0] Manual override of noise estimation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31268	R/W																	Thresh Long								Thresh Short								0x00003000

Thresh Short [7:0] Noise threshold for short exposure data
Format: unsigned 4.4-bit floating-point

Thresh Long [7:0] Noise threshold for long exposure data
Format: unsigned 4.4-bit floating-point

35.24. raw frontend np

Noise profile controls for RAW frontend

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3126C	R/W																	Exp Thresh																0x0000FFFF

Exp Thresh [15:0] Threshold for determining long/short exposure data

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31270	R/W																	Long Ratio								Short Ratio								0x00000420

Short Ratio [7:0] Multiplier applied to short exposure data for noise profile calculation
Format: unsigned 6.2-bit fixed-point

Long Ratio [7:0] Multiplier applied to long exposure data for noise profile calculation
Format: unsigned 6.2-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x31274	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
									NP off reflect		NP off							

NP off [6:0] Noise profile black level offset

NP off reflect Defines how values below black level are obtained.
0: Repeat the first table entry.
1: Reflect the noise profile curve below black level.

35.25. raw frontend np lut

Noise profile controls for RAW frontend

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31278	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x3127C	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x312F4	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x31278 + 4 * int(i / 4).

35.26. defect pixel

Detection and processing of static defect-pixels

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x312FC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Detection enable	Show Static Defect Pixels	Correction Enable	Show Reference	

Show Reference For debug purposes. Show reference values which are compared with actual values to detect bad pixels
Correction Enable Correction enable: 0=off 1=on
Show Static Defect Pixels Show which pixels have been detected as bad
Detection enable Starts detection

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x31300	R/O					Table Start												--
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
					Defect Pixel Count												Overflow	

Overflow Table overflow flag
Defect Pixel Count [11:0] Number of defect-pixels detected
Table Start [11:0] Address of first defect-pixel in defect-pixel store

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31304	R/W																					Defect Pixel Count In												0x00000000

Defect Pixel Count In [11:0] Number of defect-pixels in the written table

35.27. sinter

Spatial noise reduction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x31308	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x0000001C
										rm enable	Int select	Filter select	Enable	Rsvd	Rsvd	Rsvd	Rsvd	

Enable Sinter enable: 0=off 1=on
Filter select Sinter filter fine tuning. Should not be modified from suggested values.
Int select Select intensity filter. Should not be modified from suggested values.
rm_enable Adjusts sinter strength radially from center to compensate for Lens shading correction. enable: 0=off, 1=on

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3130C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000034
										Rsvd	Rsvd	nonlinear wkgen	nlm en	int config				

int_config [3:0] Intensity blending with mosaic raw
nlm_en This config is only valid fr sinter3
Enables (1) or disables (0) the NLM filter
nonlinear_wkgen This config is only valid fr sinter3
Enables (1) or disables (0) nonlinear weight generation

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31310	R/W																									sad filt thresh								0x00000009

sad_filt_thresh [7:0] Block match difference filtering threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31314	R/W	rm center y																rm center x																0x01680280

rm_center_x [15:0] Center x coordinate of shading map
rm_center_y [15:0] Center y coordinate of shading map

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31318	R/W																	rm off center mult																0x00000100

rm_off_center_mult [15:0] Normalizing factor which scales the radial table to the edge of the image.
Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3131C	R/W	Thresh 4h								Thresh 2h								Thresh 1h								Thresh 0h								0x00000000

Thresh 0h [7:0] Noise threshold for high horizontal spatial frequencies
Thresh 1h [7:0] Noise threshold for high horizontal spatial frequencies
Thresh 2h [7:0] Noise threshold for low horizontal spatial frequencies
Thresh 4h [7:0] Noise threshold for low horizontal spatial frequencies

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31320	R/W	Thresh 4v								Thresh 2v								Thresh 1v								Thresh 0v								0x00000000

Thresh 0v [7:0] Noise threshold for high vertical spatial frequencies
Thresh 1v [7:0] Noise threshold for high vertical spatial frequencies
Thresh 2v [7:0] Noise threshold for low vertical spatial frequencies
Thresh 4v [7:0] Noise threshold for low vertical spatial frequencies

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31324	R/W	Strength 4								Strength 2								Strength 1								Strength 0								0xFFFFFFFF

Strength 0 [7:0] Unused - no effect
Strength 1 [7:0] Noise reduction effect for high spatial frequencies
Strength 2 [7:0] Unused - no effect
Strength 4 [7:0] Noise reduction effect for low spatial frequencies

35.28. sinter Noise Profile

Noise profile controls for Sinter

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x31328	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000803
		global offset													Black Reflect	use exp mask	use LUT	

use LUT 1 = use LUT data
0 = use exposure mask provided by Frame stitching or threshold
use_exp_mask 1 = use exposure mask provided by Frame stitching or threshold
Black Reflect Specifies how to deal with data below black level. 0: Clip to zero, 1: Reflect.
global offset [7:0] A global offset that will be added to each of the hlog... values above..

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3132C	R/W																	Black Level																0x00000000

Black Level [15:0] Black level offset for Mode 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31330	R/W																	Thresh1																0x00004000

Thresh1 [15:0] Exposure thresholds. Used to determine which exposure generated the current pixel.
Pixels with a value greater than or equal to a given threshold will be deemed to have been generated by the shorter exposure.
Pixels with a value less than a given threshold will be deemed to have been generated by the longer exposure.

E.G. Where 4 exposures are used:
VS >= Thresh 3 > S >= Thresh 2 > M >= Thresh 1 > L

For 3 exposures set Thresh 1 to 0
For 2 exposures set Thresh 1 and Thresh 2 to 0
For 1 exposures set all exposure thresholds to 0

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31334	R/W																	Thresh2																0x00008000

Thresh2 [15:0] See above.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x31338	R/W																	Thresh3																0x0000C000

Thresh3 [15:0] See above.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3133C	R/W	noise level 3								noise level 2								noise level 1								noise level 0								0x00000000

noise_level_0 [7:0] Noise level of VS exposure
noise_level_1 [7:0] Noise level of S exposure
noise_level_2 [7:0] Noise level of M exposure
noise_level_3 [7:0] Noise level of L exposure

35.29. sinter Noise Profile LUT

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x313F8	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x313FC	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x31474	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x313F8 + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.30. sinter shading

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x329B8	R/W	rm shading lut(3)								rm shading lut(2)								rm shading lut(1)								rm shading lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x329BC	R/W	rm shading lut(7)								rm shading lut(6)								rm shading lut(5)								rm shading lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x329D4	R/W	rm shading lut(31)								rm shading lut(30)								rm shading lut(29)								rm shading lut(28)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x329D8	R/W																									rm shading lut(32)								--

rm_shading_lut [7:0] Radial Sinter LUT. See ISP guide for more details

This is an array of 33 8-bit registers. The address for element (i) is: 0x329B8 + 4 * int(i / 4).

35.31. temper

Temporal noise reduction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x329DC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																Temper2 Mode	Enable	

Enable Temper enable: 0=off 1=on

Temper2 Mode 0: 0=Temper3 mode 1=Temper2 mode

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x329E4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000202
		Delta												Recursion Limit				

Recursion Limit [3:0] Controls length of filter history. Low values result in longer history and stronger temporal filtering.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.32. temper Noise Profile

Noise profile controls for Temper

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x329E8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000803
		global offset													Black Reflect	use exp mask	use LUT	

use LUT 1 = use LUT data
0 = use exposure mask provided by Frame stitching or threshold

use_exp_mask 1 = use exposure mask provided by Frame stitching or threshold

Black Reflect Specifies how to deal with data below black level. 0: Clip to zero, 1: Reflect.

global offset [7:0] A global offset that will be added to each of the hlog... values above..

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x329EC	R/W																	Black Level																0x00000000

Black Level [15:0] Black level offset for Mode 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x329F0	R/W																	Thresh1																0x00004000

Thresh1 [15:0] Exposure thresholds. Used to determine which exposure generated the current pixel.
Pixels with a value greater than or equal to a given threshold will be deemed to have been generated by the shorter exposure.
Pixels with a value less than a given threshold will be deemed to have been generated by the longer exposure.

E.G. Where 4 exposures are used:
VS >= Thresh 3 > S >= Thresh 2 > M >= Thresh 1 > L

For 3 exposures set Thresh 1 to 0
For 2 exposures set Thresh 1 and Thresh 2 to 0
For 1 exposures set all exposure thresholds to 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x329F4	R/W																	Thresh2																0x00008000

Thresh2 [15:0] See above.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x329F8	R/W																	Thresh3																0x0000C000

Thresh3 [15:0] See above.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x329FC	R/W	noise level 3								noise level 2								noise level 1								noise level 0								0x00000000

noise_level_0 [7:0] Noise level of VS exposure
noise_level_1 [7:0] Noise level of S exposure
noise_level_2 [7:0] Noise level of M exposure
noise_level_3 [7:0] Noise level of L exposure

35.33. temper Noise Profile LUT

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32AB8	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x32ABC	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x32B34	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT. Calculated during calibration process.

This is an array of 128 8-bit registers. The address for element (i) is: 0x32AB8 + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.34. temper dma

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32B38	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x0000000F
							temper dw							Frame read on LSB dma	Frame read on MSB dma	Frame write on LSB dma	Frame write on MSB dma	

Frame write on MSB dma This must be set to 1 only in Temper-3 mode
Frame write on LSB dma This must be set to 1 whenever Temper (either T2 or T3 mode) is enabled
Frame read on MSB dma This must be set to 1 only in Temper-3 mode
Frame read on LSB dma This must be set to 1 whenever Temper (either T2 or T3 mode) is enabled
temper_dw 0: 16bit valid data
1: upto 12 bit valid data, MSB aligened to 16 bit

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B3C	R/W																									format								0x00000014

format [7:0] 20: for 16bit data both in T3 and T2 modes
6 : for 12bit data both in T3 and T2 modes

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B40	R/O	blk status																																--

blk_status [31:0]

The bits are defined as follows:
0 Write FIFO Fail (Full)
1 Write FIFO Fail (Empty)
2 Read FIFO Fail (Full)
3 Read FIFO Fail (Empty)
4 Pack Fail (Overflow)
5 Unpack Fail (Overflow)
6 Writer fail (Active Width)
7 Writer fail (Active Height)
8 Writer fail (Interline blanking)
9 Writer fail (Interframe blanking)
10 Reader fail (Active Width)
11 Reader fail (Active Height)
12 Reader fail (Interline blanking)
13 Reader fail (Interframe blanking)
14 0
15 0
16 Writer fail (A resp)
17 Writer fail (AW wait)
18 Writer fail (W wait)
19 Writer fail (Outstanding Transactions)
20 Reader fail (AR wait)
21 Reader fail (R resp)
22 Reader fail (Oustanding Transfers)
23 0
24 intw_fail_user_intfc_sig
25 intr_fail_user_intfc_sig
26 0
27 0
28 0
29 0
30 0
31 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B44	R/W	msb bank base writer																																0x00000000

msb_bank_base_writer [31:0]

base address for frame buffer, should be word-aligned. This is used only in 16bit temper3 mode.
In 16bit temper3 mode, each 40 bit temper data (32bit data+8bit meta data) is split into 2 chunks and each
is stored in one of the buffers. The MSB part is stored into this buffer

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B48	R/W	lsb bank base writer																																0x00000000

lsb_bank_base_writer [31:0] base address for frame buffer, should be word-aligned. This is used all the times temper is used..
In 16bit temper3 mode, each 40 bit temper data (32bit data+8bit meta data) is split into 2 chunks and each
is stored in one of the buffers. The LSB part is stored into this buffer.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B4C	R/W	msb bank base reader																																0x00000000

msb_bank_base_reader [31:0] base address for frame buffer, should be word-aligned. This is used only in 16bit temper3 mode.
In 16bit temper3 mode, each 40 bit temper data (32bit data+8bit meta data) is split into 2 chunks and each
is stored in one of the buffers. The MSB part is stored into this buffer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B50	R/W	lsb bank base reader																																0x00000000

lsb_bank_base_reader [31:0] base address for frame buffer, should be word-aligned. This is used all the times temper is used..
In 16bit temper3 mode, each 40 bit temper data (32bit data+8bit meta data) is split into 2 chunks and each
is stored in one of the buffers. The LSB part is stored into this buffer.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B54	R/W	Line offset																																0x00001000

Line_offset [31:0] Indicates the offset in bytes from the start of one line to the next line.
This value should be equal to or larger than one line of image data and should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32B58	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000002
																linetick eol		

linetick_eol linetick start/end of line control. 0 = use start of line, 1 = use end of line

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B60	R/W	linetick repeat																linetick first																0x00000040

linetick_first [15:0] line number of first linetick. 0 = no linetick

linetick_repeat [15:0] line number of first linetick. 0 = no repeat

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32B68	R/W				Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F007E00
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
			Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	writer axi id multi	lsb writer axi id value				msb writer axi id value				

msb_writer_axi_id_value [3:0] value to send for awid, wid and expected on bid.

lsb_writer_axi_id_value [3:0] value to send for awid, wid and expected on bid.

writer_axi_id_multi 0= static value (axi_id_value) for awid/wid, 1 = incrementing value per transaction for awid/wid wrapping to 0 after axi_id_value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32B6C	R/W				Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F007E00
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
			Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd		lsb reader axi id value				msb reader axi id value				

msb_reader_axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = "0000"

lsb_reader_axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = "0000"

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

35.35. ca correction

Ca Correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32B70	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
												Mesh Scale					Enable	

Enable module enable, if 0 the data_i(dw*(kh-1)/2+dw-1 downto dw*(kh-1)/2) is presented at data_o after pipeline length

Mesh Scale [1:0] extra shift of mesh data: 00- no shift, 01- shift left by 1, ..., 11- shift left by 3, used to increase the range at cost of accuracy

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32B74	R/W										Mesh Height							0x00400040
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
											Mesh Width							

Mesh Width [6:0] number of tiles across. Maximum supported mesh width is 64.

Mesh Height [6:0] number of tiles vertically. Maximum supported mesh height is 64 for RGGB sensor and 42 for RGBIr sensors.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B78	R/W				Plane Offset																Line Offset													0x00400040

Line Offset [12:0] offset between lines of tiles, can differ from mesh_width, but its safe to keep same as mesh width

Plane Offset [12:0] offset between colour planes, can differ from line_offset*mesh_height

35.36. square be

sensor offset for the square module

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B80	R/W																	black level in																0x00000000

black_level_in [15:0] input Data black level

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B84	R/W													black level out																				0x00000000

black_level_out [19:0] output Data black level

35.37. sensor offset pre shading

offset offset subtraction for each color channel and exposure

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B88	R/W													offset 00																				0x00000000

offset 00 [19:0] offset offset for color channel 00 (R)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B8C	R/W													offset 01																				0x00000000

offset 01 [19:0] offset offset for color channel 01 (Gr)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B90	R/W													offset 10																				0x00000000

offset 10 [19:0] offset offset for color channel 10 (Gb)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B94	R/W													offset 11																				0x00000000

offset 11 [19:0] offset offset for color channel 11 (B)

35.38. radial shading

Radial Lens shading correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32B98	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Enable	

Enable Lens shading correction enable: 0=off, 1=on

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32B9C	R/W	centerR y																centerR x																0x021C03C0

centerR x [15:0] Center x coordinate of the red shading map
centerR y [15:0] Center y coordinate of the red shading map

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BA0	R/W	centerG y																centerG x																0x021C03C0

centerG x [15:0] Center x coordinate of the green shading map
centerG y [15:0] Center y coordinate of the green shading map

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BA4	R/W	centerB y																centerB x																0x021C03C0

centerB x [15:0] Center x coordinate of the blue shading map
centerB y [15:0] Center y coordinate of the blue shading map

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BA8	R/W	centerIr y																centerIr x																0x021C03C0

centerIr x [15:0] Center x coordinate of the IR shading map
centerIr y [15:0] Center y coordinate of the IR shading map

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BAC	R/W	off center multRy																off center multRx																0x06EA06EA

off center multRx [15:0] Normalizing X factor which scales the Red radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.
off center multRy [15:0] Normalizing Y factor which scales the Red radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BB0	R/W	off center multGy																off center multGx																0x06EA06EA

off center multGx [15:0] Normalizing X factor which scales the green radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.
off center multGy [15:0] Normalizing Y factor which scales the green radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BB4	R/W	off center multBy																off center multBx																0x06EA06EA

off center multBx [15:0] Normalizing X factor which scales the blue radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

off center multBy [15:0] Normalizing Y factor which scales the blue radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BB8	R/W	off center multIRy																off center multIRx																0x06EA06EA

off center multIRx [15:0] Normalizing X factor which scales the Ir radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

off center multIRy [15:0] Normalizing Y factor which scales the Ir radial table to the edge of the image. Calculated as 2^31/R^2 where R is the furthest distance from the center coordinate to the edge of the image in pixels.

35.39. mesh shading

Mesh Lens shading correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32BBC	R/W			Mesh height								Mesh width						0x3F3FE406
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		Mesh page Ir		Mesh page B		Mesh page G		Mesh page R			Mesh alpha mode		Mesh scale			Mesh show	Enable	

Enable Lens shading correction enable: 0=off, 1=on

Mesh show Lens shading correction debug: 0=off, 1=on (show mesh data)

Mesh scale [2:0] Selects the precision and maximal gain range of mesh shading correction
Gain range: 00- 0..2; 01- 0..4; 02- 0..8; 03- 0..16; 04- 1..2; 05- 1..3; 06- 1..5; 07- 1..9(float)

Mesh alpha mode [1:0] Sets alpha blending between mesh shading tables.
0 = no alpha blending;
1=2 banks (odd/even bytes)
2=4 banks (one per 8 bit lane in each dword)

Mesh page R [1:0] Selects memory page for red pixels correction. See ISP guide for further details

Mesh page G [1:0] Selects memory page for green pixels correction. See ISP guide for further details

Mesh page B [1:0] Selects memory page for blue pixels correction. See ISP guide for further details

Mesh page Ir [1:0] Selects memory page for IR pixels correction. See ISP guide for further details

Mesh width [5:0] Number of horizontal nodes minus 1

Mesh height [5:0] Number of vertical nodes minus 1

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32BC4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
						Mesh alpha bank Ir			Mesh alpha bank B			Mesh alpha bank G			Mesh alpha bank R			

Mesh alpha bank R [2:0] Bank selection for R blend: 0: 0+1; 1: 1+2; 2: 2:3; 3: 3+0; 4:0+2; 5: 1+3; 6,7: reserved
Mesh alpha bank G [2:0] Bank selection for G blend: 0: 0+1; 1: 1+2; 2: 2:3; 3: 3+0; 4:0+2; 5: 1+3; 6,7: reserved:
Mesh alpha bank B [2:0] Bank selection for B blend: 0: 0+1; 1: 1+2; 2: 2:3; 3: 3+0; 4:0+2; 5: 1+3; 6,7: reserved
Mesh alpha bank Ir [2:0] Bank selection for Ir blend: 0: 0+1; 1: 1+2; 2: 2:3; 3: 3+0; 4:0+2; 5: 1+3; 6,7: reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BC8	R/W	Mesh alpha Ir								Mesh alpha B								Mesh alpha G								Mesh alpha R								0x00000000

Mesh alpha R [7:0] Alpha blend coeff for R
Mesh alpha G [7:0] Alpha blend coeff for G
Mesh alpha B [7:0] Alpha blend coeff for B
Mesh alpha Ir [7:0] Alpha blend coeff for IR

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BCC	R/W																	Mesh strength																0x00001000

Mesh strength [15:0] Mesh strength in 4.12 format, e.g. 0 - no correction, 4096 - correction to match mesh data. Can be used to reduce shading correction based on AE.

35.40. white balance

Static white balance - independent gain for each color channel

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BD0	R/W					Gain 01																Gain 00												0x01000100

Gain 00 [11:0] Multiplier for color channel 00 (R)
Format: unsigned 4.8-bit fixed-point
Gain 01 [11:0] Multiplier for color channel 01 (Gr)
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BD4	R/W					Gain 11																Gain 10												0x01000100

Gain 10 [11:0] Multiplier for color channel 10 (Gb)
Format: unsigned 4.8-bit fixed-point
Gain 11 [11:0] Multiplier for color channel 11 (B)
Format: unsigned 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

35.41. white balance aexp

Static white balance - independent gain for each color channel

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BD8	R/W					Gain 01																Gain 00												0x01000100

Gain 00 [11:0] Multiplier for color channel 00 (R)
Format: unsigned 4.8-bit fixed-point

Gain 01 [11:0] Multiplier for color channel 01 (Gr)
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BDC	R/W					Gain 11																Gain 10												0x01000100

Gain 10 [11:0] Multiplier for color channel 10 (Gb)
Format: unsigned 4.8-bit fixed-point

Gain 11 [11:0] Multiplier for color channel 11 (B)
Format: unsigned 4.8-bit fixed-point

35.42. iridix gain

Digital gain for RAW sensor data

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BE0	R/W																					Gain												0x00000100

Gain [11:0] Gain applied to data in 4.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BE4	R/W													Offset																				0x00000000

Offset [19:0] Data black level

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.43. iridix

Iridix is an adaptive, space-variant tone mapping engine.
It is used to maintain or enhance shadow detail while preserving highlights.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32BE8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00004629
		stat mult					Rsvd	Rsvd	Rsvd		postgamma pos	black level amp0		max alg type			iridix on	

iridix_on Iridix enable: 0=off 1=on
max_alg_type Max Bayer Algorithm Type.
black_level_amp0 1=Ignore Black level (set to zero) in amplificator. 0=Use Black level value.
postgamma_pos PosGamma application 0=gain 1=data

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32BEC	R/W									slope min								0x00408012
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		slope max								variance intensity				variance space				

variance_space [3:0] Sets the degree of spatial sensitivity of the algorithm(Irdx7F)
variance_intensity [3:0] Sets the degree of luminance sensitivity of the algorithm(Irdx7F)
slope_max [7:0] Restricts the maximum slope (gain) which can be generated by the adaptive algorithm
slope_min [7:0] Restricts the minimum slope (gain) which can be generated by the adaptive algorithm

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BF0	R/W													black level																				0x00000000

black_level [19:0] Iridix black level. Values below this will not be affected by Iridix.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BF4	R/W													white level																				0x0000FFFF

white_level [19:0] Iridix white level. Values above this will not be affected by Iridix.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32BF8	R/W																					collection correction												0x00000100

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32BFC	R/W							strength inroi										0x02000101
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
								rev percept control								fwd percept control		

fwd_percept_control [1:0] Iridix gamma processing select: 0=pass through 1=gamma_dl 2=sqrt 3=gamma_lut.
rev_percept_control [1:0] Iridix gamma processing select: 0=pass through 1=gamma_dl 2=sqrt 3=gamma_lut.
strength_inroi [9:0] Manual Strength value for inside of ROI

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32C00	R/W																							strength outroi										0x00000200

strength_outroi [9:0] Manual Strength value for outside of ROI

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32C04	R/W	roi hor end																roi hor start																0xFFFF0000

roi_hor_start [15:0] Horizontal starting point of ROI
roi_hor_end [15:0] Horizontal ending point of ROI

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32C08	R/W	roi ver end																roi ver start																0xFFFF0000

roi_ver_start [15:0] Vertical starting point of ROI
roi_ver_end [15:0] Vertical ending point of ROI

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32C0C	R/W	contrast								bright pr								0xB0A00001
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						svariance											filter mux	

filter_mux Selects between Iridix8 and Iridix7, 1=Iridix8 and 0=Iridix7
svariance [3:0] Iridix8 transform sensitivity to different areas of image
bright_pr [7:0] Manual Bright_Preserve value to control Iridix core
contrast [7:0] Iridix8 contrast control parameter

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32C10	R/W																	dark enh																0x00001000

dark_enh [15:0] Manual Dark_Enhance value to control Iridix core

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32C14	R/W															fwd alpha																		0x00000100

fwd_alpha [17:0] alpha for gamma_dl

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32C18	R/W															rev alpha																		0x00001000

rev_alpha [17:0] alpha for gamma_dl

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32C1C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																context no		

context_no [1:0] Context id of a input Frame

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32C20	R/W													wb offset																				0x00000000

wb_offset [19:0] White balance offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32C24	R/W					gain gr																gain r												0x01000100

gain_r [11:0] White balance gain for R
Format: unsigned 4.8-bit fixed-point

gain_gr [11:0] White balance gain for GR
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32C28	R/W					gain b																gain gb												0x01000100

gain_gb [11:0] White balance gain for GB
Format: unsigned 4.8-bit fixed-point

gain_b [11:0] White balance gain for B
Format: unsigned 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32C2C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	GTm select	

GTm_select Global Tone map select : 0 : Local TM 1: Full Global TM

35.44. iridix LUT

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32C30	R/W													Asymmetry LUT(0)																				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x32C34	R/W													Asymmetry LUT(1)																				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x32D30	R/W													Asymmetry LUT(64)																				--

Asymmetry LUT [19:0] Iridix target curve.

This is an array of 65 20-bit registers. The address for element (i) is: 0x32C30 + 4i.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32D34	R/W													GlobalTM X LUT(0)																				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x32D38	R/W													GlobalTM X LUT(1)																				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x32DB4	R/W													GlobalTM X LUT(32)																				--

This is an array of 33 20-bit registers. The address for element (i) is: 0x32D34 + 4i.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32DB8	R/W													GlobalTM Y LUT(0)																				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x32DBC	R/W													GlobalTM Y LUT(1)																				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x32E38	R/W													GlobalTM Y LUT(32)																				--

This is an array of 33 20-bit registers. The address for element (i) is: 0x32DB8 + 4i.

35.45. demosaic rgb

Bayer Demosaic

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E3C	R/W	UU Slope								VA Slope								AA Slope								VH Slope								0xADAAC0C0

VH Slope [7:0] Slope of vertical/horizontal blending threshold in 4.4 logarithmic format.
High values will tend to favor one direction over the other (depending on VH Thresh) while lower values will give smoother blending.

AA Slope [7:0] Slope of angular (45/135) blending threshold in 4.4 format.
High values will tend to favor one direction over the other (depending on AA Thresh) while lower values will give smoother blending.

VA Slope [7:0] Slope of VH-AA blending threshold in 4.4 log format.
High values will tend to favor one direction over the other (depending on VA Thresh) while lower values will give smoother blending.

UU Slope [7:0] Slope of undefined blending threshold in 4.4 logarithmic format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E40	R/W																									Sat Slope								0x0000005D

Sat Slope [7:0] Slope of saturation blending threshold in linear format 2.6

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E44	R/W					AA Thresh																VH Thresh												0x00A00131

VH Thresh [11:0] Threshold for the range of vertical/horizontal blending
The threshold defines the difference of vertical and horizontal gradients at which the vertical gradient will
start to be taken into account in the blending (if VH Offset is set to 0).
Setting the offset not null (or the slope low) will include proportion of the vertical gradient in the blending before even the gradient difference reaches the threshold (see VH Offset for more details).

AA Thresh [11:0] Threshold for the range of angular (45/135) blending.
The threshold defines the difference of 45 and 135 gradients at which the 45 gradient will start to be taken into account in the
blending (if AA Offset is set to 0).
Setting the offset not null (or the slope low) will include proportion of the 45 gradient in the blending before
even the gradient difierence reaches the threshold (see AA Offset for more details).

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E48	R/W					UU Thresh																VA Thresh												0x01710070

VA Thresh [11:0] Threshold for the range of VH-AA blending.
The threshold defines the difference of VH and AA gradients at which the VH gradient will start to be taken into account in the blending
(if VA Offset is set to 0). Setting the offset not null (or the slope low) will include proportion of the VH gradient
in the blending before even the gradient difference reaches the threshold (see VA Offiset for more details).

UU Thresh [11:0] Threshold for the range of undefined blending

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E4C	R/W					lum thresh																Sat Thresh												0x00600171

Sat Thresh [11:0] Threshold for the range of saturation blending in signed 2.9 format
lum_thresh [11:0] Luminance threshold for directional sharpening

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E50	R/W					AA Offset																VH Offset												0x08000800

VH Offset [11:0] Offset for vertical/horizontal blending threshold
AA Offset [11:0] Offset for angular (A45/A135) blending threshold.
This register has great impact on how AA Thresh is used.
Setting this register to a value offset tells the blending process to weight the 45 and 135 gradients,
at the threshold, with respectively offset/16 and 255 - (offset/16).
If AA Thresh not equals to 0, these same blending weights apply from -AA Thresh to +AA Thresh.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E54	R/W					UU Offset																VA Offset												0x00000800

VA Offset [11:0] Offset for VH-AA blending threshold. This register has great impact on how VA Thresh is used.
Setting this register to a value offset tells the blending process to weight the VH and AA gradients,
at the threshold, with respectively offset/16 and 255 - (offset/16).
If VA Thresh not equals to 0, these same blending weights apply from -VA Thresh to +VA Thresh.

UU Offset [11:0] Offset for undefined blending threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E5C	R/W									np offset								sharp alt ud								sharp alt d								0x00002030

sharp_alt_d [7:0] Directional sharp mask strength in signed 4.4 format
sharp_alt_ud [7:0] Non-directional sharp mask strength in signed 4.4 format
np_offset [7:0] Noise profile offset in logarithmic 4.4 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E60	R/W																									Dmsc config								0x00000000

Dmsc config [7:0] Debug output select. Set to 0x00 for normal operation.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E64	R/W									AC Slope												AC Thresh												0x00CF01B3

AC Thresh [11:0] Threshold for the range of AC blending in signed 2.9 format
AC Slope [7:0] Slope of AC blending threshold in linear format 2.6

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E68	R/W									FC Alias Thresh								FC Alias Slope								FC Slope								0x00005580

FC Slope [7:0] Slope (strength) of false color correction
FC Alias Slope [7:0] Slope (strength) of false colour correction after blending with saturation value in 2.6 unsigned format
FC Alias Thresh [7:0] Threshold of false colour correction after blending with saturation valuet in in 0.8 unsigned format

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32E6C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										NP off reflect	NP off							

NP off [6:0] Noise profile black level offset

NP off reflect Defines how values below black level are obtained.
0: Repeat the first table entry.
1: Reflect the noise profile curve below black level.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E70	R/W	sad amp								sharp alt lu								sharp alt ldu								sharp alt ld								0x10101010

sharp_alt_ld [7:0] Sharpen strength for L_Ld in unsigned 4.4 format

sharp_alt_ldu [7:0] Sharpen strength for L_Ldu in unsigned 4.4 format

sharp_alt_lu [7:0] Sharpen strength for L_Lu in unsigned 4.4 format

sad_amp [7:0] Sad amplifier in unsigned 4.4 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E74	R/W																				min d strength													0x00001F33

min_d_strength [12:0] Min threshold for the directional L_L in signed 2's complement s.12 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E78	R/W																				min ud strength													0x00001F48

min_ud_strength [12:0] Min threshold for the un-directional L_Lu in signed 2's complement s.12 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32E7C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	sharpen alg select	

sharpen_alg_select To select new sharp algorithm or not

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E80	R/W									grey det thresh								lg det thresh								UU SH Slope								0x00080880

UU SH Slope [7:0] Slope of undefined blending threshold in 4.4 logarithmic format

lg_det_thresh [7:0] Level to which the green channel is considered low in which case the gradient is calculated using only the blue and red channels

grey_det_thresh [7:0] Threshold applied to the inter-channel difference for detecting grey region

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E84	R/W					UU SH Offset																UU SH Thresh												0x00000008

UU SH Thresh [11:0] Threshold for the range of undefined blending
UU SH Offset [11:0] Offset for undefined blending threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E88	R/W	grey det slope																lg det slope																0x10688000

lg_det_slope [15:0] Control the ramp of the linear thresholding for the low green detector
grey_det_slope [15:0] Control the ramp of the linear thresholding for the grey detector

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E8C	R/W				max ud strength																max d strength													0x03330333

max_d_strength [12:0] Max threshold for the directional L_L in signed 2's complement s1+0.12 format
max_ud_strength [12:0] Max threshold for the undirectional L_Lu in signed 2's complement s1+0.12 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E90	R/W									luma offset low d												luma thresh low d												0x00000008

luma_thresh_low_d [11:0] Intensity values above this value will be sharpen
luma_offset_low_d [7:0] Linear threshold offset corresponding to luma_thresh_low_d

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E94	R/W													luma slope low d																				0x00004000

luma_slope_low_d [19:0] Linear threshold slope corresponding to luma_thresh_low_d

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E98	R/W					luma thresh high d																												0x0FA00000

luma_thresh_high_d [11:0] Intensity values below this value will be sharpen

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32E9C	R/W													luma slope high d																				0x00004000

luma_slope_high_d [19:0] Linear threshold slope corresponding to luma_thresh_high_d

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32EA0	R/W									luma offset low ud												luma thresh low ud												0x00000008

luma_thresh_low_ud [11:0] Intensity values above this value will be sharpen
luma_offset_low_ud [7:0] Linear threshold offset corresponding to luma_thresh_low_ud

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32EA4	R/W													luma slope low ud																				0x00004000

luma_slope_low_ud [19:0] Linear threshold slope corresponding to luma_thresh_low_ud

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32EA8	R/W																					luma thresh high ud												0x00000FA0

luma_thresh_high_ud [11:0] Intensity values below this value will be sharpen

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32EAC	R/W													luma slope high ud																				0x00004000

luma_slope_high_ud [19:0] Linear threshold slope corresponding to luma_thresh_high_ud

35.46. demosaic rgb Noise Profile

Bayer Demosaic lookup

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32EB0	R/W	Weight lut(3)								Weight lut(2)								Weight lut(1)								Weight lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x32EB4	R/W	Weight lut(7)								Weight lut(6)								Weight lut(5)								Weight lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x32F2C	R/W	Weight lut(127)								Weight lut(126)								Weight lut(125)								Weight lut(124)								--

Weight lut [7:0] Noise profile LUT

This is an array of 128 8-bit registers. The address for element (i) is: 0x32EB0 + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.47. demosaic rgbir

Demosaic rgbir Config

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32F30	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
															rgbir config			

rgbir_config [2:0] Debug related configurations to select out different internal signals, and normal RGBIR will be outputted by default

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F34	R/W																					clip level												0x00000E66

clip_level [11:0] clip level

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F38	R/W																					clip debloom												0x00000CCD

clip_debloom [11:0] clip level for debloom

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32F3C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	ir on blue row	

ir_on_blue_row to indicate that the IR is on the same line of Blue

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32F40	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	declip mode	

declip_mode Declip mode

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F44	R/W					gain b																gain r												0x01000100

gain_r [11:0] gain for red
gain_b [11:0] gain for blue

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F48	R/W					static gain b																static gain r												0x01000100

static_gain_r [11:0] static gain for red
static_gain_b [11:0] static gain for red

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F4C	R/W																					static gain i												0x00000100

static_gain_i [11:0] static gain for ir

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F50	R/W																					interpolation directionality												0x00000400

interpolation_directionality [11:0] Interpolation Directionality

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F54	R/W																					sharp limit												0x000005C8

sharp_limit [11:0] sharp limit

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F58	R/W																					sharp high												0x00000666

sharp_high [11:0] sharp high

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F5C	R/W																					sharp low												0x00000032

sharp_low [11:0] sharp low

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F60	R/W																					fc low												0x000008F2

fc_low [11:0] fc low

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F64	R/W																					fc grad												0x000000E6

fc_grad [11:0] fc grad

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F68	R/W					ir correct mat01																ir correct mat00												0x00000400

ir_correct_mat00 [11:0] ir correct mat 00
ir_correct_mat01 [11:0] ir correct mat 01

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F6C	R/W					ir correct mat03																ir correct mat02												0x00000000

ir_correct_mat02 [11:0] ir correct mat 02
ir_correct_mat03 [11:0] ir correct mat 03

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F70	R/W					ir correct mat11																ir correct mat10												0x04000000

ir_correct_mat10 [11:0] ir correct mat 10
ir_correct_mat11 [11:0] ir correct mat 11

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F74	R/W					ir correct mat13																ir correct mat12												0x00000000

ir_correct_mat12 [11:0] ir correct mat 12
ir_correct_mat13 [11:0] ir correct mat 13

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F78	R/W					ir correct mat21																ir correct mat20												0x00000000

ir_correct_mat20 [11:0] ir correct mat 20
ir_correct_mat21 [11:0] ir correct mat 21

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F7C	R/W					ir correct mat23																ir correct mat22												0x00000400

ir_correct_mat22 [11:0] ir correct mat 22
ir_correct_mat23 [11:0] ir correct mat 23

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F80	R/W					ir correct mat31																ir correct mat30												0x00000000

ir_correct_mat30 [11:0] ir correct mat 30
ir_correct_mat31 [11:0] ir correct mat 31

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F84	R/W					ir correct mat33																ir correct mat32												0x04000000

ir_correct_mat32 [11:0] ir correct mat 32
ir_correct_mat33 [11:0] ir correct mat 33

35.48. pf correction

purple fringing correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x32F88	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	use color corrected rgb	

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F8C	R/W																					hue strength												0x00000200

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F90	R/W					luma strength																sat strength												0x04000200

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F94	R/W									saturation strength												purple strength												0x00260400

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F98	R/W																	off center mult																0x00000F8F

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32F9C	R/W	center y																center x																0x02800168

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FA0	R/W																				ccm coeff rr													0x000001CB

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FA4	R/W																				ccm coeff rg													0x000010C1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FA8	R/W																				ccm coeff rb													0x0000100A

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FAC	R/W																				ccm coeff gr													0x00001028

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FB0	R/W																				ccm coeff gg													0x0000016D

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FB4	R/W																				ccm coeff gb													0x00001045

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FB8	R/W																				ccm coeff br													0x00000012

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FBC	R/W																				ccm coeff bg													0x000010AC

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FC0	R/W																				ccm coeff bb													0x0000019A

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FC4	R/W					sad offset																sad slope												0x00000001

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FC8	R/W																					sad thresh												0x00000148

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FCC	R/W					hue low offset																hue low slope												0x00000131

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FD0	R/W																					hue low thresh												0x00000733

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FD4	R/W					hue high offset																hue high slope												0x00000855

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FD8	R/W																					hue high thresh												0x000008E1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FDC	R/W					sat low offset																sat low slope												0x00000021

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FE0	R/W																					sat low thresh												0x000000A4

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FE4	R/W					sat high offset																sat high slope												0x0FFF0000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FE8	R/W																					sat high thresh												0x00000000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FEC	R/W					luma1 low offset																luma1 low slope												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FF0	R/W																					luma1 low thresh												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FF4	R/W					luma1 high offset																luma1 high slope												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FF8	R/W																					luma1 high thresh												0x00000000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x32FFC	R/W					luma2 low offset																luma2 low slope												0x00000140

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33000	R/W																					luma2 low thresh												0x000000CD

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33004	R/W					luma2 high offset																luma2 high slope												0x00000026

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33008	R/W																					luma2 high thresh												0x000001A0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3300C	R/W					hsl offset																hsl slope												0x00000024

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33010	R/W																					hsl thresh												0x00000000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33014	R/W																									debug sel								0x00000000

debug_sel [7:0]
0: normal operation
1: radial weight in 0.8 format
2: sad_mask in 0.12 format
3: hue mask in 0.12 format
4: saturation mask in 0.12 format
5: luma mask in 12.0 format
6: pf mask in 12.0 format

35.49. pf correction Shading

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33018	R/W	shading lut(3)								shading lut(2)								shading lut(1)								shading lut(0)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x3301C	R/W	shading lut(7)								shading lut(6)								shading lut(5)								shading lut(4)								--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33034	R/W	shading lut(31)								shading lut(30)								shading lut(29)								shading lut(28)								--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33038	R/W																									shading lut(32)								--

shading_lut [7:0] Radial Purple Fringe Correction LUT.

This is an array of 33 8-bit registers. The address for element (i) is: 0x33018 + 4 * int(i / 4).

35.50. ccm

Color correction on RGB data using a 3x3 color matrix

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3303C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	Enable	

Enable Color matrix enable: 0=off 1=on

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33040	R/W																				Coefft R-R													0x00000100

Coefft R-R [12:0] Matrix coefficient for red-red multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33044	R/W																				Coefft R-G													0x00000000

Coefft R-G [12:0] Matrix coefficient for red-green multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33048	R/W																				Coefft R-B													0x00000000

Coefft R-B [12:0] Matrix coefficient for red-blue multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3304C	R/W																				Coefft R-IR													0x00000000

Coefft R-IR [12:0] Matrix coefficient for red-ir multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33050	R/W																				Coefft G-R													0x00000000

Coefft G-R [12:0] Matrix coefficient for green-red multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33054	R/W																				Coefft G-G													0x00000100

Coefft G-G [12:0] Matrix coefficient for green-green multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33058	R/W																				Coefft G-B													0x00000000

Coefft G-B [12:0] Matrix coefficient for green-blue multiplier
Format: sign/magnitude 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3305C	R/W																				Coefft G-IR													0x00000000

Coefft G-IR [12:0] Matrix coefficient for green-ir multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33060	R/W																				Coefft B-R													0x00000000

Coefft B-R [12:0] Matrix coefficient for blue-red multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33064	R/W																				Coefft B-G													0x00000000

Coefft B-G [12:0] Matrix coefficient for blue-green multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33068	R/W																				Coefft B-B													0x00000100

Coefft B-B [12:0] Matrix coefficient for blue-blue multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3306C	R/W																				Coefft B-IR													0x00000100

Coefft B-IR [12:0] Matrix coefficient for blue-ir multiplier
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33070	R/W																					Coefft WB R												0x00000100

Coefft WB R [11:0] gain for Red channel for antifog function
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33074	R/W																					Coefft WB G												0x00000100

Coefft WB G [11:0] gain for Green channel for antifog function
Format: sign/magnitude 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33078	R/W																					Coefft WB B												0x00000100

Coefft WB B [11:0] gain for Blue channel for antifog function
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3307C	R/W																					Coefft WB IR												0x00000100

Coefft WB IR [11:0] gain for IR channel for antifog function
Format: sign/magnitude 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33080	R/W																					Coefft fog offset R												0x00000000

Coefft fog offset R [11:0] Offset R for antifog function
Format: unsigned 12-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33084	R/W																					Coefft fog offset G												0x00000000

Coefft fog offset G [11:0] Offset G for antifog function
Format: unsigned 12-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33088	R/W																					Coefft fog offset B												0x00000000

Coefft fog offset B [11:0] Offset B for antifog function
Format: unsigned 12-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3308C	R/W																					Coefft fog offset IR												0x00000000

Coefft fog offset IR [11:0] Offset Ir for antifog function
Format: unsigned 12-bit integer

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.51. cnr

Colour Noise Reduction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x33090	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	square root enable	

square_root_enable pre-CNR square root and the post-CNR square modules enable condition enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x33094	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	enable	

enable CNR enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33098	R/W																	debug reg																0x00000000

debug_reg [15:0] CNR Debug: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3309C	R/W																									mode								0x00000000

mode [7:0] CNR enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330A0	R/W																					delta factor												0x00000277

delta_factor [11:0] CNR enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x330A4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x0000003F
											effective kernel							

effective_kernel [6:0] Effective kernel

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330A8	R/W																					u center												0x00000200

u_center [11:0] Coordinates of u center

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330AC	R/W																					v center												0x00000200

v_center [11:0] Coordinates of v center

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330B0	R/W																					global offset												0x00000332

global_offset [11:0] umean1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330B4	R/W																	global slope																0x000000CD

global_slope [15:0] umean1 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330B8	R/W																					uv seg1 threshold												0x00000000

uv_seg1_threshold [11:0] uv_seg1 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330BC	R/W																					uv seg1 offset												0x000000AE

uv_seg1_offset [11:0] uv_seg1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330C0	R/W																	uv seg1 slope																0x0000FBD8

uv_seg1_slope [15:0] uv_seg1 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330C4	R/W																					umean1 threshold												0x00000000

umean1_threshold [11:0] umean1 threshold

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330C8	R/W																					umean1 offset												0x0000003E

umean1_offset [11:0] umean1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330CC	R/W																	umean1 slope																0x0000E7B4

umean1_slope [15:0] umean1 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330D0	R/W																					umean2 threshold												0x00000000

umean2_threshold [11:0] umean2 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330D4	R/W																					umean2 offset												0x0000003E

umean2_offset [11:0] umean2 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330D8	R/W																	umean2 slope																0x0000E7B4

umean2_slope [15:0] umean2 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330DC	R/W																					vmean1 threshold												0x00000000

vmean1_threshold [11:0] vmean1 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330E0	R/W																					vmean1 offset												0x0000003E

vmean1_offset [11:0] vmean1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330E4	R/W																	vmean1 slope																0x0000E7B4

vmean1_slope [15:0] vmean1 slope

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330E8	R/W																					vmean2 threshold												0x00000000

vmean2_threshold [11:0] vmean2 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330EC	R/W																					vmean2 offset												0x0000003E

vmean2_offset [11:0] vmean2 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330F0	R/W																	vmean2 slope																0x0000E7B4

vmean2_slope [15:0] vmean2 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330F4	R/W																					uv var1 threshold												0x00000000

uv_var1_threshold [11:0] uv_var1 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330F8	R/W																					uv var1 offset												0x000003FF

uv_var1_offset [11:0] uv_var1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x330FC	R/W																	uv var1 slope																0x0000FFFF

uv_var1_slope [15:0] uv_var2 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33100	R/W																					uv var2 threshold												0x00000000

uv_var2_threshold [11:0] uv_var2 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33104	R/W																					uv var2 offset												0x000003FF

uv_var2_offset [11:0] uv_var2 offset

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33108	R/W																	uv var2 slope																0x0000FFFF

uv_var2_slope [15:0] uv_var2 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3310C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00001010
				uv var2 scale								uv var1 scale						

uv_var1_scale [5:0] uv_var1 scale
uv_var2_scale [5:0] uv_var2 scale

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33110	R/W																					uv delta1 threshold												0x00000000

uv_delta1_threshold [11:0] uv_delta1 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33114	R/W																					uv delta1 offset												0x000000B9

uv_delta1_offset [11:0] uv_delta1 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33118	R/W																	uv delta1 slope																0x00000600

uv_delta1_slope [15:0] uv_delta1 slope

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3311C	R/W																					uv delta2 threshold												0x00000000

uv_delta2_threshold [11:0] uv_delta2 threshold

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33120	R/W																					uv delta2 offset												0x000000B9

uv_delta2_offset [11:0] uv_delta2 offset

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33124	R/W																	uv delta2 slope																0x00000600

uv_delta2_slope [15:0] uv_delta2 slope

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33128	R/O	Statusb																Statusa																--

Statusa [15:0] CNR Debug Port
Statusb [15:0] CNR Debug Port

35.52. nonequ gamma

nonequ_gamma module

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3312C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	srgb lut enable	

srgb_lut_enable enables gamma sRGB

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33130	R/W																			srgb lut coeff LUT(0)														--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33134	R/W																			srgb lut coeff LUT(1)														--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33138	R/W																			srgb lut coeff LUT(2)														--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x3313C	R/W																			srgb lut coeff LUT(3)														--
... repeated until ...																																		
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33228	R/W																			srgb lut coeff LUT(62)														--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x3322C	R/W																			srgb lut coeff LUT(63)														--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33230	R/W																			srgb lut coeff LUT(64)														--

srgb_lut_coeff LUT [13:0] Color space (HDR Linear to sRGB) LUT

This is an array of 65 14-bit registers. The address for element (i) is: 0x33130 + 4i.

35.53. lumvar

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33234	R/W	active height																active width																0x04380780

active_width [15:0] Active width. This depends on the position of the luma variance module. if this module is connected to the
full resolution pipeline, then the active_width should be the full resolution frame width.
if its in the downscaled pipeline, then the active_width should be the post-scaler width

active_height [15:0] Active height. This depends on the position of the luma variance module. if this module is connected to the
full resolution pipeline, then the active_height should be the full resolution frame height.
if its in the downscaled pipeline, then the active_height should be the post-scaler height

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.54. metering aexp

Derives information for use by the AE and AWB modules

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33238	R/W																					Hist Thresh 0 1												0x00000010

Hist Thresh 0 1 [11:0] Histogram threshold for bin 0/1 boundary

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3323C	R/W																					Hist Thresh 1 2												0x00000020

Hist Thresh 1 2 [11:0] Histogram threshold for bin 1/2 boundary

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33240	R/W																					Hist Thresh 3 4												0x000000D0

Hist Thresh 3 4 [11:0] Histogram threshold for bin 2/3 boundary

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33244	R/W																					Hist Thresh 4 5												0x000000E0

Hist Thresh 4 5 [11:0] Histogram threshold for bin 3/4 boundary

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33248	R/O																	Hist 0																--

Hist 0 [15:0] Normalized histogram results for bin 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3324C	R/O																	Hist 1																--

Hist 1 [15:0] Normalized histogram results for bin 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33250	R/O																	Hist 3																--

Hist 3 [15:0] Normalized histogram results for bin 3

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33254	R/O																	Hist 4																--

Hist 4 [15:0] Normalized histogram results for bin 4

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33258	R/W																	Nodes Used Vert								Nodes Used Horiz								0x00001517

Nodes Used Horiz [7:0] Number of active zones horizontally for AE stats collection
Nodes Used Vert [7:0] Number of active zones vertically for AE stats collection

35.55. metering awb

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3325C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	stats mode	

stats mode Statistics mode: 0 - legacy(G/R,B/R), 1 - current (R/G, B/G)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33260	R/W																							White Level AWB										0x000003FF

White Level AWB [9:0] Upper limit of valid data for AWB

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33264	R/W																							Black Level AWB										0x00000000

Black Level AWB [9:0] Lower limit of valid data for AWB

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33268	R/W																					Cr Ref Max AWB												0x000001FF

Cr Ref Max AWB [11:0] Maximum value of R/G for white region
Format: unsigned 4.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3326C	R/W																					Cr Ref Min AWB												0x00000040

Cr Ref Min AWB [11:0] Minimum value of R/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33270	R/W																					Cb Ref Max AWB												0x000001FF

Cb Ref Max AWB [11:0] Maximum value of B/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33274	R/W																					Cb Ref Min AWB												0x00000040

Cb Ref Min AWB [11:0] Minimum value of B/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33278	R/O																					RG												--

RG [11:0] AWB statistics R/G color ratio output
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3327C	R/O																					BG												--

BG [11:0] AWB statistics B/G color ratio output
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33280	R/O	SUM																																--

SUM [31:0] AWB output population. Number of pixels used for AWB statistics
Format: unsigned 32-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33284	R/W																	Nodes Used Vert								Nodes Used Horiz								0x00000F0F

Nodes Used Horiz [7:0] Number of active zones horizontally for AWB stats
Nodes Used Vert [7:0] Number of active zones vertically for AWB stats

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33288	R/W																					Cr Ref High AWB												0x00000FFF

Cr Ref High AWB [11:0] Maximum value of R/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3328C	R/W																					Cr Ref Low AWB												0x00000000

Cr Ref Low AWB [11:0] Minimum value of R/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33290	R/W																					Cb Ref High AWB												0x00000FFF

Cb Ref High AWB [11:0] Maximum value of B/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33294	R/W																					Cb Ref Low AWB												0x00000000

Cb Ref Low AWB [11:0] Minimum value of B/G for white region
Format: unsigned 4.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3329C	R/W					Zones Weight(3)								Zones Weight(2)								Zones Weight(1)								Zones Weight(0)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x332A0	R/W					Zones Weight(7)								Zones Weight(6)								Zones Weight(5)								Zones Weight(4)				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x336D8	R/W					Zones Weight(1087)								Zones Weight(1086)								Zones Weight(1085)								Zones Weight(1084)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x336DC	R/W																													Zones Weight(1088)				--

Zones Weight [3:0] Sets zone weighting for auto white balance. Index is (row,col) where (0,0) is top-left zone

This is an array of 1089 4-bit registers. The address for element (i) is: 0x3329C + 4 * int(i / 4).

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

35.56. metering af

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x336E0	R/W																	Nodes Used Vert								Nodes Used Horiz								0x00000F0F

Nodes Used Horiz [7:0] Number of active zones horizontally for AF stats
Nodes Used Vert [7:0] Number of active zones vertically for AF stats

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x336E8	R/W	Active Height																Active Width																0x04380780

Active Width [15:0] Active video width for AF module
Active Height [15:0] Active video height for AF module

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x336EC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																kernel select		

kernel select [1:0] Size of Narrow AF Kernel
0 = 3x3
1 = 7x3
2 = 11x3
3 = 15x3

35.57. metering hist aexp

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x336F0	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										offset y	skip y			offset x	skip x			

skip x [2:0] Histogram decimation in horizontal direction: 0=every 2nd pixel; 1=every 3rd pixel; 2=every 4th pixel; 3=every 5th pixel; 4=every 8th pixel ; 5+=every 9th pixel
offset x 0= start from the first column; 1=start from second column
skip y [2:0] Histogram decimation in vertical direction: 0=every pixel; 1=every 2nd pixel; 2=every 3rd pixel; 3=every 4th pixel; 4=every 5th pixel; 5=every 8th pixel ; 6+=every 9th pixel
offset y 0= start from the first row; 1= start from second row

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x336F4	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										scale top				scale bottom				

scale bottom [3:0] scale of bottom half of the range: 0=1x ,1=2x, 2=4x, 4=8x, 4=16x
scale top [3:0] scale of top half of the range: 0=1x ,1=2x, 2=4x, 4=8x, 4=16x

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x336F8	R/O	Total Pixels																																--

Total Pixels [31:0] Total number of pixels processed (skip x and skip y are taken into account)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x336FC	R/O	Counted Pixels																																--

Counted Pixels [31:0] Number of pixels accumulated (with nonzero weight)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x33700	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
															Plane mode			

Plane mode [2:0] Plane separation mode
0 = Collect all the planes in one histogram
1 = Collect 4 Bayer planes into 4 separate banks
2 = Reserved
3 = Reserved
4 = Collect odd x odd y plane to bank 0, rest to bank 1
5 = Collect even x odd y plane to bank 0, rest to bank 1
6 = Collect odd x even y plane to bank 0, rest to bank 1
7 = Collect even x even y plane to bank 0, rest to bank 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33704	R/O	Plane Total 0																																--

Plane Total 0 [31:0] Total pixels processed for plane 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33708	R/O	Plane Total 1																																--

Plane Total 1 [31:0] Total pixels processed for plane 1

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3370C	R/O	Plane Total 2																																--

Plane Total 2 [31:0] Total pixels processed for plane 2

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33710	R/O	Plane Total 3																																--

Plane Total 3 [31:0] Total pixels processed for plane 3

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33714	R/O	Plane Counted 0																																--

Plane Counted 0 [31:0] Total pixels accumulated for plane 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33718	R/O	Plane Counted 1																																--

Plane Counted 1 [31:0] Total pixels accumulated for plane 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3371C	R/O	Plane Counted 2																																--

Plane Counted 2 [31:0] Total pixels accumulated for plane 2

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33720	R/O	Plane Counted 3																																--

Plane Counted 3 [31:0] Total pixels accumulated for plane 3

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33724	R/W																	Nodes Used Vert								Nodes Used Horiz								0x00000F0F

Nodes Used Horiz [7:0] Number of active zones horizontally for Histogram
Nodes Used Vert [7:0] Number of active zones vertically for Histogram

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33728	R/W					Zones Weight(3)								Zones Weight(2)								Zones Weight(1)								Zones Weight(0)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x3372C	R/W					Zones Weight(7)								Zones Weight(6)								Zones Weight(5)								Zones Weight(4)				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33B64	R/W					Zones Weight(1087)								Zones Weight(1086)								Zones Weight(1085)								Zones Weight(1084)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33B68	R/W																													Zones Weight(1088)				--

Zones Weight [3:0] Sets zone weighting for Histogram. Index is (row,col) where (0,0) is top-left zone

This is an array of 1089 4-bit registers. The address for element (i) is: 0x33728 + 4 * int(i / 4).

35.58. metering ihist

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x33B6C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										offset y	skip y			offset x	skip x			

skip x [2:0] Histogram decimation in horizontal direction: 0=every 2nd pixel; 1=every 3rd pixel; 2=every 4th pixel; 3=every 5th pixel; 4=every 8th pixel ; 5+=every 9th pixel

offset x 0= start from the first column; 1=start from second column

skip y [2:0] Histogram decimation in vertical direction: 0=every pixel; 1=every 2nd pixel; 2=every 3rd pixel; 3=every 4th pixel; 4=every 5th pixel; 5=every 8th pixel ; 6+=every 9th pixel

offset y 0= start from the first row; 1= start from second row

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x33B70	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
										scale top				scale bottom				

scale bottom [3:0] scale of bottom half of the range: 0=1x ,1=2x, 2=4x, 4=8x, 4=16x

scale top [3:0] scale of top half of the range: 0=1x ,1=2x, 2=4x, 4=8x, 4=16x

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33B74	R/O	Total Pixels																																--

Total Pixels [31:0] Total number of pixels processed (skip x and skip y are taken into account)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33B78	R/O	Counted Pixels																																--

Counted Pixels [31:0] Number of pixels accumulated (with nonzero weight)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x33B7C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
															Plane mode			

Plane mode [2:0] Plane separation mode

0 = Collect all the planes in one histogram
1 = Collect 4 Bayer planes into 4 separate banks
2 = Reserved
3 = Reserved
4 = Collect odd x odd y plane to bank 0, rest to bank 1
5 = Collect even x odd y plane to bank 0, rest to bank 1
6 = Collect odd x even y plane to bank 0, rest to bank 1
7 = Collect even x even y plane to bank 0, rest to bank 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33B80	R/O	Plane Total 0																																--

Plane Total 0 [31:0] Total pixels processed for plane 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33B84	R/O	Plane Total 1																																--

Plane Total 1 [31:0] Total pixels processed for plane 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33B88	R/O	Plane Total 2																																--

Plane Total 2 [31:0] Total pixels processed for plane 2

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33B8C	R/O	Plane Total 3																																--

Plane Total 3 [31:0] Total pixels processed for plane 3

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33B90	R/O	Plane Counted 0																																--

Plane Counted 0 [31:0] Total pixels accumulated for plane 0

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33B94	R/O	Plane Counted 1																																--

Plane Counted 1 [31:0] Total pixels accumulated for plane 1

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33B98	R/O	Plane Counted 2																																--

Plane Counted 2 [31:0] Total pixels accumulated for plane 2

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33B9C	R/O	Plane Counted 3																																--

Plane Counted 3 [31:0] Total pixels accumulated for plane 3

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33BA0	R/W																	Nodes Used Vert								Nodes Used Horiz								0x00000F0F

Nodes Used Horiz [7:0] Number of active zones horizontally for Histogram
Nodes Used Vert [7:0] Number of active zones vertically for Histogram

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33BA4	R/W					Zones Weight(3)								Zones Weight(2)								Zones Weight(1)								Zones Weight(0)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33BA8	R/W					Zones Weight(7)								Zones Weight(6)								Zones Weight(5)								Zones Weight(4)				--
... repeated until ...																																		
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33FE0	R/W					Zones Weight(1087)								Zones Weight(1086)								Zones Weight(1085)								Zones Weight(1084)				--
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x33FE4	R/W																													Zones Weight(1088)				--

Zones Weight [3:0] Sets zone weighting for Histogram. Index is (row,col) where (0,0) is top-left zone

This is an array of 1089 4-bit registers. The address for element (i) is: 0x33BA4 + 4 * int(i / 4).

35.59. fr crop

Crop for full resolution output

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x33FE8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Enable crop	

Enable crop Crop enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33FEC	R/W																	start x																0x00000000

start x [15:0] Horizontal offset from left side of image in pixels for output crop window

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33FF0	R/W																	start y																0x00000000

start y [15:0] Vertical offset from top of image in lines for output crop window

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33FF4	R/W																	size x																0x0000FFFF

size x [15:0] width of output crop window

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x33FF8	R/W																	size y																0x0000FFFF

size y [15:0] height of output crop window

35.60. fr gamma rgb

Gamma correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34024	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	Enable	

Enable Gamma enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34028	R/W					gain g																gain r												0x01000100

gain_r [11:0] gain applied to the R chanel in 4.8 format
gain_g [11:0] gain applied to the G chanel in 4.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3402C	R/W																					gain b												0x00000100

gain_b [11:0] gain applied to the B chanel in 4.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34030	R/W					offset g																offset r												0x00000000

offset_r [11:0] Offset subtracted from the R chanel
offset_g [11:0] Offset subtracted from the G chanel

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34034	R/W																					offset b												0x00000000

offset_b [11:0] Offset subtracted from the B chanel

35.61. fr sharpen

Sharpen
Luma transform red coefficient. u0.8
Luma transform blue coefficient. u0.8

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34038	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Enable	

Enable Sharpening enable: 0=off, 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3403C	R/W																									Strength								0x00000010

Strength [8:0] Controls strength of sharpening effect. u5.4

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34040	R/W									Alpha Undershoot								Control B								Control R								0x00131E4C

Alpha Undershoot [7:0] Alpha blending of undershoot and overshoot u0.7, 0 = only unsershoot, 255 = only overshoot

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34044	R/W									Luma Offset Low														Luma Thresh Low										0x00000000

Luma Thresh Low [9:0] Luma threshold below this value, no sharpening will be applied.
Luma Offset Low [7:0] Luma offset (min value) of thre region of less than Luma Thresh Low.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34048	R/W							Luma Thresh High										Luma Slope Low																0x033203FC

Luma Slope Low [15:0] Luma linear threshold slope at dark luminance region
Luma Thresh High [9:0] Luma threshold above this value, sharpening level will be dicreased.

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3404C	R/W	Luma Slope High																								Luma Offset High								0x06A40000

Luma Offset High [7:0] Luma offset (min value) of thre region of more than Luma Thresh High.
Luma Slope High [15:0] Luma linear threshold slope at bright luminance region

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34050	R/W			Clip Str Min																Clip Str Max														0x00CD3FFF

Clip Str Max [13:0] clips sharpening mask of max value. This will control overshoot. U0.14. (0 ~ 16383)
Clip Str Min [13:0] clips sharpening mask of min value. This will control undershoot. U0.14. It is used as negative value. (0 ~ -16383)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34054	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Debug				

Debug [3:0] To support different debug output. 0 = normal operation, 1 = luma, 2 = sharpening mask

35.62. fr cs conv

Conversion of RGB to YUV data using a 3x3 color matrix plus offsets

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34058	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Enable vertical downsample	Enable horizontal downsample	Enable filter	Enable matrix	

Enable matrix Color matrix enable: 0=off 1=on
Enable filter Filter enable: 0=off 1=on
Enable horizontal downsample Horizontal Downsampling Enable: 0=off 1=on
Enable vertical downsample Vertical Downsampling Enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3405C	R/W																	Coefft 11																0x0000002F

Coefft 11 [15:0] Matrix coefficient for R-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34060	R/W																	Coefft 12																0x0000009D

Coefft 12 [15:0] Matrix coefficient for G-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34064	R/W																	Coefft 13																0x00000010

Coefft 13 [15:0] Matrix coefficient for B-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34068	R/W																	Coefft 21																0x0000801A

Coefft 21 [15:0] Matrix coefficient for R-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3406C	R/W																	Coefft 22																0x00008057

Coefft 22 [15:0] Matrix coefficient for G-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34070	R/W																	Coefft 23																0x00000070

Coefft 23 [15:0] Matrix coefficient for B-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34074	R/W																	Coefft 31																0x00000070

Coefft 31 [15:0] Matrix coefficient for R-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34078	R/W																	Coefft 32																0x00008066

Coefft 32 [15:0] Matrix coefficient for G-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3407C	R/W																	Coefft 33																0x0000800A

Coefft 33 [15:0] Matrix coefficient for B-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34080	R/W																						Coefft o1											0x00000000

Coefft o1 [10:0] Offset for Y
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34084	R/W																						Coefft o2											0x00000200

Coefft o2 [10:0] Offset for Cb
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34088	R/W																						Coefft o3											0x00000200

Coefft o3 [10:0] Offset for Cr
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3408C	R/W																							Clip min Y										0x00000000

Clip min Y [9:0] Minimal value for Y. Values below this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34090	R/W																							Clip max Y										0x000003FF

Clip max Y [9:0] Maximal value for Y. Values above this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34094	R/W																							Clip min UV										0x00000000

Clip min UV [9:0] Minimal value for Cb, Cr. Values below this are clipped.
Format: signed (2's complement) 10-bit integer

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34098	R/W																							Clip max UV										0x000003FF

Clip max UV [9:0] Maximal value for Cb, Cr. Values above this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3409C	R/W																							Data mask RY										0x000003FF

Data mask RY [9:0] Data mask for channel 1 (R or Y). Bit-wise and of this value and video data.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340A0	R/W																							Data mask GU										0x000003FF

Data mask GU [9:0] Data mask for channel 2 (G or U). Bit-wise and of this value and video data.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340A4	R/W																							Data mask BV										0x000003FF

Data mask BV [9:0] Data mask for channel 3 (B or V). Bit-wise and of this value and video data.

35.63. fr cs conv dither

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x340A8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Shift mode		Dither amount		Enable dither	

Enable dither Enables dithering module
Dither amount [1:0] 0= dither to 9 bits; 1=dither to 8 bits; 2=dither to 7 bits; 3=dither to 6 bits
Shift mode 0= output is LSB aligned; 1=output is MSB aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.64. fr dma writer

DMA writer controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x340AC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
						axi xact comp		frame write on	Rsvd	Plane select		Rsvd	Base mode					

Base mode [4:0] Base DMA packing mode for RGB/RAW/YUV etc (see ISP guide)

Plane select [1:0] Plane select for planar base modes. Only used if planar outputs required. Not used. Should be set to 0

frame write on 0 = no frames written(when switched from 1, current frame completes writing before stopping),
1= write frame(s) (write single or continous frame(s))

axi xact comp 0 = dont wait for axi transaction completion at end of frame(just all transfers accepted). 1 = wait for all transactions completed

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340B0	R/W	active height																active width																0x04380780

active width [15:0] Active video width in pixels 128-8000

active height [15:0] Active video height in lines 128-8000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340B4	R/W	bank0 base																																0x00000000

bank0_base [31:0] bank 0 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340B8	R/W	bank1 base																																0x00000000

bank1_base [31:0] bank 1 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340BC	R/W	bank2 base																																0x00000000

bank2_base [31:0] bank 2 base address for frame buffer, should be word-aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340C0	R/W	bank3 base																																0x00000000

bank3_base [31:0] bank 3 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340C4	R/W	bank4 base																																0x00000000

bank4_base [31:0] bank 4 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x340C8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Rsvd	max bank			

max bank [2:0] highest bank*_base to use for frame writes before recycling to bank0_base, only 0 to 4 are valid

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340CC	R/W	Line offset																																0x00001000

Line_offset [31:0] Indicates the offset in bytes from the start of one line to the next line.
This value should be equal to or larger than one line of image data and should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x340D0	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
														wbank curr			wbank active	

wbank active 1 = wbank_curr is being written to. Goes high at start of writes, low at last write transfer/completion on axi.

wbank curr [2:0] write bank currently active. valid values =0-4. updated at start of frame write

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340DC	R/O	frame wcount																frame icount																--

frame icount [15:0] count of incomming frames (starts) to vdma_writer on video input, non resetable, rolls over, updates at pixel 1 of new frame on video in

frame wcount [15:0] count of outgoing frame writes (starts) from vdma_writer sent to AXI output, non resetable, rolls over, updates at pixel 1 of new frame on video in

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x340E4	R/O	23	22	21	20	19	18	17	16	--
		15	14	13	12	11	10	9	8	
									video alarm	
		7	6	5	4	3	2	1	0	
		vi fail interframe blanks	**vi fail interline blanks**	**vi fail active height**	**vi fail active width**	**axi fail wxact ostand**	**axi fail wmaxwait**	**axi fail awmaxwait**	**axi fail bresp**	

axi_fail_bresp clearable alarm, high to indicate bad bresp captured
axi_fail_awmaxwait clearable alarm, high when awmaxwait_limit reached
axi_fail_wmaxwait clearable alarm, high when wmaxwait_limit reached
axi_fail_wxact_ostand clearable alarm, high when wxact_ostand_limit reached
vi_fail_active_width clearable alarm, high to indicate mismatched active_width detected
vi_fail_active_height clearable alarm, high to indicate mismatched active_height detected (also raised on missing field!)
vi_fail_interline_blanks clearable alarm, high to indicate interline blanking below min
vi_fail_interframe_blanks clearable alarm, high to indicate interframe blanking below min
video_alarm active high, problem found on video port(s) (active width/height or interline/frame blanks failure)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340E8	R/O	**blk status**																																--

blk_status [31:0] block status output (reserved)
-- blk_status(0) = wfifo_fail_full
-- blk_status(1) = wfifo_fail_empty
-- blk_status(4) = pack_fail_overflow
-- blk_status(24) = intw_fail_user_intfc_sig
-- blk_status(others) = zero

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340EC	R/W																	**lines wrapped**																0x00000000

lines_wrapped [15:0] Number of lines to write from base address before wrapping back to base address. 0 = no wrapping, >0 = last line written before wrapping

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340F0	R/W																	**linetick first**																0x00000000

linetick_first [15:0] Line number of first linetick. 0 = no linetick, >0 = line number to generate linetick

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x340F4	R/W																	linetick repeat																0x00000000

linetick_repeat [15:0] Line repeat interval of linetick. 0 = no repeat, >0 = repeat interval in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x340F8	R/W	linetick delay																0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																	linetick eol	

linetick_eol Linetick start/end of line control. 0 = use start of line, 1 = use end of line to generate linetick

linetick_delay [15:0] Linetick delay in vcke cycles to add to min 3 cycle latency from acl_vi. 0-65535.
Must be less than next linetick generation time or count will not mature and no linetick is not produced.
--NOTE: linetick delay can run past end of frame/field and also into next frame!
-- Take care maturity time is less than next configured linetick generation postion!
-- Take care when changing config between frame too!

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x340FC	R/W					Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F000F0C
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						Rsvd	Rsvd	Rsvd	Rsvd					Rsvd	Rsvd	axi id multi	Rsvd	

axi_id_multi 0= static value (axi_id_value) for awid/wid, 1 = incrementing value per transaction for awid/wid wrapping to 0 after axi_id_value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34100	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														axi id value				

axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = 0000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.65. fr uv dma writer

DMA writer controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34104	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
						axi xact comp		frame write on	Rsvd	Plane select		Rsvd	Base mode					

Base mode [4:0] Base DMA packing mode for RGB/RAW/YUV etc (see ISP guide)

Plane select [1:0] Plane select for planar base modes. Only used if planar outputs required. Not used. Should be set to 0

frame write on 0 = no frames written(when switched from 1, current frame completes writing before stopping),
1= write frame(s) (write single or continous frame(s))

axi xact comp 0 = dont wait for axi transaction completion at end of frame(just all transfers accepted). 1 = wait for all transactions completed

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34108	R/W	active height																active width																0x04380780

active width [15:0] Active video width in pixels 128-8000

active height [15:0] Active video height in lines 128-8000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3410C	R/W	bank0 base																																0x00000000

bank0_base [31:0] bank 0 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34110	R/W	bank1 base																																0x00000000

bank1_base [31:0] bank 1 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34114	R/W	bank2 base																																0x00000000

bank2_base [31:0] bank 2 base address for frame buffer, should be word-aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34118	R/W	bank3 base																																0x00000000

bank3_base [31:0] bank 3 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3411C	R/W	bank4 base																																0x00000000

bank4_base [31:0] bank 4 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34120	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Rsvd	max bank			

max bank [2:0] highest bank*_base to use for frame writes before recycling to bank0_base, only 0 to 4 are valid

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34124	R/W	Line offset																																0x00001000

Line_offset [31:0] Indicates the offset in bytes from the start of one line to the next line.
This value should be equal to or larger than one line of image data and should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34128	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
														wbank curr			wbank active	

wbank active 1 = wbank_curr is being written to. Goes high at start of writes, low at last write transfer/completion on axi.

wbank curr [2:0] write bank currently active. valid values =0-4. updated at start of frame write

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34134	R/O	frame wcount																frame icount																--

frame icount [15:0] count of incomming frames (starts) to vdma_writer on video input, non resetable, rolls over, updates at pixel 1 of new frame on video in

frame wcount [15:0] count of outgoing frame writes (starts) from vdma_writer sent to AXI output, non resetable, rolls over, updates at pixel 1 of new frame on video in

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x3413C	R/O	23	22	21	20	19	18	17	16	--
		15	14	13	12	11	10	9	8	
									video alarm	
		7	6	5	4	3	2	1	0	
		vi fail interframe blanks	**vi fail interline blanks**	**vi fail active height**	**vi fail active width**	**axi fail wxact ostand**	**axi fail wmaxwait**	**axi fail awmaxwait**	**axi fail bresp**	

axi_fail_bresp clearable alarm, high to indicate bad bresp captured
axi_fail_awmaxwait clearable alarm, high when awmaxwait_limit reached
axi_fail_wmaxwait clearable alarm, high when wmaxwait_limit reached
axi_fail_wxact_ostand clearable alarm, high when wxact_ostand_limit reached
vi_fail_active_width clearable alarm, high to indicate mismatched active_width detected
vi_fail_active_height clearable alarm, high to indicate mismatched active_height detected (also raised on missing field!)
vi_fail_interline_blanks clearable alarm, high to indicate interline blanking below min
vi_fail_interframe_blanks clearable alarm, high to indicate interframe blanking below min
video_alarm active high, problem found on video port(s) (active width/height or interline/frame blanks failure)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34140	R/O	**blk status**																																--

blk_status [31:0] block status output (reserved)
-- blk_status(0) = wfifo_fail_full
-- blk_status(1) = wfifo_fail_empty
-- blk_status(4) = pack_fail_overflow
-- blk_status(24) = intw_fail_user_intfc_sig
-- blk_status(others) = zero

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34144	R/W																	**lines wrapped**																0x00000000

lines_wrapped [15:0] Number of lines to write from base address before wrapping back to base address. 0 = no wrapping, >0 = last line written before wrapping

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34148	R/W																	**linetick first**																0x00000000

linetick_first [15:0] Line number of first linetick. 0 = no linetick, >0 = line number to generate linetick

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3414C	R/W																	linetick repeat																0x00000000

linetick_repeat [15:0] Line repeat interval of linetick. 0 = no repeat, >0 = repeat interval in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34150	R/W	linetick delay																0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																	linetick eol	

linetick_eol Linetick start/end of line control. 0 = use start of line, 1 = use end of line to generate linetick

linetick_delay [15:0] Linetick delay in vcke cycles to add to min 3 cycle latency from acl_vi. 0-65535.
Must be less than next linetick generation time or count will not mature and no linetick is not produced.
--NOTE: linetick delay can run past end of frame/field and also into next frame!
-- Take care maturity time is less than next configured linetick generation postion!
-- Take care when changing config between frame too!

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34154	R/W					Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F000F0C
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						Rsvd	Rsvd	Rsvd	Rsvd					Rsvd	Rsvd	axi id multi	Rsvd	

axi_id_multi 0= static value (axi_id_value) for awid/wid, 1 = incrementing value per transaction for awid/wid wrapping to 0 after axi_id_value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34158	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														axi id value				

axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = 0000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.66. ds crop

Crop for full resolution output

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3415C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Enable crop	

Enable crop Crop enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34160	R/W																	start x																0x00000000

start x [15:0] Horizontal offset from left side of image in pixels for output crop window

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34164	R/W																	start y																0x00000000

start y [15:0] Vertical offset from top of image in lines for output crop window

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34168	R/W																	size x																0x0000FFFF

size x [15:0] width of output crop window

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3416C	R/W																	size y																0x0000FFFF

size y [15:0] height of output crop window

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.67. ds scaler

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34170	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
										Rsvd	Rsvd	Rsvd	Rsvd	**Timeout IRQ**	**Underflow IRQ**	Rsvd	**Overflow IRQ**	

Overflow IRQ 0 : No overflow
1 : FIFO overflow has occurred

Underflow IRQ 0 : No underflow
1 : FIFO underflow has occurred

Timeout IRQ 0 : No timeout
1 : Timeout on frame done

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34174	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000010
												Rsvd	**Timeout Enable**	**Clear Alarms**				

Clear Alarms Scaler control
IRQ CLR bit
0 : In-active
1 : Clear-off IRQ status to 0

Timeout Enable 0 : Timeout disabled.
1 : Timeout enabled. Automatic frame reset if frame has not completed after anticipated time.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34178	R/W																	**WIDTH**																0x00000780

WIDTH [15:0] Input frame width in pixels

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3417C	R/W																	**HEIGHT**																0x00000438

HEIGHT [15:0] Input frame height in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34180	R/W																				**OWIDTH**													0x00000500

OWIDTH [12:0] Output frame width in pixels

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34184	R/W																	OHEIGHT																0x000002D0

OHEIGHT [15:0] Output frame height in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34188	R/W									HFILT TINC																								0x00180000

HFILT_TINC [23:0] Horizontal scaling factor equal to the

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3418C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														HFILT COEFSET				

HFILT_COEFSET [3:0] HFILT Coeff. control.
HFILT_COEFSET[3:0] - Selects horizontal Coef set for scaler.
0000 : use set 0
0001 : use set 1
.....
1111 : use set 15

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34190	R/W									VFILT TINC																								0x00180000

VFILT_TINC [23:0] VFILT TINC

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34194	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														VFILT COEFSET				

VFILT_COEFSET [3:0] VFILT Coeff. control
FILT_COEFSET[3:0] - Selects vertical Coef set for scaler
0000 : use set 0
0001 : use set 1
.....
1111 : use set 15

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.68. ds gamma rgb

Gamma correction

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34198	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000001
																	Enable	

Enable Gamma enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3419C	R/W					gain g																gain r												0x01000100

gain_r [11:0] gain applied to the R chanel in 4.8 format
gain_g [11:0] gain applied to the G chanel in 4.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341A0	R/W																					gain b												0x00000100

gain_b [11:0] gain applied to the B chanel in 4.8 format

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341A4	R/W					offset g																offset r												0x00000000

offset_r [11:0] Offset subtracted from the R chanel
offset_g [11:0] Offset subtracted from the G chanel

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341A8	R/W																					offset b												0x00000000

offset_b [11:0] Offset subtracted from the B chanel

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.69. ds sharpen

Sharpen
Luma transform red coefficient. u0.8
Luma transform blue coefficient. u0.8

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x341AC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Enable	

Enable Sharpening enable: 0=off, 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341B0	R/W																								Strength									0x00000010

Strength [8:0] Controls strength of sharpening effect. u5.4

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341B4	R/W									Alpha Undershoot								Control B								Control R								0x00131E4C

Alpha Undershoot [7:0] Alpha blending of undershoot and overshoot u0.7, 0 = only unsershoot, 255 = only overshoot

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341B8	R/W									Luma Offset Low														Luma Thresh Low										0x00000000

Luma Thresh Low [9:0] Luma threshold below this value, no sharpening will be applied.
Luma Offset Low [7:0] Luma offset (min value) of thre region of less than Luma Thresh Low.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341BC	R/W							Luma Thresh High										Luma Slope Low																0x033203FC

Luma Slope Low [15:0] Luma linear threshold slope at dark luminance region
Luma Thresh High [9:0] Luma threshold above this value, sharpening level will be dicreased.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341C0	R/W																									Luma Offset High								0x06A40000

Luma Offset High [7:0] Luma offset (min value) of thre region of more than Luma Thresh High.
Luma Slope High [15:0] Luma linear threshold slope at bright luminance region

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341C4	R/W			Clip Str Min																Clip Str Max														0x00CD3FFF

Clip Str Max [13:0] clips sharpening mask of max value. This will control overshoot. U0.14. (0 ~ 16383)

Clip Str Min [13:0] clips sharpening mask of min value. This will control undershoot. U0.14. It is used as negative value. (0 ~ -16383)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x341C8	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Debug				

Debug [3:0] To support different debug output. 0 = normal operation, 1 = luma, 2 = sharpening mask

35.70. ds cs conv

Conversion of RGB to YUV data using a 3x3 color matrix plus offsets

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x341CC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Enable vertical downsample	Enable horizontal downsample	Enable filter	Enable matrix	

Enable matrix Color matrix enable: 0=off 1=on

Enable filter Filter enable: 0=off 1=on

Enable horizontal downsample Horizontal Downsampling Enable: 0=off 1=on

Enable vertical downsample Vertical Downsampling Enable: 0=off 1=on

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341D0	R/W																	Coefft 11																0x0000002F

Coefft 11 [15:0] Matrix coefficient for R-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341D4	R/W																	Coefft 12																0x0000009D

Coefft 12 [15:0] Matrix coefficient for G-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341D8	R/W																	Coefft 13																0x00000010

Coefft 13 [15:0] Matrix coefficient for B-Y multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341DC	R/W																	Coefft 21																0x0000801A

Coefft 21 [15:0] Matrix coefficient for R-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341E0	R/W																	Coefft 22																0x00008057

Coefft 22 [15:0] Matrix coefficient for G-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341E4	R/W																	Coefft 23																0x00000070

Coefft 23 [15:0] Matrix coefficient for B-Cb multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341E8	R/W																	Coefft 31																0x00000070

Coefft 31 [15:0] Matrix coefficient for R-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341EC	R/W																	Coefft 32																0x00008066

Coefft 32 [15:0] Matrix coefficient for G-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341F0	R/W																	Coefft 33																0x0000800A

Coefft 33 [15:0] Matrix coefficient for B-Cr multiplier
Format: sign/magnitude 8.8-bit fixed-point

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341F4	R/W																						Coefft o1											0x00000000

Coefft o1 [10:0] Offset for Y
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341F8	R/W																						Coefft o2											0x00000200

Coefft o2 [10:0] Offset for Cb
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x341FC	R/W																						Coefft o3											0x00000200

Coefft o3 [10:0] Offset for Cr
Format: signed (2's complement) 11-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34200	R/W																							Clip min Y										0x00000000

Clip min Y [9:0] Minimal value for Y. Values below this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34204	R/W																							Clip max Y										0x000003FF

Clip max Y [9:0] Maximal value for Y. Values above this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34208	R/W																							Clip min UV										0x00000000

Clip min UV [9:0] Minimal value for Cb, Cr. Values below this are clipped.
Format: signed (2's complement) 10-bit integer

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3420C	R/W																							Clip max UV										0x000003FF

Clip max UV [9:0] Maximal value for Cb, Cr. Values above this are clipped.
Format: signed (2's complement) 10-bit integer

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34210	R/W																							Data mask RY										0x000003FF

Data mask RY [9:0] Data mask for channel 1 (R or Y). Bit-wise and of this value and video data.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34214	R/W																							Data mask GU										0x000003FF

Data mask GU [9:0] Data mask for channel 2 (G or U). Bit-wise and of this value and video data.

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34218	R/W																							Data mask BV										0x000003FF

Data mask BV [9:0] Data mask for channel 3 (B or V). Bit-wise and of this value and video data.

35.71. ds cs conv dither

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3421C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
													Shift mode		Dither amount		Enable dither	

Enable dither Enables dithering module
Dither amount [1:0] 0= dither to 9 bits; 1=dither to 8 bits; 2=dither to 7 bits; 3=dither to 6 bits
Shift mode 0= output is LSB aligned; 1=output is MSB aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.72. ds dma writer

DMA writer controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34220	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
						axi xact comp		frame write on	Rsvd	Plane select		Rsvd	Base mode					

Base mode [4:0] Base DMA packing mode for RGB/RAW/YUV etc (see ISP guide)

Plane select [1:0] Plane select for planar base modes. Only used if planar outputs required. Not used. Should be set to 0

frame write on 0 = no frames written(when switched from 1, current frame completes writing before stopping),
1= write frame(s) (write single or continous frame(s))

axi xact comp 0 = dont wait for axi transaction completion at end of frame(just all transfers accepted). 1 = wait for all transactions completed

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34224	R/W	active height																active width																0x04380780

active width [15:0] Active video width in pixels 128-8000

active height [15:0] Active video height in lines 128-8000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34228	R/W	bank0 base																																0x00000000

bank0_base [31:0] bank 0 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3422C	R/W	bank1 base																																0x00000000

bank1_base [31:0] bank 1 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34230	R/W	bank2 base																																0x00000000

bank2_base [31:0] bank 2 base address for frame buffer, should be word-aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34234	R/W	bank3 base																																0x00000000

bank3_base [31:0] bank 3 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34238	R/W	bank4 base																																0x00000000

bank4_base [31:0] bank 4 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3423C	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Rsvd	max bank			

max bank [2:0] highest bank*_base to use for frame writes before recycling to bank0_base, only 0 to 4 are valid

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34240	R/W	Line offset																																0x00001000

Line_offset [31:0] Indicates the offset in bytes from the start of one line to the next line.
This value should be equal to or larger than one line of image data and should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34244	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
														wbank curr			wbank active	

wbank active 1 = wbank_curr is being written to. Goes high at start of writes, low at last write transfer/completion on axi.

wbank curr [2:0] write bank currently active. valid values =0-4. updated at start of frame write

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34250	R/O	frame wcount																frame icount																--

frame icount [15:0] count of incomming frames (starts) to vdma_writer on video input, non resetable, rolls over, updates at pixel 1 of new frame on video in

frame wcount [15:0] count of outgoing frame writes (starts) from vdma_writer sent to AXI output, non resetable, rolls over, updates at pixel 1 of new frame on video in

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x34258	R/O	23	22	21	20	19	18	17	16	--
		15	14	13	12	11	10	9	8	
									video alarm	
		7	6	5	4	3	2	1	0	
		vi fail interframe blanks	**vi fail interline blanks**	**vi fail active height**	**vi fail active width**	**axi fail wxact ostand**	**axi fail wmaxwait**	**axi fail awmaxwait**	**axi fail bresp**	

axi_fail_bresp clearable alarm, high to indicate bad bresp captured
axi_fail_awmaxwait clearable alarm, high when awmaxwait_limit reached
axi_fail_wmaxwait clearable alarm, high when wmaxwait_limit reached
axi_fail_wxact_ostand clearable alarm, high when wxact_ostand_limit reached
vi_fail_active_width clearable alarm, high to indicate mismatched active_width detected
vi_fail_active_height clearable alarm, high to indicate mismatched active_height detected (also raised on missing field!)
vi_fail_interline_blanks clearable alarm, high to indicate interline blanking below min
vi_fail_interframe_blanks clearable alarm, high to indicate interframe blanking below min
video_alarm active high, problem found on video port(s) (active width/height or interline/frame blanks failure)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3425C	R/O	**blk status**																																--

blk_status [31:0] block status output (reserved)
-- blk_status(0) = wfifo_fail_full
-- blk_status(1) = wfifo_fail_empty
-- blk_status(4) = pack_fail_overflow
-- blk_status(24) = intw_fail_user_intfc_sig
-- blk_status(others) = zero

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34260	R/W																	**lines wrapped**																0x00000000

lines_wrapped [15:0] Number of lines to write from base address before wrapping back to base address. 0 = no wrapping, >0 = last line written before wrapping

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34264	R/W																	**linetick first**																0x00000000

linetick_first [15:0] Line number of first linetick. 0 = no linetick, >0 = line number to generate linetick

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34268	R/W																	linetick repeat																0x00000000

linetick_repeat [15:0] Line repeat interval of linetick. 0 = no repeat, >0 = repeat interval in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3426C	R/W	linetick delay																0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																	linetick eol	

linetick_eol Linetick start/end of line control. 0 = use start of line, 1 = use end of line to generate linetick

linetick_delay [15:0] Linetick delay in vcke cycles to add to min 3 cycle latency from acl_vi. 0-65535.
Must be less than next linetick generation time or count will not mature and no linetick is not produced.
--NOTE: linetick delay can run past end of frame/field and also into next frame!
-- Take care maturity time is less than next configured linetick generation postion!
-- Take care when changing config between frame too!

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34270	R/W					Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F000F0C
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						Rsvd	Rsvd	Rsvd	Rsvd					Rsvd	Rsvd	axi id multi	Rsvd	

axi_id_multi 0= static value (axi_id_value) for awid/wid, 1 = incrementing value per transaction for awid/wid wrapping to 0 after axi_id_value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34274	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														axi id value				

axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = 0000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.73. ds uv dma writer

DMA writer controls

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34278	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
						axi xact comp		frame write on	Rsvd	Plane select		Rsvd	Base mode					

Base mode [4:0] Base DMA packing mode for RGB/RAW/YUV etc (see ISP guide)

Plane select [1:0] Plane select for planar base modes. Only used if planar outputs required. Not used. Should be set to 0

frame write on 0 = no frames written(when switched from 1, current frame completes writing before stopping),
1= write frame(s) (write single or continous frame(s))

axi xact comp 0 = dont wait for axi transaction completion at end of frame(just all transfers accepted). 1 = wait for all transactions completed

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3427C	R/W	active height																active width																0x04380780

active width [15:0] Active video width in pixels 128-8000

active height [15:0] Active video height in lines 128-8000

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34280	R/W	bank0 base																																0x00000000

bank0_base [31:0] bank 0 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34284	R/W	bank1 base																																0x00000000

bank1_base [31:0] bank 1 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34288	R/W	bank2 base																																0x00000000

bank2_base [31:0] bank 2 base address for frame buffer, should be word-aligned

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x3428C	R/W	bank3 base																																0x00000000

bank3_base [31:0] bank 3 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34290	R/W	bank4 base																																0x00000000

bank4_base [31:0] bank 4 base address for frame buffer, should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x34294	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														Rsvd	max bank			

max bank [2:0] highest bank*_base to use for frame writes before recycling to bank0_base, only 0 to 4 are valid

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x34298	R/W	Line offset																																0x00001000

Line_offset [31:0] Indicates the offset in bytes from the start of one line to the next line.
This value should be equal to or larger than one line of image data and should be word-aligned

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x3429C	R/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	--
														wbank curr			wbank active	

wbank active 1 = wbank_curr is being written to. Goes high at start of writes, low at last write transfer/completion on axi.

wbank curr [2:0] write bank currently active. valid values =0-4. updated at start of frame write

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x342A8	R/O	frame wcount																frame icount																--

frame icount [15:0] count of incomming frames (starts) to vdma_writer on video input, non resetable, rolls over, updates at pixel 1 of new frame on video in

frame wcount [15:0] count of outgoing frame writes (starts) from vdma_writer sent to AXI output, non resetable, rolls over, updates at pixel 1 of new frame on video in

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	Default
0x342B0	R/O	23	22	21	20	19	18	17	16	--
		15	14	13	12	11	10	9	8	
									video alarm	
		7	6	5	4	3	2	1	0	
		vi fail interframe blanks	**vi fail interline blanks**	**vi fail active height**	**vi fail active width**	**axi fail wxact ostand**	**axi fail wmaxwait**	**axi fail awmaxwait**	**axi fail bresp**	

axi_fail_bresp	clearable alarm, high to indicate bad bresp captured
axi_fail_awmaxwait	clearable alarm, high when awmaxwait_limit reached
axi_fail_wmaxwait	clearable alarm, high when wmaxwait_limit reached
axi_fail_wxact_ostand	clearable alarm, high when wxact_ostand_limit reached
vi_fail_active_width	clearable alarm, high to indicate mismatched active_width detected
vi_fail_active_height	clearable alarm, high to indicate mismatched active_height detected (also raised on missing field!)
vi_fail_interline_blanks	clearable alarm, high to indicate interline blanking below min
vi_fail_interframe_blanks	clearable alarm, high to indicate interframe blanking below min
video_alarm	active high, problem found on video port(s) (active width/height or interline/frame blanks failure)

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x342B4	R/O	**blk status**																																--

blk_status [31:0] block status output (reserved)
-- blk_status(0) = wfifo_fail_full
-- blk_status(1) = wfifo_fail_empty
-- blk_status(4) = pack_fail_overflow
-- blk_status(24) = intw_fail_user_intfc_sig
-- blk_status(others) = zero

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x342B8	R/W																	**lines wrapped**																0x00000000

lines_wrapped [15:0] Number of lines to write from base address before wrapping back to base address. 0 = no wrapping, >0 = last line written before wrapping

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x342BC	R/W																	**linetick first**																0x00000000

linetick_first [15:0] Line number of first linetick. 0 = no linetick, >0 = line number to generate linetick

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0x342C0	R/W																	linetick repeat																0x00000000

linetick_repeat [15:0] Line repeat interval of linetick. 0 = no repeat, >0 = repeat interval in lines

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x342C4	R/W	linetick delay																0x00000000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																	linetick eol	

linetick_eol Linetick start/end of line control. 0 = use start of line, 1 = use end of line to generate linetick

linetick_delay [15:0] Linetick delay in vcke cycles to add to min 3 cycle latency from acl_vi. 0-65535.
Must be less than next linetick generation time or count will not mature and no linetick is not produced.
--NOTE: linetick delay can run past end of frame/field and also into next frame!
-- Take care maturity time is less than next configured linetick generation postion!
-- Take care when changing config between frame too!

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x342C8	R/W					Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	0x0F000F0C
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						Rsvd	Rsvd	Rsvd	Rsvd					Rsvd	Rsvd	axi id multi	Rsvd	

axi_id_multi 0= static value (axi_id_value) for awid/wid, 1 = incrementing value per transaction for awid/wid wrapping to 0 after axi_id_value

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x342CC	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
														axi id value				

axi_id_value [3:0] value to send for awid, wid and expected on bid. Good default = 0000

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL

35.74. multi ctx

Addr	Mode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Default
0x342D0	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0x00000000
																	Config done	

Config done This signal is only required in multi-context mode
Once configuration for ping/pong address space is done, MCU must write 1 into this address
This register is self-clearing. So the read-back will be 0

Copyright © 2018 ARM Limited or its affiliates.
All rights reserved
CONFIDENTIAL