Using the EiceDRIVER™ 2EDi product family of dual-channel functional and reinforced isolated MOSFET gate drivers

Design guidelines and application example in the Infineon 800 W ZVS PSFB evaluation board

About this document

Scope and purpose

This application note introduces the EiceDRIVER™ 2EDi product family of dual-channel isolated gate drivers for power MOSFETs.
The document opens with an overview of safety isolation standards and certifications. A second section provides guidelines to properly design a gate drive circuit using 2EDi. Finally a practical application example is given; in particular, the 2EDS is evaluated in a phase-shift full-bridge (PSFB) DC-DC converter and compared with the widely-used gate transformer solution.

Intended audience

This application note is targeted for application engineers and designers of switch mode power supplies (SMPS) looking for isolated solutions to drive power MOSFETs. The benefits 2EDi products offer in most of the commonly used SMPS stages (PFC, LLC, PSFB, ..) are discussed.

Table of contents

About this document **1**
Table of contents **2**
1 Introduction to EiceDRIVER™ 2EDi **3**
2 Overview of isolation standards **4**
2.1 System isolation standards: IEC60950, IEC62368 4
2.2 Isolator component standards: IEC60747-17, UL1577, VDE-0884-1x 5
3 Design guidelines **7**
3.1 Shunt resistor dimensioning 7
3.2 Bypass capacitors dimensioning 9
3.2.1 Input bypass capacitor 9
3.2.2 Output bypass capacitor 10
3.3 Bootstrap circuit dimensioning 11
3.4 Gate resistance dimensioning 12
4 PCB layout recommendations **14**
5 Evaluation of 2EDS vs gate transformer in 800W PSFB evaluation board **16**
5.1 Reduced gate switching noise 16
5.2 Efficiency improvement at light-load 18
5.3 Volume saving with 2EDS 18
5.4 No concerns about core saturation with the 2EDi product family 20
6 Summary **21**
7 References **22**
Revision history **23**

1 Introduction to EiceDRIVER™ 2EDi

The 2EDi products benefit from the well-known features of the EiceDRIVER™ family; they are particularly attractive in fast switching power systems (for further details please visit the EiceDRIVER™ family webpages ([1], [2], [3]) and the dedicated documentation (e.g., [3]).

The key feature of EiceDRIVER™ 2EDi is isolation based on coreless transformer (CT) technology. The 2EDi-family offers functional and reinforced isolated gate driver solutions for power MOSFETs. Different isolation levels are associated with the different creepage and clearance distances of the packages offered.

Figure 1 shows the intended range of usage for the 2EDi products:

- 2EDFxx75F (NB-DSO16 package) in high voltage (HV) PFC stages based on half-bridge structure
- 2EDSxx65H (WB-DSO16 package) in isolated DC-DC stages
- 2EDF72x5K (LGA 5 mm x 5 mm) in isolated and non-isolated DC-DC bricks; the compact LGA package is preferred here since low voltage (LV) DC-DC bricks are less demanding in terms of working voltage and package size.

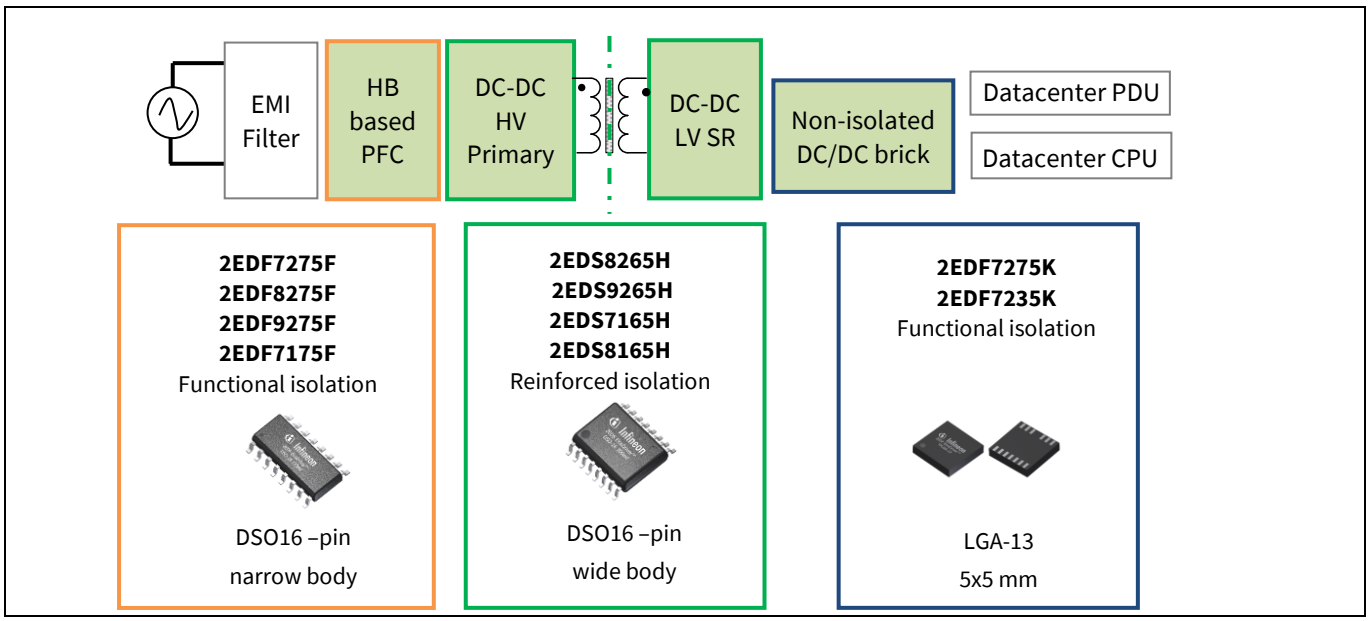


Figure 1 Intended usage range for 2EDi products in SMPS

The input-to-output and channel-to-channel isolation makes the 2EDi drivers suitable to drive both high- and low-side switches in half-bridge (HB) and full-bridge (FB) structures.

But even systems utilizing low-side switches only may exhibit significant differences between driver and controller ground potential, e.g. when 4-pin switches with Kelvin source connection have to be driven or when high parasitic PCB inductances cannot be avoided. Then a functionally isolated driver is a solution to safely avoid any erroneous interpretation of the control signal.

If functional isolation is not sufficient in terms of safety, the 2EDS reinforced input-to-output isolation ensures “double protection” according to the safety isolation standards (see section 3).

2 Overview of isolation standards

EiceDriver™ 2EDi can be regarded as a family of magnetic digital isolators and thus must be certified according to common isolation standards.

Isolation standards are mainly separated into two categories:

- System standards, defining the safety requirements of the overall end-system
- Isolator component standards, defining test-procedures to test the robustness of single isolators

Due to the robust on-chip isolation utilizing a thick SiO2 layer, the isolation level of a 2EDi product is usually limited by the package.
The system standards of interest define minimum distances (creepage and clearance) between any two conductive points of the system (pins/pads) to avoid creation of undesired conductive paths (due to pollution on the PCB or air-spark). The single packages must meet this criterion regarding input-to-output or channel-to-channel pin distances.
The isolator "package" then forms the bridge between system and component standards.
Component standards define test voltages according to system standards and package limitations.

2.1 System isolation standards: IEC60950, IEC62368

System isolation standards define the overall system operating environment, human safety requirements and test procedures to make end equipment safe and production tests standardized globally.

The system standard of highest relevance for 2EDi applications is IEC60950. This standard has been widely used over the years for information processing, office machinery and telecom equipment.
Today, the new IEC62368 standard is taking the lead; its 3rd version has been published in 2018 including the IEC60950 together with the IEC60660 standard for audio and video equipment. It addresses consumer electronics (game station, musical instruments etc.), data processing and computer network equipment (PCs, laptop, servers, routers etc.), office appliances (electronic type-writers, copy machines etc.) and telecommunications equipment (telephone system, modem etc.).

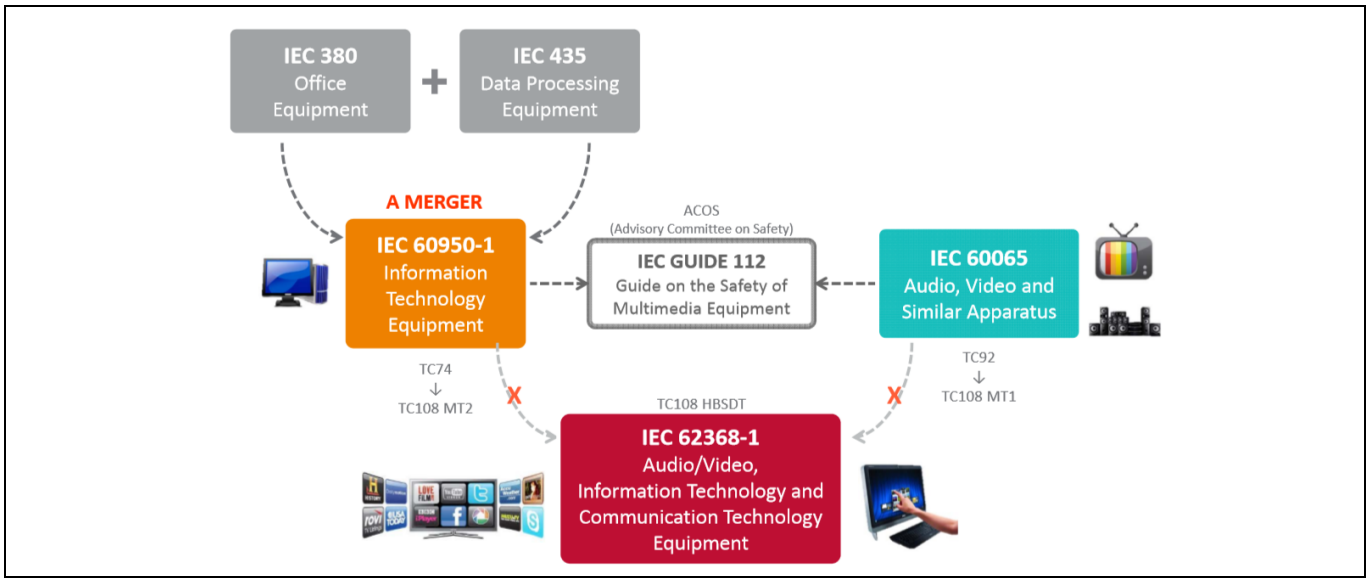


Figure 2 Evolution of relevant end-system standards

Compared to the previous standards, the IEC62368 introduces a different approach (hazard-based approach) that focuses on clarifying the hazards mechanisms and causes rather than prescribing solutions. A long transition period has been considered necessary to adapt to the new safety approach. Actually the standards are coexisting but certification bodies will be forced to only certify according to the new standard from June 2019; the previous standards will be completely replaced in December 2020.
The 2EDi product family is certified according to the IEC62368 and the included IEC60950 system standards with related European, Canadian (CSA) and Chinese (CQC) certifications.

The isolation specification section of the 2EDi datasheet [5] includes several references to different IEC standards; these are simply sub-standards including specific sections of the global IEC62368 standard. For example, the IEC60664-x defines the minimum creepage (CPG) and clearance (CLR) distances required to ensure system level isolation.

2.2 Isolator component standards: IEC60747-17, UL1577, VDE-0884-1x

The isolator component standards define certification tests for the isolation barrier robustness in isolated ICs.

UL1577 is the first isolator component standard, released in USA for optocouplers. Its international equivalent, IEC60747-5-5, came in 2007 followed by the compliant German standard VDE0884-5-5.

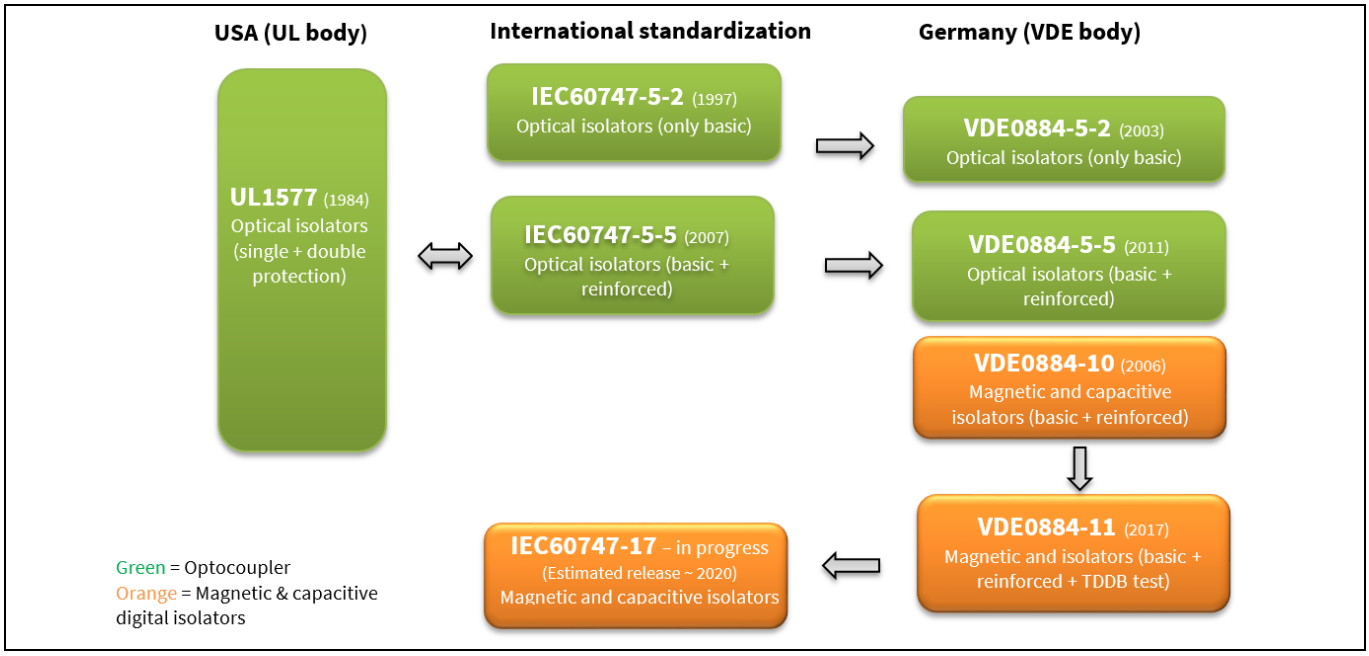


Figure 3 Evolution of isolator component standards

With the development of digital isolators based on magnetic or capacitive isolation, component isolation standards for both magnetic and capacitive couplers have been introduced (Figure 3); the first standard (VDE0884-10) has been developed under the coordination of VDE in Germany working as an independent body for certification.

The most recent German standard VDE-0884-11, released in January 2017, is the basis for the future global world wide standard IEC60747-17 (release planned in 2020) for magnetic and capacitive isolated devices.

As UL1577 is the only component standard available in USA, it has been widely used even to certify non-optical digital isolator. The reinforced isolated 2EDS is certified according to VDE0884-10 (VDE0884-11 is planned) as well as according to UL1577.

The VDE-0884-1x standards define additional test methods emulating possible stresses on the isolation barrier in operating conditions. Key tests include the determination of the parameters below:

- maximum surge isolation voltage (V_{IOSM})
- maximum transient isolation voltage (V_{IOTM})
- maximum repetitive peak voltage (V_{IORM})
- working voltage (V_{IOWM})

V_{IOSM} tests simulate a lightning strike on the isolation barrier coming from the electrical power grid.

V_{IOTM} tests simulate a non-periodic stress on the isolation barrier, e.g. an unintended voltage overshoot due to load jumps.

V_{IORM} and V_{IOWM} tests simulate a periodic stress on the isolation barrier; an example is the periodic HV signal applied between primary and secondary GND in a high-side driver.

In addition, the VDE-0884-1x standards define a common mode transient immunity (CMTI) test. Going beyond pure robustness tests, CMTI intends to test the noise immunity of the isolation barrier by applying fast voltage transients between primary and secondary side.

The new VDE-0884-11 standard adds the time dependent dielectric breakdown (TDDB) test. It intends to test the long-term reliability of the insulation material through an accelerated test-stress. A DC or AC voltage significantly higher than V_{IOWM} is applied across the barrier for a time necessary to break down the barrier. The test is repeated varying the voltage level in order to obtain a voltage versus time graph; the product lifetime at the rated working voltage is determined by extrapolation.

3 Design guidelines

The CT technology, decoupling input and output sides, makes the 2EDi family suitable to drive half-bridge and full-bridge configurations; in particular, the reinforced isolated 2EDS is suggested to drive the HV primary-side MOSFETs in common PSFB and LLC topologies based on secondary-side control, while the functional isolated 2EDF is suggested to drive PFCs and LV synchronous rectifier topologies based on half-bridge or full-bridge structures. A typical example of a 2EDS based gate drive circuit driving such a half-bridge is given in Figure 4.

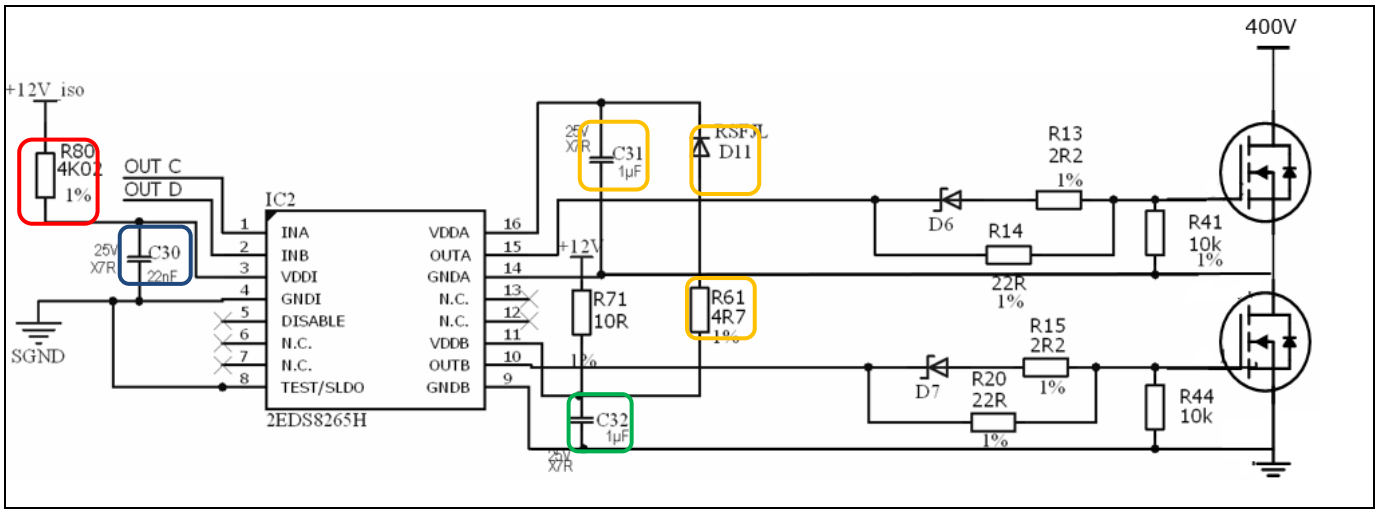


Figure 4 Gate driving circuit using 2EDS to drive HV MOSFETs in a PSFB converter

The following subchapters provide guidelines for dimensioning the driving circuit components:

- Shunt resistor (R80)
- Input bypass capacitance C_{in} (C30)
- Output bypass capacitance C_{out} (C32)
- Boostrap components: resistance RB (R61), capacitance CB (C31) and diode DB (D11)
- Source (R14, R20) and sink (R13, R15) gate resistances.

3.1 Shunt resistor dimensioning

The input side of 2EDi must be powered with a nominal 3.3 V (maximum 3.5 V) through the pin VDDI in Figure 5. If the available input side supply (V_{IN_SUPPLY} in Figure 5) is exceeding 3.5 V, the shunt low-dropout regulator (SLDO) embedded in the driver must be activated. For that purpose the IC provides an active-low SLDO pin; to activate the SLDO, the pin must be connected to GNDI. In this situation, a proper resistor has to be placed between the available supply voltage (e.g. 12 V) and the VDDI pin (regulated to 3.3 V); its value must ensure a driver input current high enough to properly feed both the input logic and the SLDO.

Figure 5 shows the VDDI supply with and without activated SLDO.

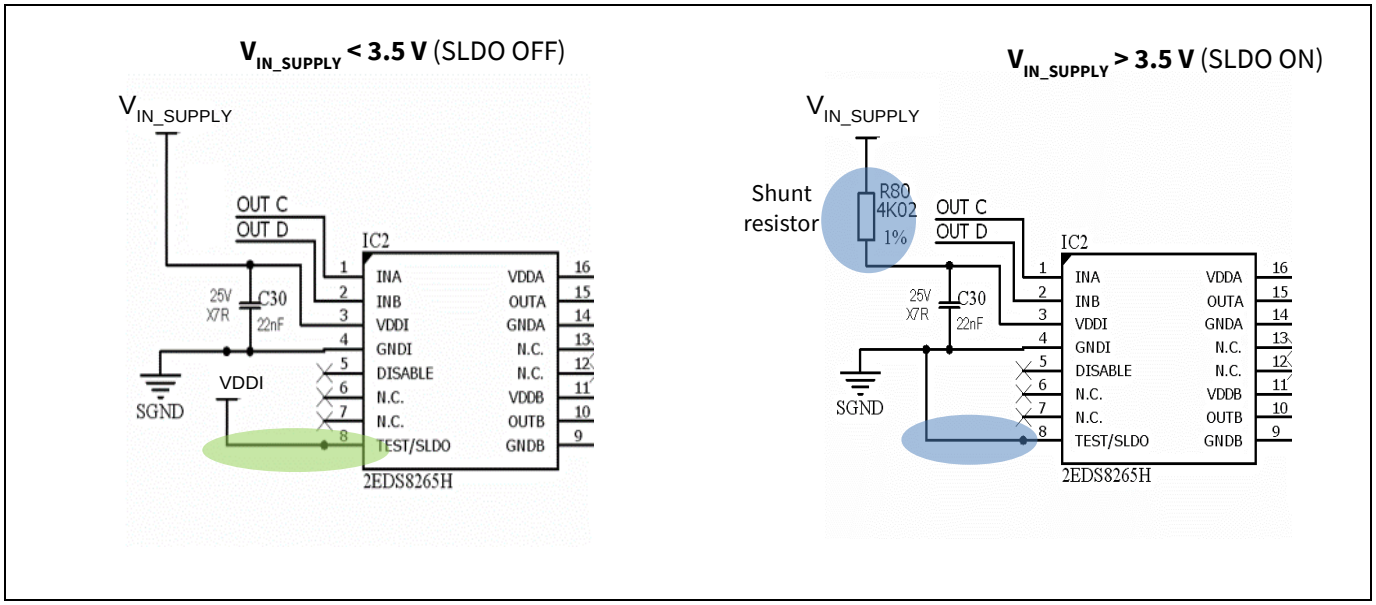
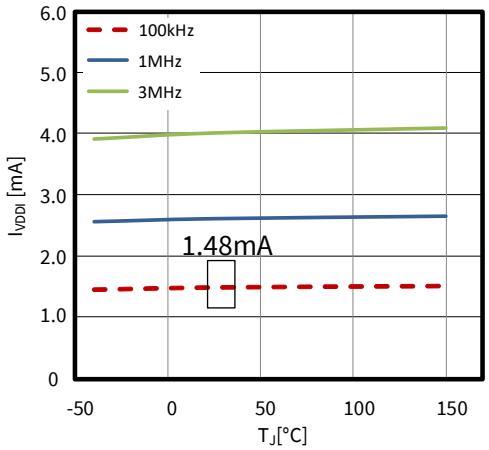


Figure 5 Direct and SLDO-regulated VDDI supply

When the SLDO is active, the supply current entering the input chip flows into the logic circuit and into the SLDO. The input logic is responsible to encode the input PWM signals into a sequence of short current pulses to drive the coreless transformer. Depending on the PWM switching frequency, the logic circuit is absorbing the almost constant current with temperature shown in Figure 6 and reported in the 2EDi datasheet.



Typical VDDI current vs. temperature and frequency

Figure 6 Current consumption vs frequency of driver input logic

To properly run the SLDO, a minimum current of 0.5 mA must flow into the SLDO. Then, the input current provided to the driver must exceed at least 0.5 mA the current I_{VDDI} absorbed by the logic circuitry for encoding operations (Figure 6). The minimum requirement for the input current leads to a limitation on the selectableSLDO resistor value:

$$R_{VDDI} \leq \frac{V_{DD,min} - 3.3\,V}{I_{VDDI} + 0.5mA} \quad (1)$$

In (1) the minimum value, due to ripple, of the DC supply voltage ($V_{DD,min}$) has to be considered.

For typical switching frequencies, the current absorbed by the input logic is 1.48 mA (Figure 6). Considering 0.5 mA margin on this current and 5% ripple on the supply voltage, the shunt resistances in Table 1 are recommended for different external supply voltages and switching frequencies.

It is recommended to use resistors in SMD 0805 package with 1 percent tolerance.

Table 1 Suggested shunt resistances

Available supply VDD	Switching frequency		
	100 KHz	**1 MHz**	**3 MHz**
5 V	≤732 Ω	≤453 Ω	≤316 Ω
8 V	≤2.15 kΩ	≤1.37 kΩ	≤953 Ω
12 V	≤4.02 kΩ	≤2.61 kΩ	≤1.78 kΩ
15 V	≤5.49 kΩ	≤3.48 kΩ	≤2.43 kΩ

The SLDO provides flexibility in selecting the input side supply. This could bring a layout benefit since the closest low-voltage plane can be connected to the driver VDDI just activating the SLDO and placing the shunt resistor; any long connection to a 3.3 V microcontroller supply can thus be avoided in this case.

Moreover, the input side robustness is strongly increased using the SLDO. In case of overvoltages on the input supply the shunt resistor may act as a fuse and disconnect the driver. This is particularly beneficial for the protection of the isolation barrier on the input chip.

Finally, the shunt resistor together with the input bypass capacitanceforms a high-frequency bidirectional filter dampening both the noise injected from the auxiliary supply into the driver and the noise generated by the driver due to the CT current pulses.

3.2 Bypass capacitors dimensioning

Both the high gate current during switching transients and the short current pulses driving the coreless transformer cause voltage drops on the parasitic resistances and inductances of the driver supply connections; this could affect the driver supply introducing unacceptable noise.

It is thus mandatory to use bypass capacitors between the supply pins and the related GND pins both on input and output side of the IC (see Figure 4). The bypass capacitors must be located as close as possible to the driver.

3.2.1 Input bypass capacitor

Even in non-switching operation the CT is driven by a sequence of 150 mA/2ns current pulses at a non-constant repetition rate (0.4 to 1.6 µs). Each of these pulses corresponds to a charge ΔQ of 0.3 nC; this causes a voltage ripple on the input bypass capacitance (C_{in}) given by

$$\Delta V = \frac{\Delta Q}{C_{in}} \quad (2)$$

To keep ΔV sufficiently low (e.g. in the few tens of mV range), a minimum C_{in} of 10 nF is recommended. On the other hand, if the SLDO is activated, C_{in} should not exceed 22 nF due to stability reasons.

It is suggested to use a ceramic capacitor in SMD 0805 package with 25 V DC voltage rating.

3.2.2 Output bypass capacitor

During the turn-on commutation of a MOSFET a short high-current pulse is drained from the driver output bypass capacitance to charge the equivalent input capacitance of the MOSFET (C_{load}). That operation leads to a partial discharge of the bypass capacitance C_{out} by a value ΔV depending on the ratio of the two involved capacitances:

$$\Delta V = V_{DDA} \times \frac{C_{load}}{C_{out} + C_{load}} \quad (4)$$

It is important to distinguish between the equivalent input capacitance C_{load} and the input capacitance C_{iss} as reported in the MOSFET's datasheet. C_{iss} is the instantaneous value of the input capacitance for a certain gate-to-source and drain-to-source voltage; it changes during a switching transient.

The MOSFET equivalent input capacitance C_{load} is, instead, a mean value and can be derived from the total gate charge Q_G necessary to switch the MOSFET according to

$$C_{load} = \frac{Q_G}{V_{GS}} \quad (5)$$

In MOSFET datasheets Q_G is usually provided in the gate charge characteristics, a graph showing the dependence of gate-to-source voltage from gate charge; an example is given in Figure 7 for a specific 280 mΩ CoolMOS™ switch.

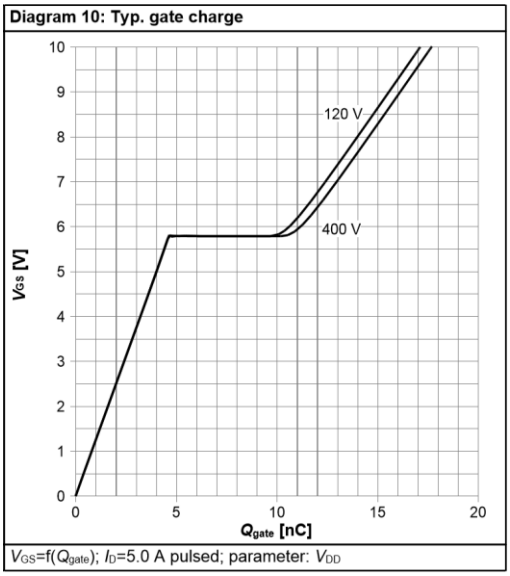


Figure 7 Typical gate charge characteristic of CoolMOS™ IPA60R280CFD7

A reasonable output supply voltage ripple below 5% would then from equation (4) result in

$$\frac{\Delta V}{V_{DDA}} < 5\% \quad \rightarrow \quad C_{out} > 19\, C_{load} \quad (6)$$

A proper dimensioning thus requires to choose an output bypass capacitance which is at least 20 times larger than the equivalent input capacitance of the MOSFET; a range from 100 nF to 1 µF is common when driving Infineon CoolMOS™ switches. As for the input bypass capacitance, it is suggested to use a ceramic capacitance in SMD 0805 package with 25 V DC voltage rating.

3.3 Bootstrap circuit dimensioning

Bootstrapping is a very cost effective method to create the floating supply voltage for driving high-side MOSFETs in half-bridge topologies.

The bootstrap circuit is highlighted in Figure 8 and is made up by three components: bootstrap capacitor (C_B), bootstrap resistor (R_B) and fast recovery diode (D_B).

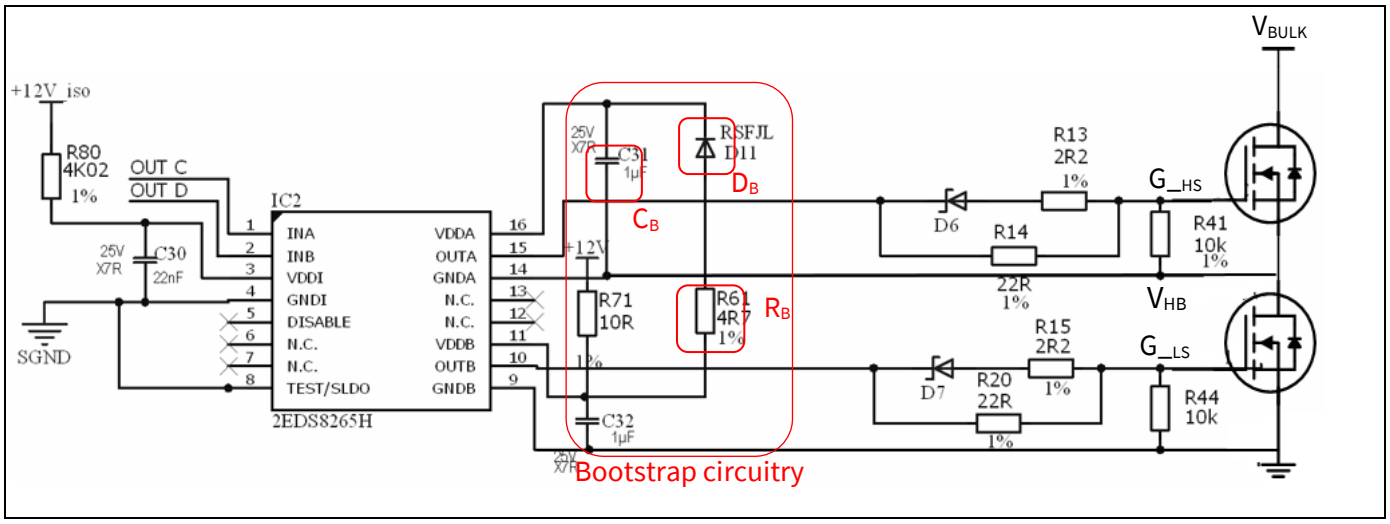


Figure 8 Bootstrap circuit to generate the HV floating supply

The bootstrap circuit operation is defined by two main periods:

- **Charging period**: capacitor C_B is charged while the low-side (LS) switch is ON and the high-side switch is OFF. When the LS MOSFET is ON, the diode D_B is forward-biased ($V_{HB} \cong 0V$) and the current flows from the isolated LS voltage source VDDB (+12 V) into C_B through the bootstrap resistor R_B, diode D_B, and the low-side switch that finally closes the loop to ground. Simultaneously, the necessary quiescent current ($I_{VDDAqu2}$) is supplied to the driver.
- **Sourcing period**: when the low-side switch is turned off and/or the high-side switch starts conducting, the source voltage of the HS switch (V_{HB}) quickly rises until it approaches the half-bridge supply voltage (V_{BULK}). As a consequence, the bootstrap diode D_B gets reverse biased and disconnects the ground supply from C_B. The capacitor C_B must be dimensioned to store the energy required to keep the HS switch ON until the next commutation; in this way, a supply voltage of V_{BULK} + VDDA (+12 V) is ensured during the sourcing period for proper HS MOSFET driving.

The bootstrap circuit requires careful design in order to ensure robust and safe operation. More specifically, the charging period must be sufficiently large to charge C_B, and the ripple on the supply voltage due to C_B discharge during the sourcing period must fulfil the specifications (e.g. 5 percent maximum ripple).

Additional situations of discharge must also be taken into account; the burst mode is in particular critical from C_B dimensioning point of view. Burst mode is characterized by extended non-switching times with duration t_{SKIP} (e.g. 1 ms) during low-load operation. The driver quiescent current discharges the capacitance C_B during t_{SKIP}; the risk is that for very long t_{SKIP} C_B is discharged below the UVLO level of the driver. The dimensioning of C_B based on burst mode consideration is then more restrictive than for normal PWM mode operation to avoid any false triggering of UVLO.

This section provides some guidelines for dimensioning the bootstrap components C_B, R_B and for selecting the current and voltage ratings of the bootstrap diode D_B.

The dimensioning of C_B must guarantee a voltage ripple (ΔV_{CB}) within specifications; ΔV_{CB} depends on the charge Q_{CB} that has to be provided by C_B as follows:

$$\Delta V_{CB} = \frac{Q_{CB}}{C_B} \tag{7}$$

C_B thus can be dimensioned by calculating the charge Q_{CB} and considering the limitation on the maximum ripple ΔV_{CB}.

During normal PWM mode, the Q_{CB} is given by the gate charge Q_g transferred in order to turn-on the HS MOSFET and the quiescent current drawn by the driver during the sourcing period. The worst case in terms of C_B discharge has to be considered: longest sourcing period and maximum HS MOSFET duty cycle (D_{MAX}):

$$Q_{CB} = Q_g + D_{MAX} \times I_{VDDAqu2} \frac{1}{F_{PWM}} \tag{8}$$

In systems with burst mode operation at low-load, the discharging during t_{SKIP} must be considered by adding the term ($I_{VDDAqu2} \times t_{SKIP}$) to (8).

The capacitor C_B is defined by the maximum ripple ΔV_{CB}. A common criterion is to accept a maximum ripple of 5 percent of VDD. Considering burst mode operation, the dimensioning is more critical and must always guarantee a supply voltage above the driver UVLO level.

The value of the bootstrap resistor R_B can be determined from the requirement to ensure full charge of C_B during the charging period. Assuming five time constants as a proper duration for full charging

$$t_{min} = \frac{(1 - D_{MAX})}{f_{PWM}} \geq 5\, R_B\, C_B \tag{10}$$

Then the equation for R_B results as follows:

$$R_B \leq \frac{1 - D_{MAX}}{5 \times C_B \times f_{PWM}} \tag{11}$$

After dimensioning of C_B and R_B, the selection of the proper bootstrap diode D_B can follow. D_B should have a current rating ($I_{F(AV)}$) higher than or equal to $I_{AV,max}$:

$$I_{AV,max} = \frac{Q_{CB}}{1 - D_{MAX}} \times f_{PWM} \tag{12}$$

$I_{AV,max}$ is the maximum average current through the diode; the largest value is given by the shortest charging period.

The voltage rating of $D_B$must be sufficiently high to block V_{BULK} during the sourcing period. Finally, the diode must have a sufficiently fast reverse recovery time to avoid that its reverse current discharge the capacitor C_B.

3.4 Gate resistance dimensioning

As widely known, the total resistance in the gate path ($R_{G,TOT}$) defines switching time and switching losses. $R_{G,TOT}$ is made up by three contributions: the sourcing/sinking output resistance of the driver IC (R_{on_SRC}/ R_{on_SNK}), the external sourcing/sinking resistance ($R_{G,SOURCE}$ / $R_{G,SINK}$) and the internal gate resistance of the MOSFET (R_G).

The low-ohmic output stage of the 2EDi family results in negligible R_{on_SRC} and R_{on_SNK} contributions.

The internal gate resistance of the MOSFET changes with the MOSFET technology; when driving Infineon CoolMOS™ devices, it is suggested to refer to the dedicated CoolMOS™ application notes for getting first indications on how to select the external source and sink resistances for a specific product.

The differentiation of the external gate resistance allows to independently optimize ”on” and “off” transients; this is particularly important in soft switching topologies. In the PSFB topology e.g., the zero voltage switching (for low output currents) at turn-on allows to select an external source resistance larger than the sink resistance as the turn-on switching losses are not affected in the soft switching approach. Besides, an increased source resistance dampens gate voltage overshoots during turn-on.

Optimizing gate resistors is a complex task: it requires to consider the basic tradeoffs between switching time/efficiency and voltage overshoots/EMI, as well as the interaction mechanisms between the switches in a half-bridge (spurious turn-on, shoot-through). In addition, a good estimation of package and PCB parasitics (particularly power loop inductance) is indispensable.

A detailed discussion on how to select and dimension optimized gate resistors is beyond the purpose of this application note. Dedicated application notes, e.g. [6], describe the main parameters to consider.

4 PCB layout recommendations

The impact of PCB parasitics is particularly critical in fast-switching power systems and requires a proper layout. This section provides hints to optimize and speed up the PCB layout around EiceDRIVER™ 2EDi products:

- Use a low-ESR decoupling capacitance for each input (VDDI) and output (VDDA, VDDB) supply and place it as close as possible to the driver
- Place the gate resistors and the MOSFETs as close as possible to the driver in order to minimize the gate loop inductance
- Use GND planes to reduce the parasitic inductance of ground connections
- Use vias in parallel to reduce the resistance of connections
- When using the dead-time control (DTC) functionality(2EDF7235K), place the external DTC resistor (see Figure 11) as close as possible to the driver; any coupling capacitance to a high-side node has to be strictly avoided

Figure 9, Figure 10 and Figure 11 provide layout recommendations for 2EDSxx65H, 2EDFxx75F and 2EDF7235K, respectively.

The figures show top layer layouts with the gate driver and the MOSFETs on the same side; this is suggested when using SMD MOSFETs. Only single gate resistance (no differentiation between source and sink behaviour) are considered for sake of simplicity.

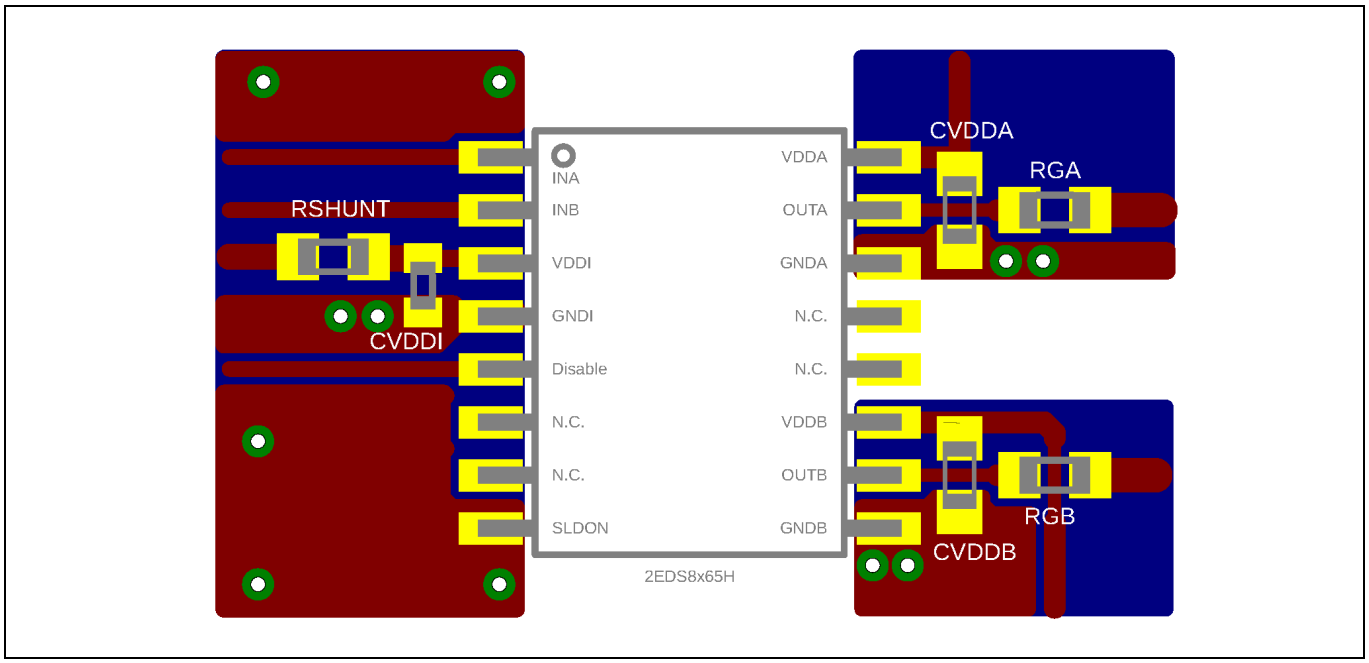


Figure 9 2EDS8x65H in shunt mode – Layout recommendation

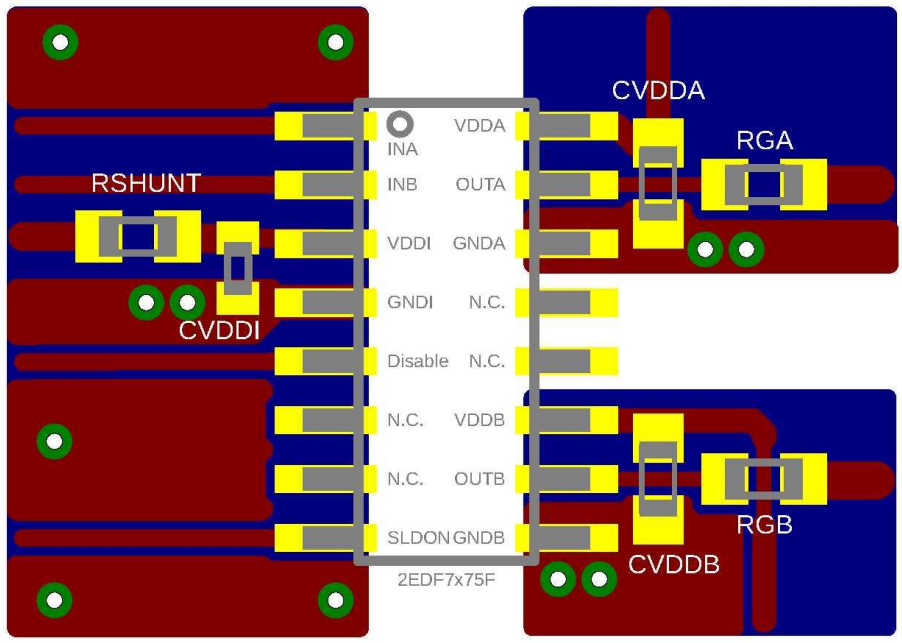


Figure 10 2EDF7x75F – Layout recommendation

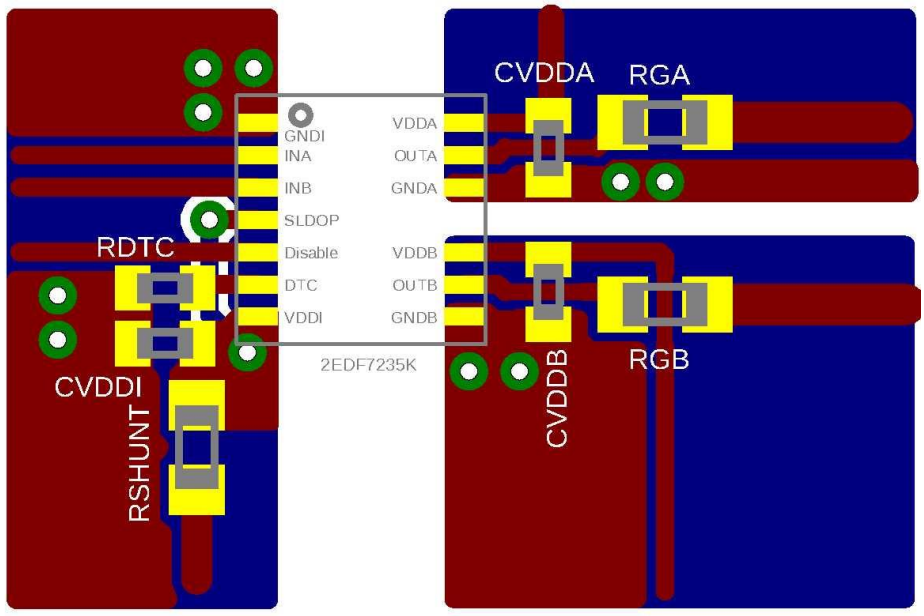


Figure 11 2EDF7235K – Layout recommendation

5 Evaluation of 2EDS vs gate transformer in 800 W PSFB evaluation board

A 2EDSx gate driver has been tested in Infineon's 800 W zero voltage switching (ZVS) phase-shift full-bridge (PSFB) evaluation board.

This board is a DC-DC converter intended for use in SMPS for server and industrial applications [1].

Driving the HV primary side from the secondary side microcontroller requires an isolated driving scheme; the original version of the board uses a non-isolated gate driver (EiceDRIVER™ 2EDN) plus a gate transformer (ICE G TO5-111-100) and is available at the webpage **Evaluation board Eval_800w_zvs_fb_cfd7**.

The modified evaluation board in Figure 12 has been realized by re-designing the HV full-bridge gate drive scheme with the reinforced isolated 2EDS gate drivers. Purpose of the new design is to test the 2EDS gate driver behavior in a real and widely used application. In addition to the necessary PCB changes, this requires to redimension the gate resistors and adapt the software for optimizing dead times.

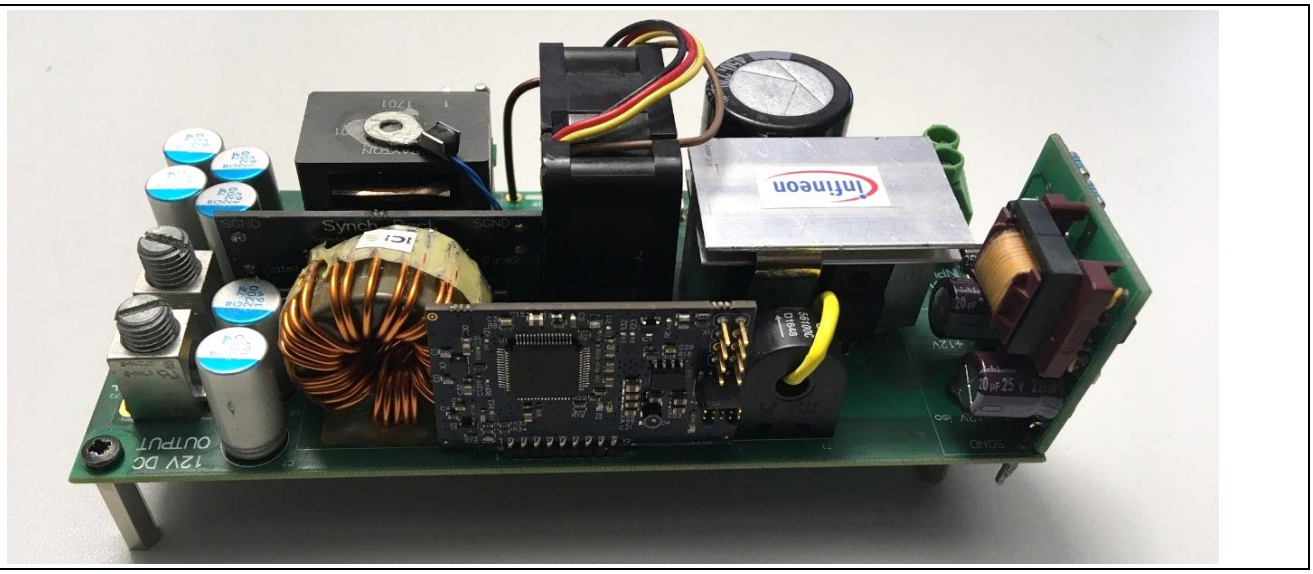


Figure 12 Internal variant of the 800 W ZVS PSFB board using the 2EDS for evaluation purposes

The evaluation shows that 2EDS works properly in the application representing an attractive alternative to the gate transformer solution with lower volume and increased low-load efficiency.

5.1 Reduced gate switching noise

It is well known that the lower limit of the gate resistors is on the one hand defined by the switching node's voltage overshoots; this strongly depends on parasitic inductances and switching conditions (hard/soft). On the other hand the gate resistors also have to dampen ringing in the gate loop. From oscillator theory, this depends on gate loop inductance and gate capacitance. Here the 2EDS solution is by far superior due to the removal of the leakage inductance associated with the gate driver transformer.

The coreless transformer used in the 2EDi product family, however, is characterized by a nearly negligible leakage inductance.

This is evident also from the measured waveforms in Figure 13 and Figure 14 depicting the induced noise during a hard turn-on transition (10 A load); the same dV_{DS}/dt of 12.9 V/ns is guaranteed in both versions.

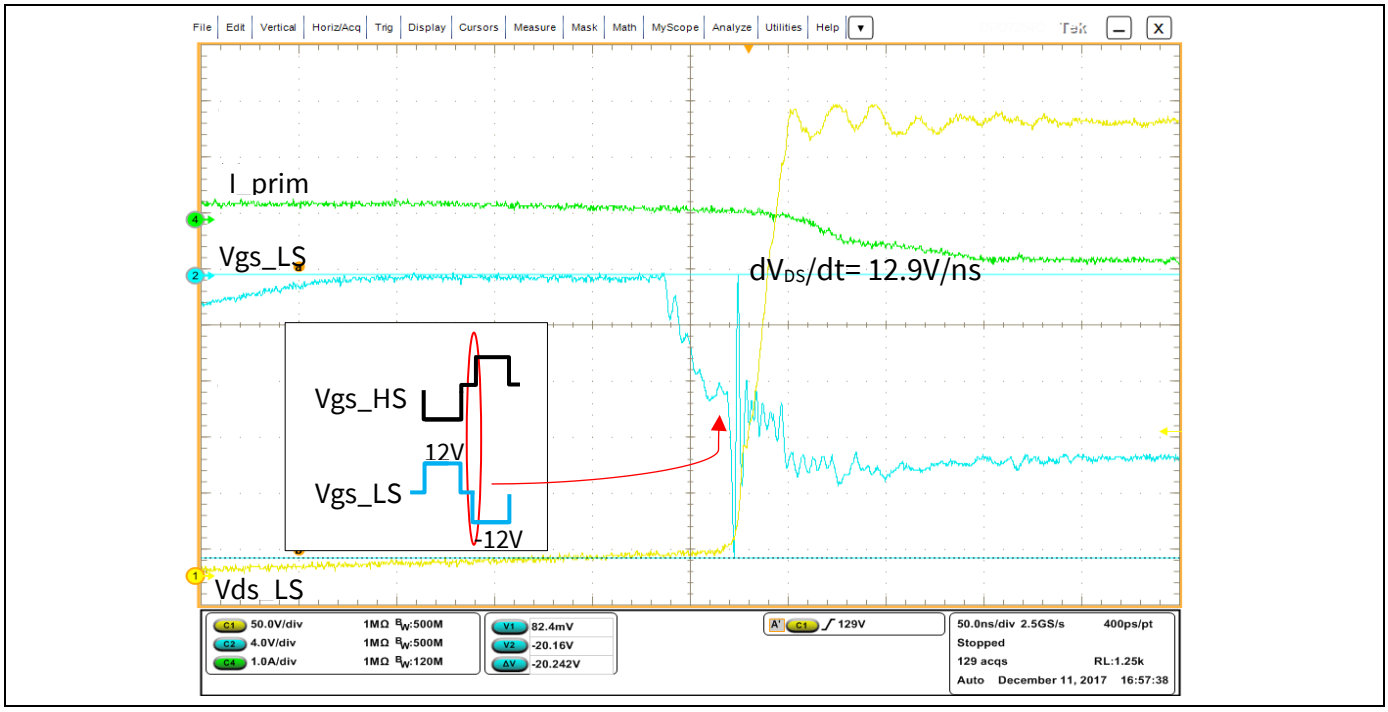


Figure 13 **Gate voltage noise during hard turn-on (10 A) in the original evaluation board using 2EDN plus gate transformer – gate-to-source voltage of the leading leg LS MOSFET [cyan], its drain-to-source voltage [yellow], and current in the transformer [green]**

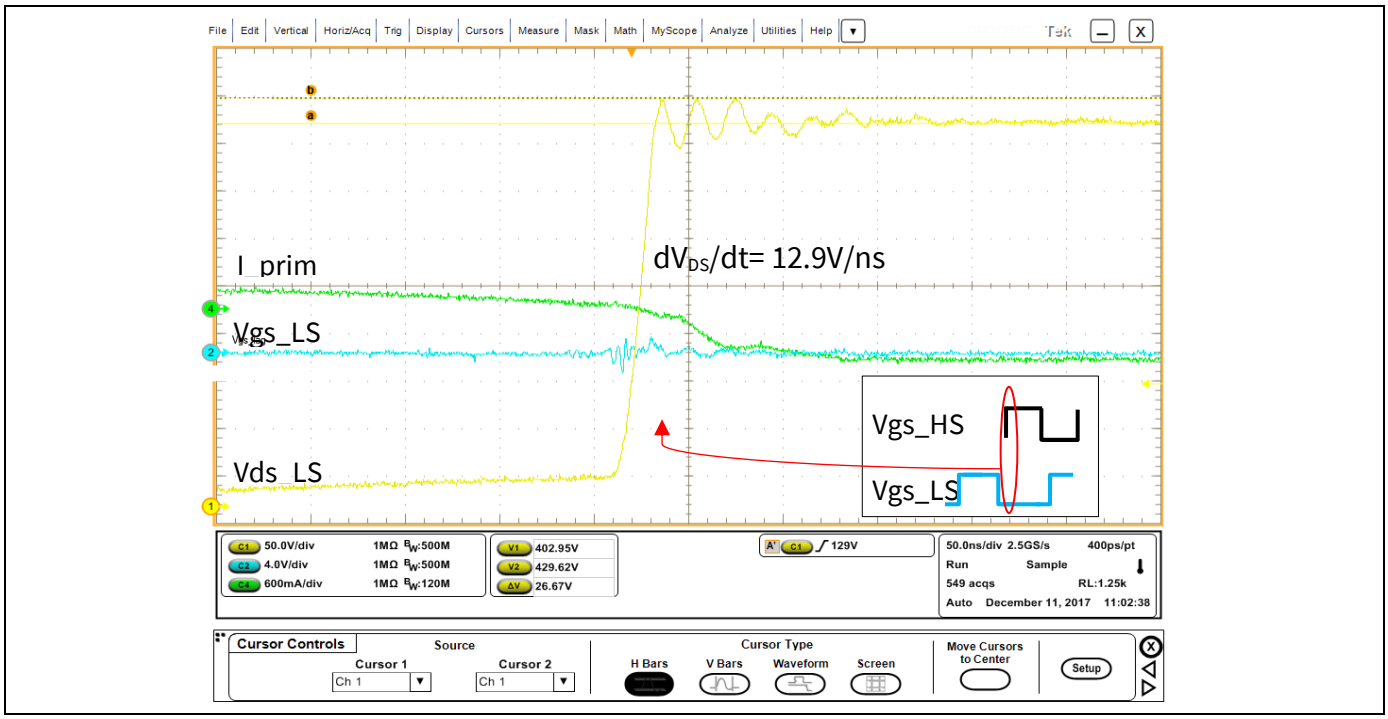


Figure 14 **Gate voltage noise during hard turn-on (10 A) in the new evaluation board using 2EDS - gate-to-source voltage of the leading leg LS MOSFET [cyan], its drain-to-source voltage [yellow], and the current in the transformer [green]**

Figure 13 shows that, in order to avoid cross-conduction in the half-bridge due to the significant gate transformer induced noise, a bipolar voltage driving has been used in the original board; this allows to be safe

and avoid shoot-through events without increasing the gate resistance and without sacrificing the switching losses. However, higher gate drive losses result from bipolar voltage operation.

With the 2EDS solution the limited gate noise obtained for the same dV_{DS}/dt does not require a bipolar driving. Moreover, the lower noise with the 2EDS driver provides some margin to increase dV_{DS}/dt by reducing the gate resistor, thereby speeding up switching transients and gaining efficiency without the risk of shoot-through issues.

5.2 Efficiency improvement at light-load

The efficiency characterization is done for the complete output current range including the bias and the fan absorption.

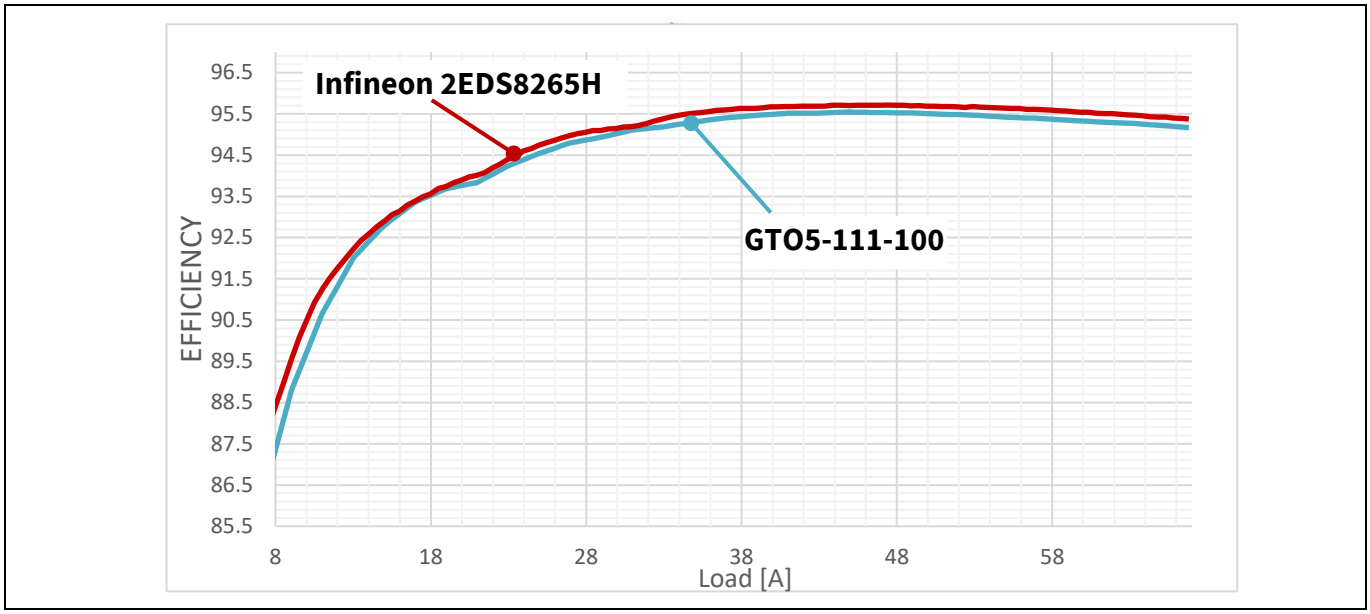


Figure 15 Efficiency plots

The plot highlights that 2EDS works properly in this application, keeping the efficiency of the converter nearly unchanged (except for light-load, the efficiency mismatch in the remaining range is simply due to the different tolerances of the 2 PCBs under test).

The higher noise immunity with 2EDS (section 5.1) allows to speed up the switching event and reduce the switching losses compared to the gate transformer solution. However, switching losses significantly influence overall efficiency only for low output currents, as in this range zero-voltage switching (ZVS) is not completely achieved.

5.3 Volume saving with 2EDS

Using 2EDS allows to remove the discrete gate transformer, which for the typical PSFB switching frequencies (100 KHz) is a bulky component; the gate transformers originally used in the evaluation board are highlighted in the board top view in Figure 16. The 2EDN dríver is not visible since it is located on the bottom side of the PCB.

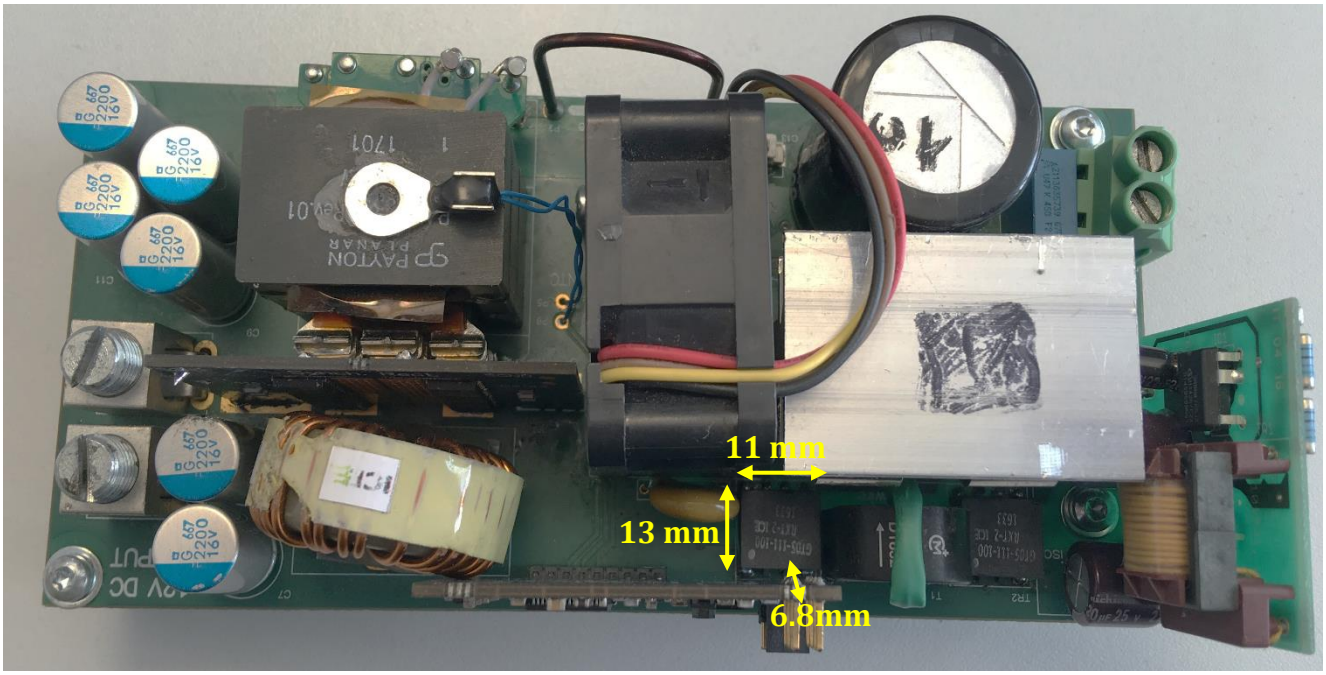


Figure 16 Bulky gate transfomers in the top layer of the original evaluation board

In the new design, 2EDN and gate transformers are replaced by 2EDS. The 2EDS gate drivers are located on the bottom side of the PCB across the isolation barrier, as can be seen in Figure 17.

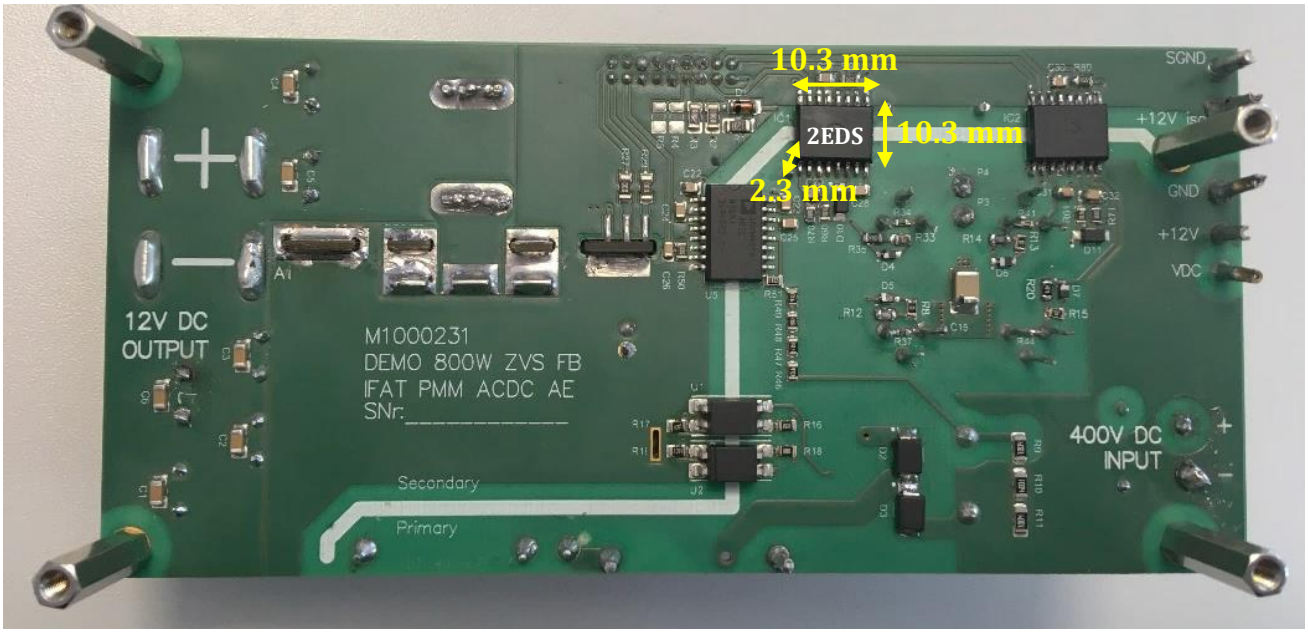


Figure 17 2EDS replace the 2EDN and the gate transformer in the modified evaluation board

The volume saving that can be achieved by replacing the gate transformers with 2EDS drivers is estimated to be at least 25 percent. This would allow a significant increase in power density (40 W/inch^3 in the original board).

5.4 No concerns about core saturation with the 2EDi product family

Additional concerns are due to the nature of the discrete gate transformer with the well-known problem of core saturation imposing a limit on the minimum switching frequency in the converter. Besides, it requires an almost symmetric driving signal which limits the duty cycle to a maximum of 50 percent.

A driving solution not based on gate transformers is in generalmore flexible. With 2EDS and the CT technology the relation between core size and frequency is no longer of concern for the designer. Moreover, the minimum converter switching frequency is not limited any more, providing freedom and flexibility to test and operate a converter at different frequencies; this is particularly important during the first development phases.

In the described PSFB topology the duty cycle is 50 percent, which does not add particular concerns regarding core saturation; however, saturation could happen in special conditions like e.g. burst mode. In the original board this is avoided by applying an even number of pulses during burst mode to maintain the transformer excitation voltage symmetry; with the 2EDi product family replacing the gate transformer the designer no longer has to face such constraints.

6 Summary

This document introduces the EiceDriver™ 2EDi family of isolated gate driver for power MOSFETs. The main intention is to address the usage of 2EDi products in the different SMPS stages and to support engineers using 2EDi gate drivers.

Design and layout guidelines are provided allowing engineers to autonomously design an optimized and complete gate drive scheme using 2EDi.

Furthermore, the performance of 2EDi has been evaluated in a typical PSFB application with focus on reinforced isolated 2EDS. This evaluation has shown the advantages of 2EDi over conventional gate transformers, essentially linked to the innovative coreless transformer (CT) technology.

Adding very low parasitics to the gate loop, 2EDi represents an attractive solution in fast-switching power systems; compared to the common gate transformer driving solutions, using 2EDi guarantee limited switching noise on the gate voltage reducing the risk for dangerous situations (shoot-through).

The volume saving and increase in system power density is an additional advantage of 2EDi.

Moreover, without core saturation problems, the 2EDi CT techonology provides design flexibility and allows to simplify the control scheme. With 2EDi, asymmetrical control signals and duty cycles above 50 percent are possible. Furthermore, the converter switching frequency can be easily changed with no impact on the 2EDi driving scheme.

In addition, due to better noise immunity, 2EDi provides some margin to increase system efficiency by reduction of gate resistors.

As a conclusion, the investigation has shown that 2EDi is an attractive alternative to the gate drive transformer representing a compact, flexible and easy-to-use isolated driving solution.

7 References

[1] **Eicedriver™ 1EDN Gate Driver for Mosfets**

[2] **Eicedriver™ 2EDN Gate Driver for Mosfets**

[3] **Dual-channel isolated gate driver | Eicedriver™ 2EDI**

[4] AN_201609_PL52_031 **Benefits of low-side MOSFET drivers in SMPS**

[5] Datasheet Revision 2.2 EiceDRIVER™ 2EDi product family – fast, robust, dual-channel, functional and reinforced isolated MOSFET gate-driver with accurate and stable timing

[6] AN2015-06 **EiceDRIVER™ – gate resistor for power devices**

[7] AN_201709_PL52_027 **800 W ZVS Phase-shift full-bridge evaluation board** – using 600 V CoolMOS™ CFD7 and digital control by XMC4200

[8] T. Fujihira, “Theory of Semiconductor Superjunction Devices”, *Japanese Journal of Applied Physics* vol. 36, pp. 6254–62, 1997

Revision history

Document version	Date of release	Description of changes
V 1.0	23-11-2018	1st version
V 2.0	28-05-2019	Written form revised
V 3.0	2020-05-15	Added new 2EDF9275F, 2EDS9265H part numbers for 650V CoolSiC™ driving
		Adjusted values in Figure 6
V 4.0	2022-03-22	Added new 2EDF8275F, 2EDS7165H part numbers
V 4.1	2023-03-08	Editorial changes

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-03-08

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2023 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_1805_PL52_1806_095202

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.